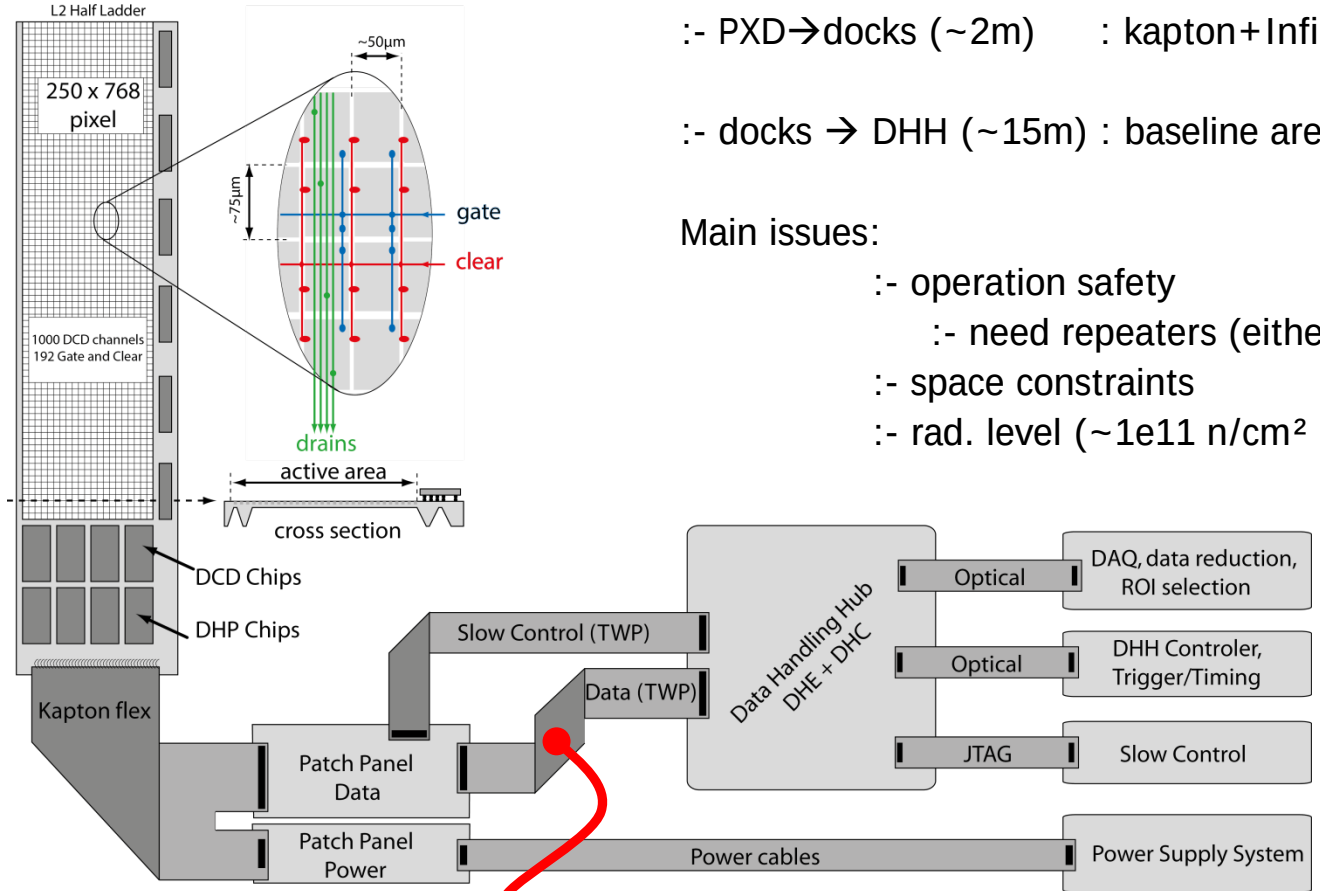
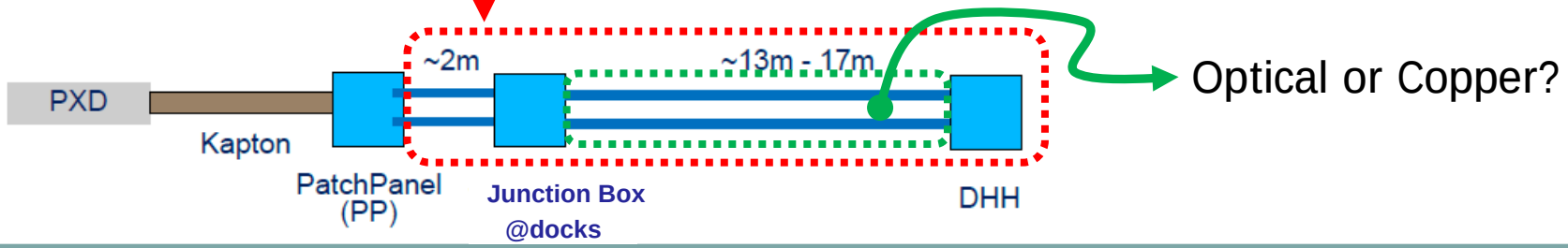
Technical Board SeeVogh meeting Dec 15, 2015

:- Data Transmission Docks → DHH

:- Status Pilot module testing, next steps

Off-module data transmission





:- PXD→docks (~2m) : kapton+Infiniband cable

:- docks → DHH (~15m) : baseline are conv. copper lines

Main issues:

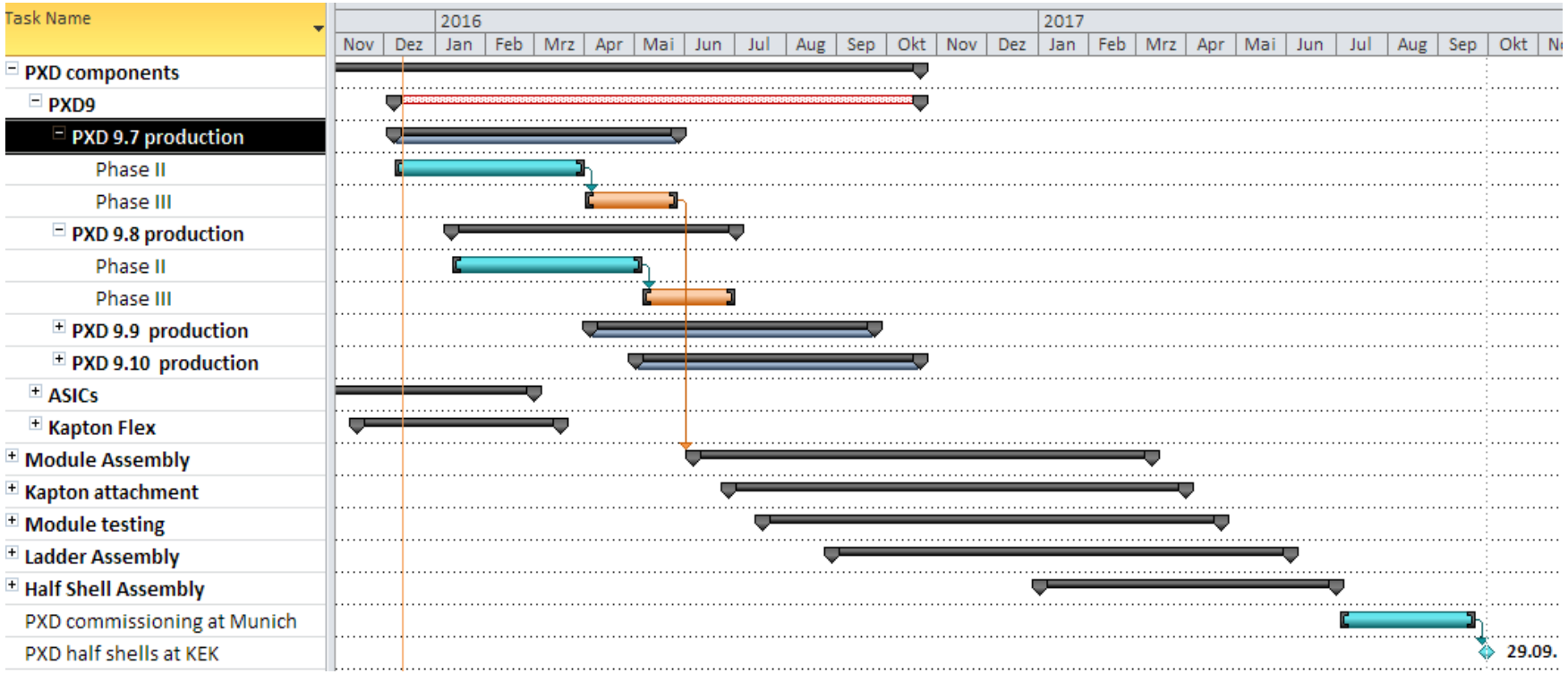
:- operation safety

:- need repeaters (either electrical or opt.)

:- space constraints

:- rad. level (~1e11 n/cm² and ~10krad p.a.)

PXD schedule



:- 28 wafers divided in 4 batches (6/8/6/7)

:- metal-1 Dec. 15, contact-2 and metal-2 Feb. 16, contact-3 and metal-3 April 16

:- 1st batch to be ready for module assembly June 1, 2016

:- stepwise assembly and test sets the scale → PXD half shells ready for commissioning at MPP July 1, 2017

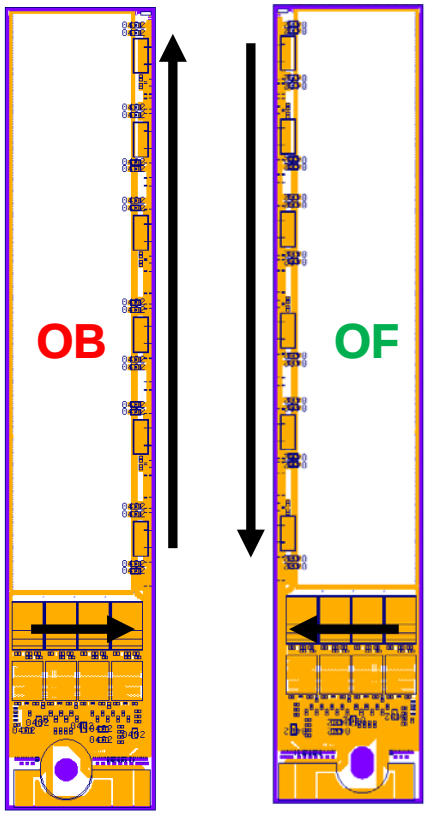
:- PXD @ KEK: October 1 2017

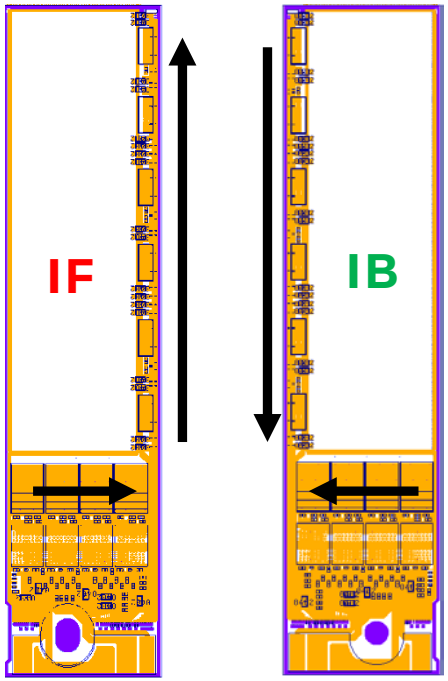
need to start now with metal1, each week more delay cuts the time for commissioning!

What do we need to know to finish PXD9?

:- pilot module full speed operation with acceptable performance (Cd109/Sr90 spectrum)
:- normal and gated mode (with laser)

:- available devices (with current ASIC versions and their known features....)
:- W30-OB1, W30-OB2 : outer backward modules with kapton attached
:- W30-OF1 : outer forward module on Hybrid7

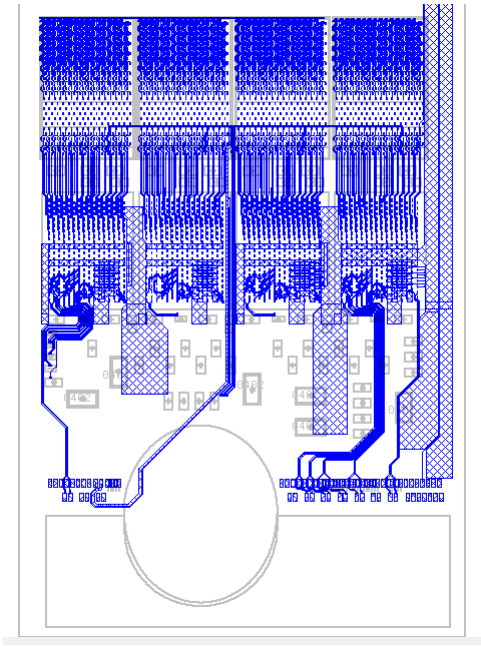


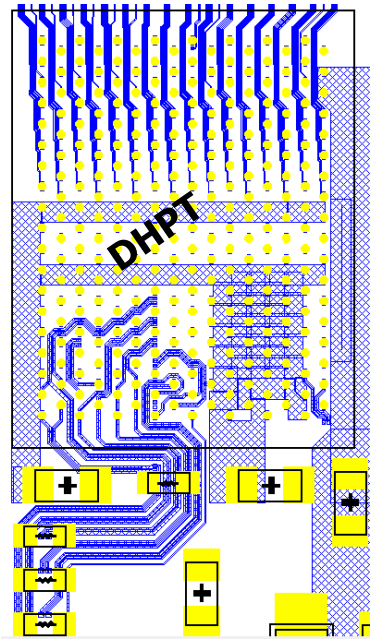


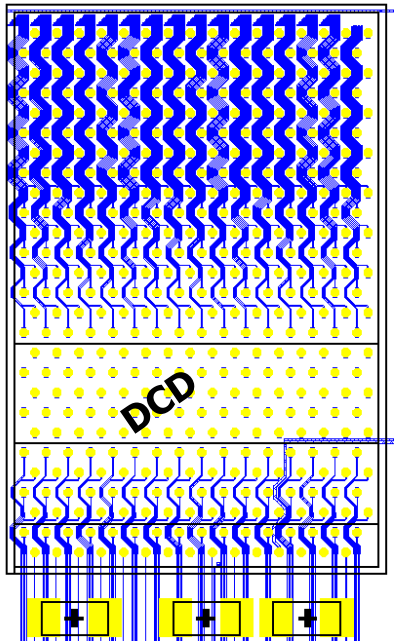
What do need to know before we start metal 1?

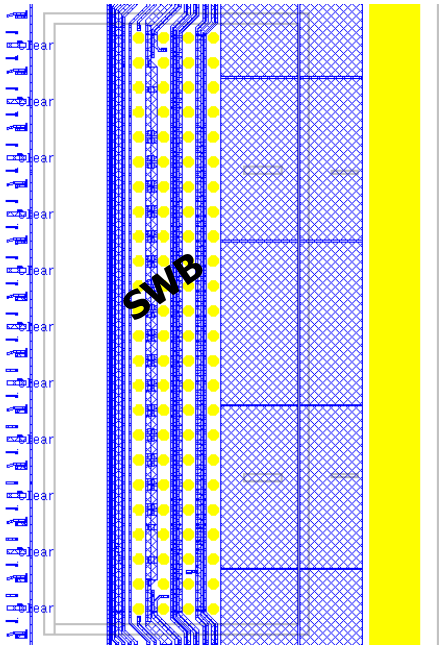
:- metal-1 defines:

- :- DHPT
  - :- JTAG, SER_, REF_, DES_CLK, partly power
- :- DCD
  - :- data lines between DCD&DHP → **changes!**
  - :- part of the DCD inputs
  - :- Monitor, some sense lines for power
- :- SWB
  - :- DGND, DVDD, JTAG, SUB, VDDREF
  - :- **control signals**: SERIN, SEROUT, SEROUT_LAST, **CLK, STR_Gate, STR_Clear**









What do need to know before we start metal 1?

:- metal-1 defines:

:- DHPT

:- JTAG, SER… REF

:- DCD

I think we need full speed operation!

Gated mode should then be possible as well
(possibly with modifications in metal-2 or metal-3)

…D, JTAG, SUB, VDDREF

:- **control signals**: SERIN, SEROUT, SEROUT_LAST, **CLK, STR_Gate, STR_Clear**