PXD9 Pilot Module

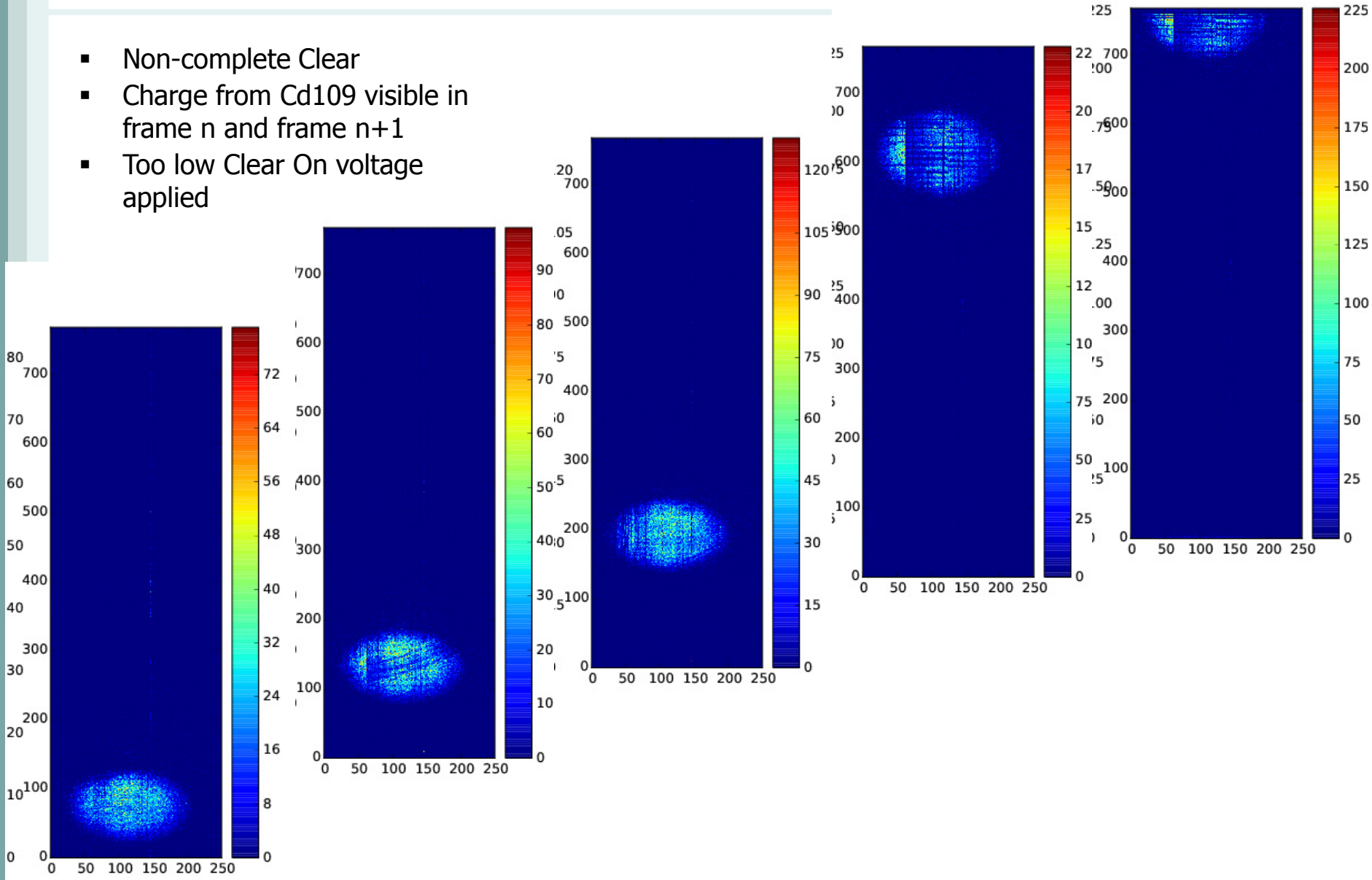
Status Pilot Module Testing

PXD TB – December 15, 2015

Felix Müller, Christian Koffmane for the Testing Crew

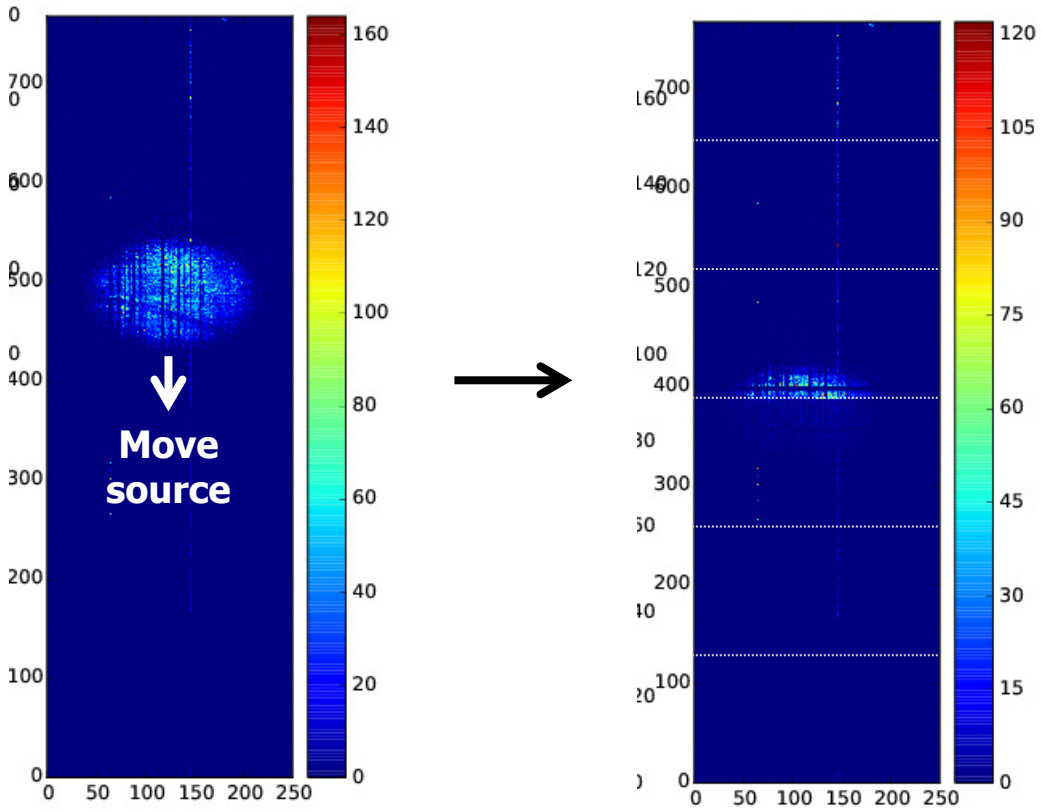
Cd109 Hitmap – Non-complete Clear

- Non-complete Clear
- Charge from Cd109 visible in frame n and frame n+1
- Too low Clear On voltage applied



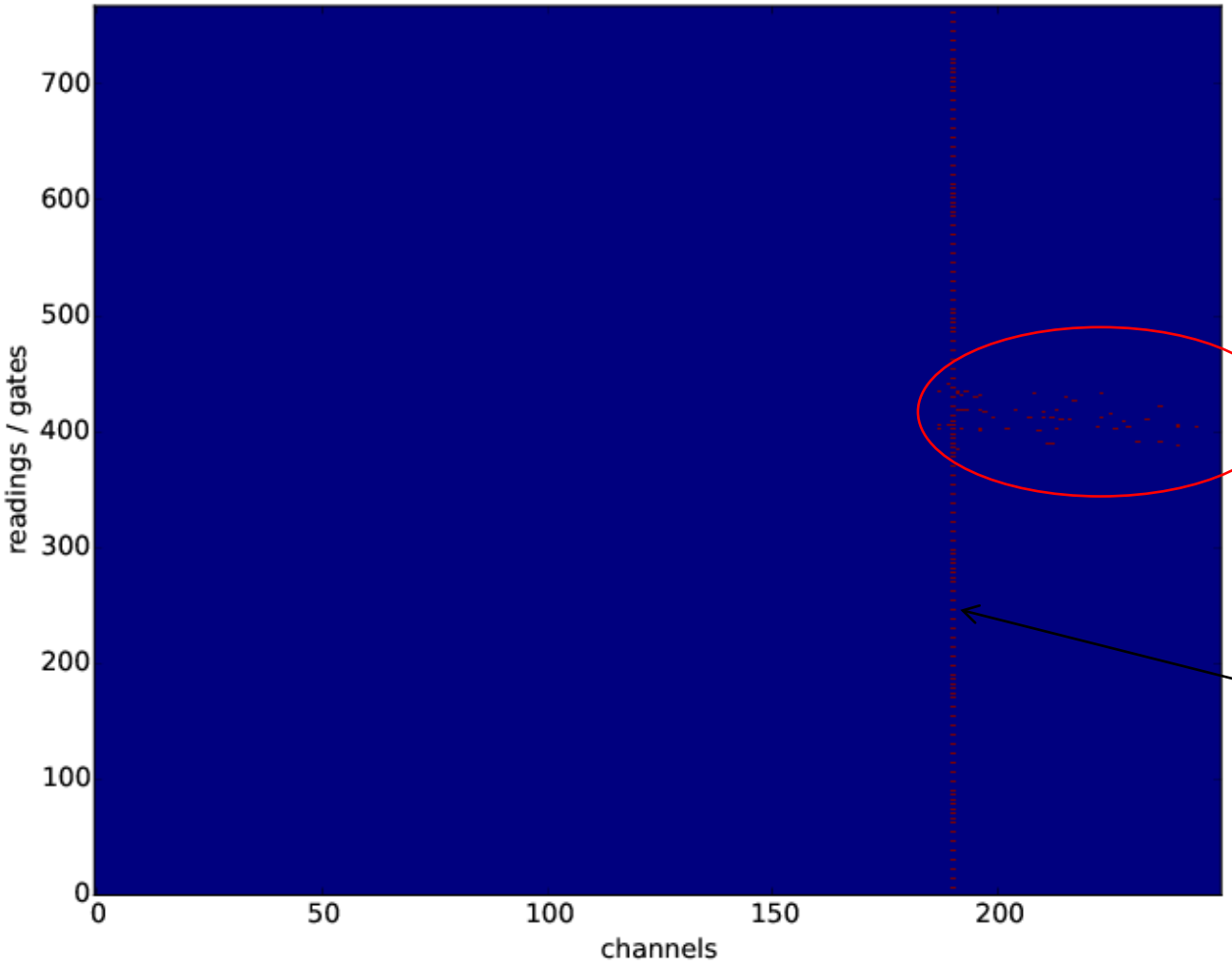
Cd109 Hitmap

- Hit map using a Cd109 source
- read-out of all ASIC simultaneously
- GCK = 62.5 MHz
- T_row = 128ns



- Change in the Clear performance between Switcher 3 and Switcher 4
- Non-complete Clear for Switcher 4, Switcher 5 and Switcher 6
- Charge from Cd109 visible in frame n and frame n+1
- Could be improved by changing the length of the StrC signal (32ns)
- Further improvement by changing the termination resistors for the control signals

Cd109 Hitmap

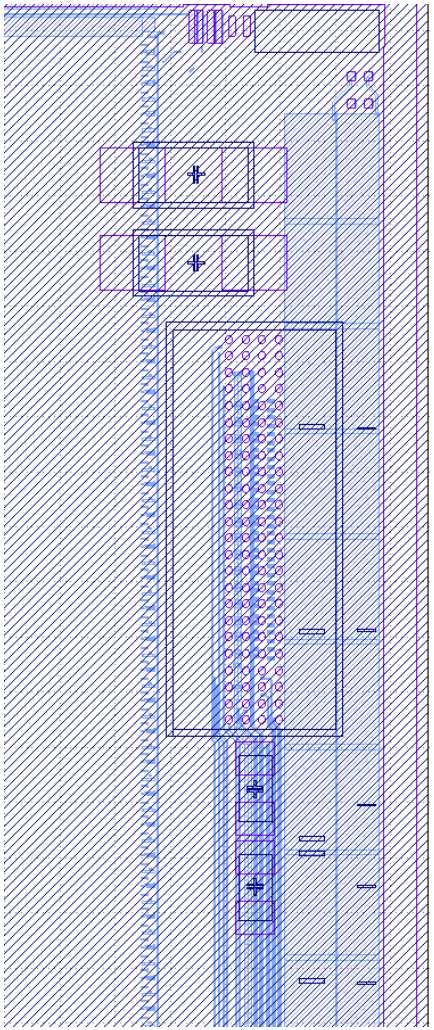


Comparison between frame n and frame n+1
Trigger length = 3072
only one DHPT read

Charge remained in internal gate in the next frame.

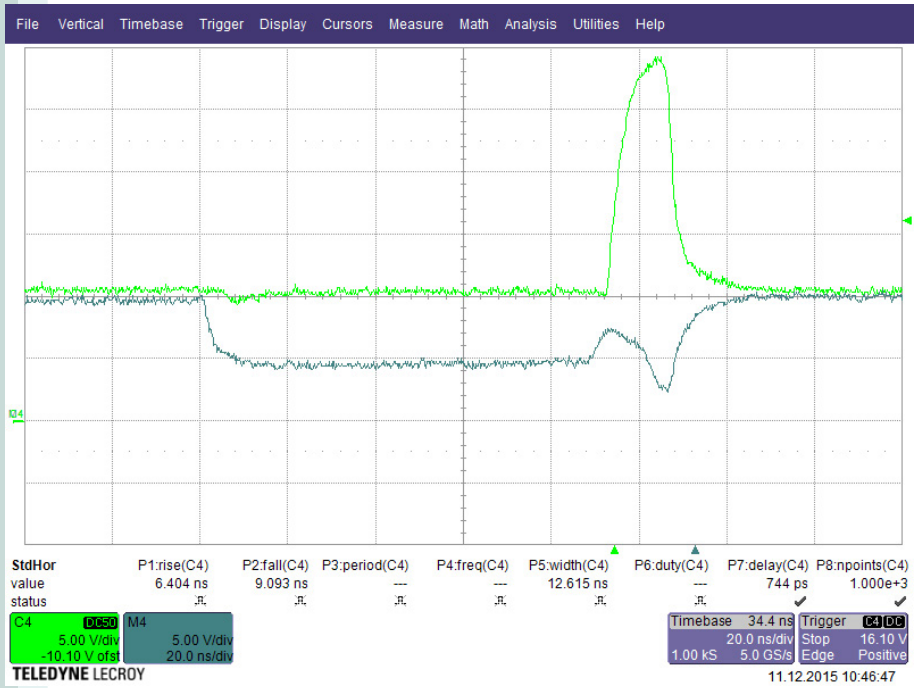
Vertical line is done on purpose to test the software

SWB Control

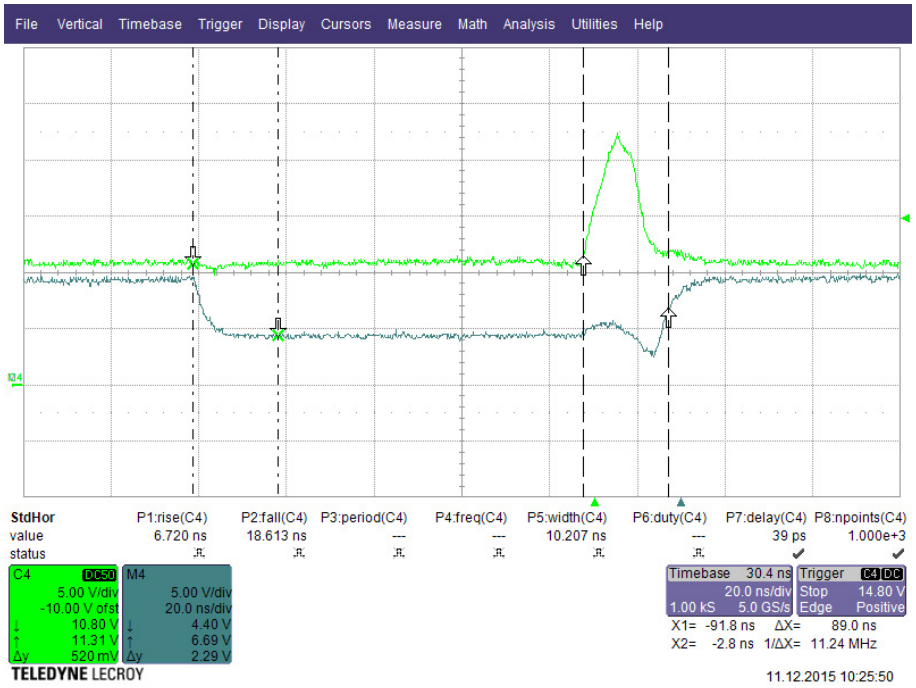


- Control signals SerIN, Clk, StrC, StrG generated by DHPT
- DHPT parameters for setting swing of the control signals sw_tx_06, sw_tx_12, sw_tx_30
- No SMD components for termination but internal resistors in Switcher ASICs

Switcher 1 and Switcher 6 – Clear and Gate output

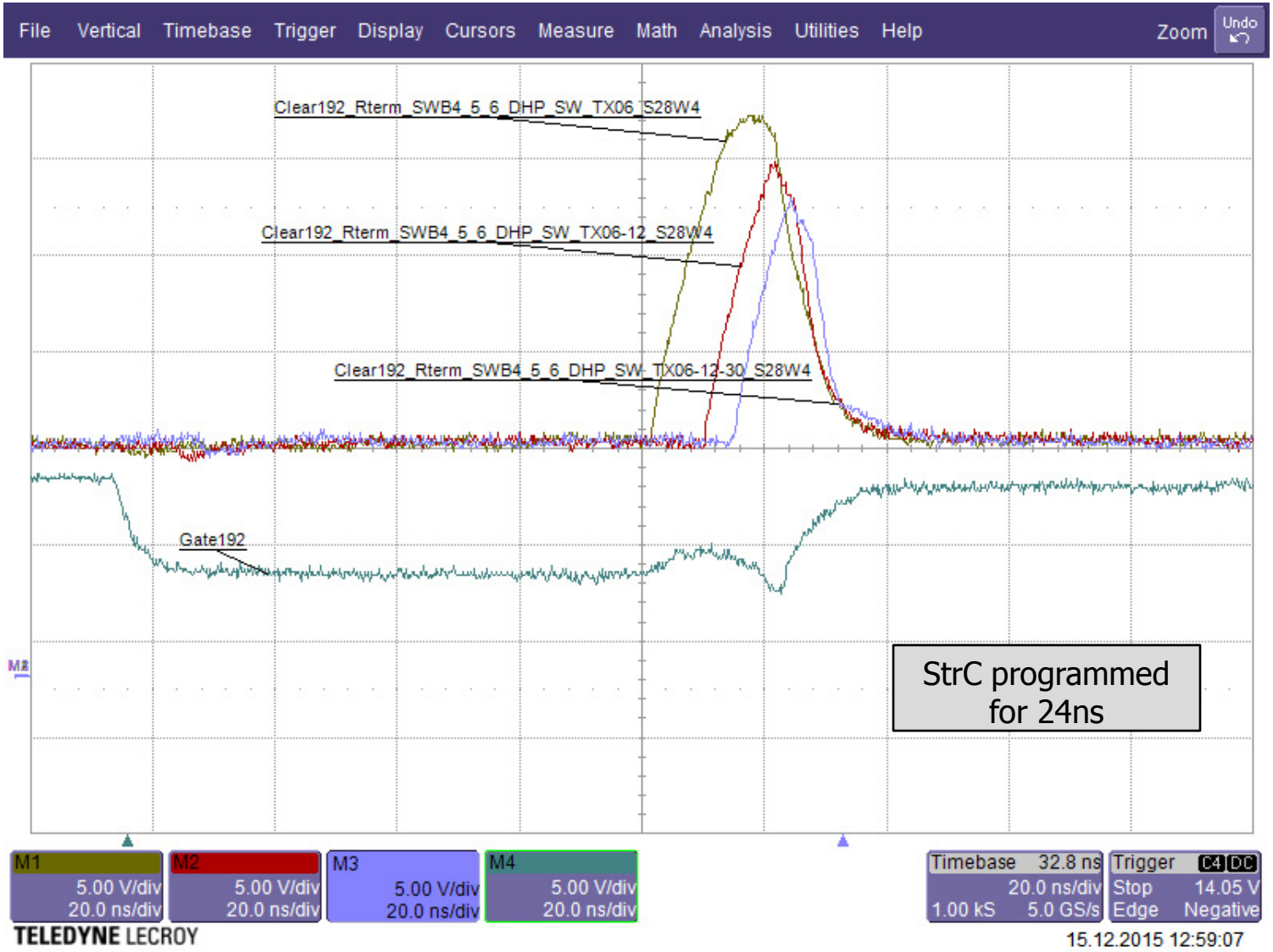


Switcher 1
Clear and Gate



Switcher 6
Clear and Gate

Switcher 6 – Clear dependency on DHPT setting

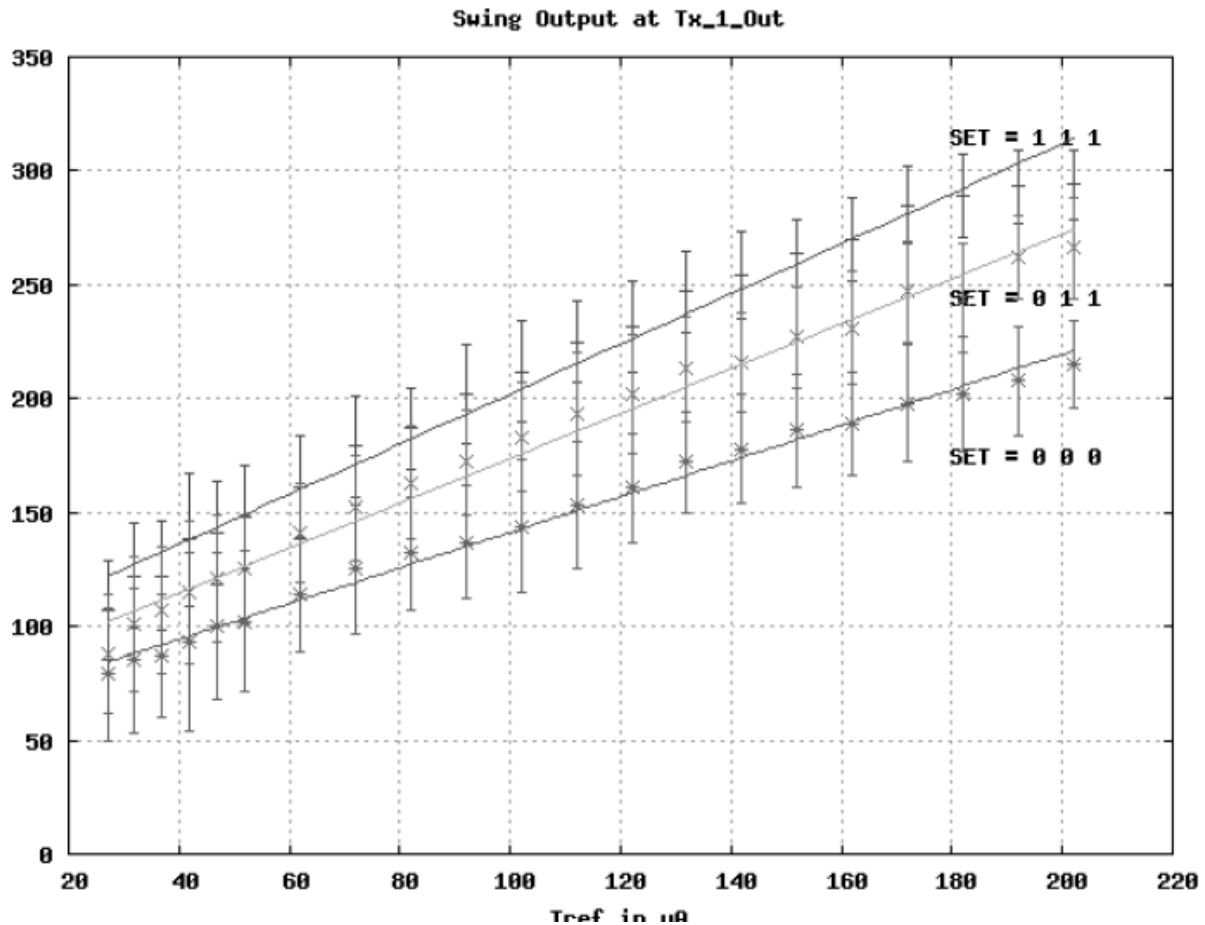


Summary

- slowly we get a better understanding of the Switcher control (at full speed)
- Source measurements to confirm the Clear performance are ongoing
- 2 important remaining items:
  - Hybrid7 → 2nd layout of the balcony
  - High common mode
- Gated mode not part for the decision of the first metallization

Backup

DHP1.0 – SW_TX_06, SW_TX_12, SW_TX_30



- DHPT setting for the Switcher output driver strength
- With 100 Ohm termination the differential output voltage can be set between 100mv and 300mV

PXD9 Pilot Verification Plan - updated

	9.13. Nov	16.-20. Nov	23.-27. Nov	30. Nov - 4.Dec.	7. Dec. - 11. Dec.	14. Dec. - 18. Dec.	Dec. 2015 / Jan. 2016
CW	46	47	48	49	50	51	47
HLL (pxdtest2)	sampling point scan	increase to nominal freq.	gated mode	**PXD9 SeeVogh Meeting**	DHPT serial link - IBERT/oscilloscope	**Go for PXD9 Alu1 metallization and agreement on the necessary changes** **Technical Board Meeting** **Dec. 15th**	gated mode
	pedestal/noise all DCDs	DHPT serial link - IBERT/oscilloscope	pedestal compression		Cd109 spectrum **Clear voltages / sequence**		
		DCD <-> DHPT (delay)	Cd109 spectrum		**Common Mode Noise**		
		sampling point scan	Laser spot				
		pedestal/noise all DCD					
		zero suppressed data					
HLL (pxdtest4)	Preparation Gated Mode Test EMCM			Hybrid 7 Testing to verify OF/IB balcony and EOS layout			