Layout for full-analog extraction

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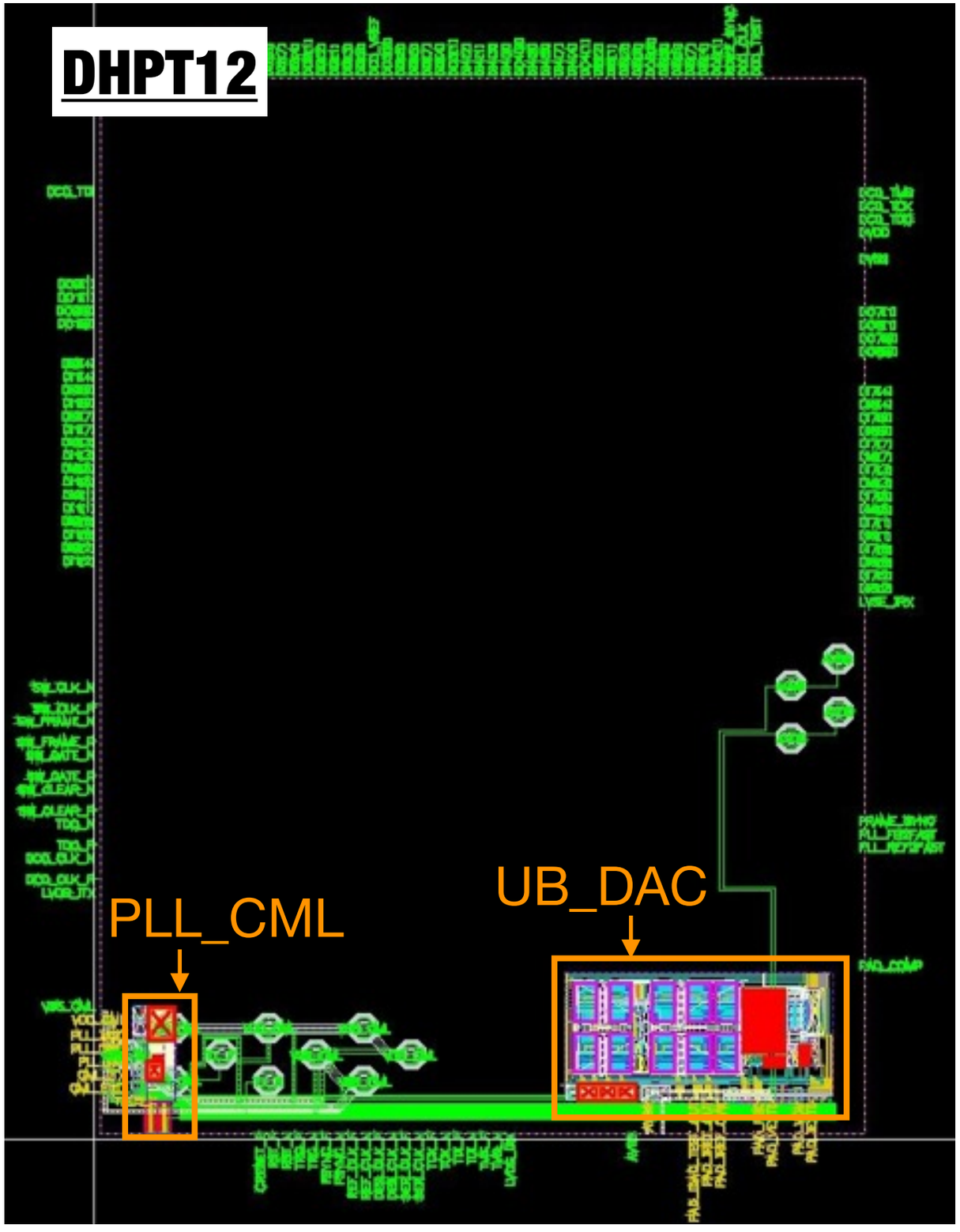


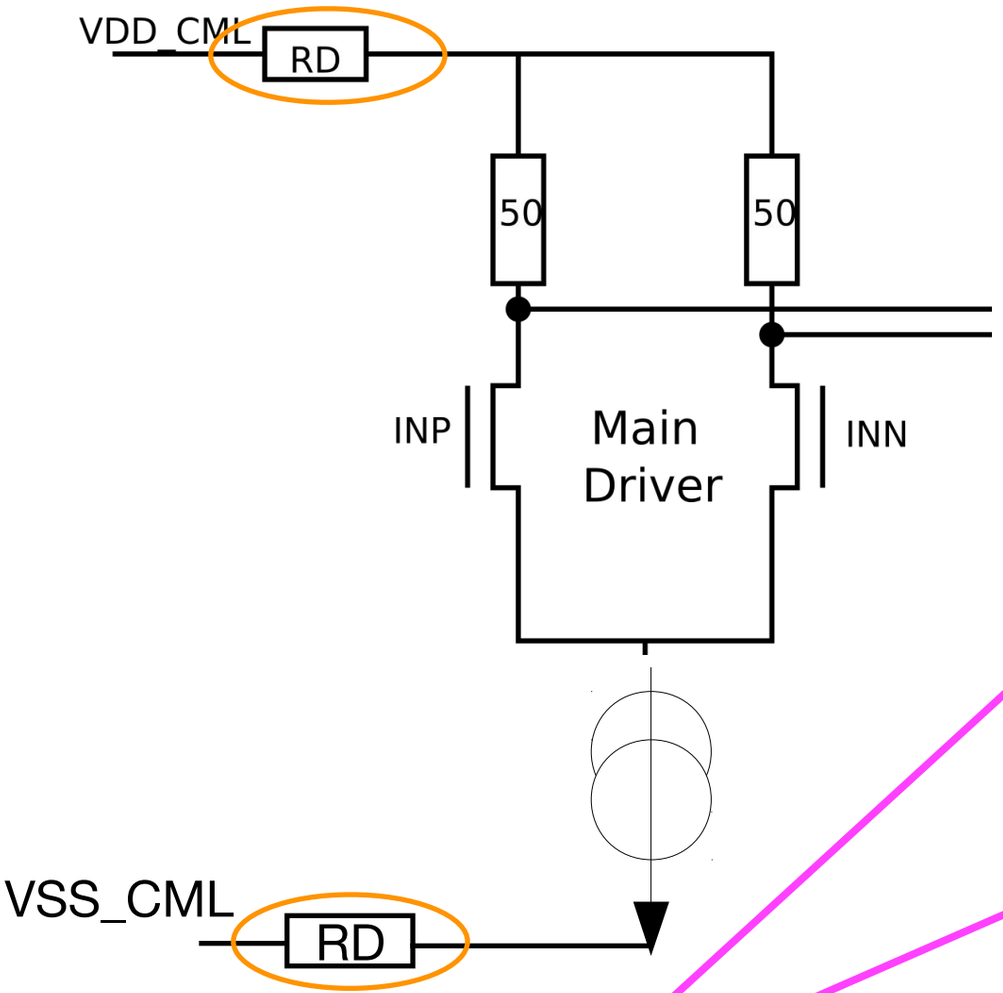
Prepared layout for full-analog extraction

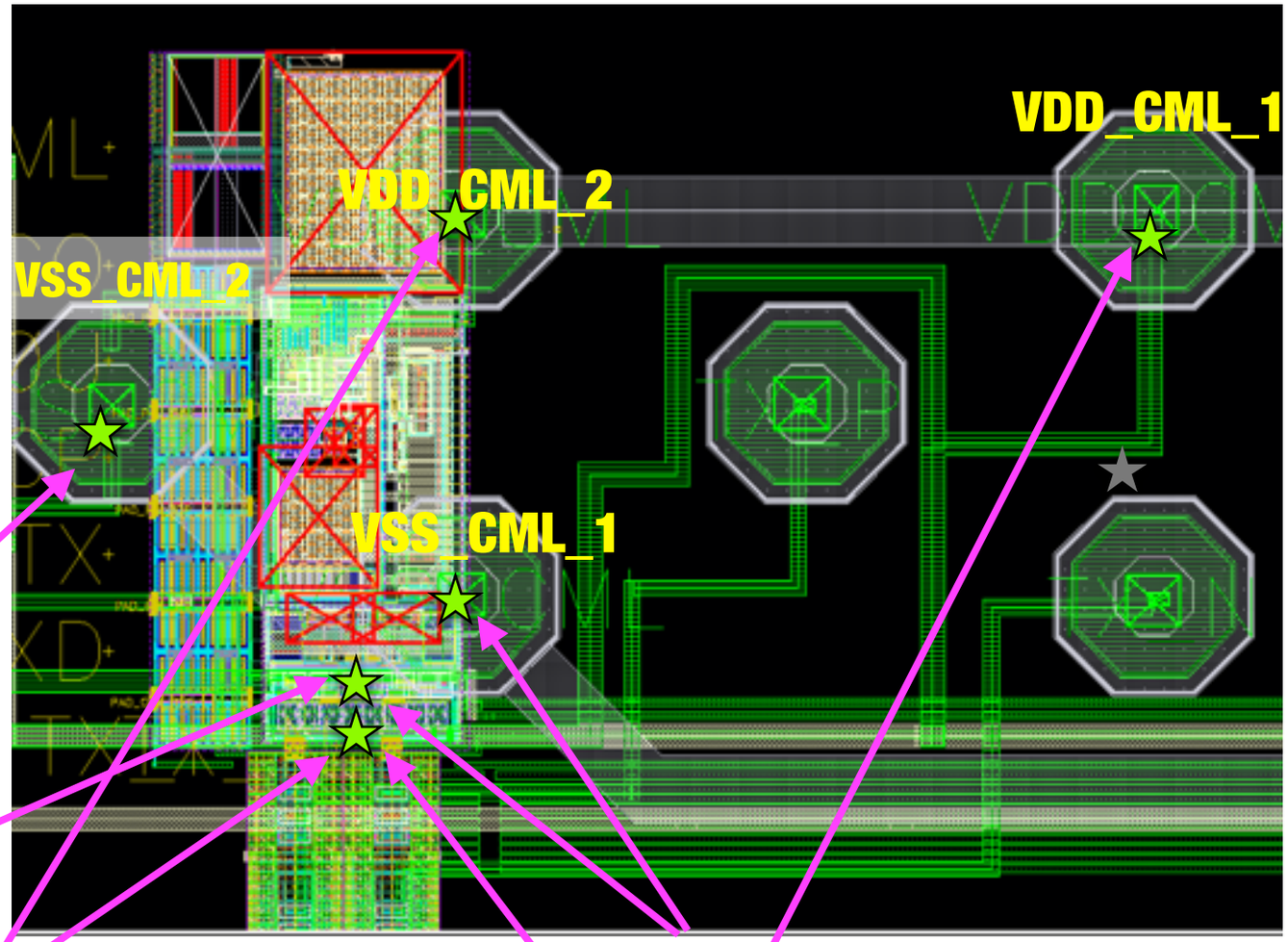
Main changes from DHPT11

- Improved power and ground connection in CML TX
- Modified wrong connections between UB_DAC and ESD
- Added additional “AP” layer for VDD_CML and VSS_CML
- Replaced CML output pad: PDB3AC→PDB1AC
- Removed all EM-hotspots in CML and UB_DAC

Serial resistance in CML TX

- checked serial resistances of VDD_CML and VSS_CML
- In DHPT11 measurements, 25 Ω for VSS_CML and 5 Ω for VDD_CML





VSS_CML_1 (M9) to NMOS source side (M4)
0.06 Ω

VDD_CML_2 (M9) to 50 Ω resistor (M2)
0.24 Ω

VSS_CML_2 (M9) to NMOS source side (M4)
0.11 Ω

VDD_CML_1 (M9) to 50 Ω resistor (M2) **0.2 Ω**

※ M9 is the top routing layer for resistance estimate in Calibre PEX

Serial-Resistance in DAC part

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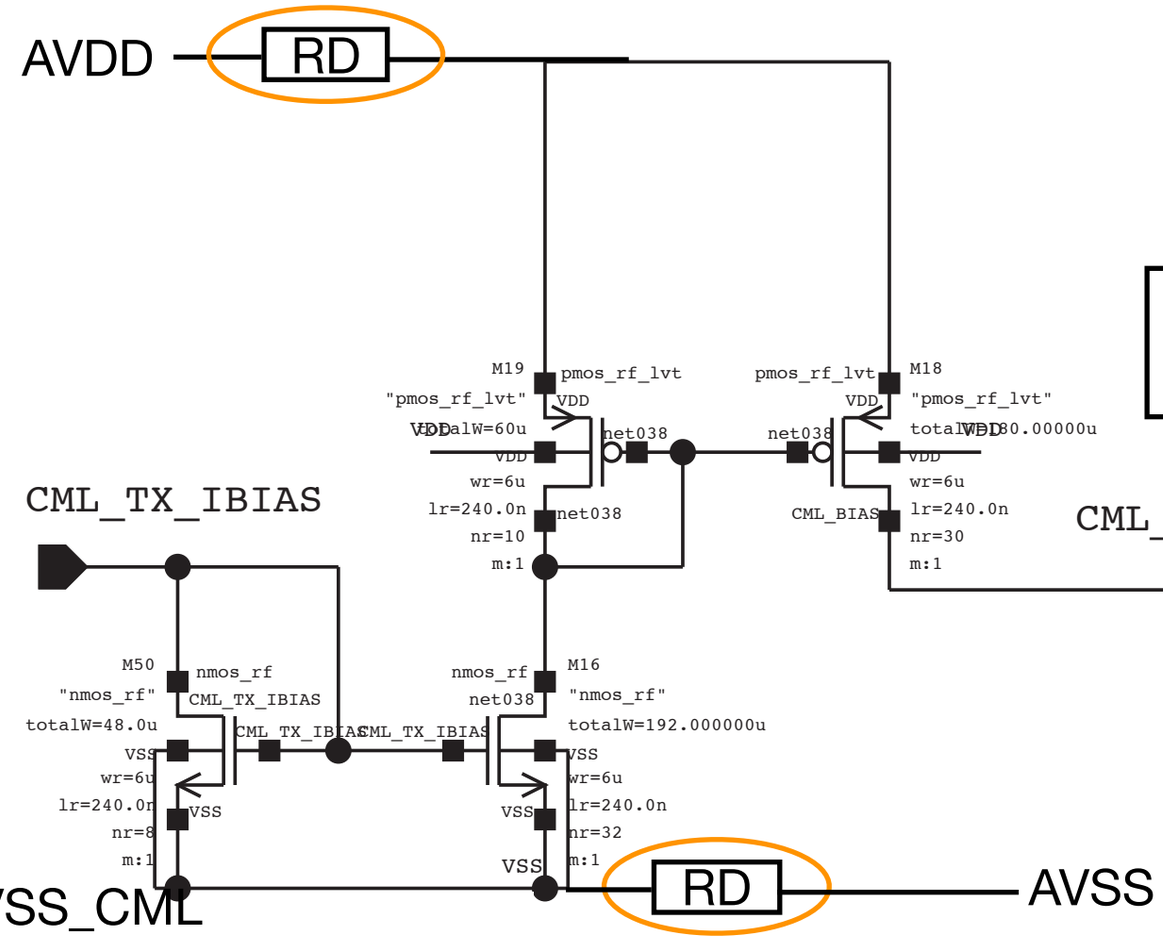
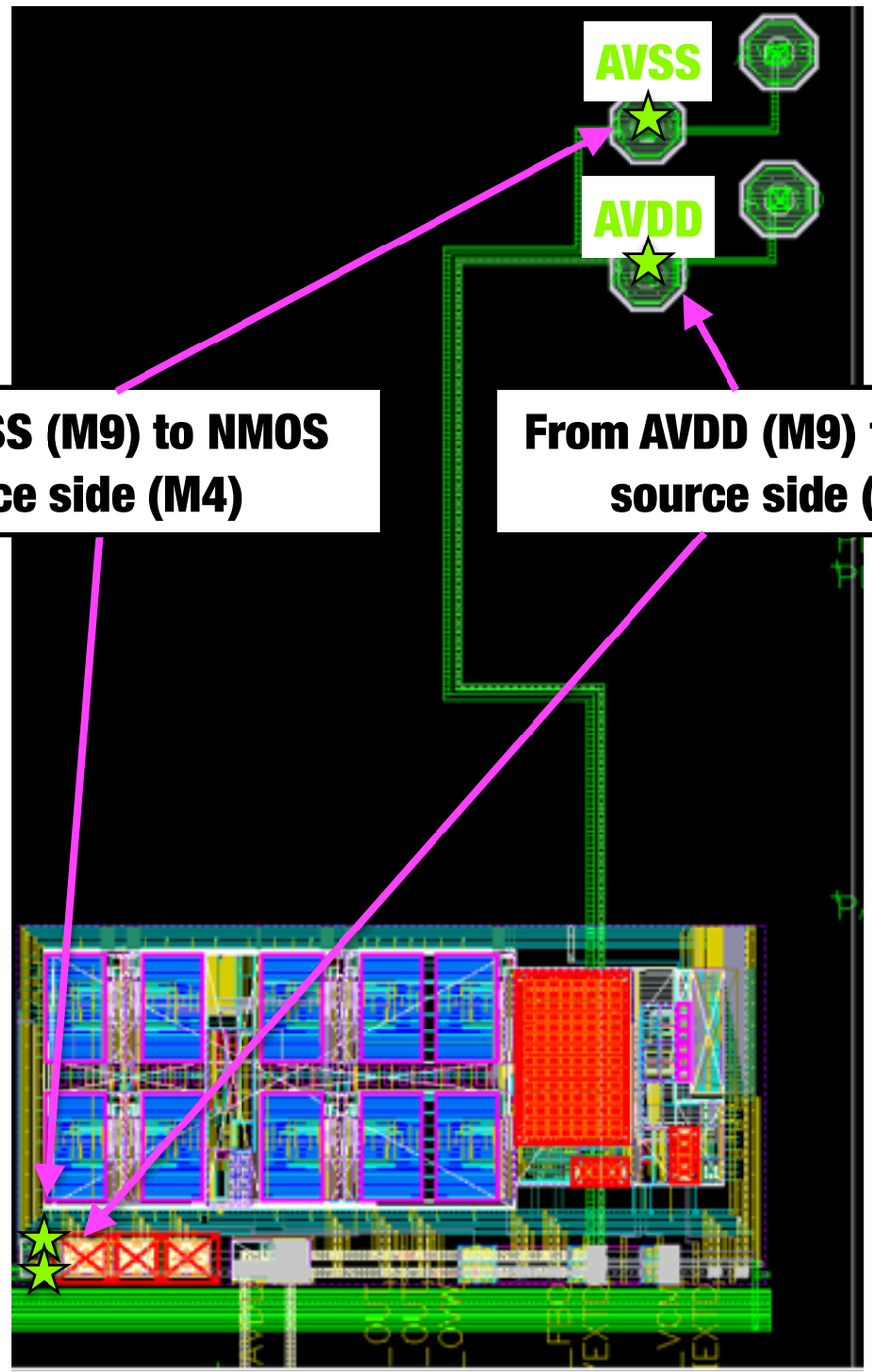
- checked serial resistances of AVDD and AVSS lines



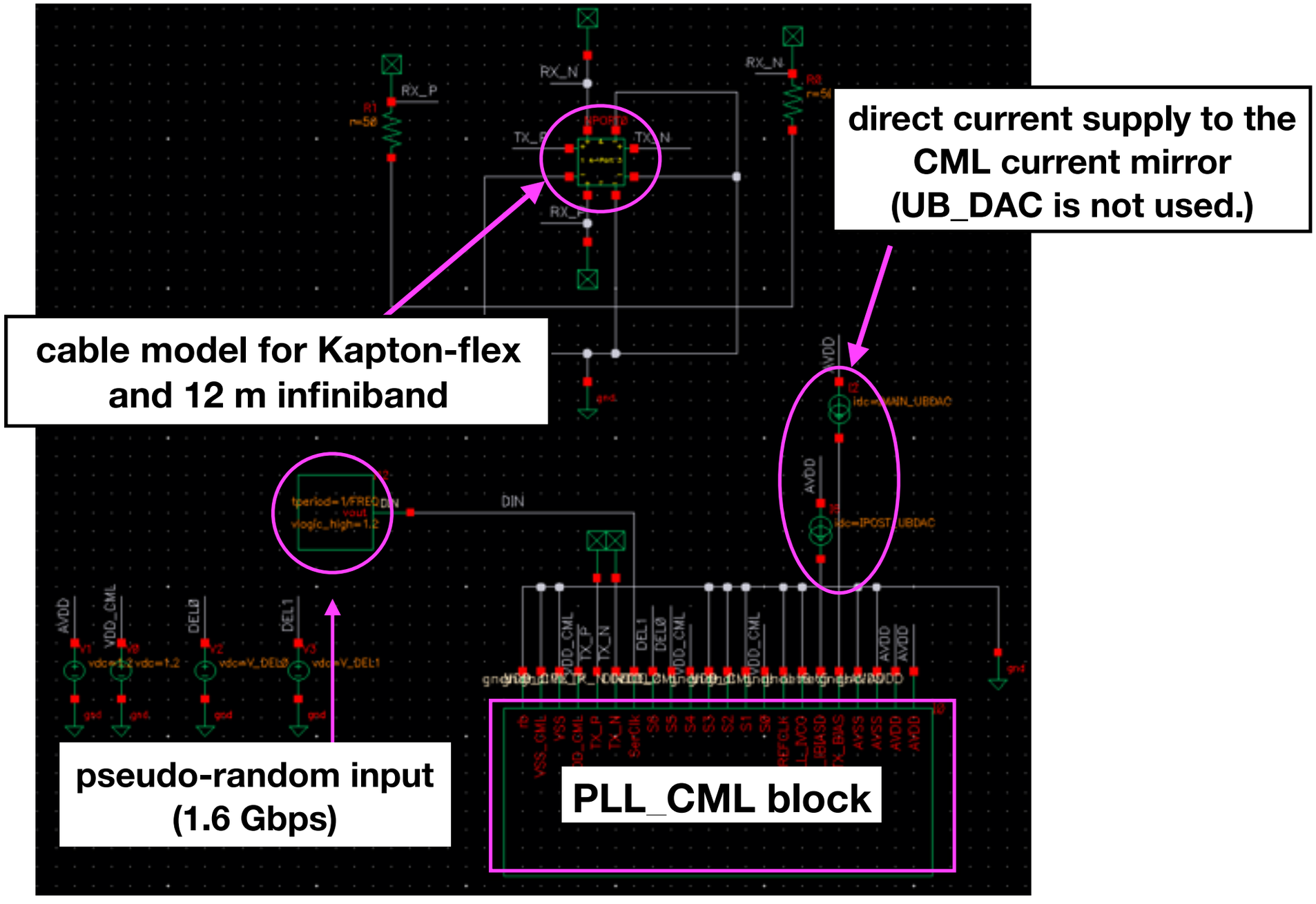


3.02 Ω

2.40 Ω

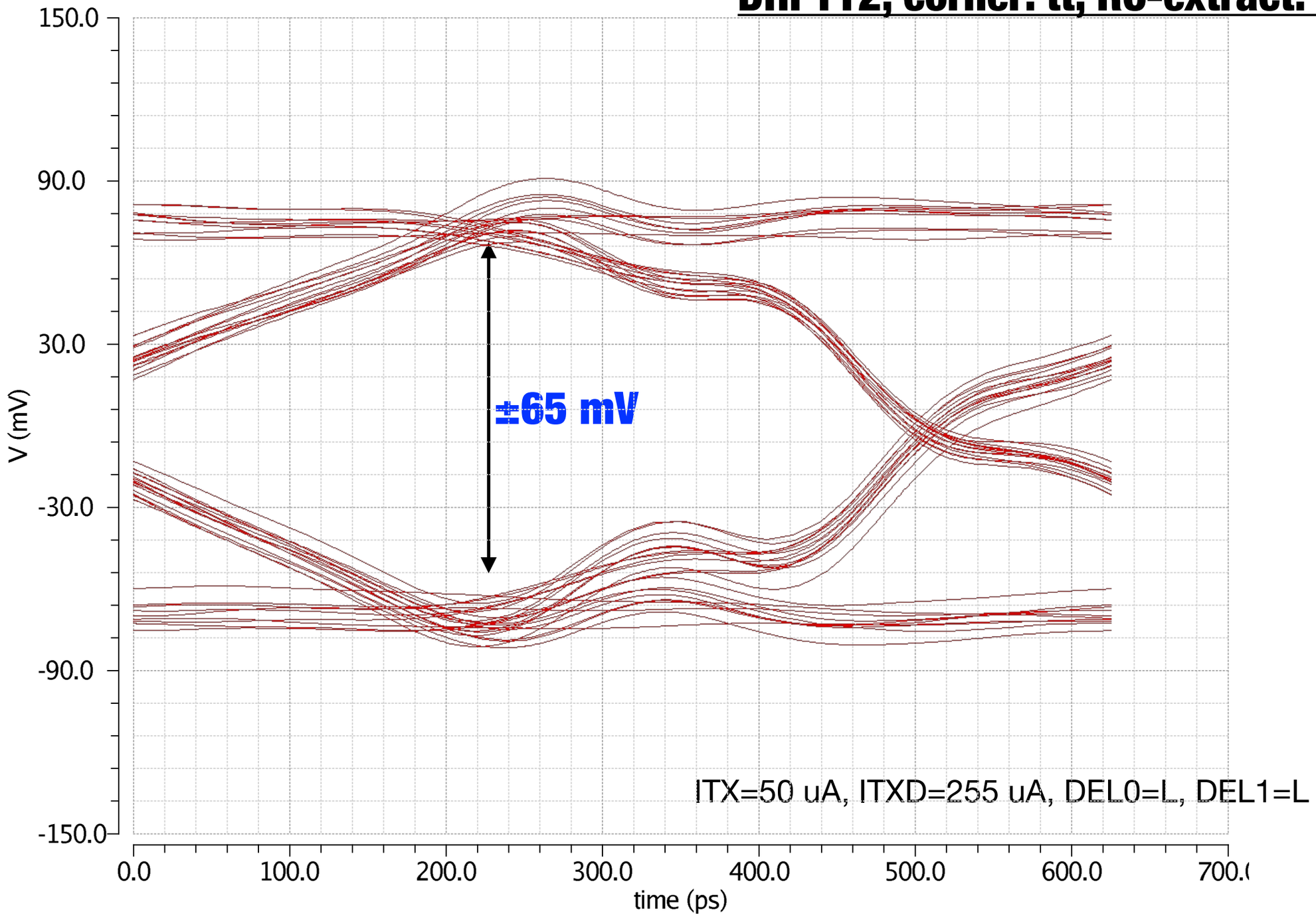
Test bench for CML TX with cable model

- cable model attached to the CML outputs
- pseudo-random input to check only CML block (PLL is not included)



Eye-diagram with extracted model

- extracted simulation with cable model



Eye-opening improves more with optimal bias setting.