DHPT 1.1 CML Driver Issues

Hans Krüger

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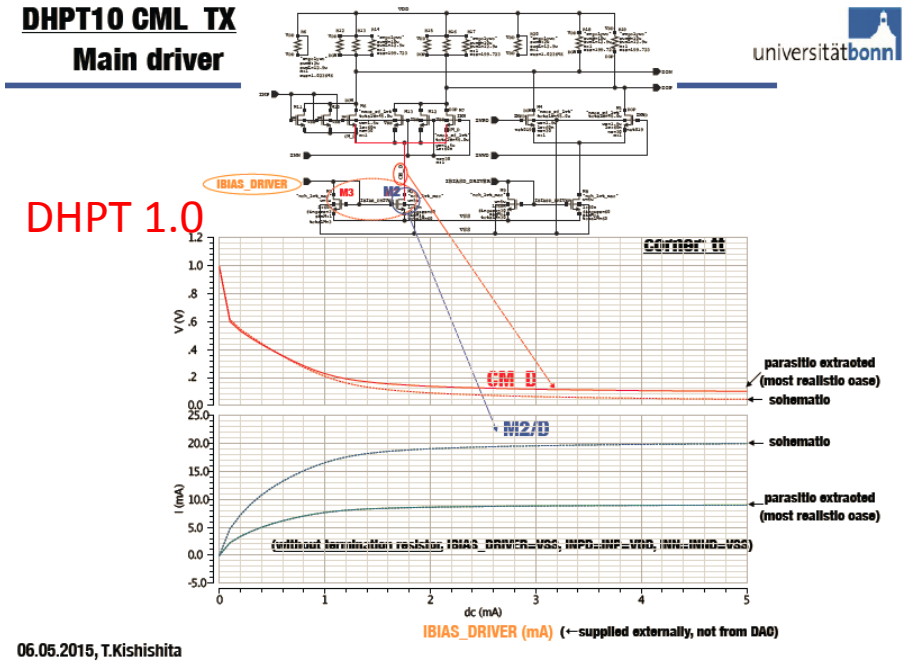
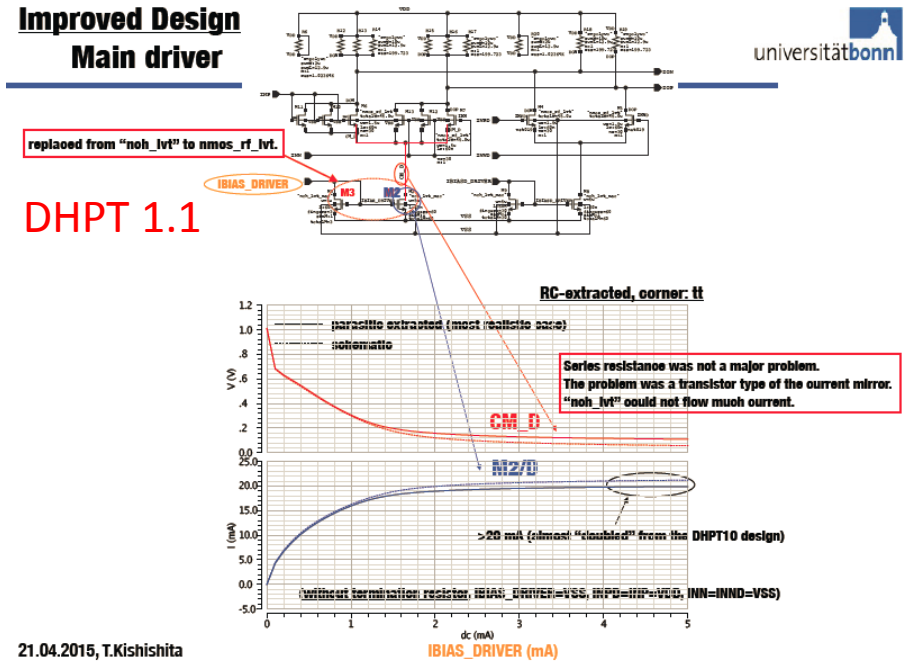
DHPT CML Driver

- Changes from DHPT1.0 to DHPT1.1

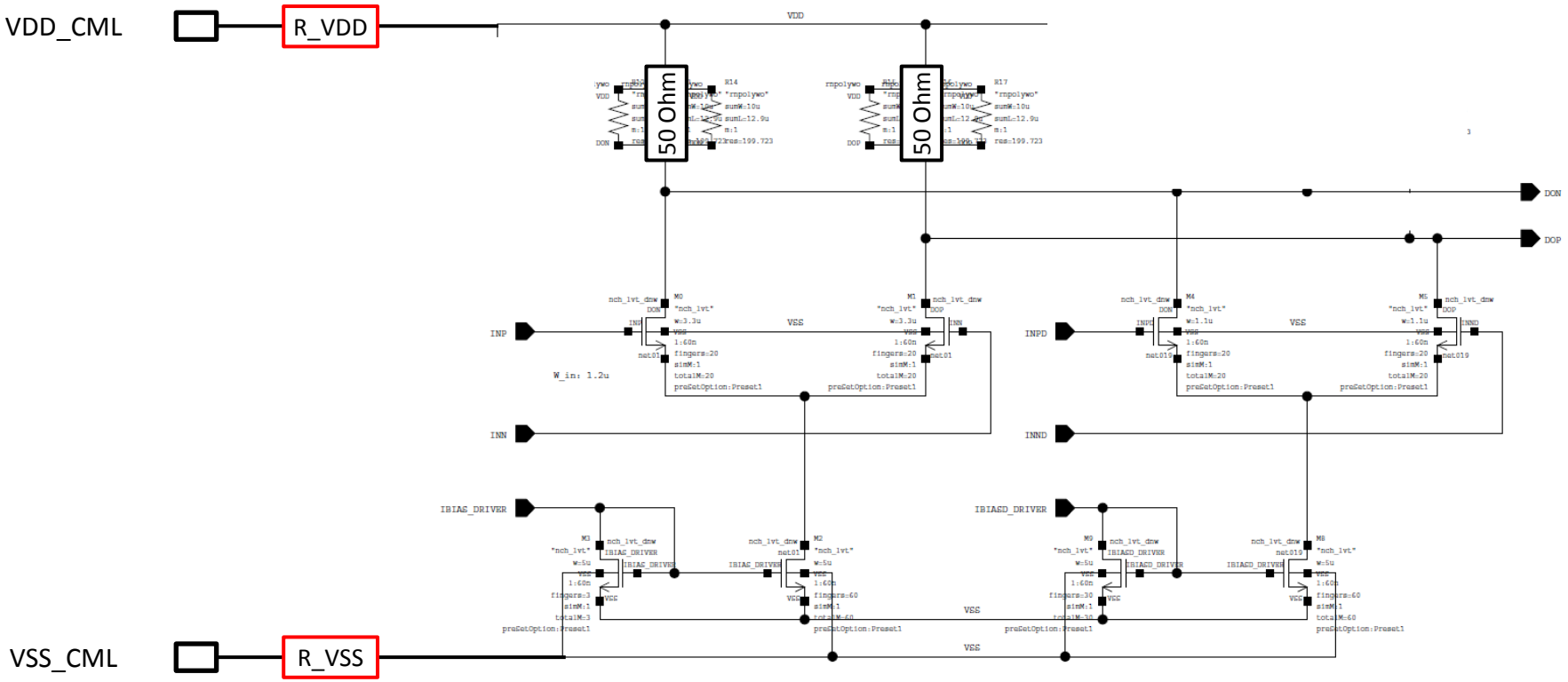




- Layout extracted with all parasitic elements
- Current in the main stage expected to be ~20mA after improvement of the transistor layout
- However measurements on DHPT 1.1 indicated ~10mA only

DHPT CML Driver

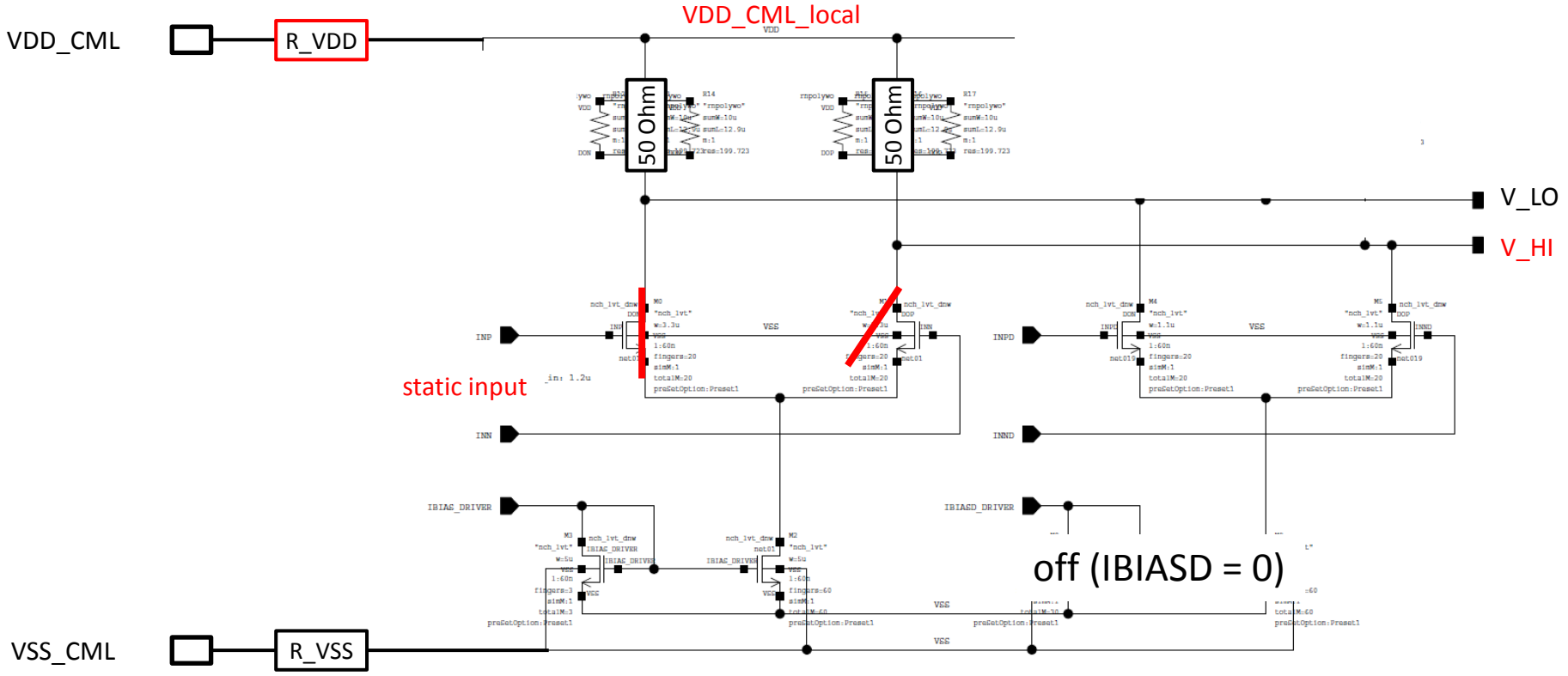
- Possible explanation: layout extraction underestimated the **parasitic** resistances R_VDD and R_VSS on the power lines



Measurement of the Parasitic Resistance R_VDD

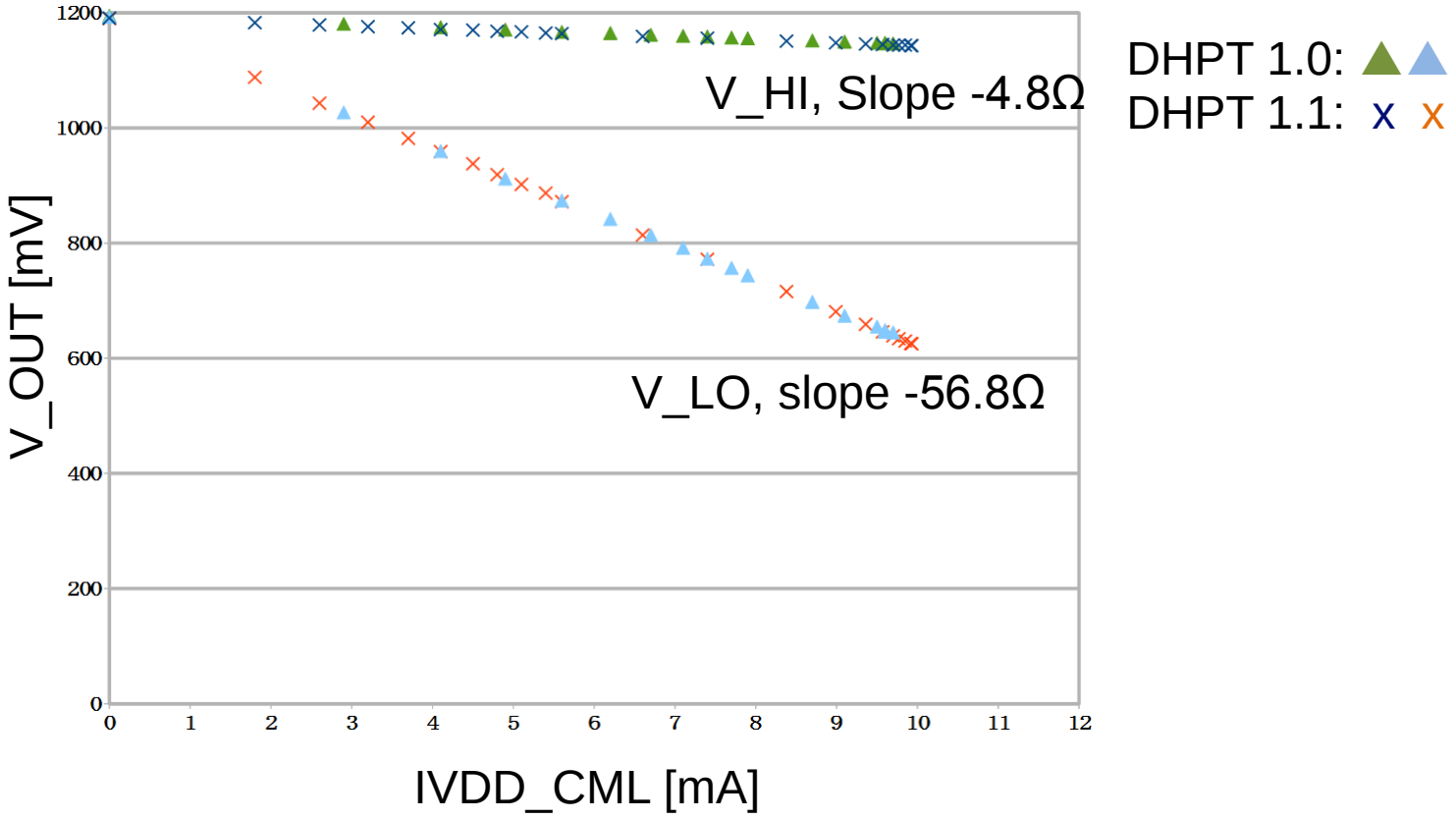
- Measure V_HI as a function of I_VDD_CML by changing IBIAS
  - no termination at driver output
  - no data line switching

➔ V_HI = VDD_CML_local = VDD_CML – I_VDD_CML x R_VDD



Measurement of the Parasitic Resistance R_VDD

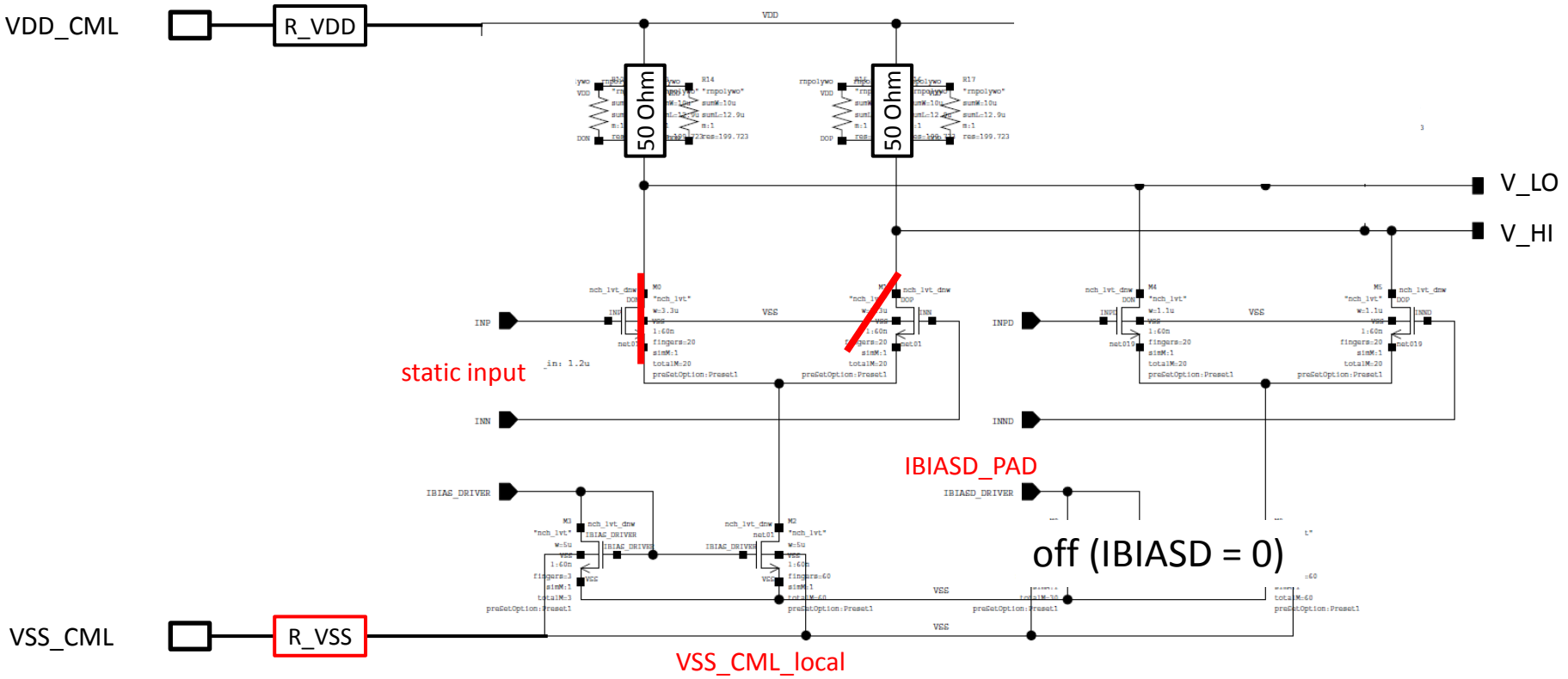
- Measurements indicate a parasitic resistance of about 5 Ohm in the VDD_CML line
- This is in agreement with the extraction of the parasitic elements of the layout, however this does not explain the loss of drive strength.



Measurement of the Parasitic Resistance R_VSS

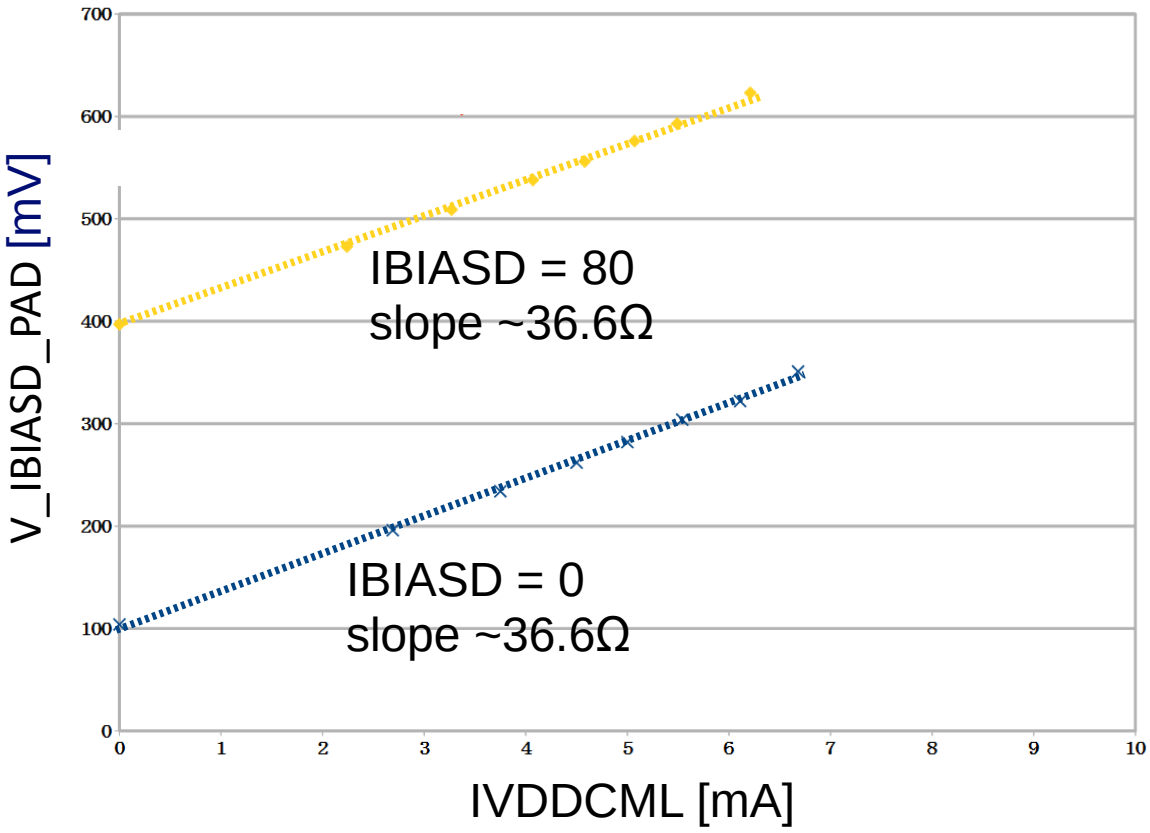
- Measure V_IBIASD_PAD as a function of I_VDD_CML by changing IBIAS, no termination at driver output

➔ V_IBIASD_PAD = VSS_CML_local + const = VSS_CML + I_VDD_CML x R_VSS



Measurement of the Parasitic Resistance R_VSS

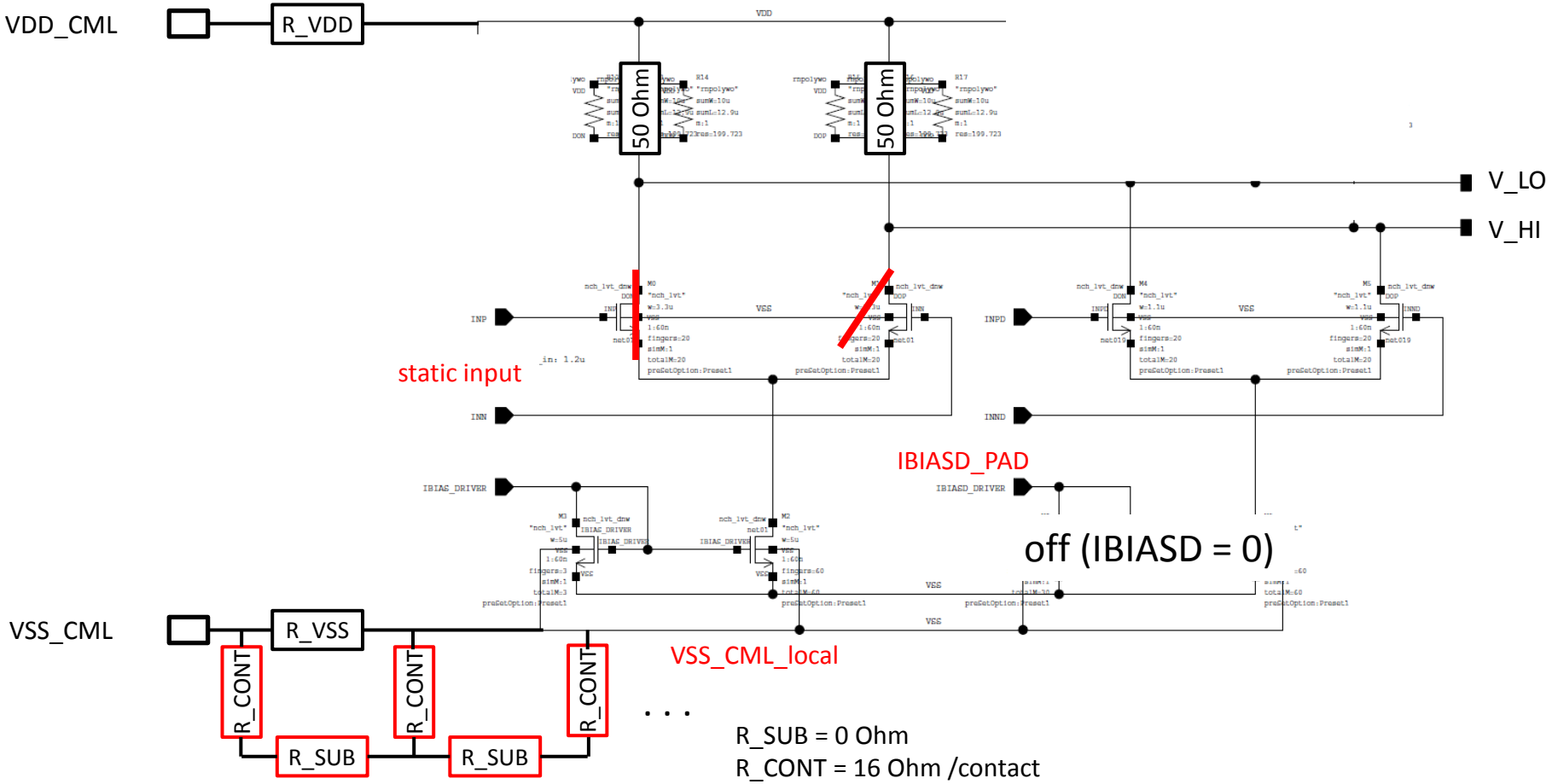
- Measurements indicate a parasitic resistance of about 36 Ohm in the VSS_CML line
- This is **not in agreement** with the simulation of the extracted layout which also shows ~5 Ohm parasitic resistance



Issue with the RC-extraction of the layout

- The extraction tool models the silicon substrate as a perfect conductor (R_SUB = 0 Ohm) and VSS_CML ins connected to the bulk with a lot of substrate contacts

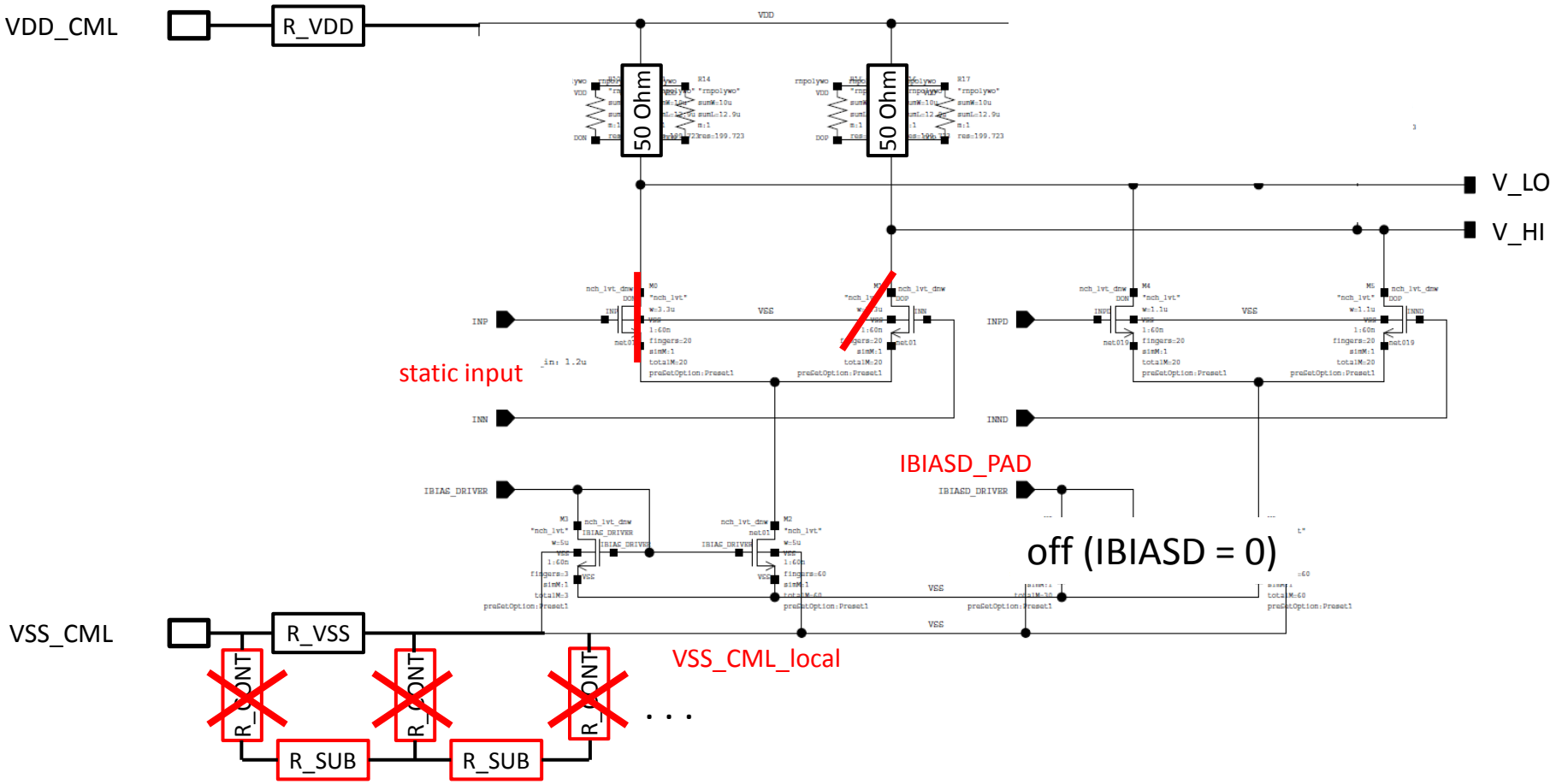
➔ Underestimation of the resistance in VSS_CML



Proof of the Explanation

- We removed the substrate contacts in the layout and extracted the parasitics again

➔ R_VSS_CML ~ 30 Ohm



CML_TX Layout toward DHPT12

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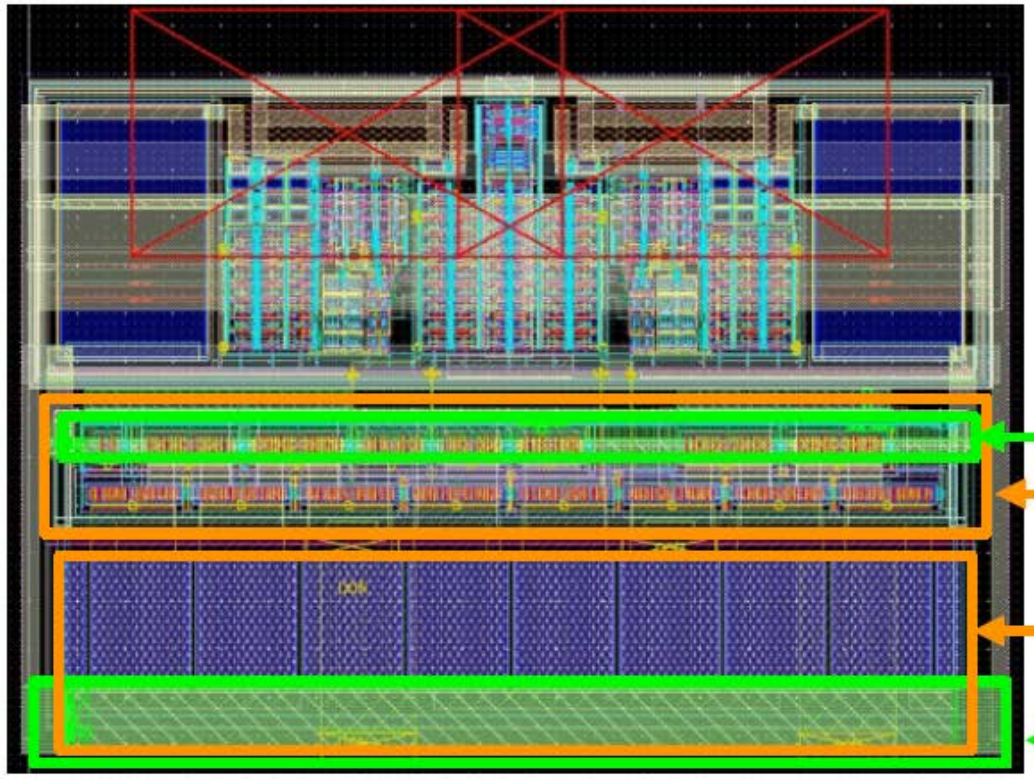
- vertical connection (M2→M9 for VDD_CML and M4→M9 for VSS_CML
- separate VSS and PSUB for Driver current mirror and switches
- avoid M1 connection between separate circuit blocks



I.Kishishita

Serial-Resistance

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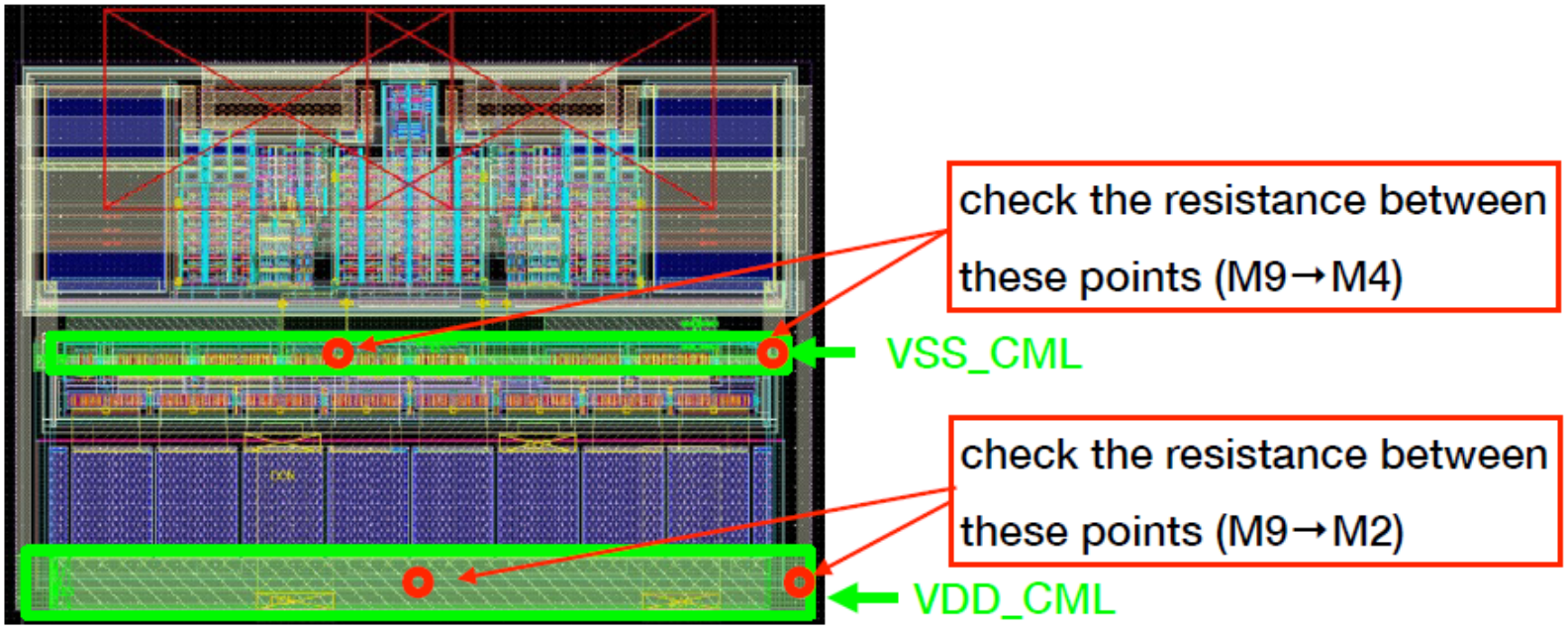

	Assura, typical	Assura, worst	Calibre, typical
VDD_CML	49.3 mΩ	66.5 mΩ	53.0 mΩ
VSS_CML	114.1 mΩ	151.4 mΩ	115.2 mΩ

ΔR_{serial}: ~30% corner dependence, and ~10% between Assura and Calibre

I.Kishishita

Summary

- The parasitic resistance in the power lines of the CML driver was underestimated (~5 Ohm as extracted would have been acceptable but the measurements indicated 36 Ohms in VSS_CML).

- The extraction tool underestimated the resistance of the VSS line because VSS is connected to the substrate which is modeled as a perfect conductor (the real substrate resistivity is 10 Ohm · cm)➔ full R-C substrate modelling is complicated and usually only done for pure RF circuits

- By the removing the substrate contacts, the extraction tool gives the same parasitic resistance as measured.

- Weak spots in the power line layout have been indicated and fixed.

- During the review of the layout hot spots with too high current densities (→ long time reliability) were spotted and fixed as well

Outlook

- We are planning a re-submission of the DHPT (→ 1.2) with an improved power layout of the CML driver

- The DHPT 1.1 is still usable for pilot (and PF) module production

- The re-design is the chance to still include changes in the digital part, in case current system test (gated mode etc.) should conclude that.

- Timeline
  - TSMC 65 MPW tape-out dates (11 weeks turn-around time)
    - March 2 (too early)
    - March 30 (possible, if no digital re-design would be necessary)
    - April 27 (possible, still **little time for digital re-design**)
    - June 1 (too late...)
  - DHPT 1.2 available: July ’16 (at the latest, constraint by module production)