Gated Mode Testing with PXD9 Pilot

20th International Workshop on DEPFET Detectors and Applications
Kloster Seeon, May 13th 2016

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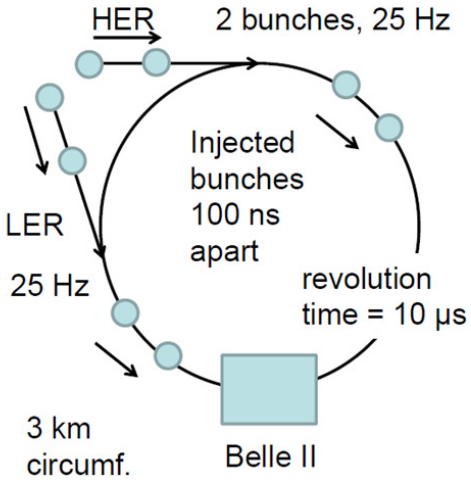
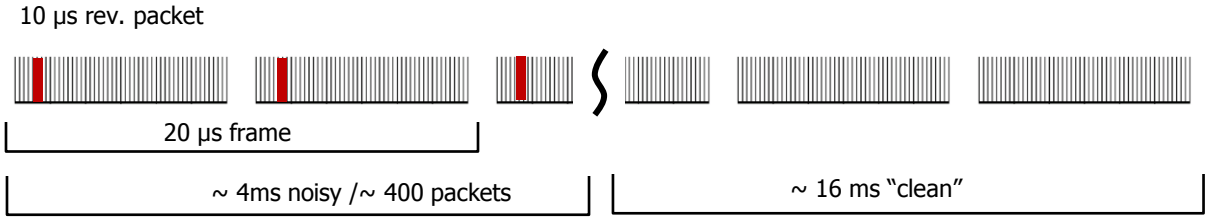
DEPFET shutter at SuperKEKB



10µs packets with 2503 bunches , 200 ns gap in-between (TDR)



- continuous injection → ~ 400 revolutions with two noisy bunches (100ns apart) every 20 ms
- DEPFET integrates two trains, these noisy bunches would blank the frames → 20% loss of data

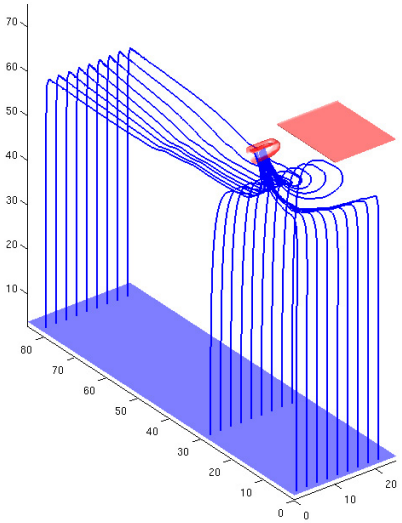
- the best solution: gate the DEPFET during the passage of the noisy bunches
- ~100ns gate, with some rise and fall times, twice per frame → 2x2µs of 20 µs blind
- assuming 4 ms relaxation time (not clear), ~200 consecutive frames with gate cycles

- DEPFET operation mode during gating: DEPFET off, Clear active (Vgs=3 .. 5V, Vclear=16 .. 20V)

DEPFET gated operation mode

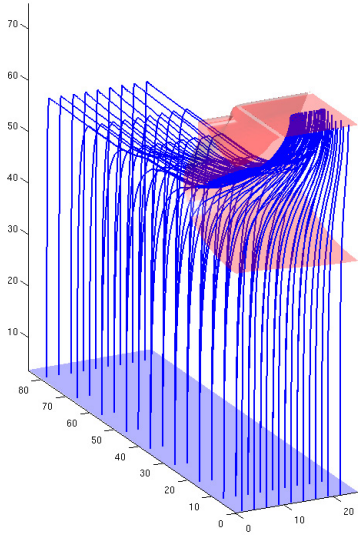
Switching to gated mode:

» DHE receives signal from acc., sends "veto" → DHPT switches to gated sequence → controls Switcher
» DCD operation mode remains untouched



Normal charge collection

» Vgs=4V, Vclear=5V
» all signal charge collected in internal gate



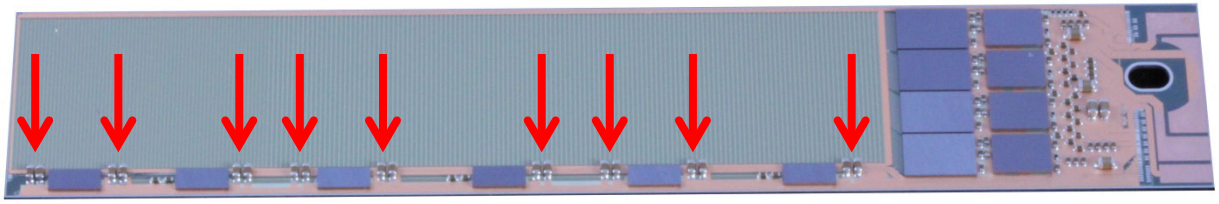
Gated mode

» Vgs=4V, Vclear=20V
» all signal charge dumped to *Clear*

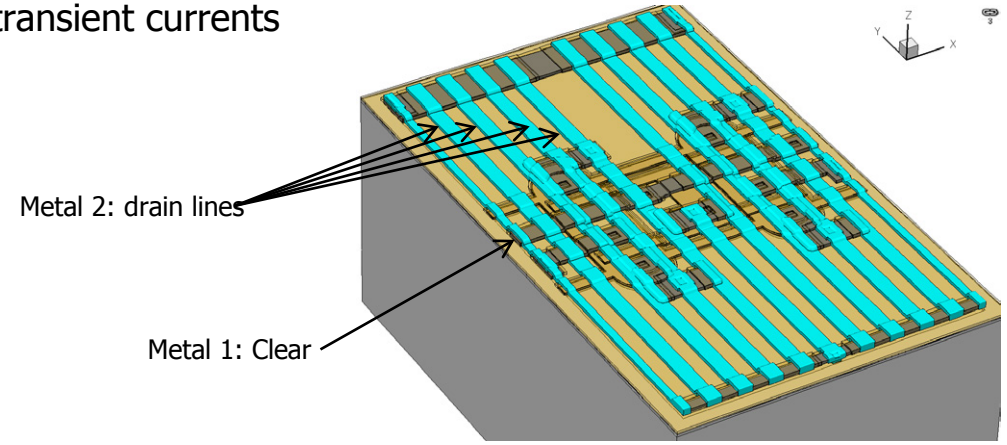
Challenge: switch all *Clear* contacts in the matrix from ~5V → ~20V
shown on small matrix, but as expected, it's more difficult on the pilot modules

Two main aspects of the gated mode

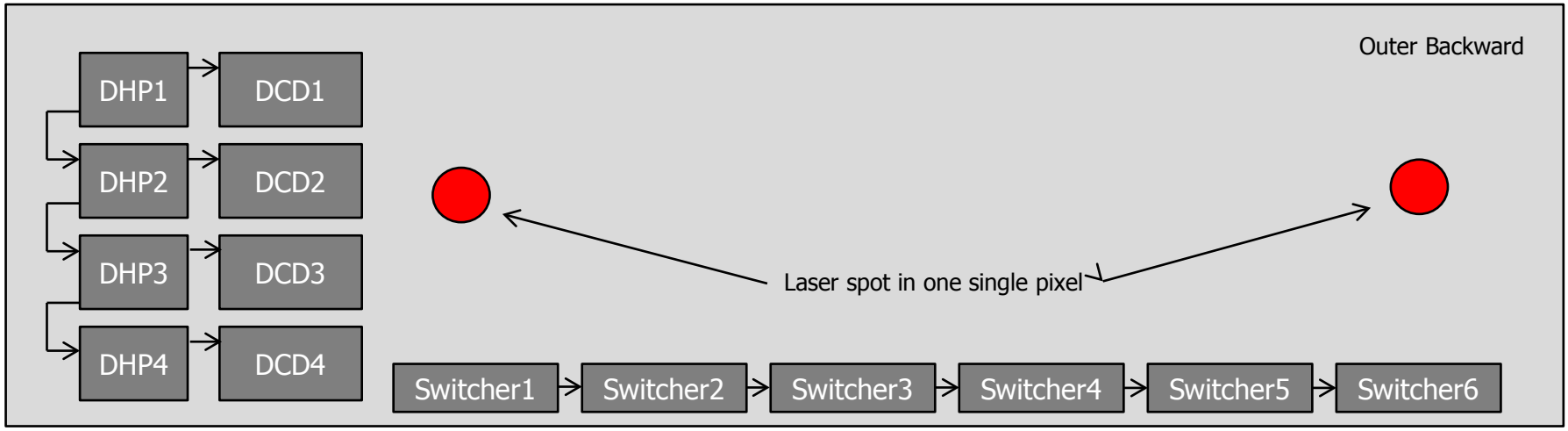
- **Fast switching of the clear signal (5V→20V)**
  - 26nF of the entire matrix → 135pF for one SWB channel (~4nF for one SWB)
  - To reduce peak current
    - Switch in groups: each SWB has **4 groups**, switched on and off consecutively
  - Provide current by local capacitors: each SWB has 100nF SMDs placed on the balcony

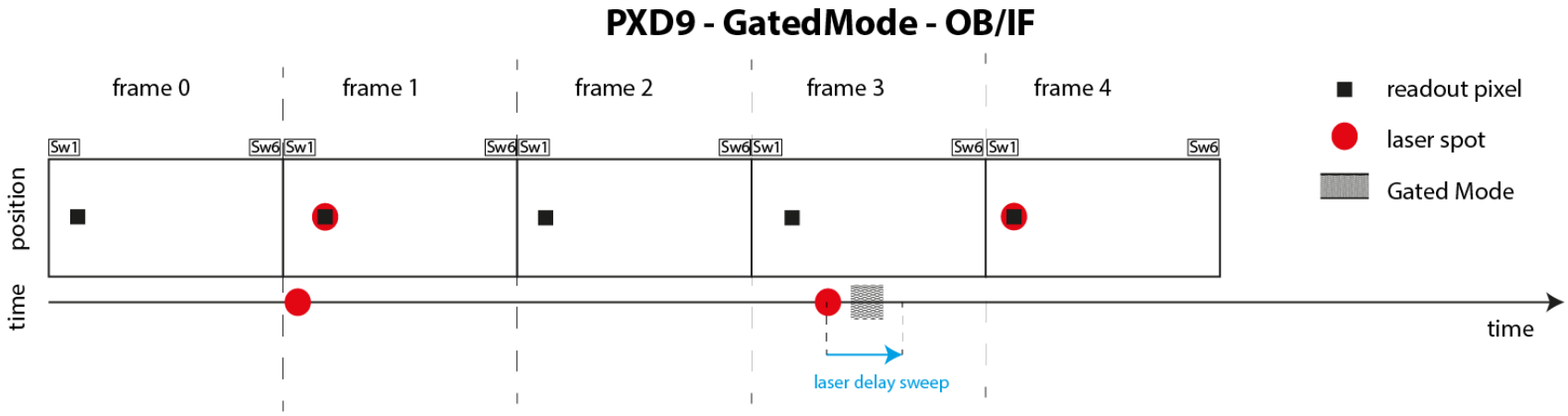


- **Analogue part of the DCD gets „upset" during gated mode**
  - Capacitive coupling between Clear and Drain lines (input of the DCD)
  - Voltage drop on supply due to high transient currents



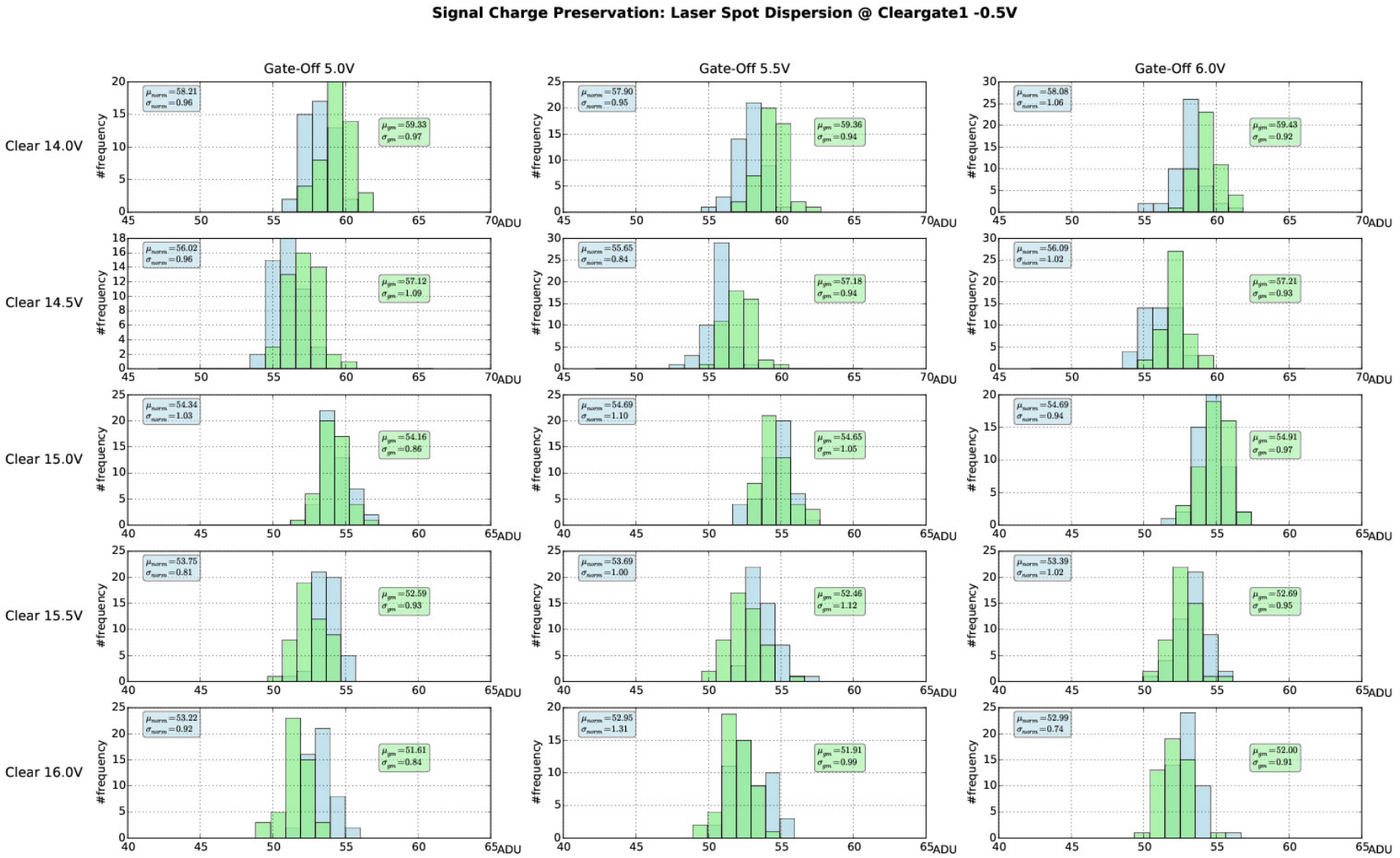
Laser tests





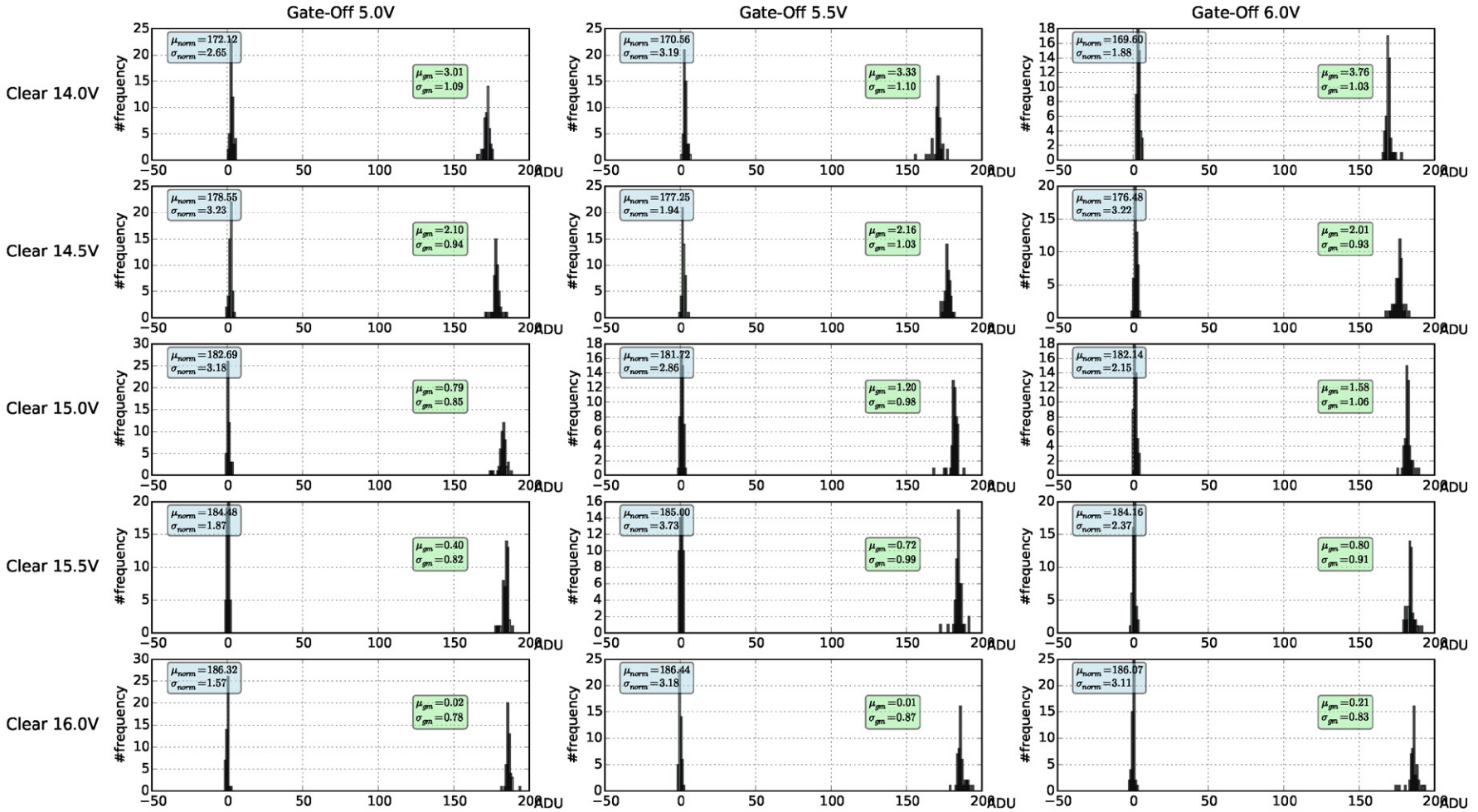
frame 0: pedestals
frame 1: pixel shows signal of the laser impinging in frame 1 (right before the pixel is read)
frame 2: pixel shows Clear efficiency
frame 3: pixel shows pedestal value; gated mode is switched on ; laser is impinging
frame 4: pixel shows signal (charge conservation & junk charge prevention), depending on timing of laser

Voltage Scan: SCP – Signal Charge Preservation



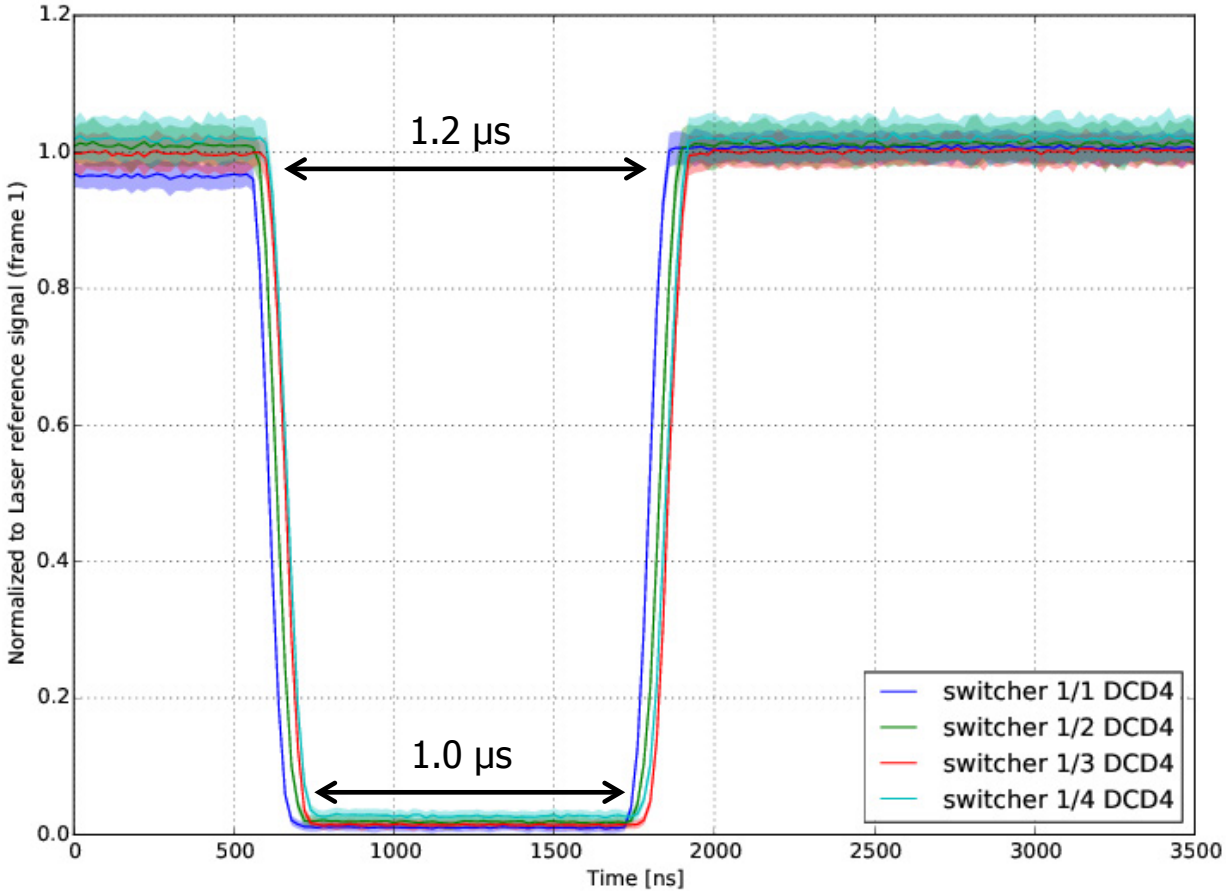
DCD analog CM off

Voltage Scan: JCP – Junk Charge Prevention, CCG =-0.5V

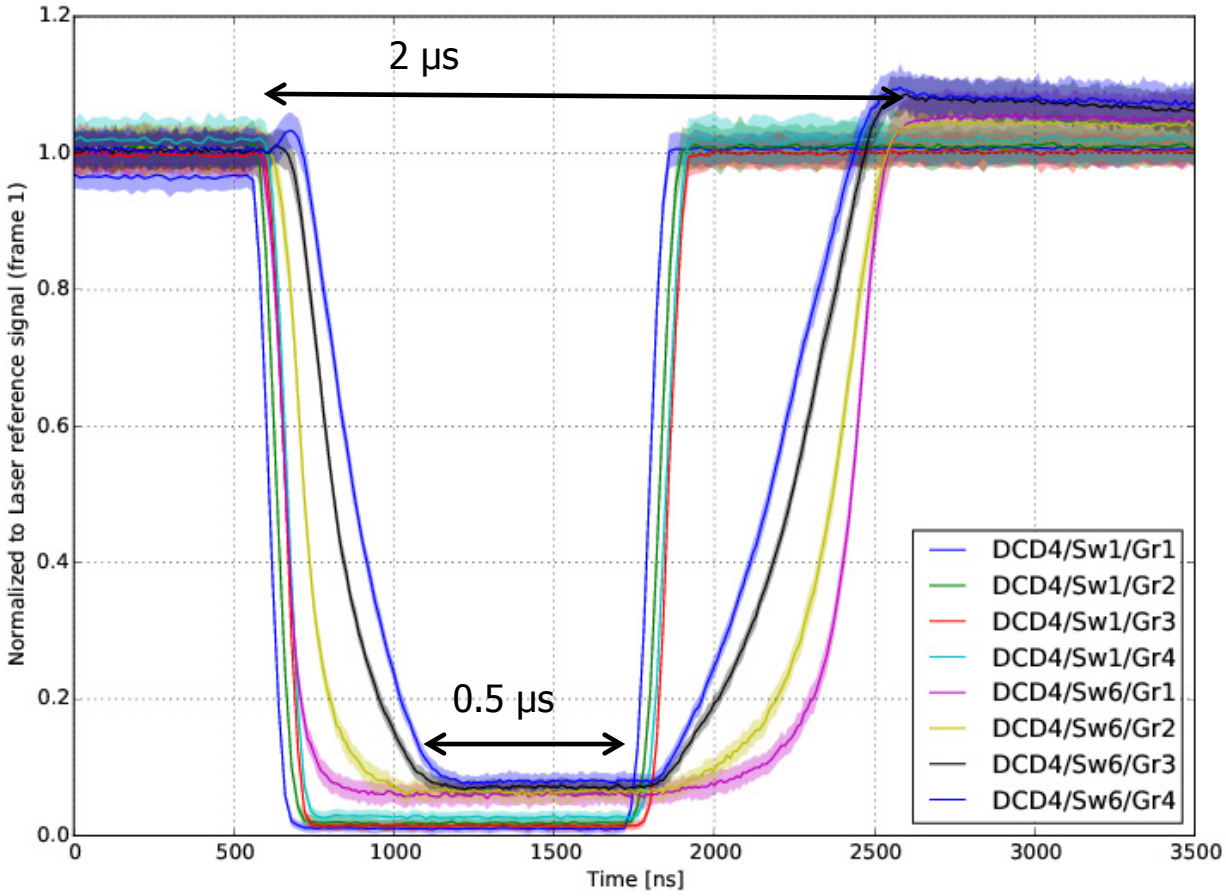


DCD analog CM off

Laser delay scan, SWB1, group1 to 4

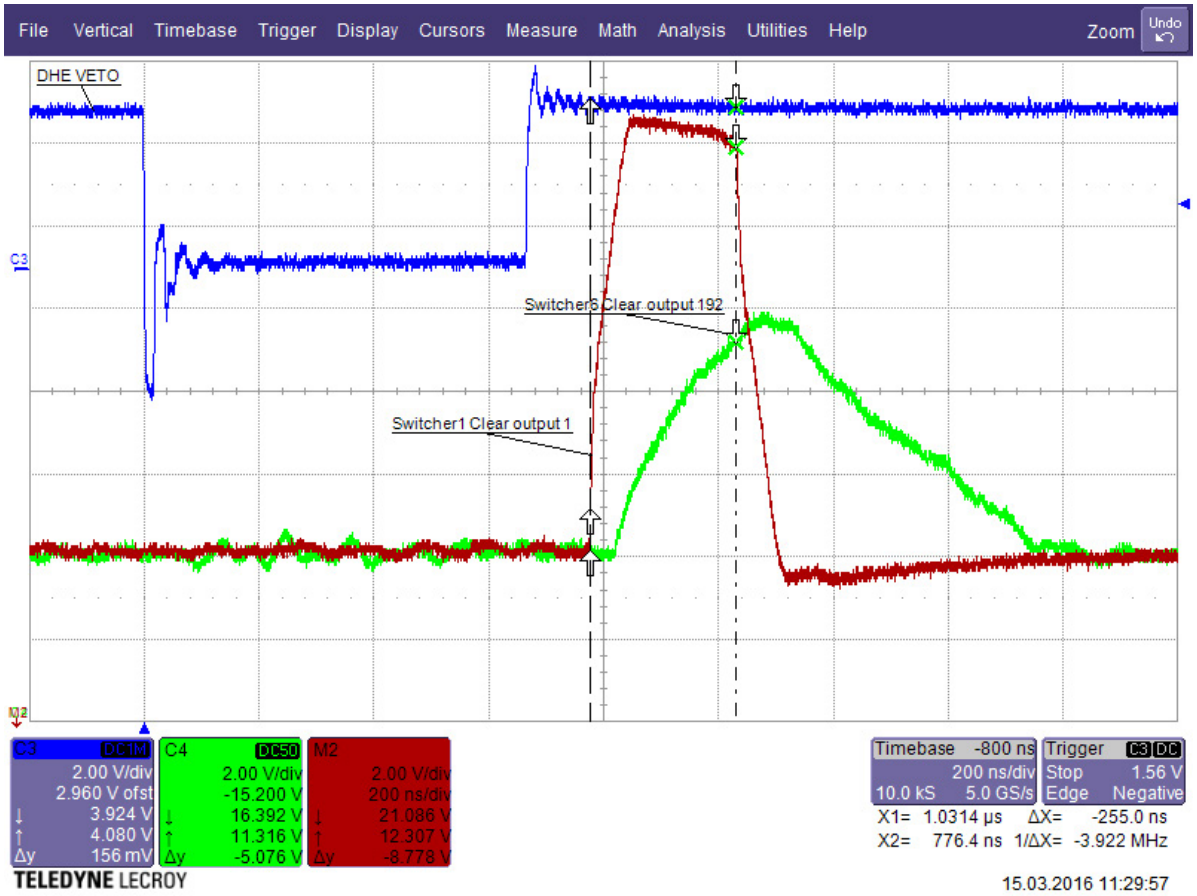


Laser delay scan, SWB1 and SWB6 , group1 to 4



Data compromised for about 2 µs for 500ns gate, in principle okay, but …

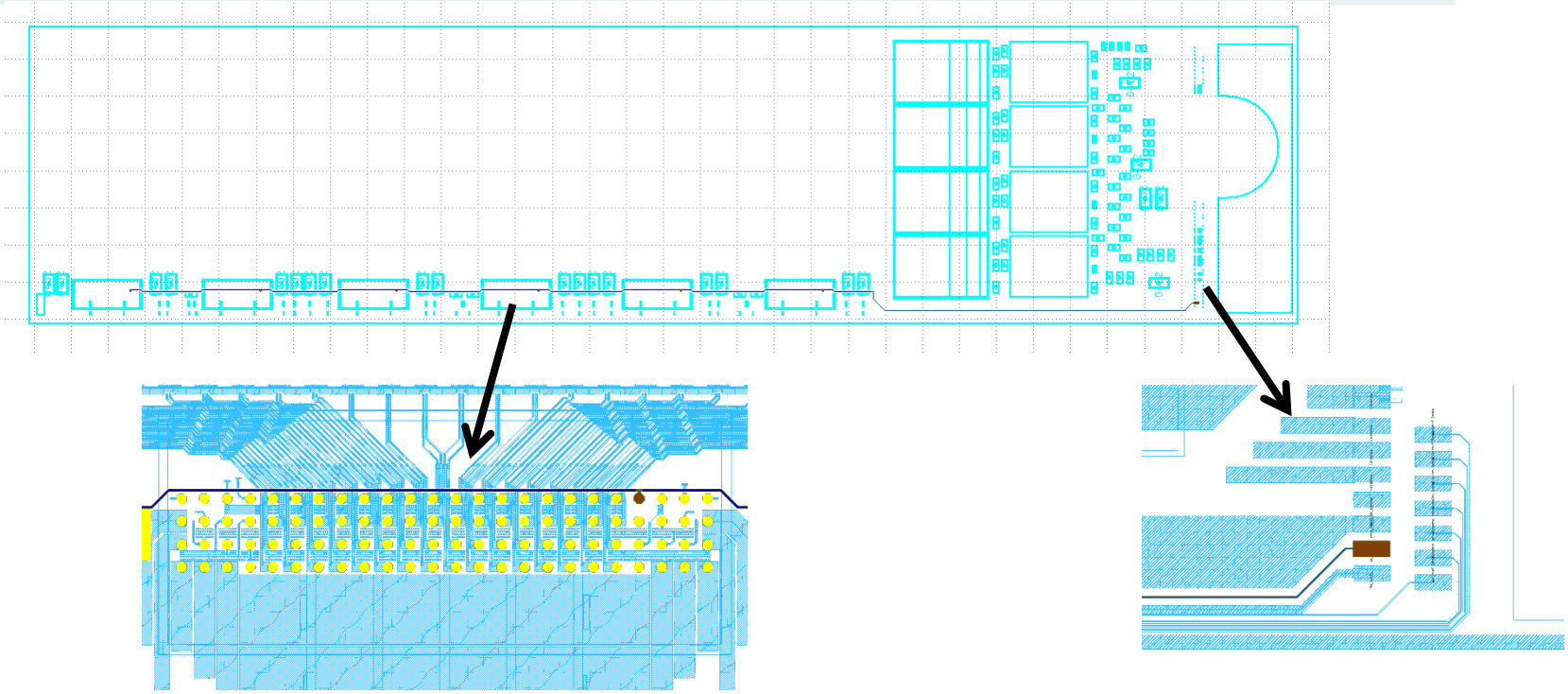
Direct measurement of the *Clear* pulse



Two reasons for this identified

1. voltage drop along Vsub line on the balcony (SWB) causes worse behaviour of output driver of last SWB
2. poor quality of the decoupling caps on the balcony

SWB V_sub routing change

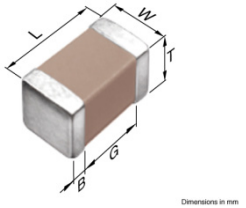


- V_sub net has to support higher current as expected from SWB docu (1.4 mA instead of 0.1 mA)
- change line width to minimize voltage drop
- Currently 14µm at EOS in metal2 and 14µm at balcony in metal1
- Modifications
  - @ EOS in metal2 to 70µm width
  - @ balcony additional Cu line in parallel to metal 1 line

Changes done for PXD9-7

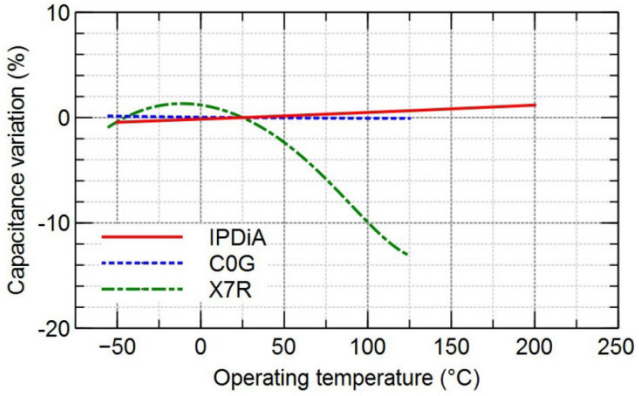
- **10x reduction of line resistance → improved SWB performance, less degradation along switcher chain**

Decoupling caps on balcony

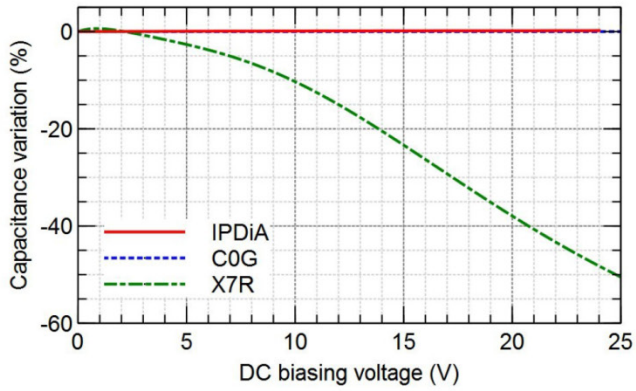


- 100nF, 20V, X5R ceramic, standard SMD 0402
  - Capacitance highly dependant on DC bias voltage and frequency
  - Effectively a few tens of nF at 20V instead of 100nF as expected
  - There are no better ceramic capacitors with this values and with this size on the market!!

- New, high-end silicon capacitors (~50x more expensive!!)
  - Makes use of novel 3D via technology (IPDiA, France)
  - 47nF/30V, and 100nF/11V, all SMD 0402
  - Available, currently under test
  - Less material … CTE fits better to our module …

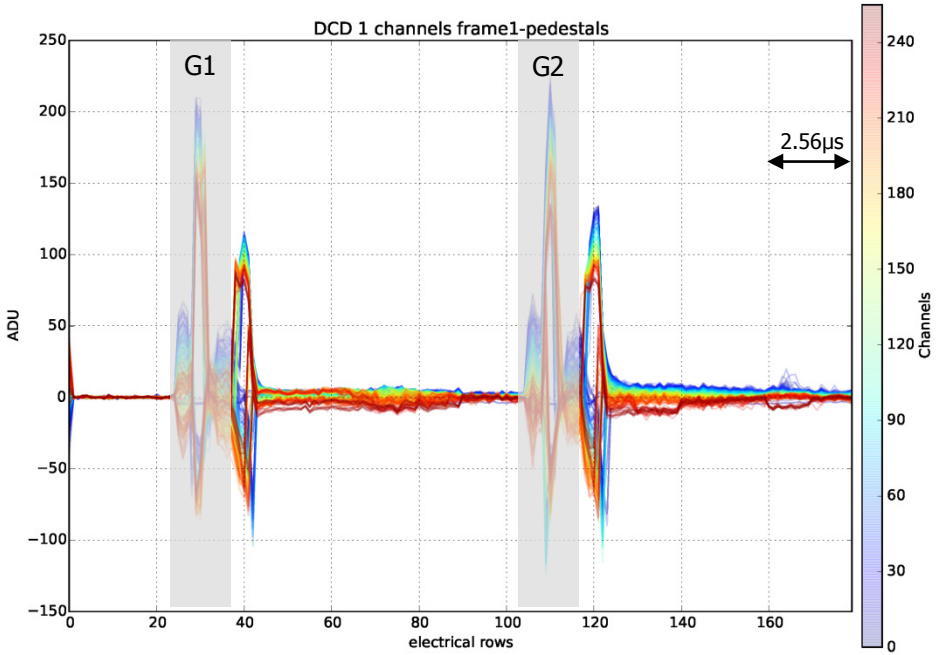


Capacitance variation vs temperature (for SiCap and MLCC technologies)



Capacitance variation vs DC biasing voltage (for SiCap and MLCC technologies)

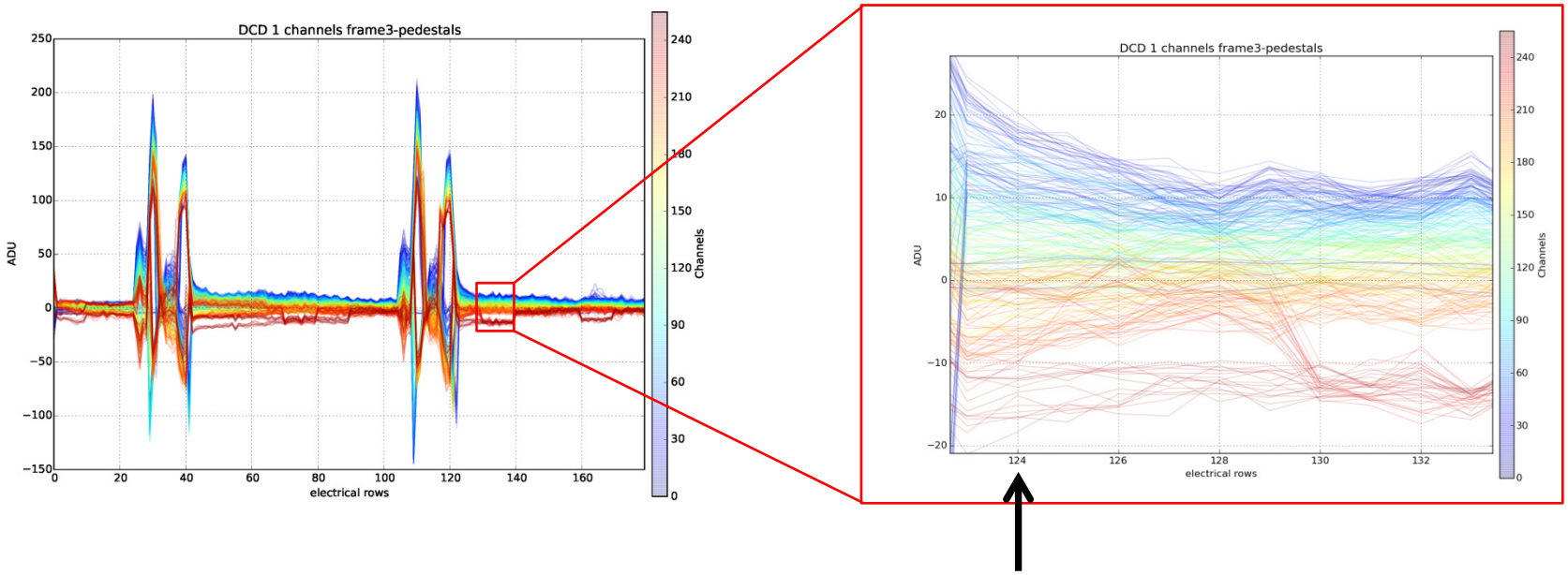
Back to normal: repetitive gated mode



- Pedestals of frame ~1 (pedestal mask in DHPT to define rows for data taking)
- 256 channels of one DCD in one plot
- Switch to gated mode twice per frame, each 1.66 µs (can be shorter, just for test..)
  - ↳ **gate1: row 24 to 36** **gate2: row 104 to 116** (one row corresponds to 128ns)
    (Veto signal in the DHE block RAM activated from row 22 to 36 - DHPT first word twice)

- Pedestals are higher after GM and spread gets bigger after 2nd GM sequence …

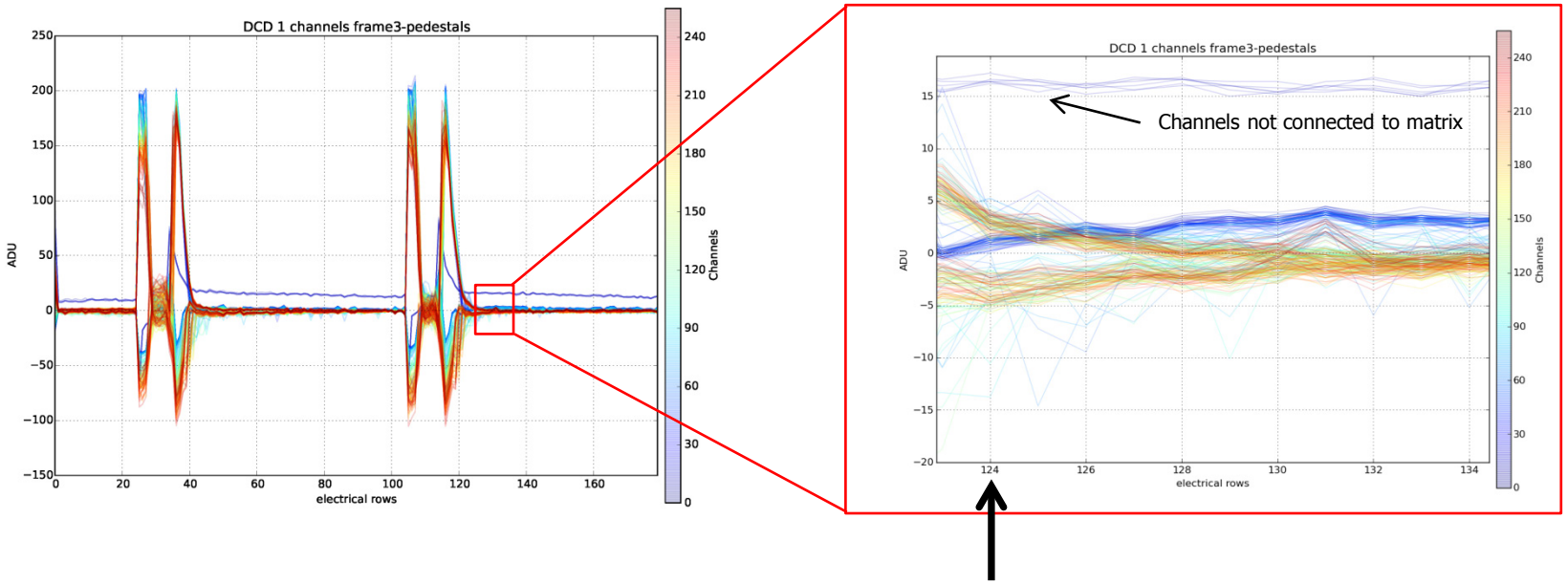
Closer look to the following frames



- Pedestals in the following frames still disturbed
- Pedestal spread at row 124 (~1µs after end of GM) still +/- 20 ADU
  - ↳ 100% occupancy!

- Try DCD analogue common mode correction!

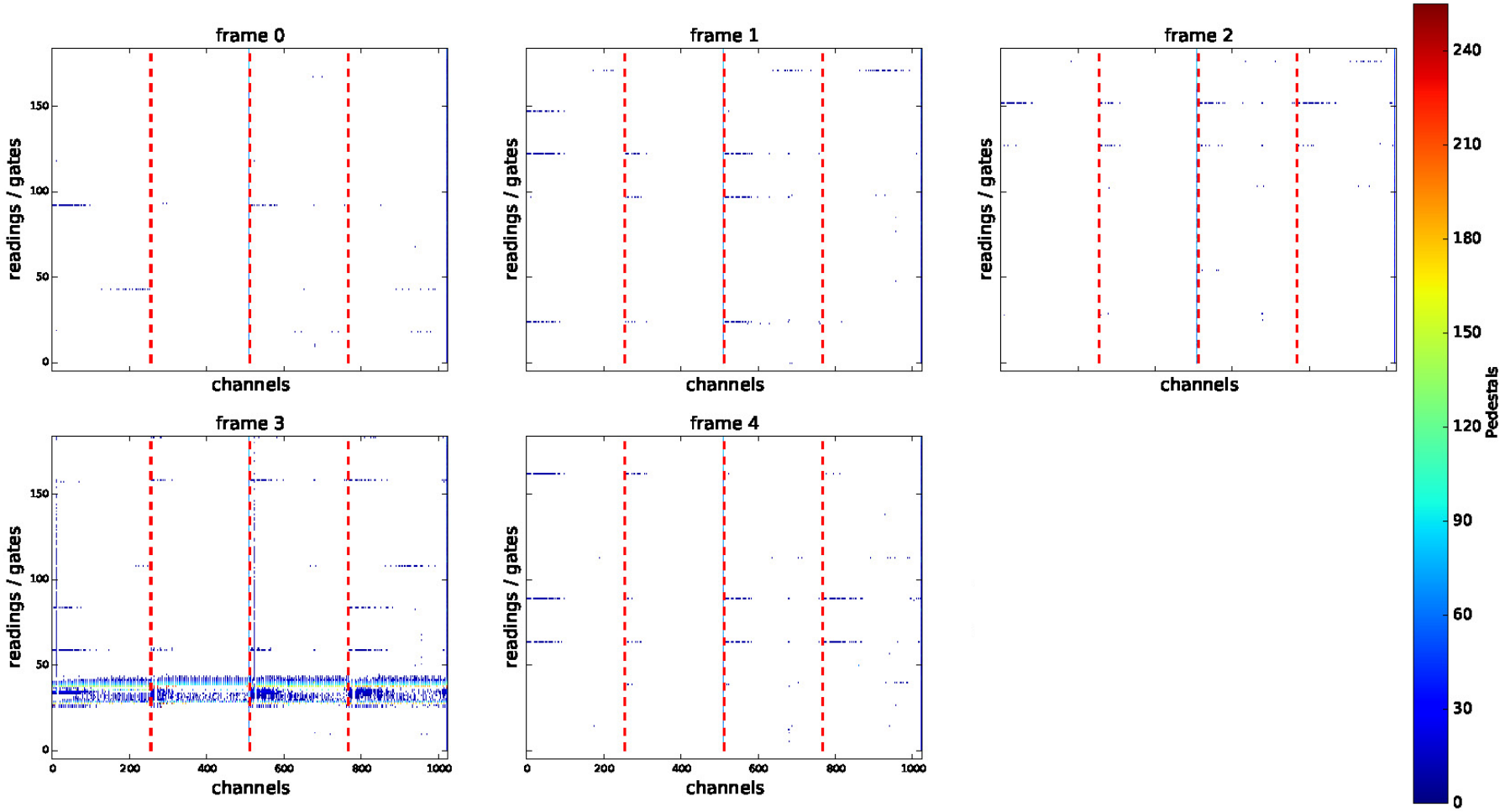
With DCD analogue CM correction



- Analogue CM correction in DCD really works, and it helps indeed!!
- Pedestal spread at row 124 (~1µs after end of GM) now at +/- 5 ADU
  - Possible to run with threshold >5
  - Further optimization (DCD parameters, ClearHigh voltage..) may further decrease this

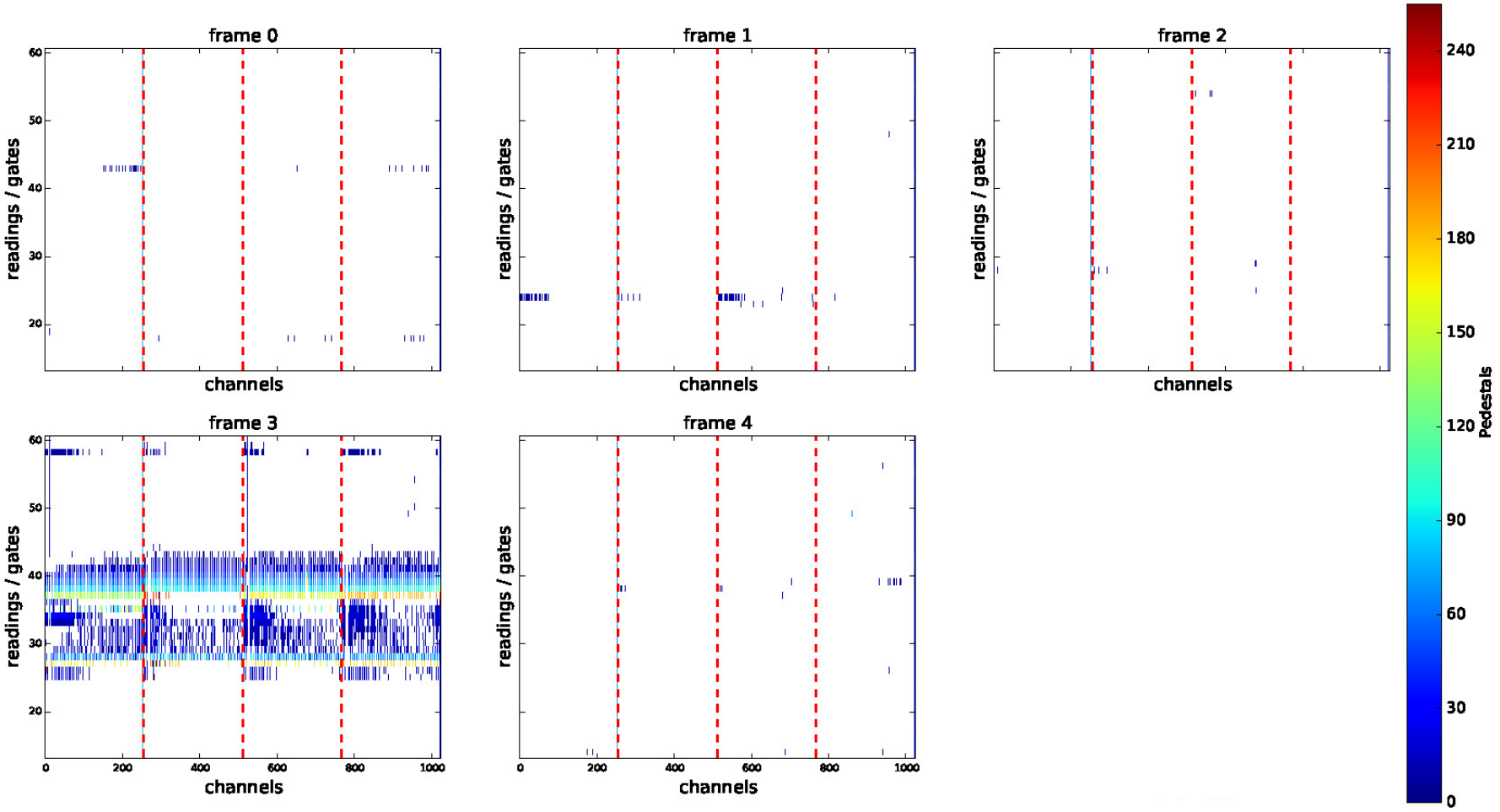
- **Conclusion as of today: Gate + relaxation time ≈ 1.5µs - 2µs for multiple GMs**

ZS-data all DHPTs



- DHPT zs readout + analog CM on @ DCD
- Threshold 5ADU

ZS-data all DHPTs



- DHPT zs readout + analog CM on @ DCD
- Threshold 5ADU

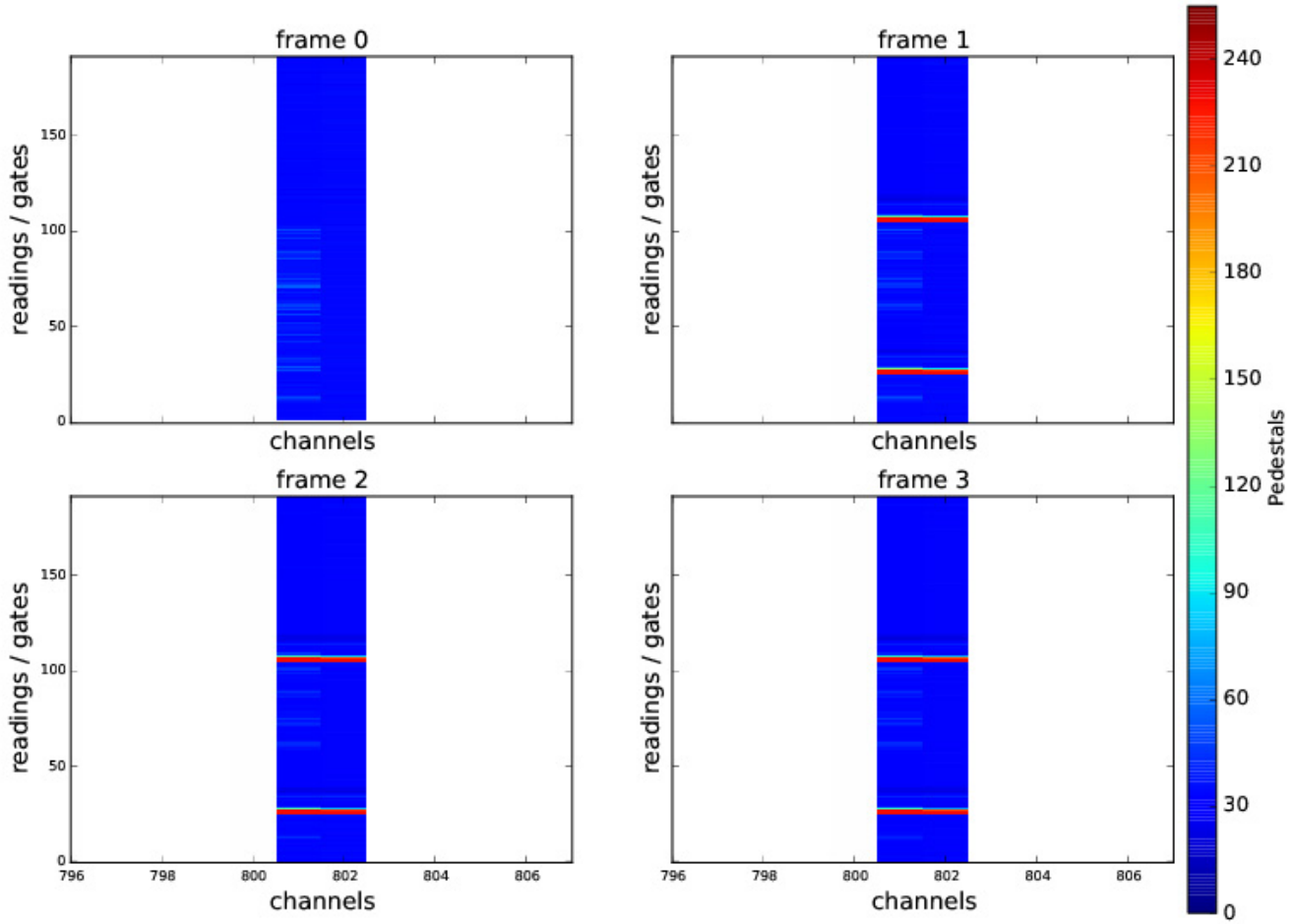
Summary

- Changes introduced …
  - Switcher V_sub routing
  - Better/different capacitors for GateOn and ClearOn close to the Switchers
- Switcher V_sub routing problem spotted only by chance!
  - In all lab setups: V_sub connected to GND since negative V_sub (more negative GateOn voltage) only needed after irradiation
  - Decrease in Vref-V_sub can explain the differences of the Switchers along the balcony in normal operation
- Gated Mode operation still being tested and optimized
  - ASIC related: DCD settings, Switcher sequence
  - DEPFET voltages: ClearOn voltage, Switcher V_sub on PXD9 pilot
  - Power supply: PS breakout board + kapton add capacitors
  - Continuous GM (4ms relaxation time)
- Question: continue PXD9 processing?

Back up: with DCD analog CM ON

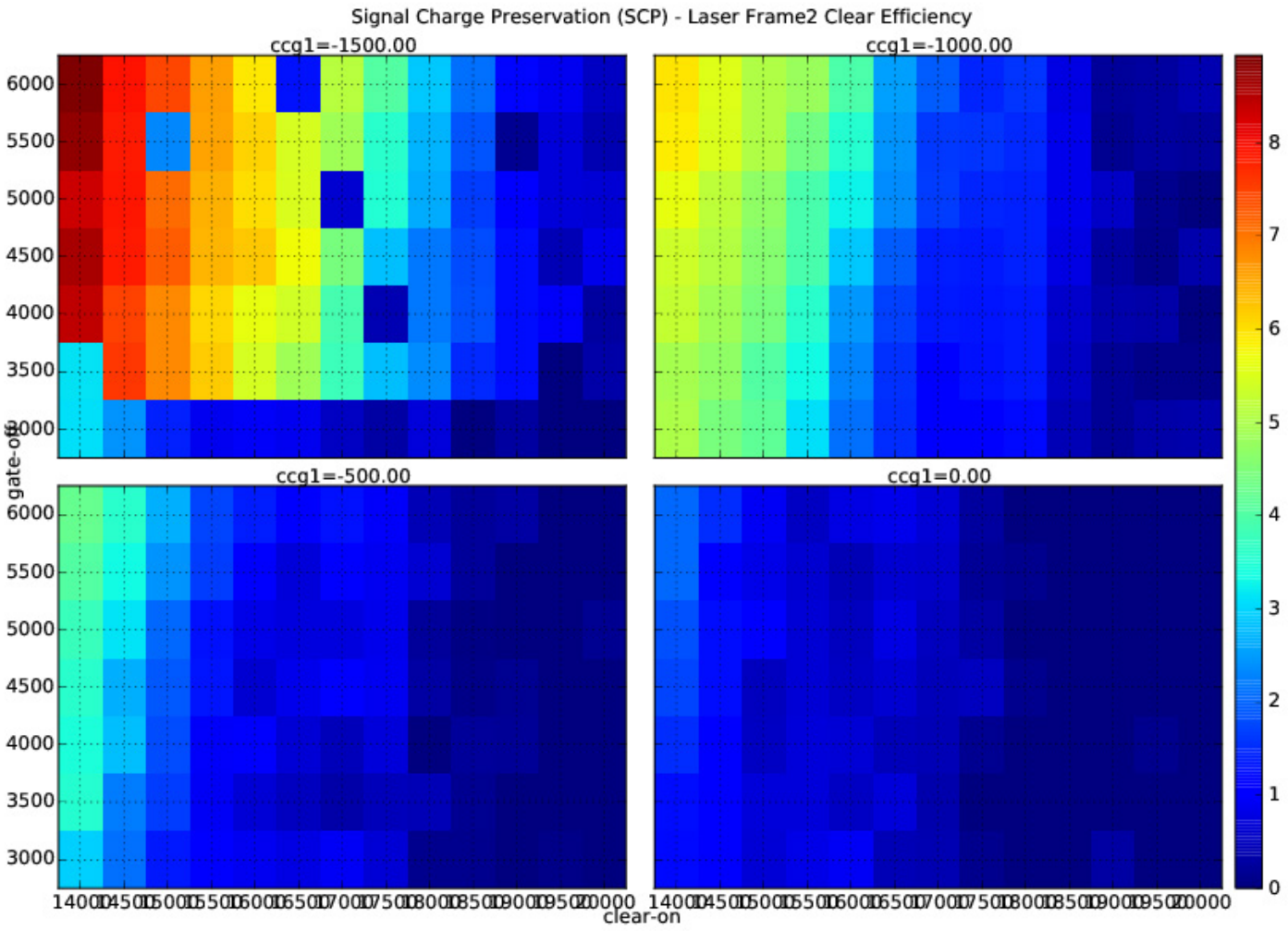
DCD4 – analog CM on

2 DCD channels – 4 frames, 2 x Gated Mode frame 1-3

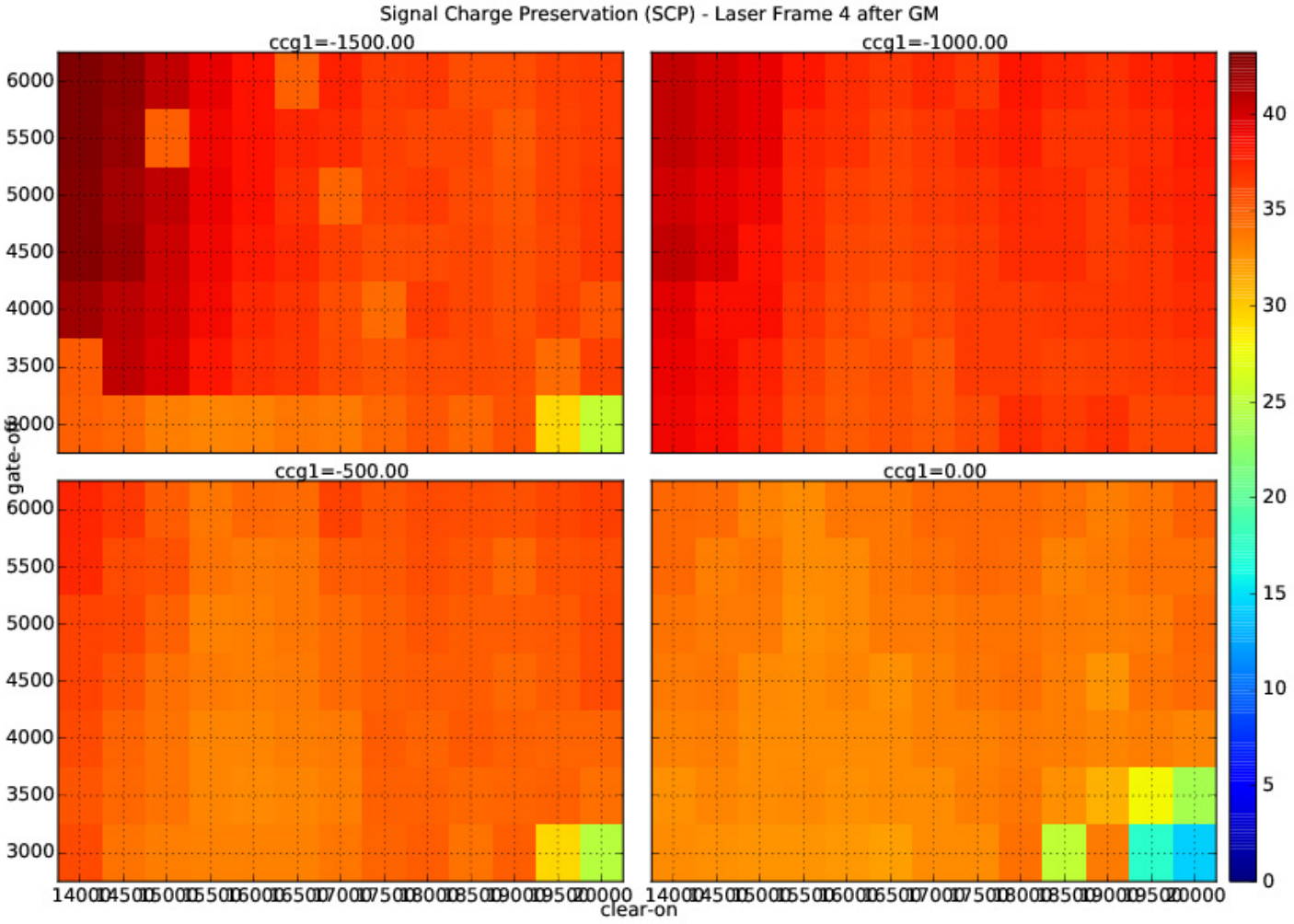


DCD1 – analog CM on

Voltage scan: Gateoff, ClearOn, CCG1 – Clear Efficiency



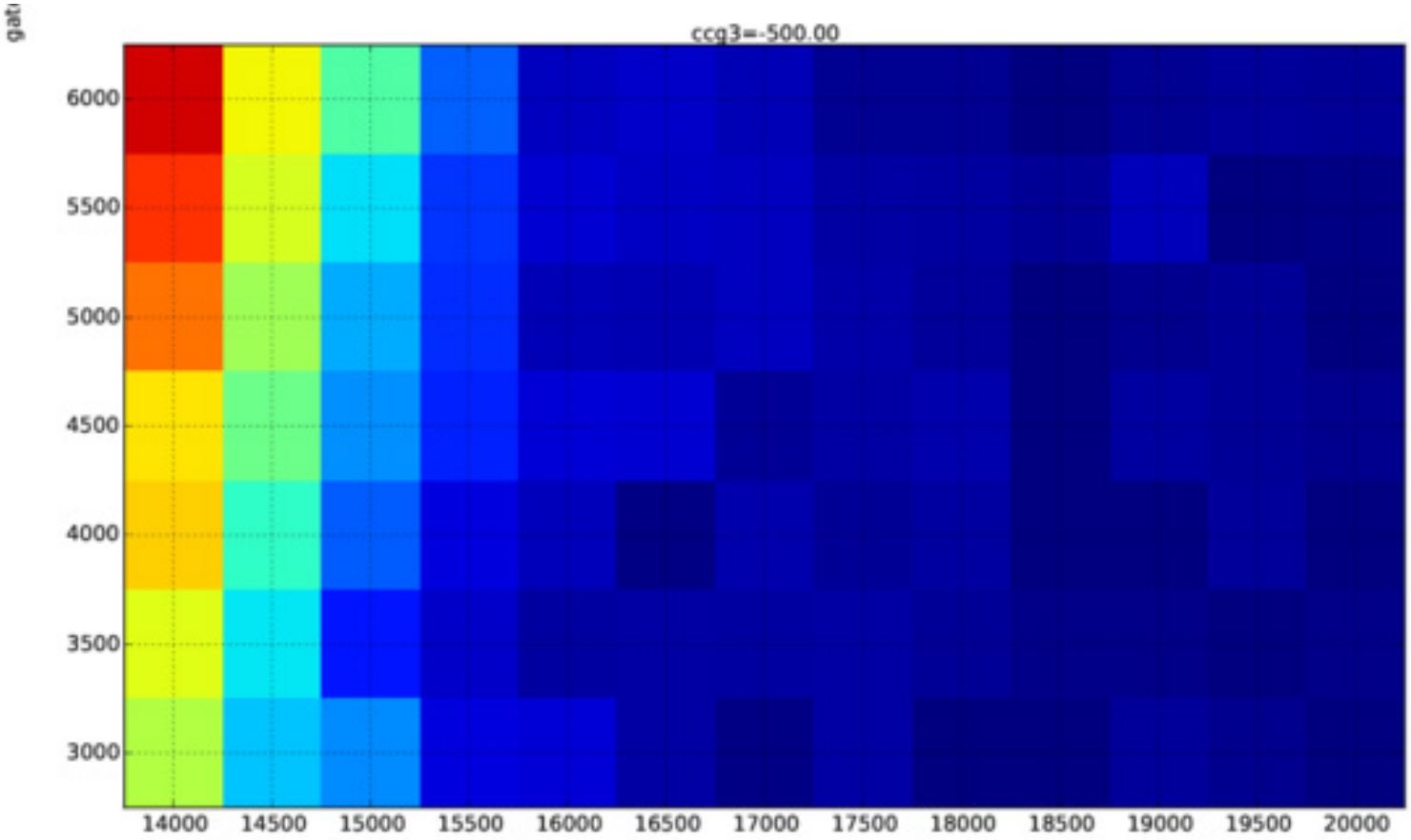
DCD1 – analog CM on
Voltage scan: Gateoff, ClearOn, CCG1 – SCP



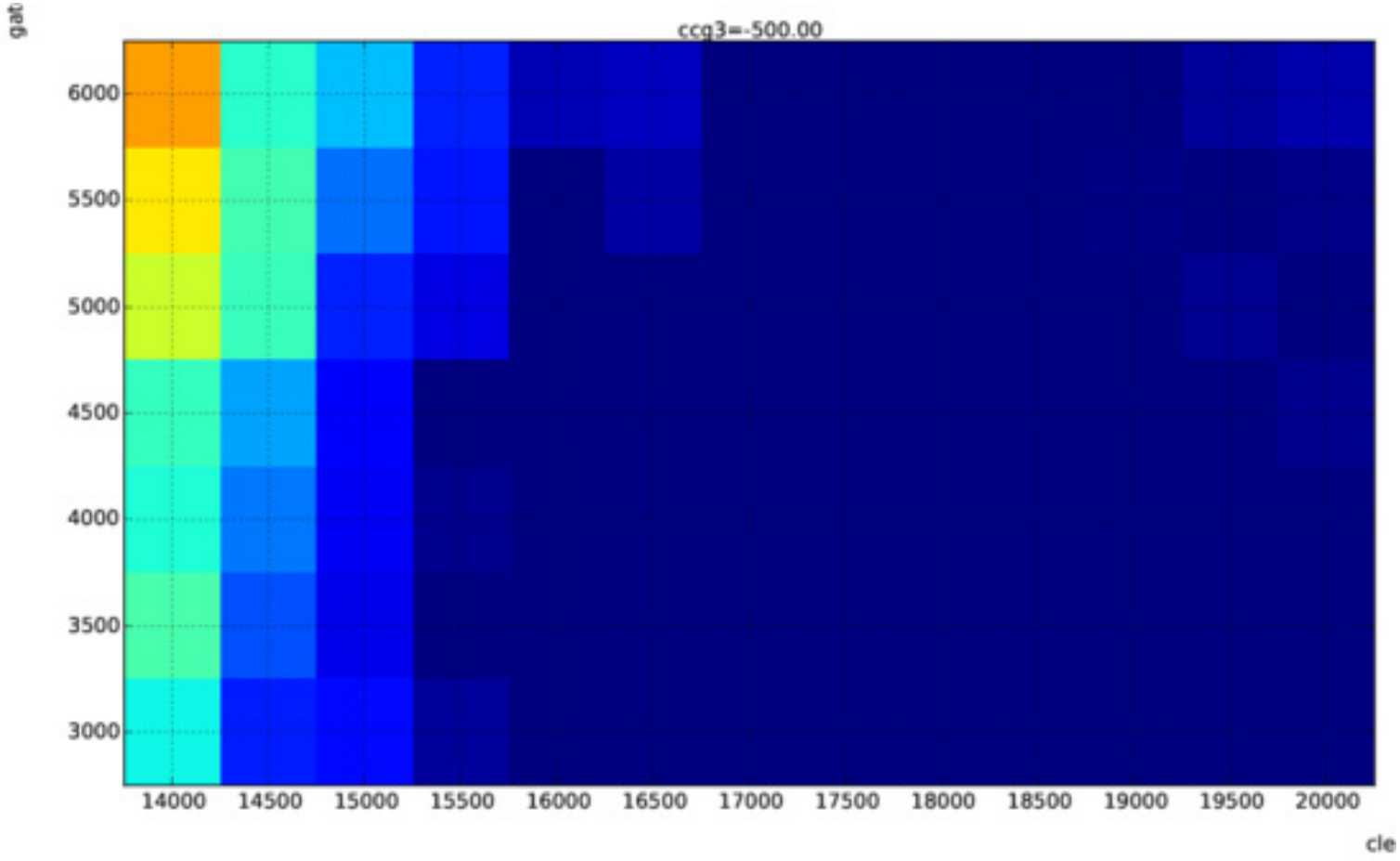
sweeps_2016_04_28_run001

Back up: with DCD analog CM OFF

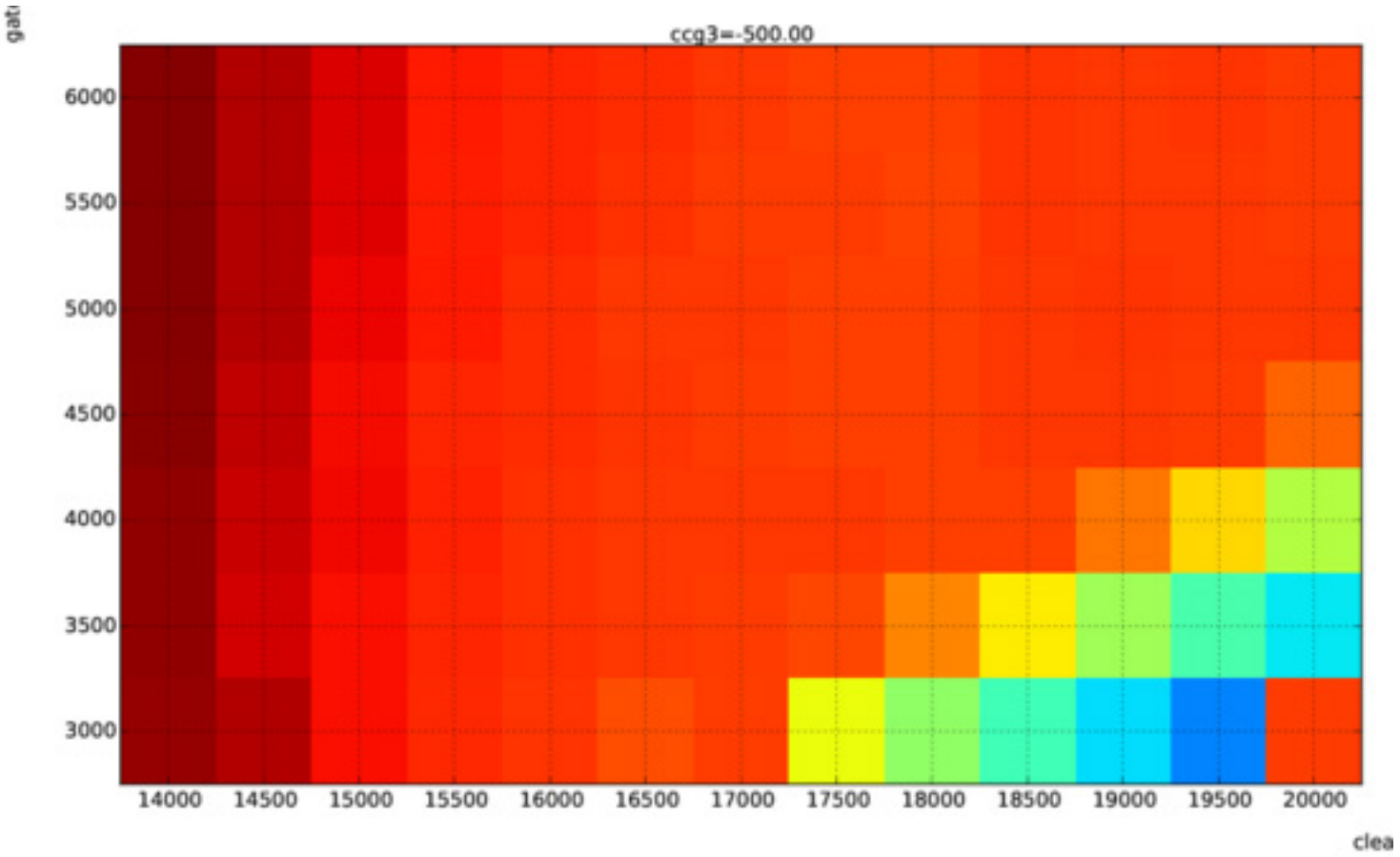
Voltage scan: Gateon, ClearOn– Clear Efficiency



Voltage scan: Gateon, ClearOn
JCP Junk Charge Protection



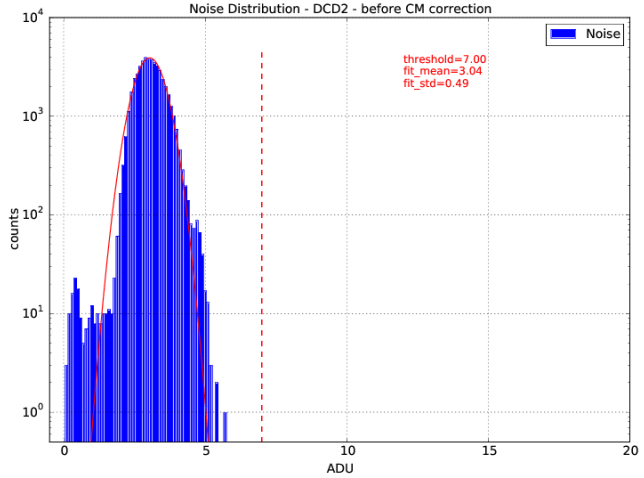
Voltage scan: Gateon, ClearOn
SCP Signal Charge Preservation

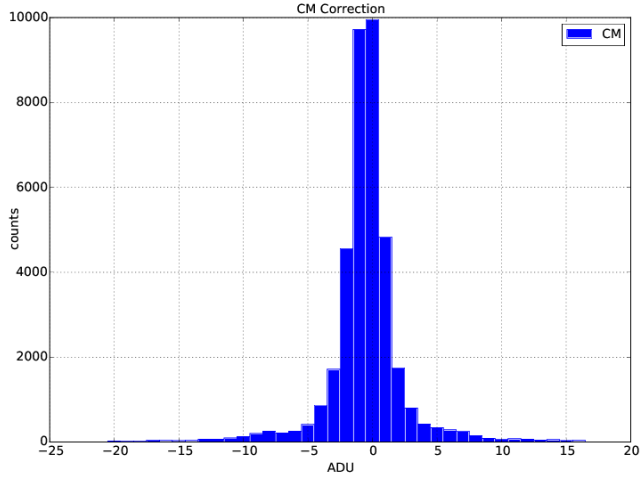


Back up: with DCD analog CM OFF /ON

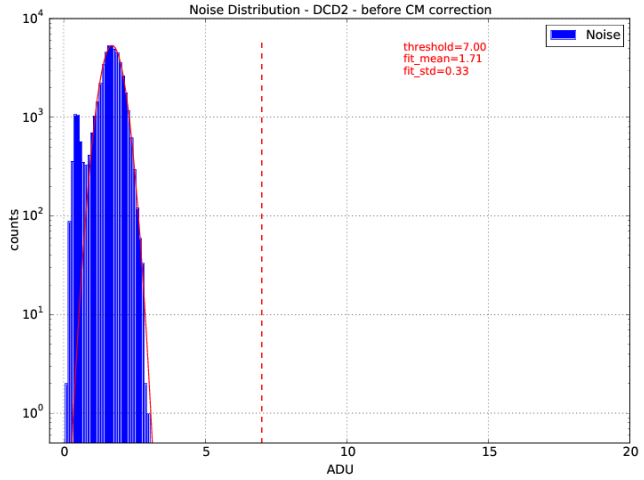
DCD2 Noise and offline CM value – with/without analog CM

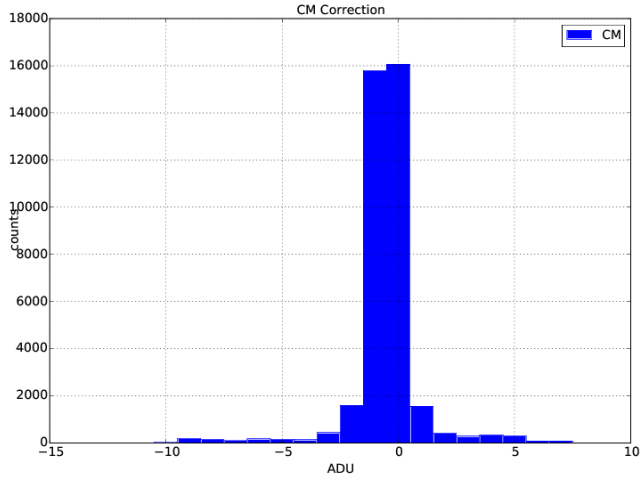
DCD analog CM: off



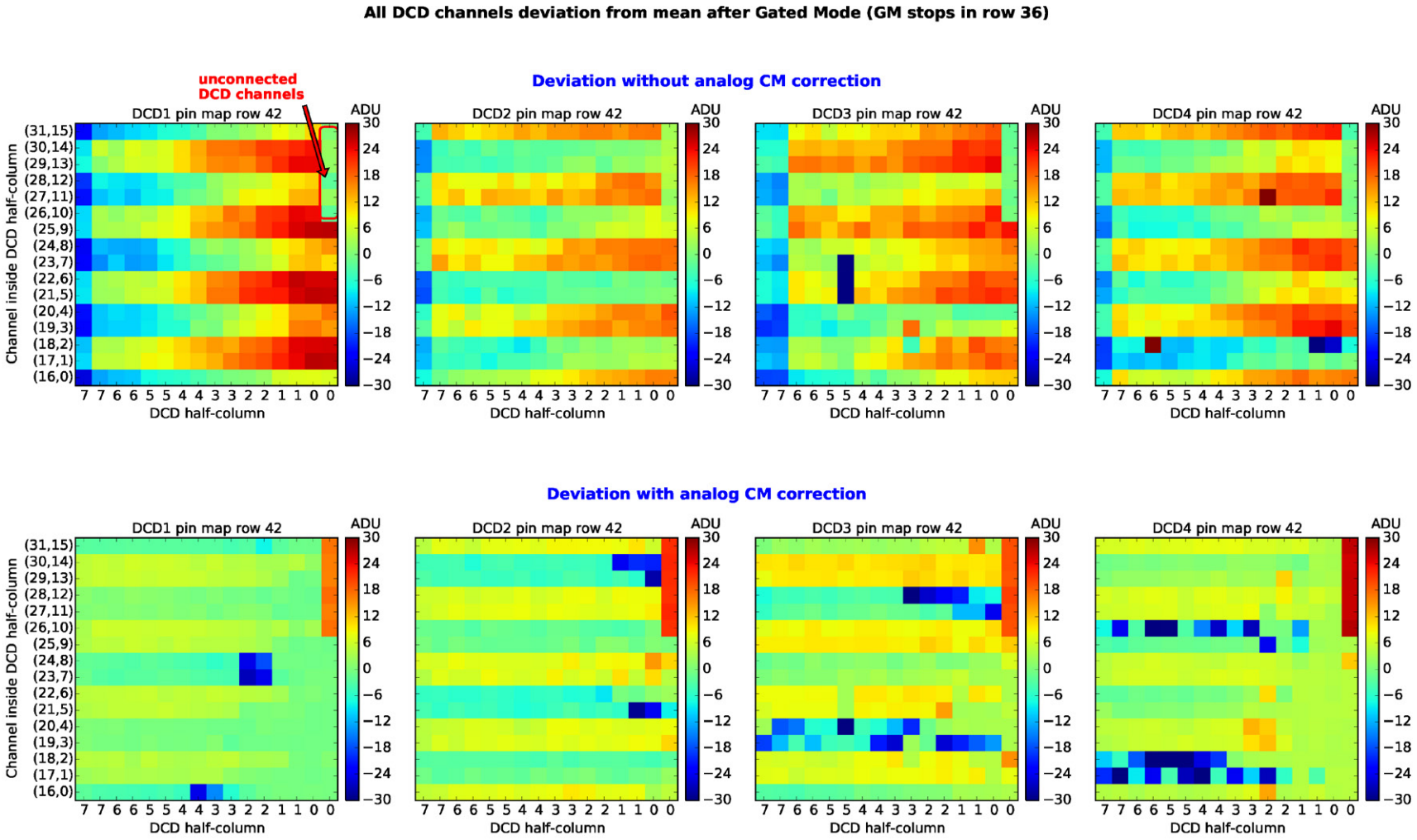


DCD analog CM: on

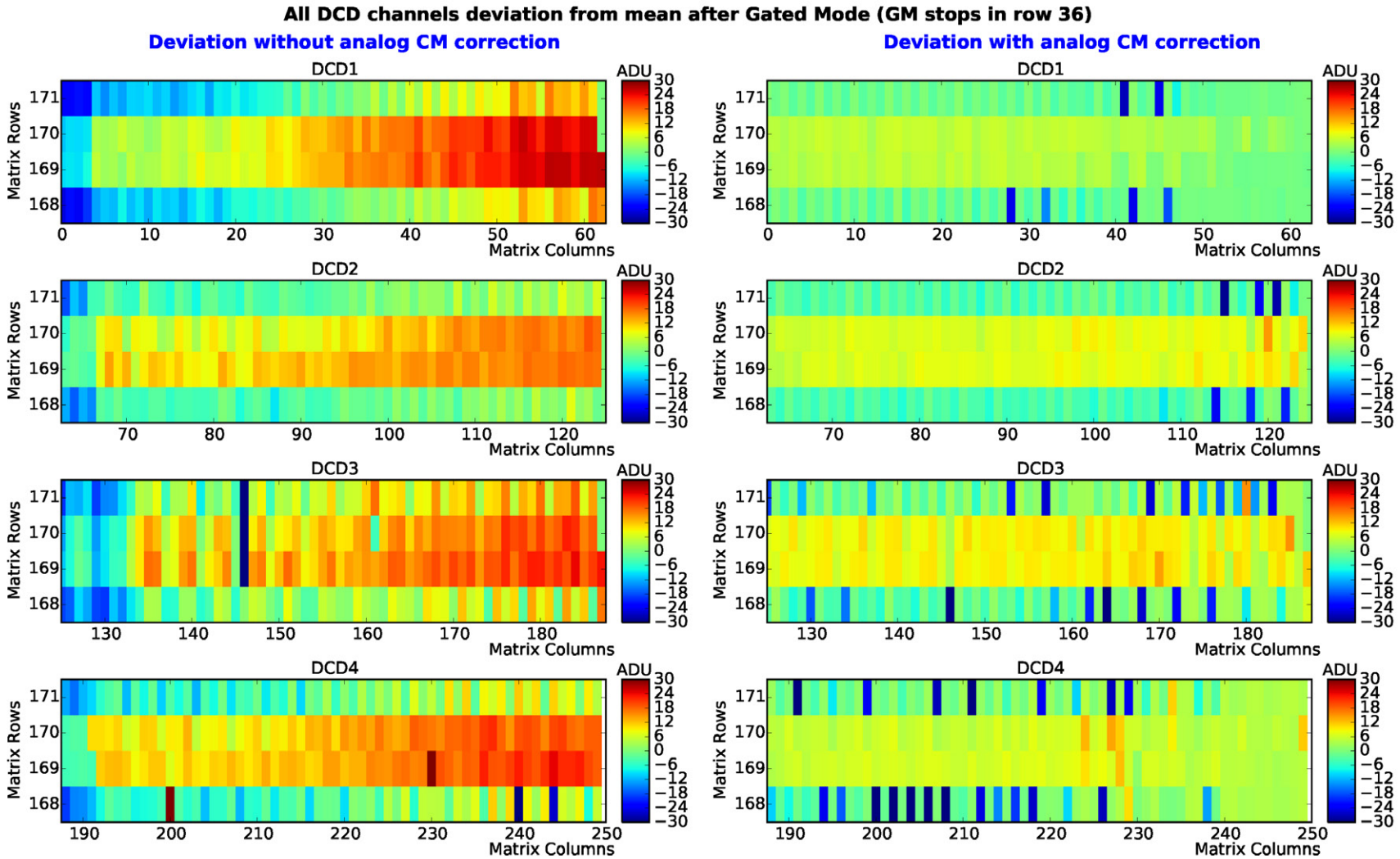




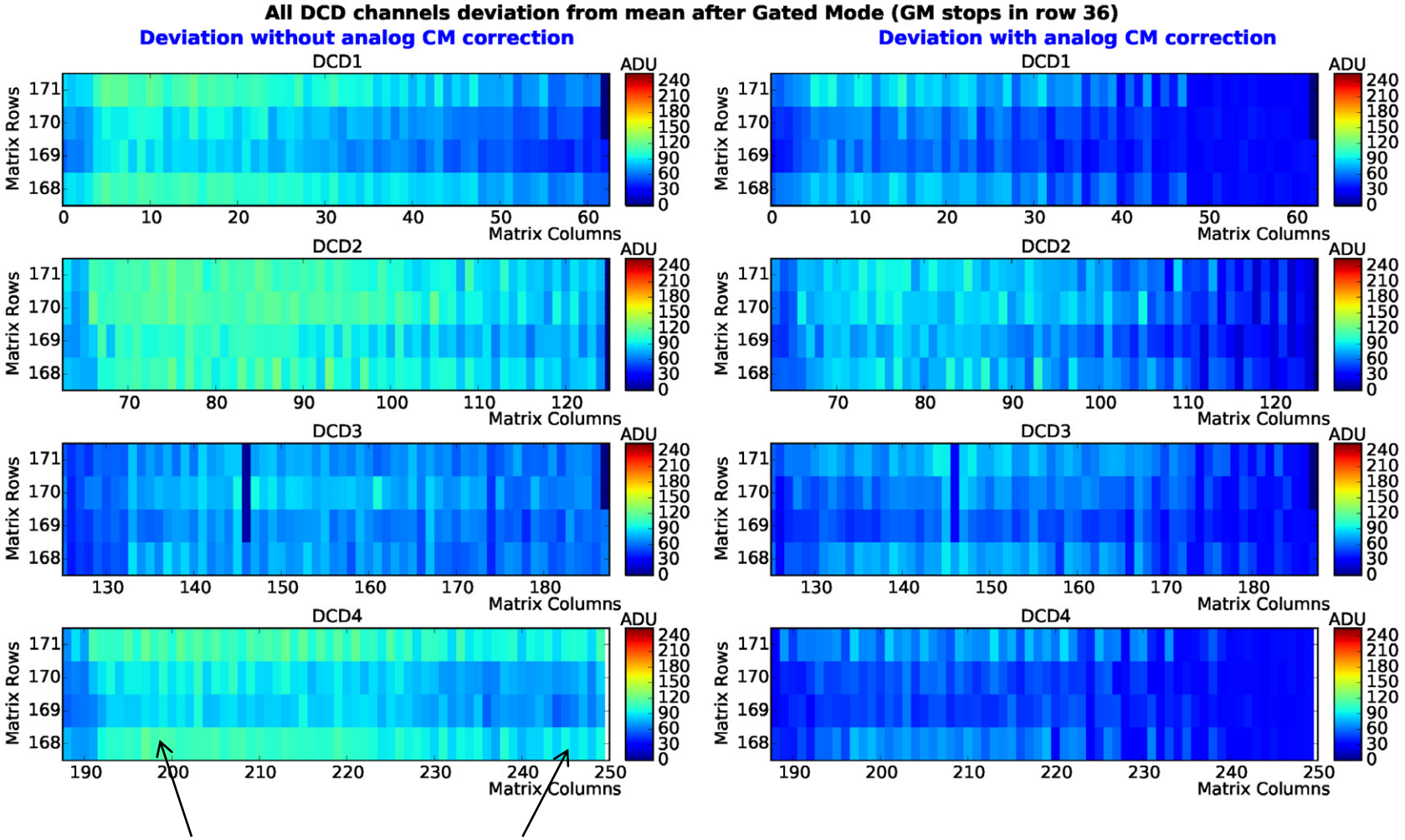
Gated Mode – DCD Pin Map, 768ns after GM

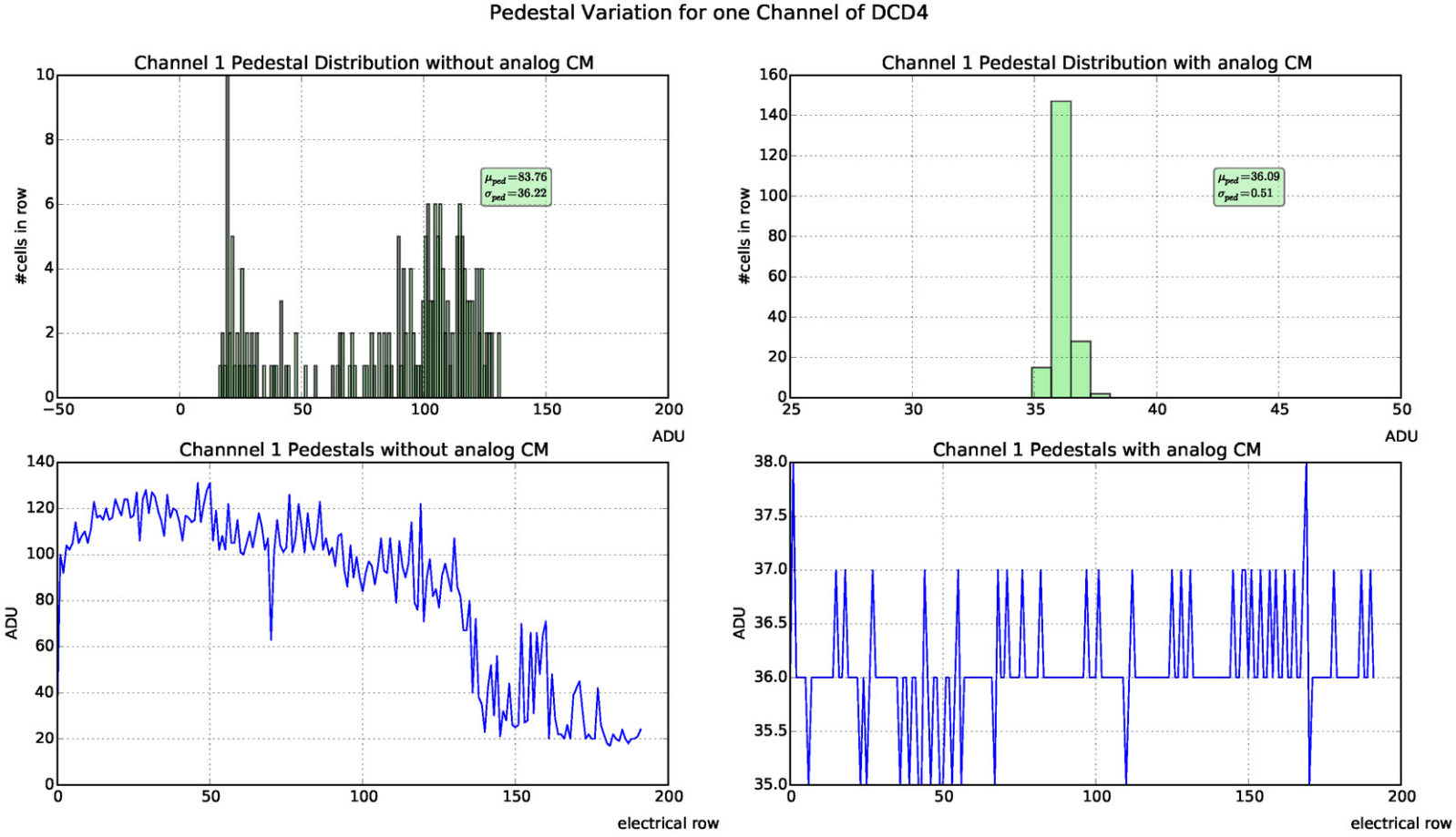


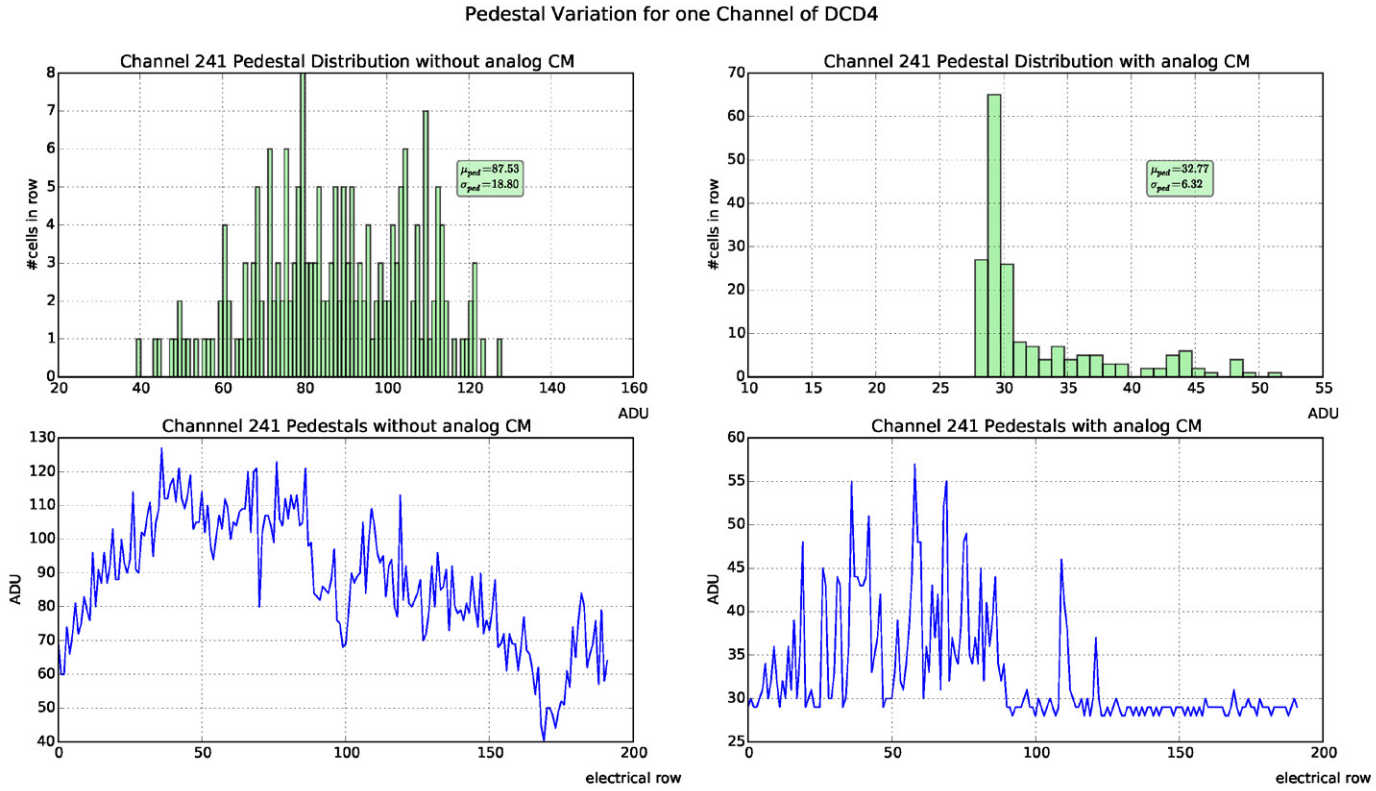
Gated Mode – PXD9 Mapping, 768ns after GM



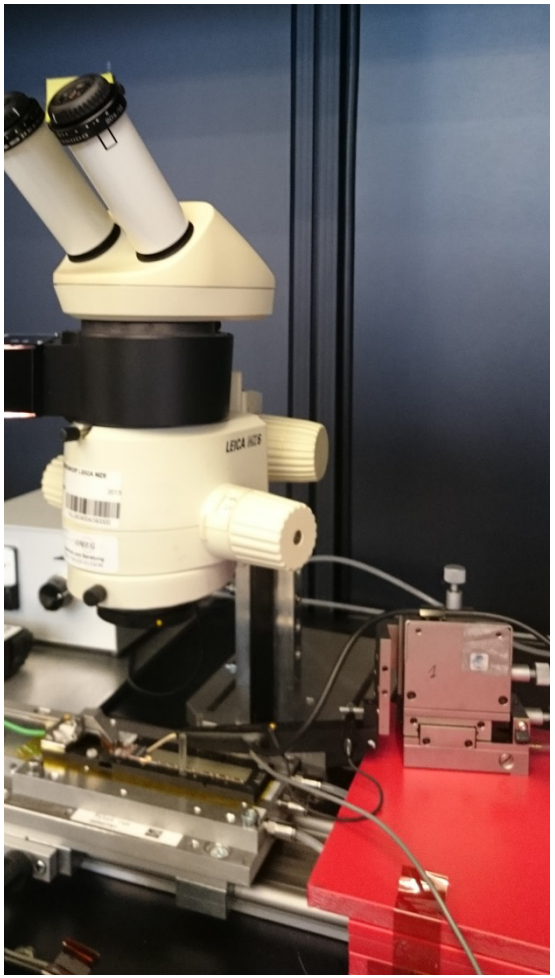
W30-OB1 Pedestal Spread along one Row




Pedestal Variation for one Channel of DCD4
Channel 1 Pedestal Distribution without analog CM
#cells in row
ADU
μ_{ped}=83.76
σ_{ped}=36.22
Channel 1 Pedestal Distribution with analog CM
#cells in row
ADU
μ_{ped}=36.09
σ_{ped}=0.51
Channnel 1 Pedestals without analog CM
ADU
electrical row
Channel 1 Pedestals with analog CM
ADU
electrical row

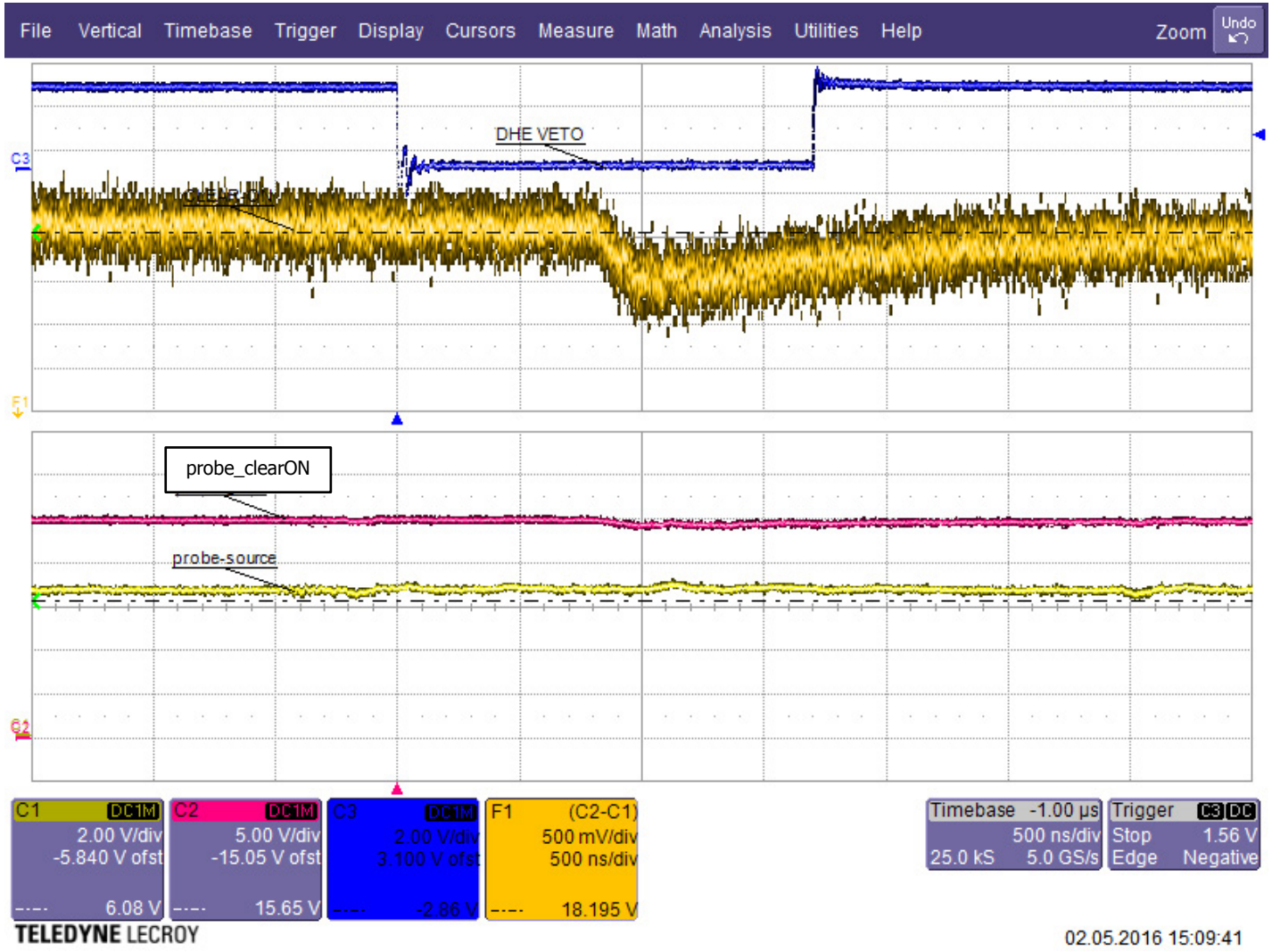

Pedestal Variation for one Channel of DCD4
Channel 241 Pedestal Distribution without analog CM
#cells in row
ADU
μ_{ped}=87.53
σ_{ped}=18.80
Channel 241 Pedestal Distribution with analog CM
#cells in row
ADU
μ_{ped}=32.77
σ_{ped}=6.32
Channnel 241 Pedestals without analog CM
ADU
electrical row
Channel 241 Pedestals with analog CM
ADU
electrical row

Probing on PXD9 – W30-OB2



- 2 probes used (Picoprobe Model 7A): supply + reference voltage
- Difference calculated by oscilloscope
- Only few voltages measured up to now due to contact problems

W30-OB2 - ClearOn



W30-OB2 VDDA to AmpLow

Switcher Voltages

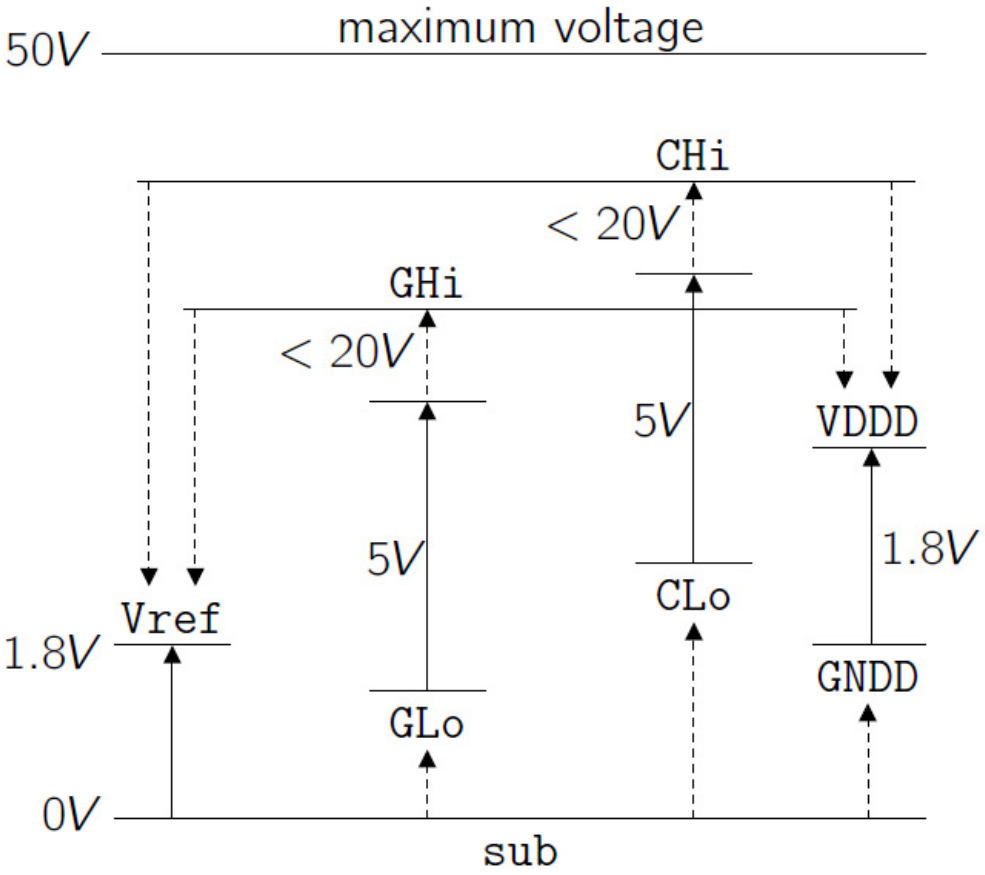
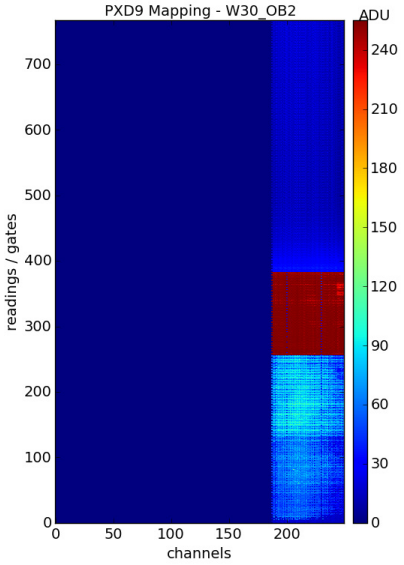


Figure 1.3: Floating Supplies Voltage Ranges

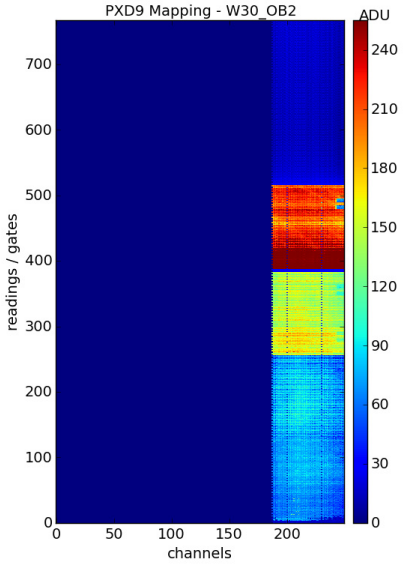
Switcher_Vref & Switcher_Substrate

- Sw_Vref sense is connected at the beginning of the balcony
- Sw_Vref is connected in alu1 (with some support in alu2) along the balcony
- Sw_Substrate is connected in alu2 from the wirebond pad to balcony. Along the balcony it is connected in alu1 (trace width design 14µm).
- Sw_Substrate not sensed on PXD9 module
- Voltage Sw_Vref @ PXD9 Patch Panel (referenced to Sw_Sub) = 1.8V (ps settings Sw_Vref = -5200, Sw_Sub = -7000)
  - Only two of six Switcher work

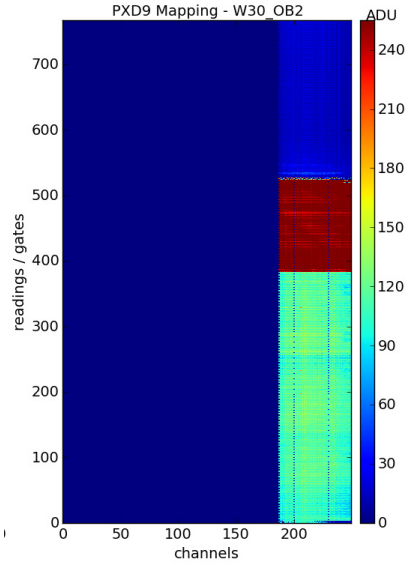
Sw_Vref = -5200mV



Sw_Vref = -5100mV



Sw_Vref = -5000mV

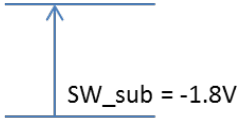


Switcher_Vref & Switcher_Substrate

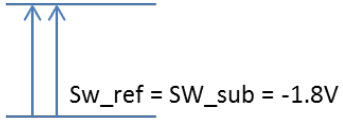
Starting condition source is 0V, Switcher_sub and Switcher_Vref are referenced to source

step

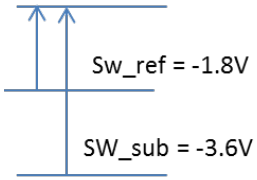
1



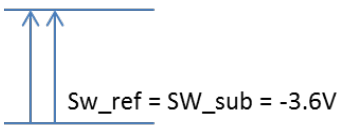
2



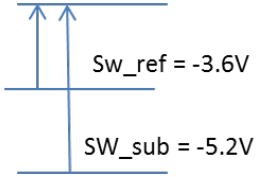
3



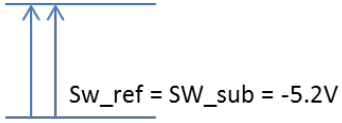
4



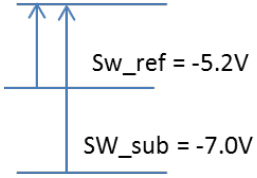
5



6



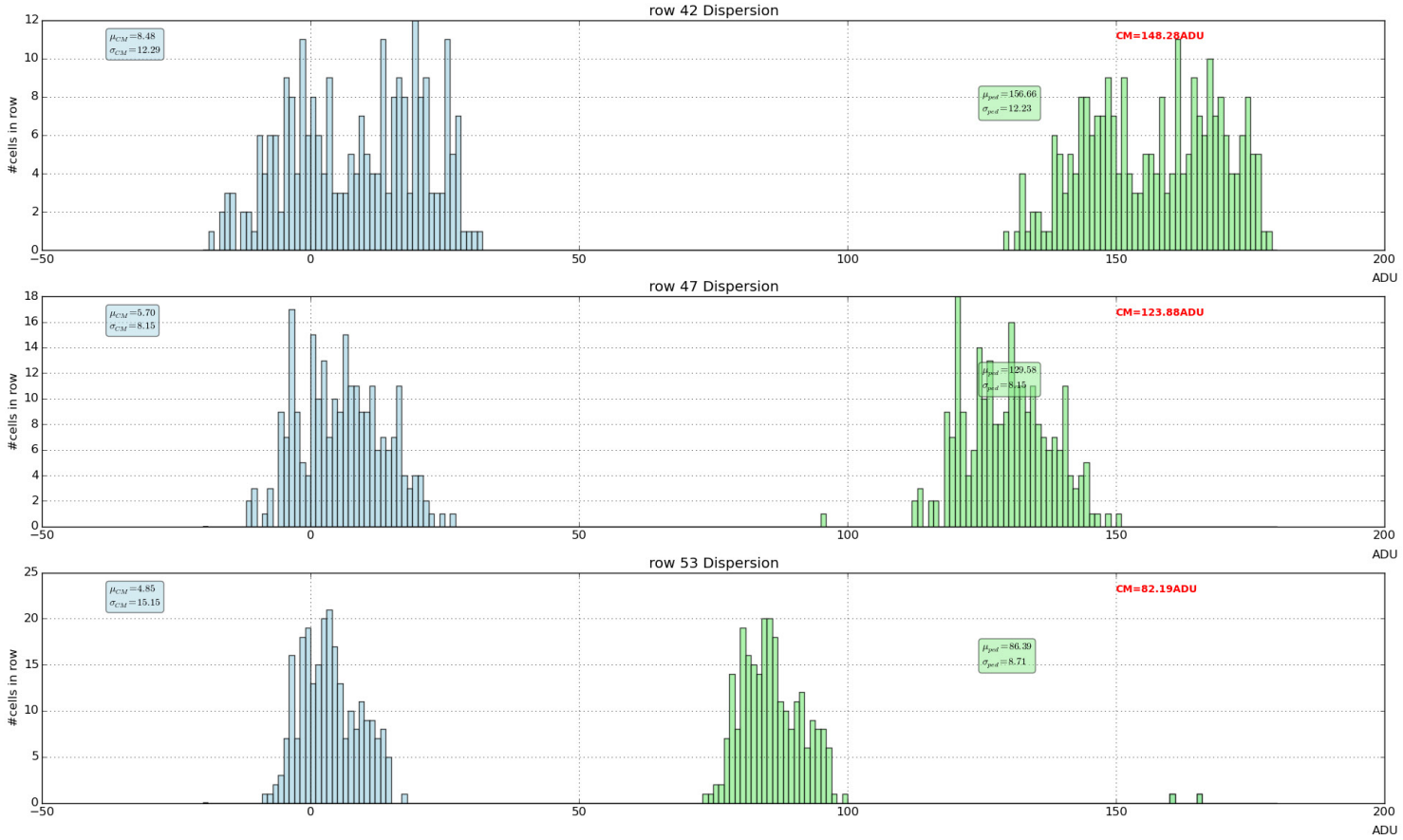
7



8

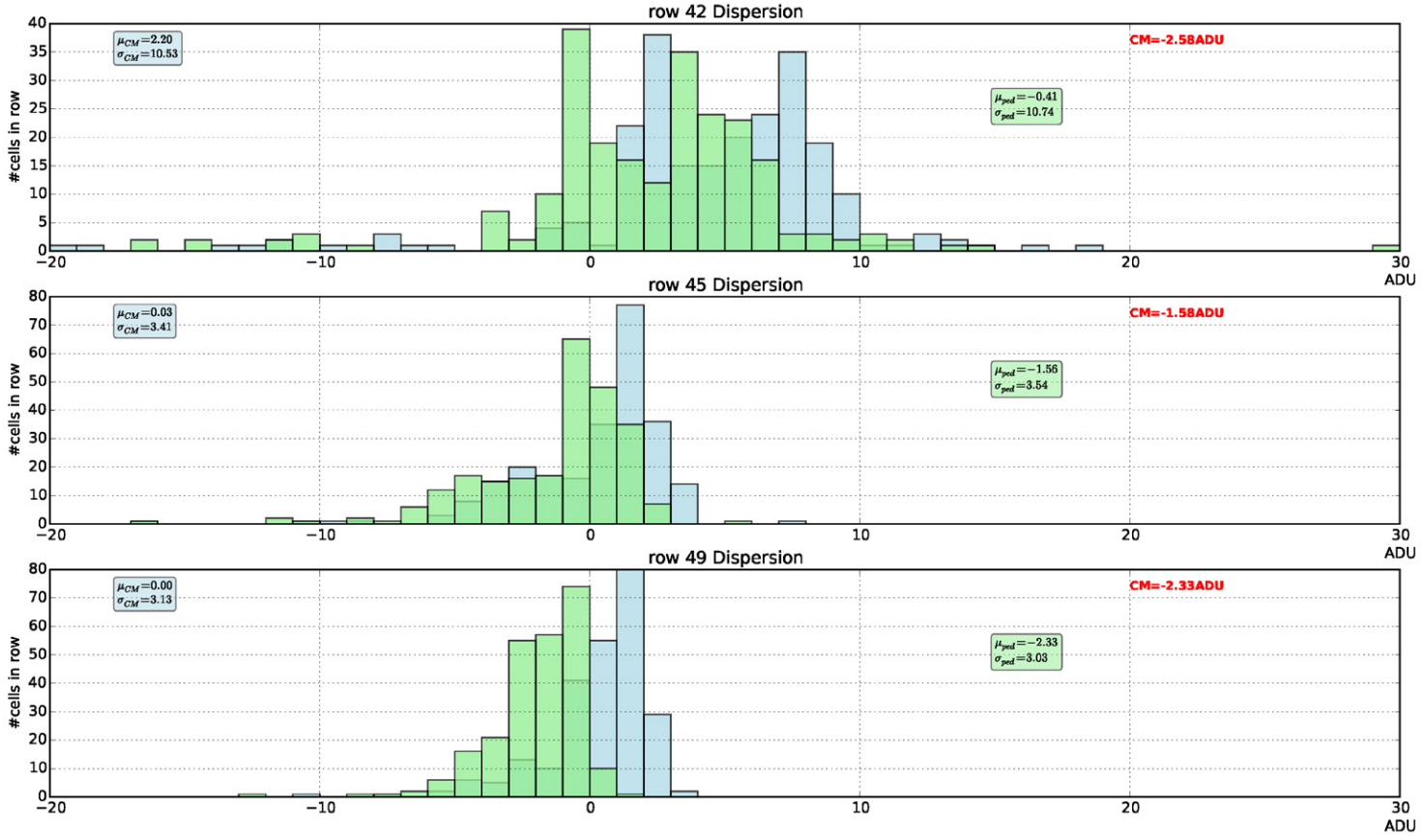
Source can be set to +7V (referenced to AGND now)
Sw_sub is -7V (referenced to Source) which is then same as AGND

Pedestal Distribution after GM w/o analog CM, Frame3



3 frames, each 2 GM

Pedestal Distribution after GM w/ analog CM, Frame 3



3 frames, each 2 GM