FANGS

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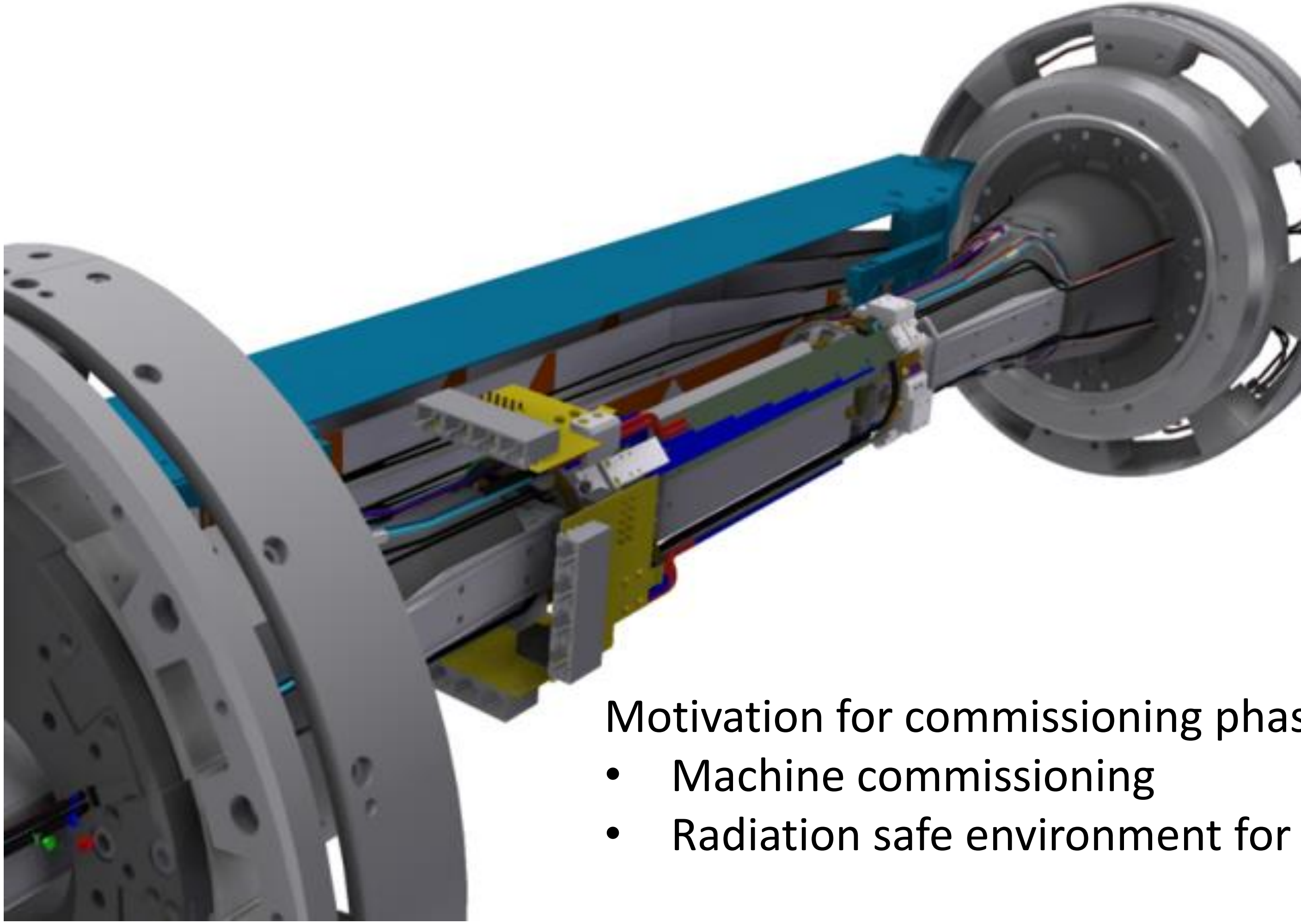
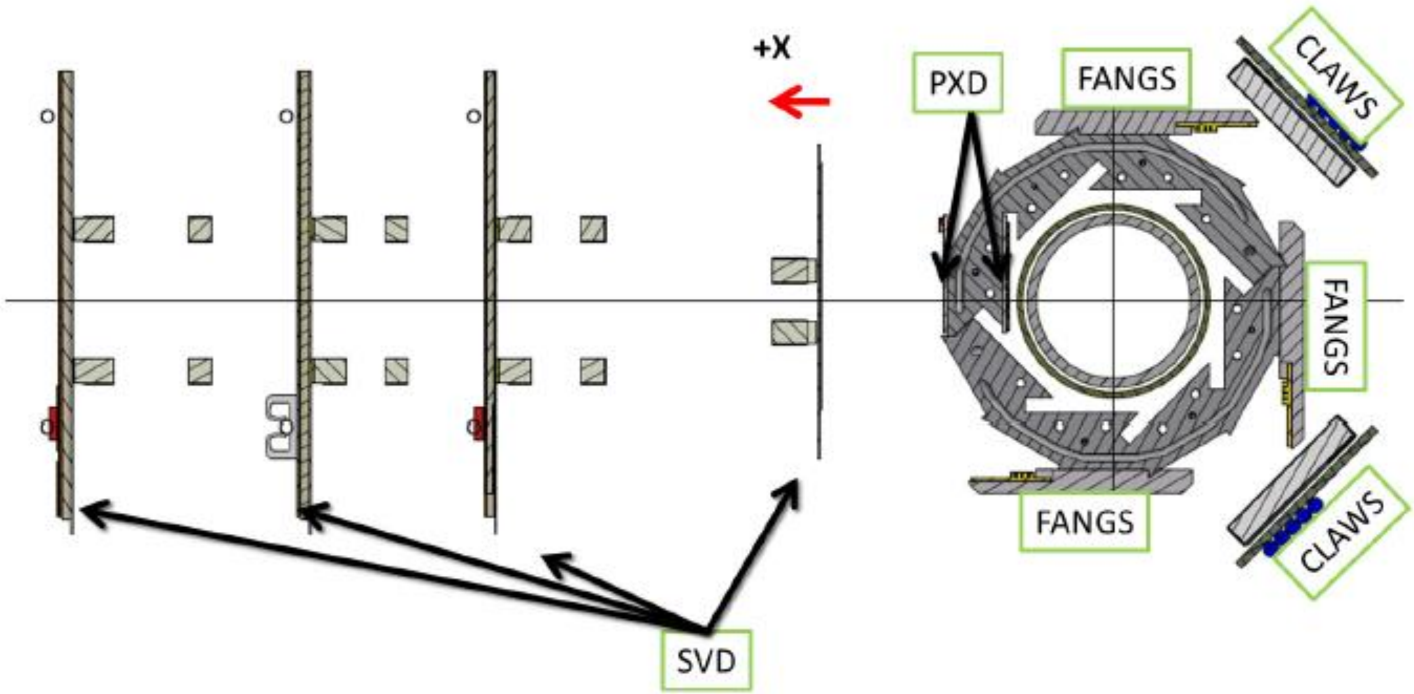
BEAST Commissioning Phase



Motivation for commissioning phase **BEAST II**:

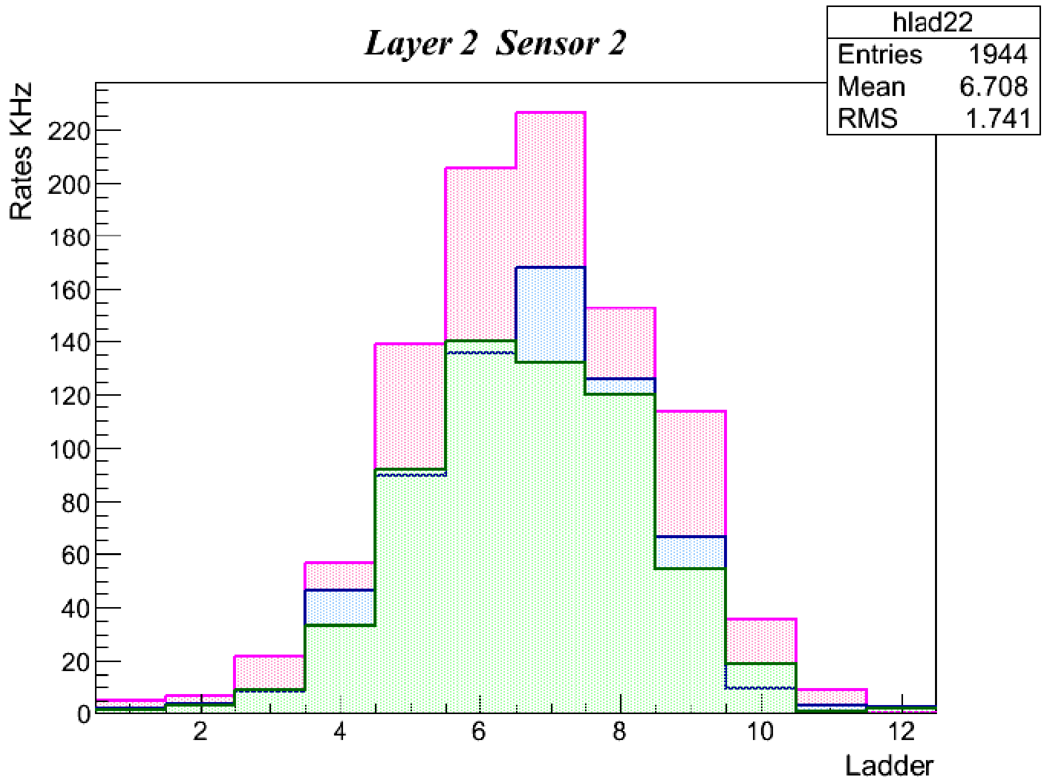
- Machine commissioning
- Radiation safe environment for the Vertex Detector (VXD):
  - Two layers DEPFET pixel detectors (PXD)
  - Four layers of double sided silicon strip detectors (SVD)

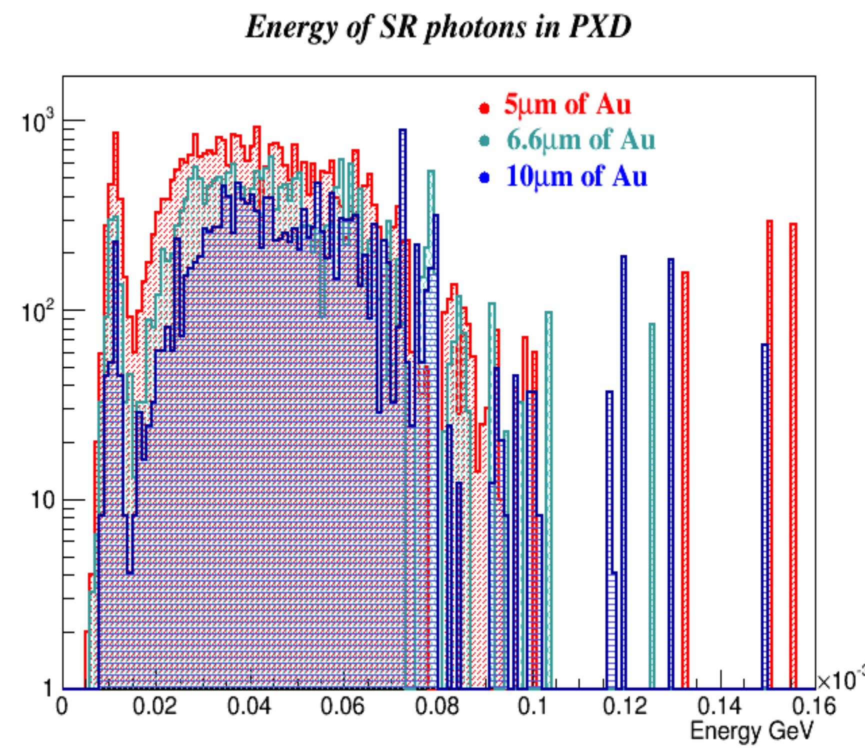
BEAST Commissioning Phase



- 2 PXD and 4 SVD layers in the direction where the highest backgrounds are expected
- At 90^0 , 180^0 and 270^0 in ϕ are the three **FANGS** staves
- **FANGS** uses the ATLAS IBL pixel detector modules for background measurements at BEAST II

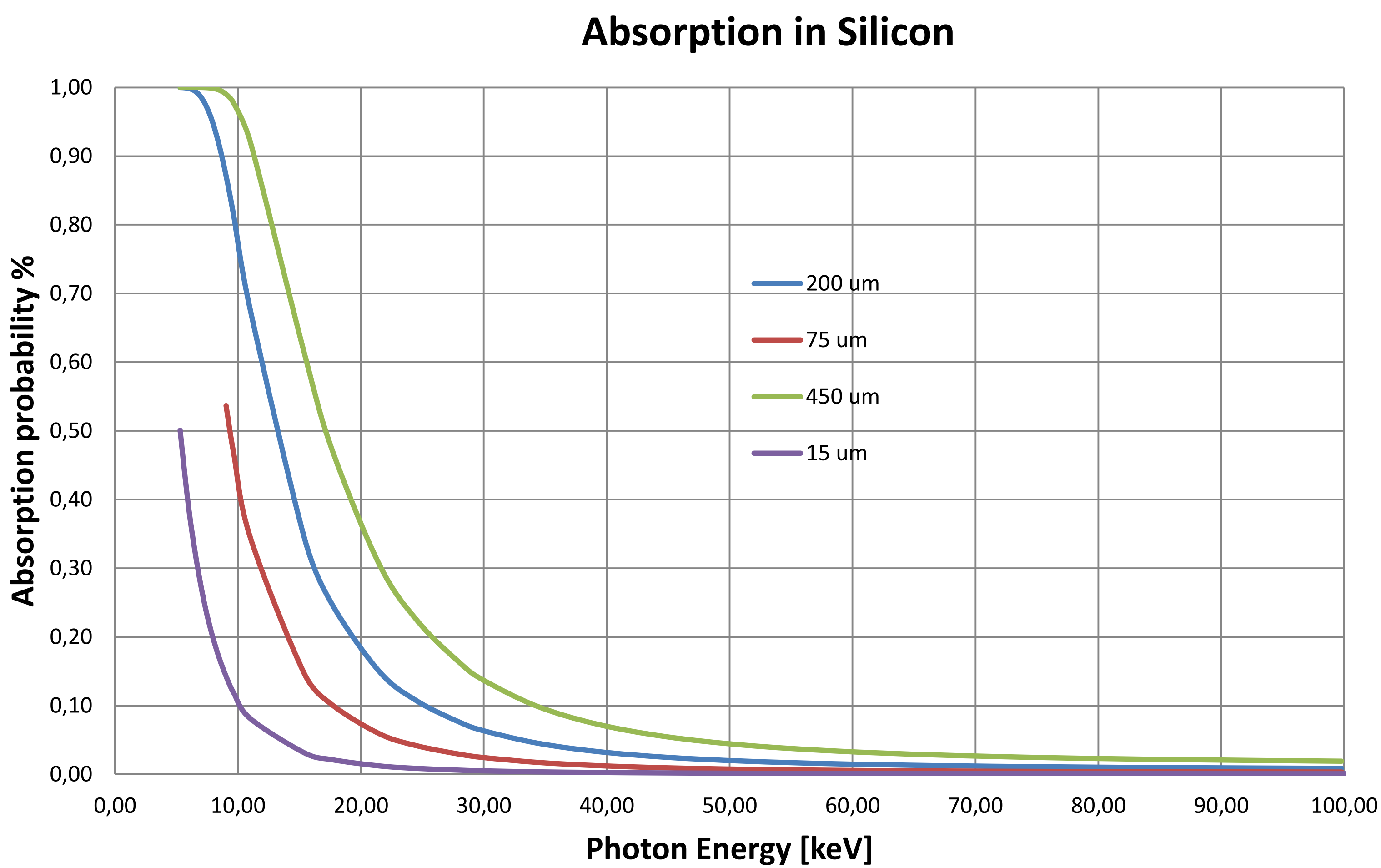
Detector Requirements



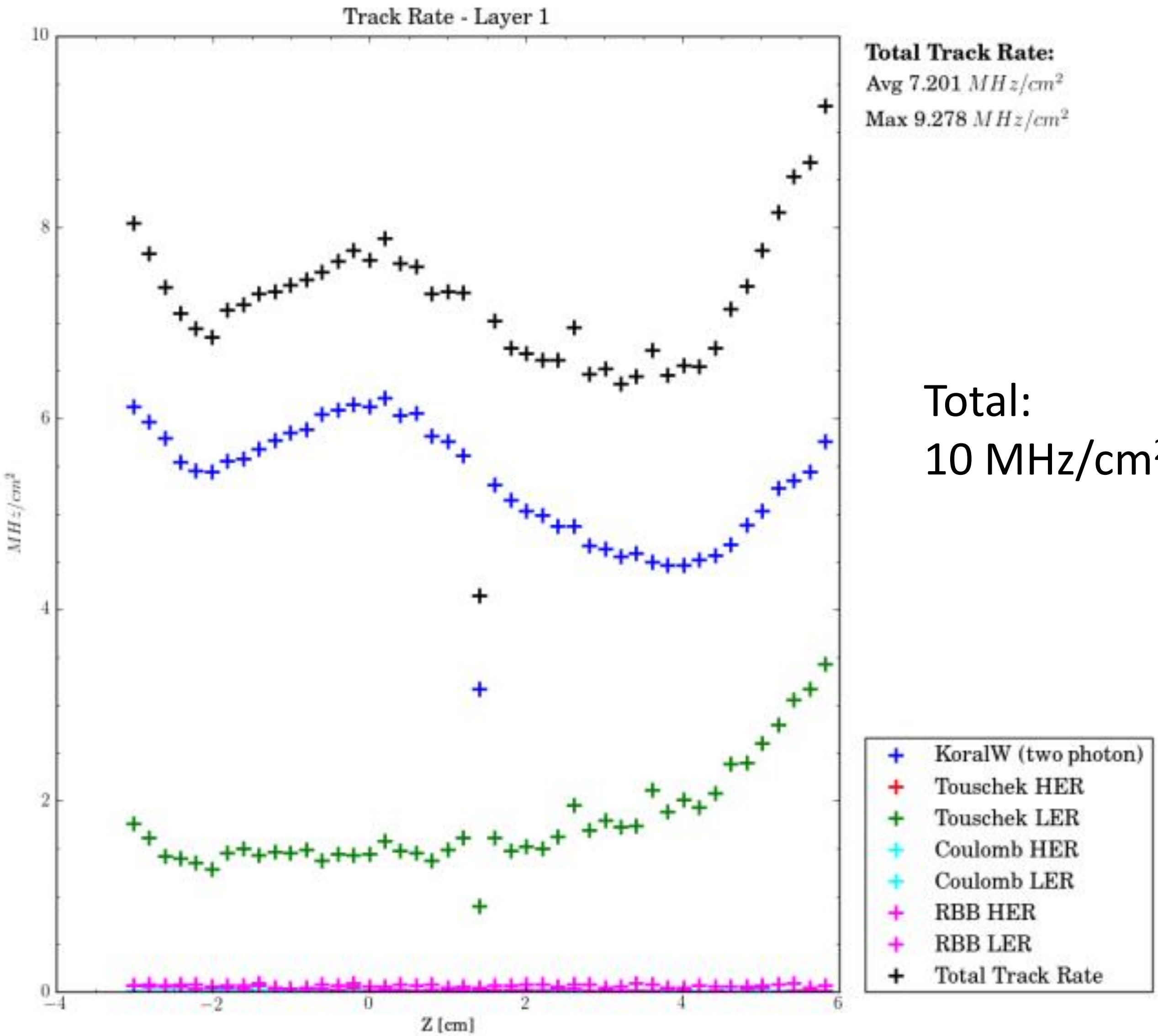


- During BEAST II: Final detector configuration (besides VXD chamber)
- 6.6 µm Au foil around beam pipe in BEAST II to enhance synchrotron radiation:
    - Maximum PXD hit rate of 28.64 KHz/cm^2 (~ factor 2 higher for FANGS)
    - Withstand a total dose of 4 Mrad
    - Largest contribution in the range of 10 - 90 keV

Absorption Probability

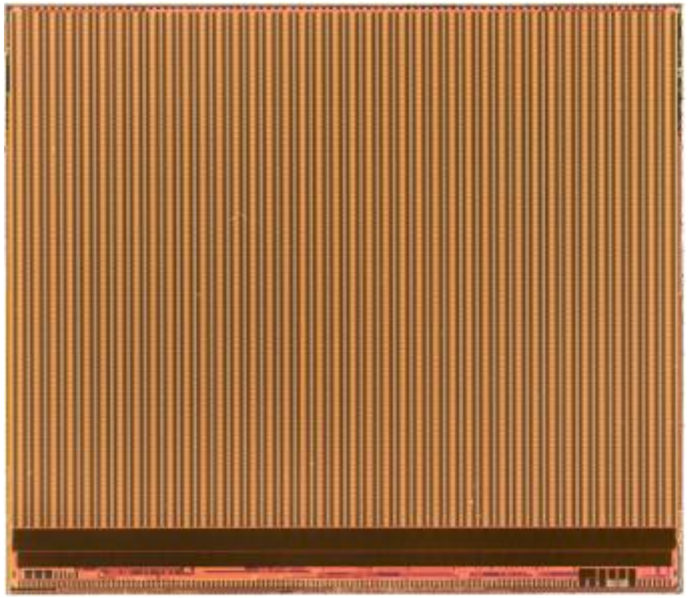


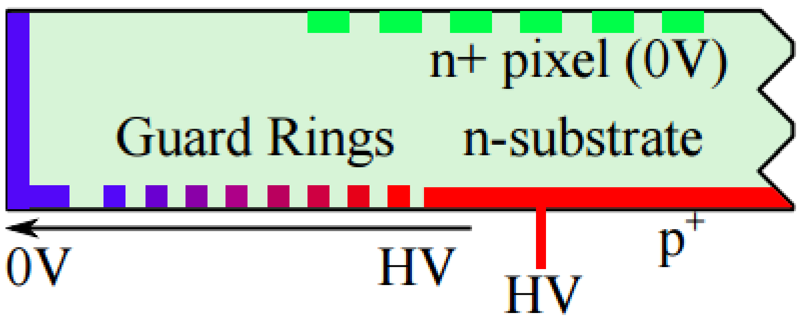
Total Particle Rates



Total:
10 MHz/cm^2 + 60 kHz/cm^2

FANGS: FE-I4 ATLAS Near Gamma Sensors





- FE-I4 read out chip
  High hit rates (400 MHz/cm²) and radiation hard (300 Mrad)
  IBM 130 nm CMOS process
  Read out for 80x336 pixels
  Thickness=150 µm
  Physical size=**21x19 mm²**

- Sensor:
  n-in-n planar
  Pitch=**50x250 µm²**
  Thickness=200 µm
  Physical size=19x20 mm²
  HV=60 V
  Power=1.2 W

- **Background radiation measurements in Phase 2:**
  - Sensitive to low keV X-rays
  - Ability to measure high particle rates

TDC Method

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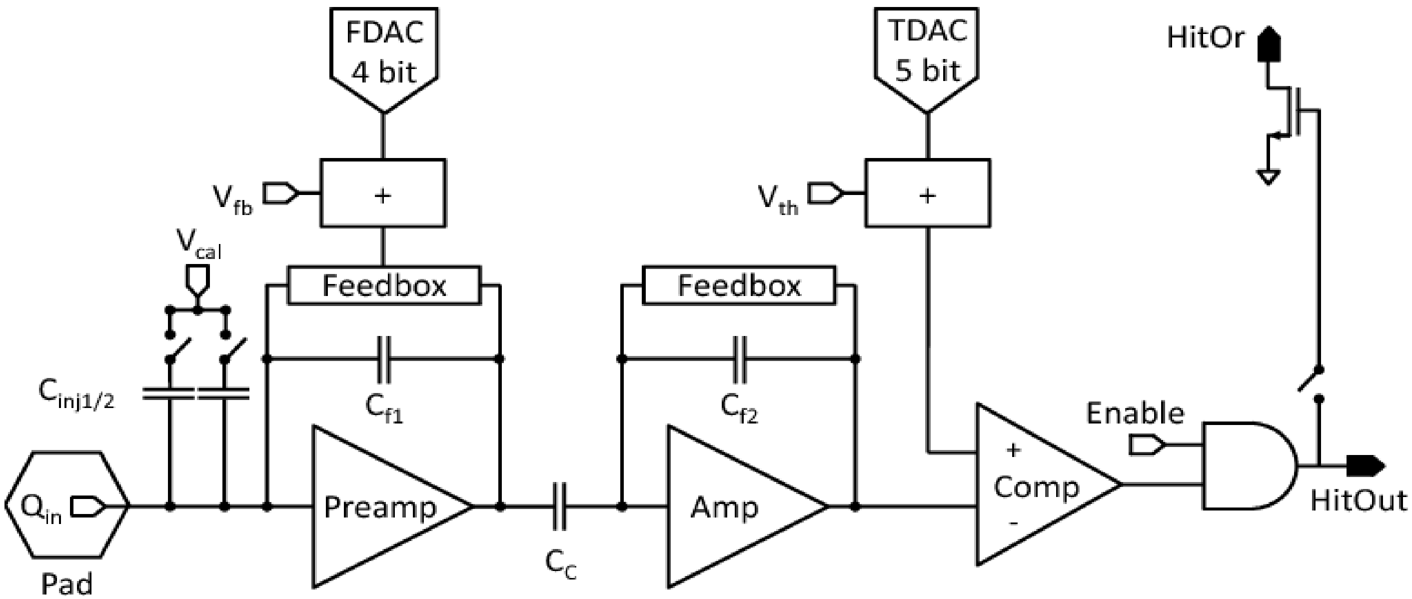
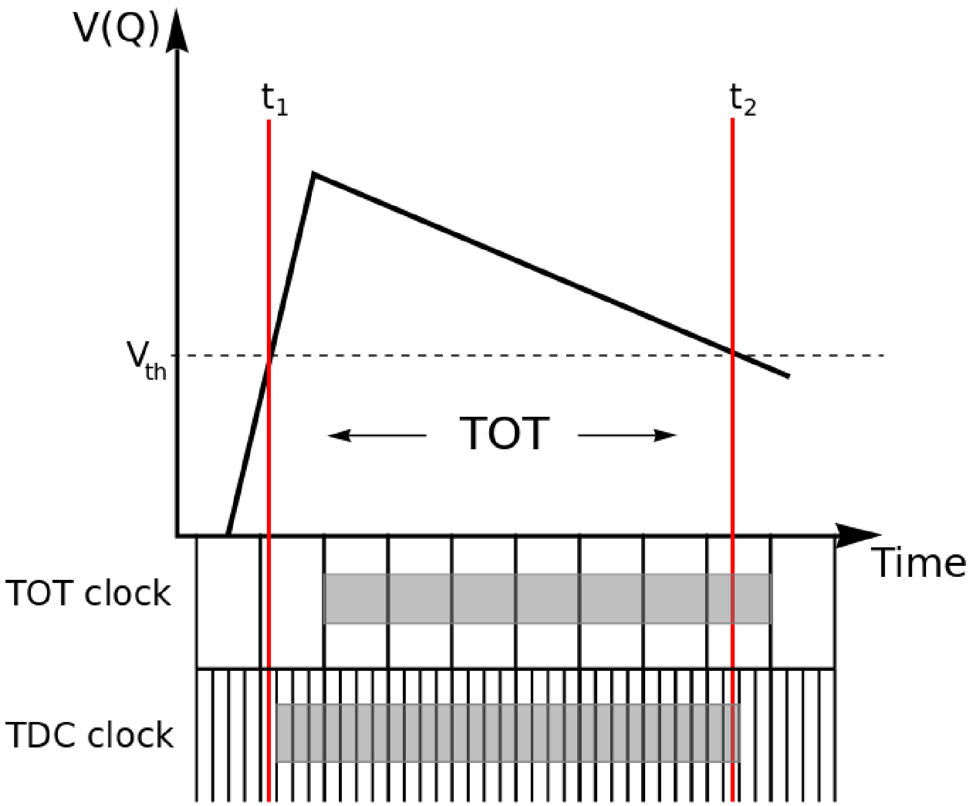


- Two stage amplifier → Discriminator with adjustable threshold.
- Time over threshold **(TOT)** with 40 MHz clock.
- Time to digital converter **(TDC)** uses 640 MHz FPGA clock.
- Output of each pixel is ORed (Trigger).
- Internal charge injection circuit for threshold tuning and calibration (PlsrDAC)

→ Both, high speed and adequate energy resolution achieved at the same time

TDC Method



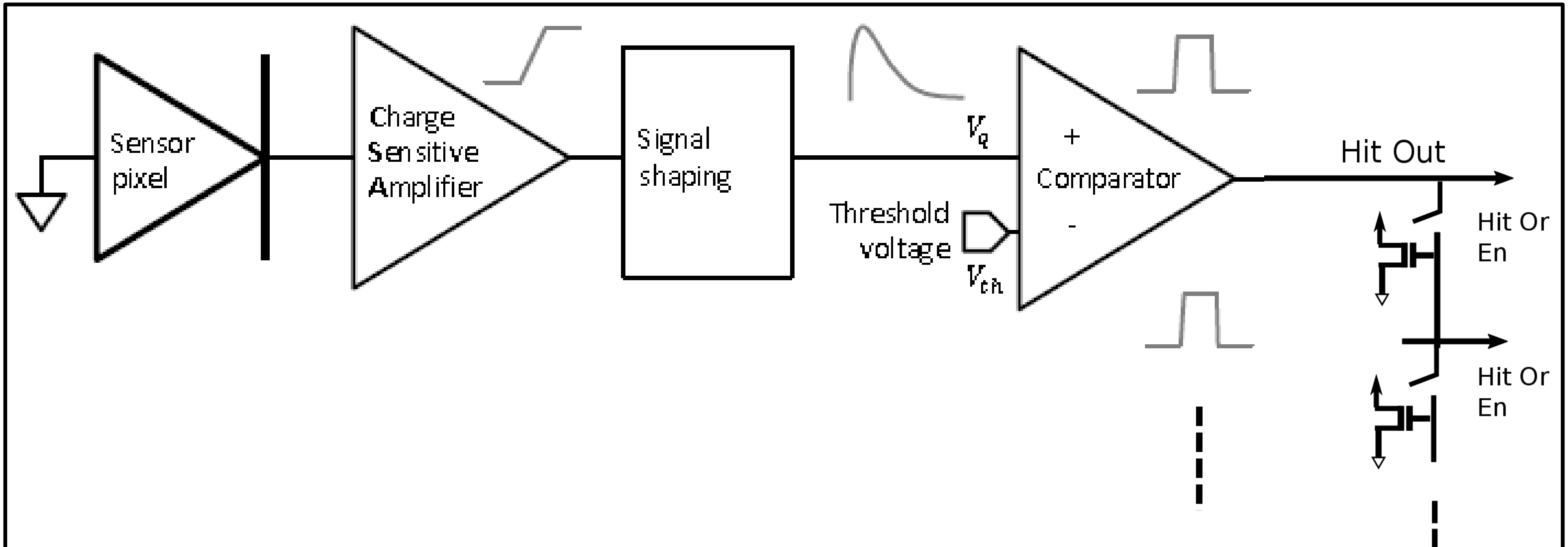
Two independent measurements simultaneously:

A. **TOT** 40 MHz clock: 4 bit resolution
   - Contains pixel and timing information

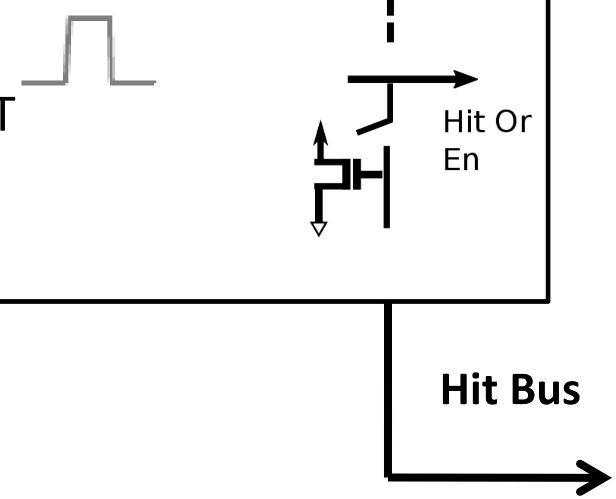
B. **TDC** with external FPGA's 640 MHz clock: 12 bit resolution
   - Voltage signal of comparator output with the highest charge
   - Limited to **one** pixel per readout

➢ Improved resolution

Pixel Schematic



- Output for each pixel in ORed : All pixels above threshold are always read. The pixel with the highest charge thus longest TOT can be additionally measured with the FPGA TDC to get the charge signal with higher precision.



- Hit Bus also used as self trigger

Experimental Setup

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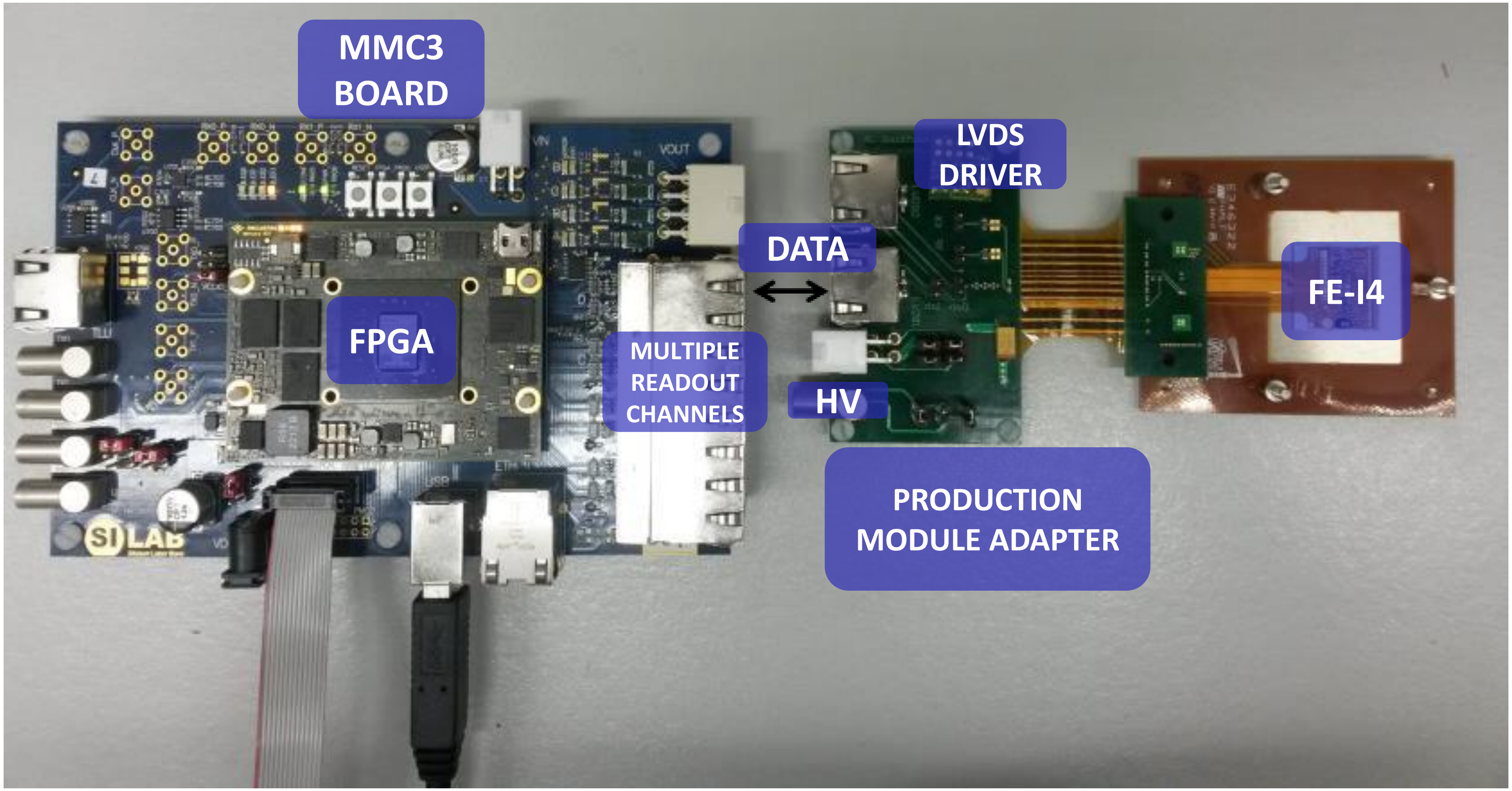
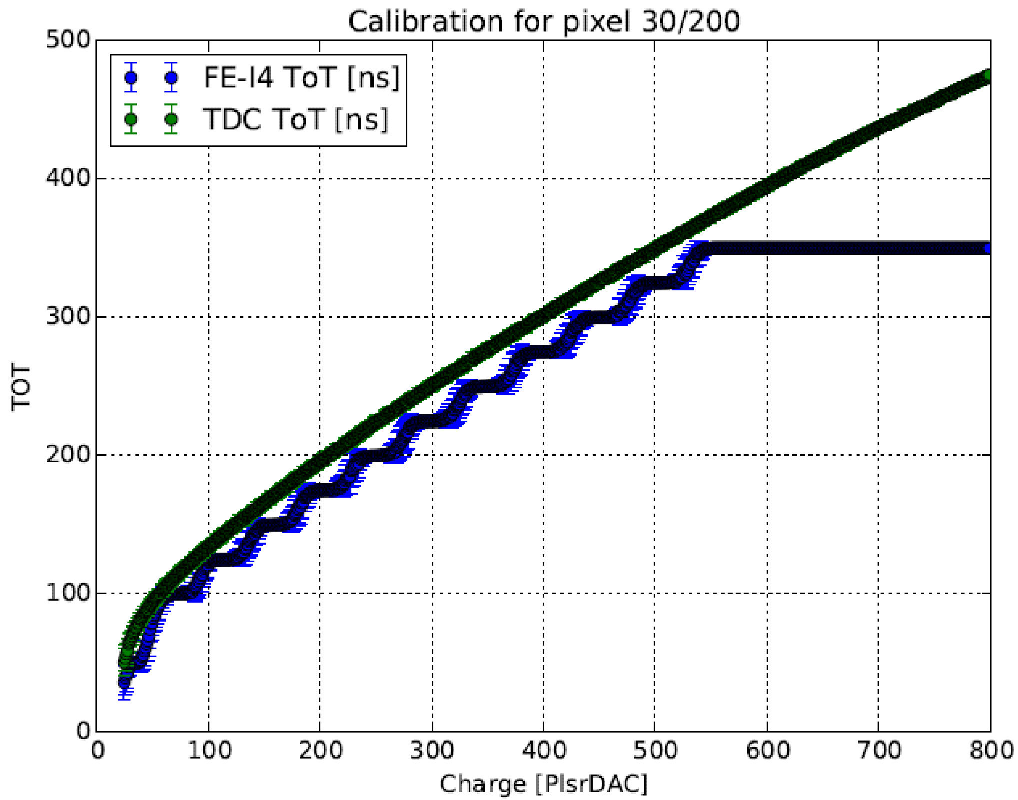


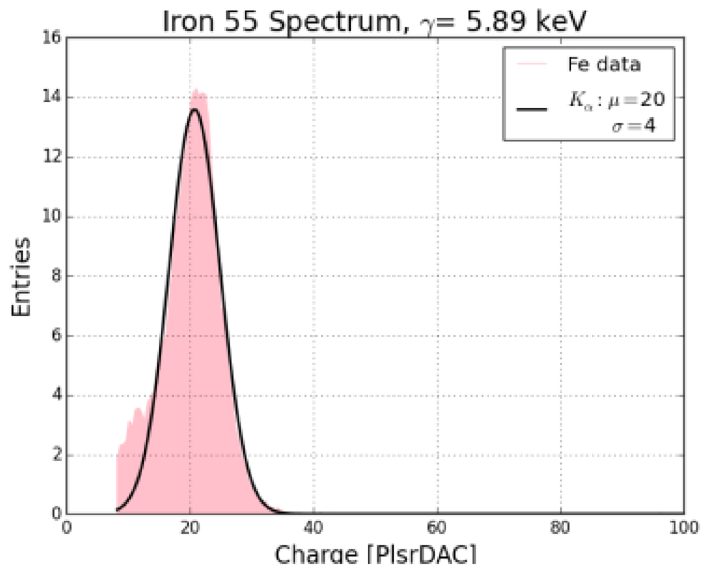
- MMC3: New data acquisition system for the BEAST experiment
  - Multiple FE read out in parallel
  - Faster FPGA; TDC Method may be improved
- Single ended HitOr signal converted to an LVDS signal.

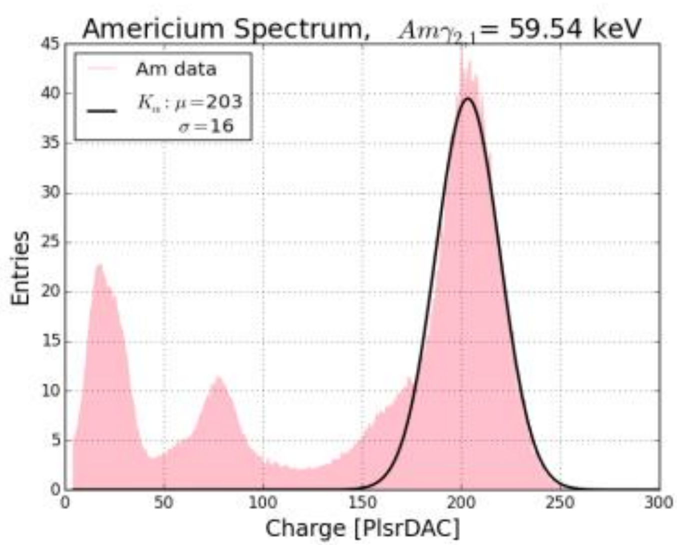
Pixel-per-pixel Calibration of Hit Or Signal

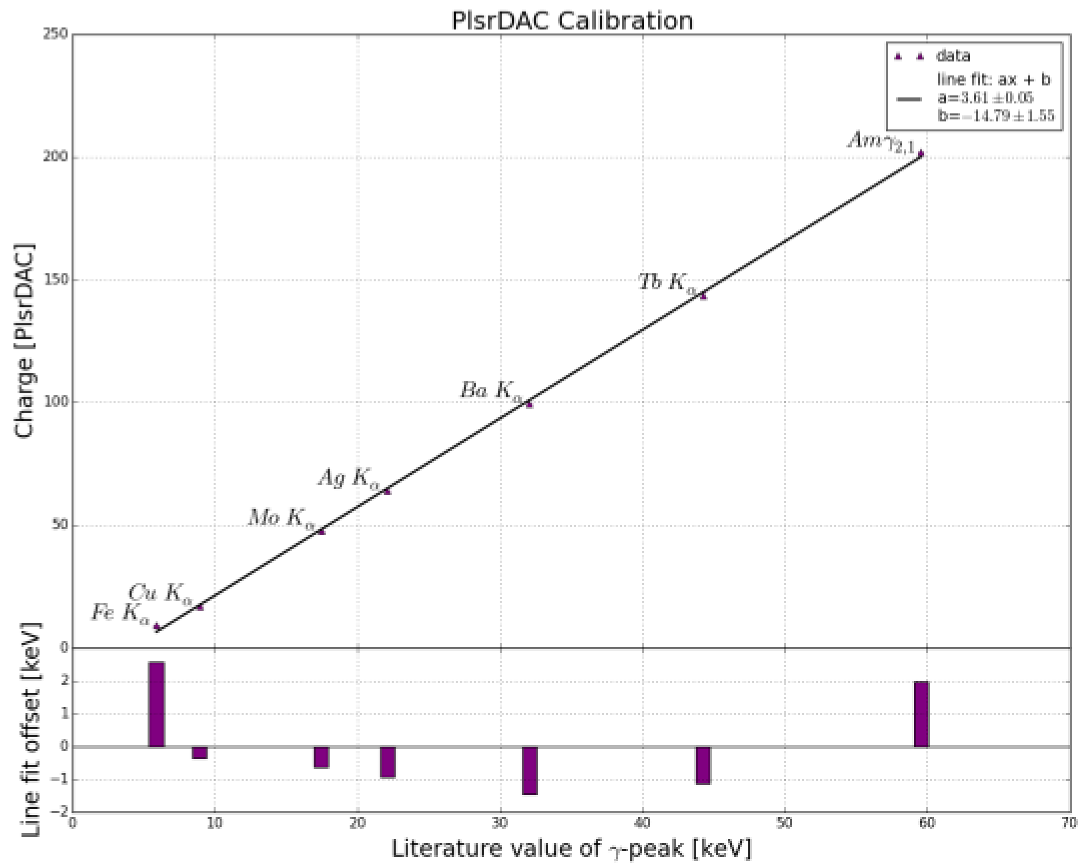


- Precise energy resolution requires pixel per pixel calibration
- Internal charge injection in units of PlsrDAC
- V_{th} and TDC as a function of charge different for each pixel.

Calibration and Dynamic Range







- Dynamic range 10-60 keV (wider also possible)
- Lowest measured plsrDAC value ~ 7
  - Threshold of ~1000 electrons feasible

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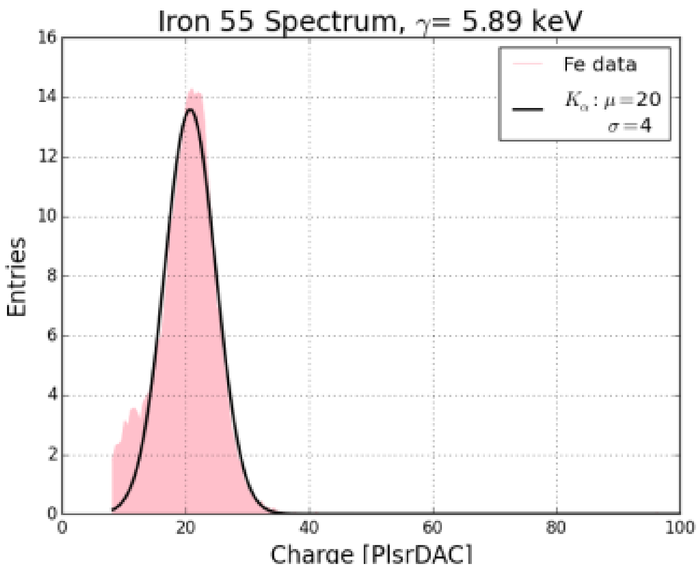
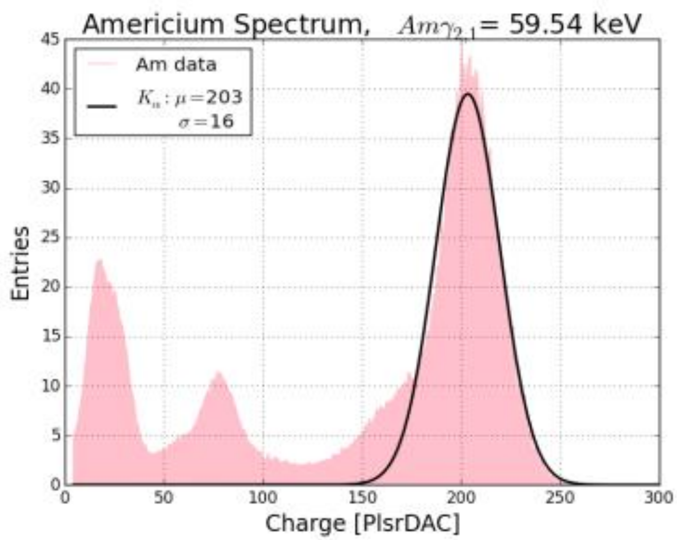
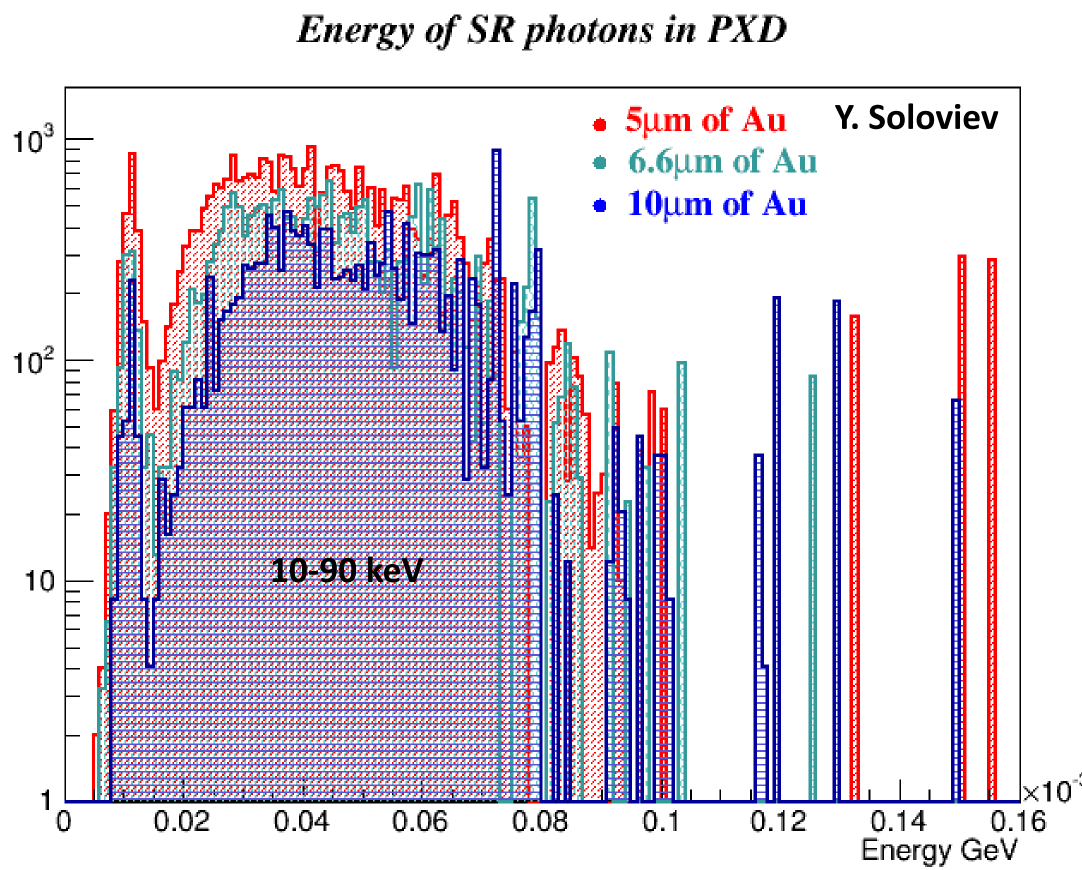
Calibration and Dynamic Range







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- Lowest measured plsrDAC value ~ 7
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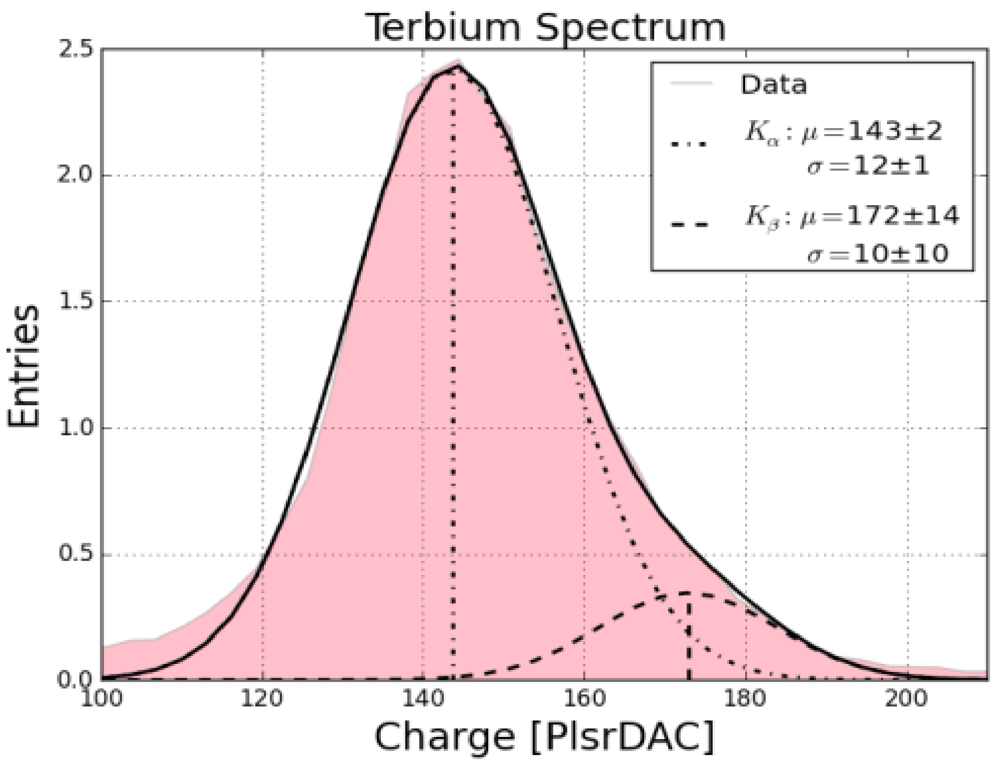
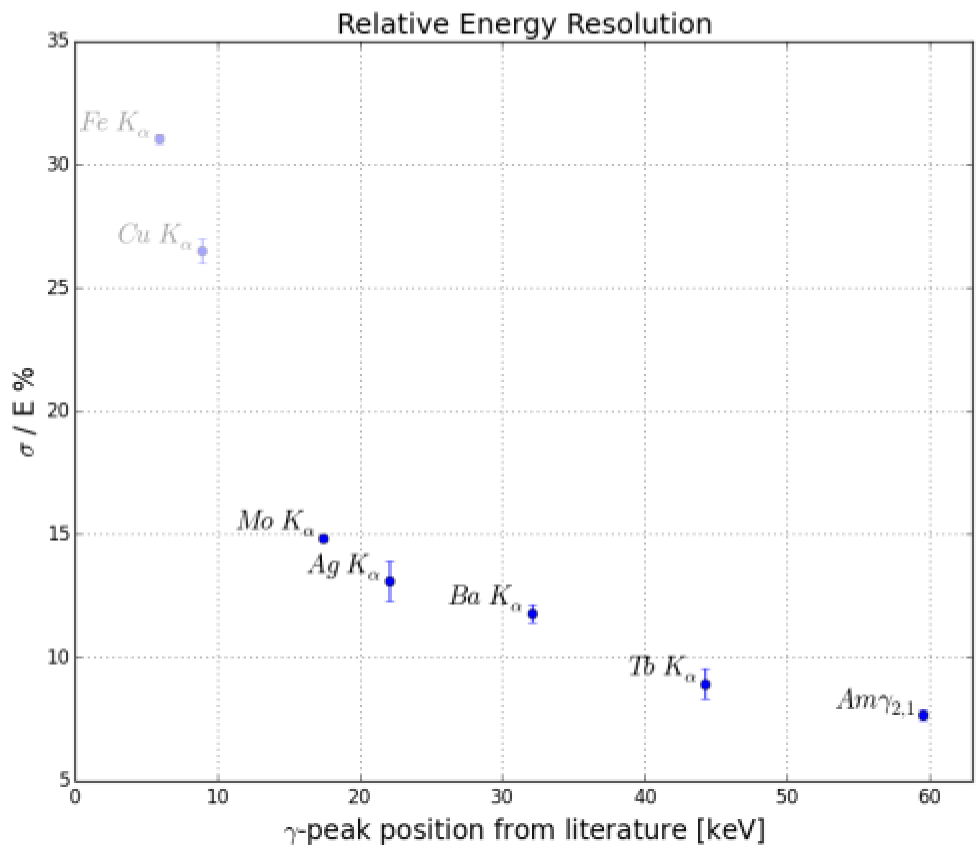
Energy Resolution

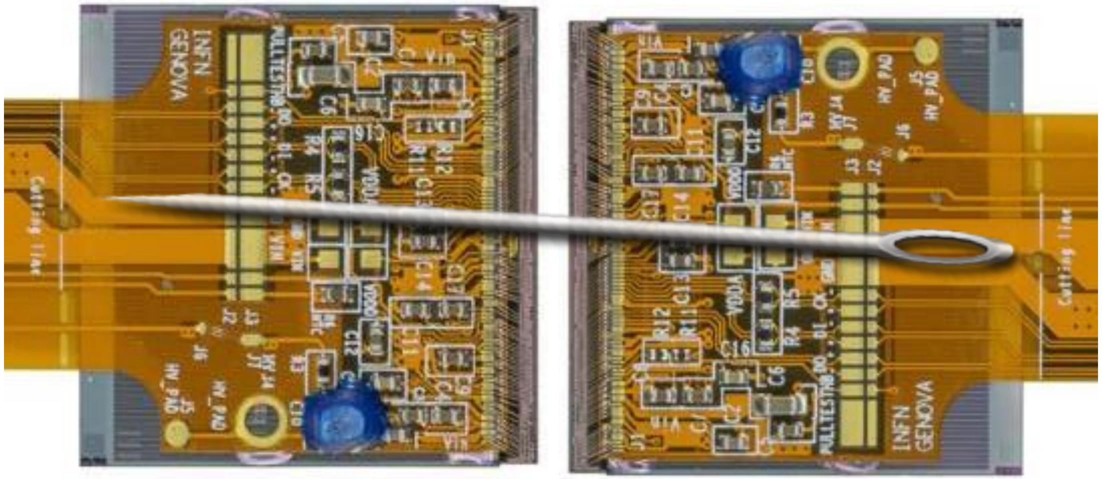


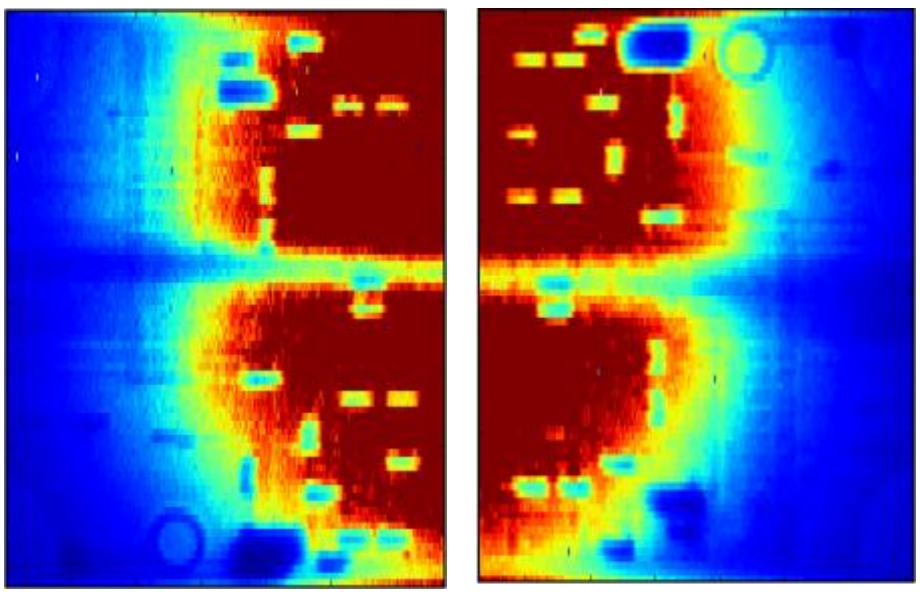


- Terbium K_α=44.2 keV, K_β =50.7 keV
- ΔE = 6.4 keV

- Adequate energy resolution
- Better than 15 % above 10 keV

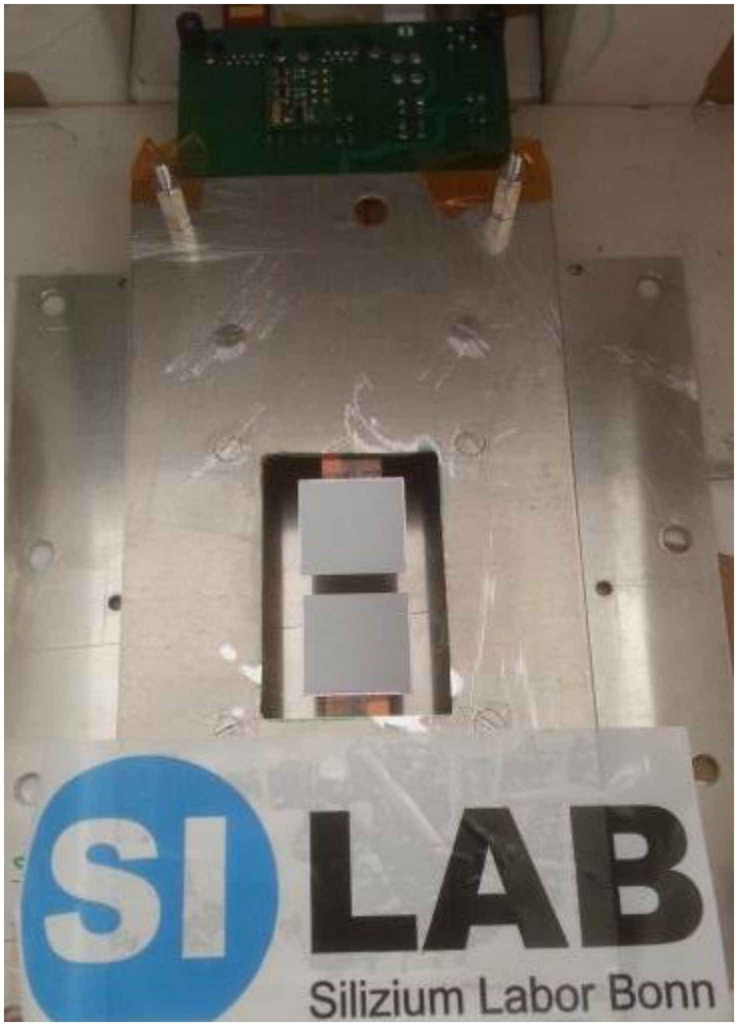
Multiple Chip Readout

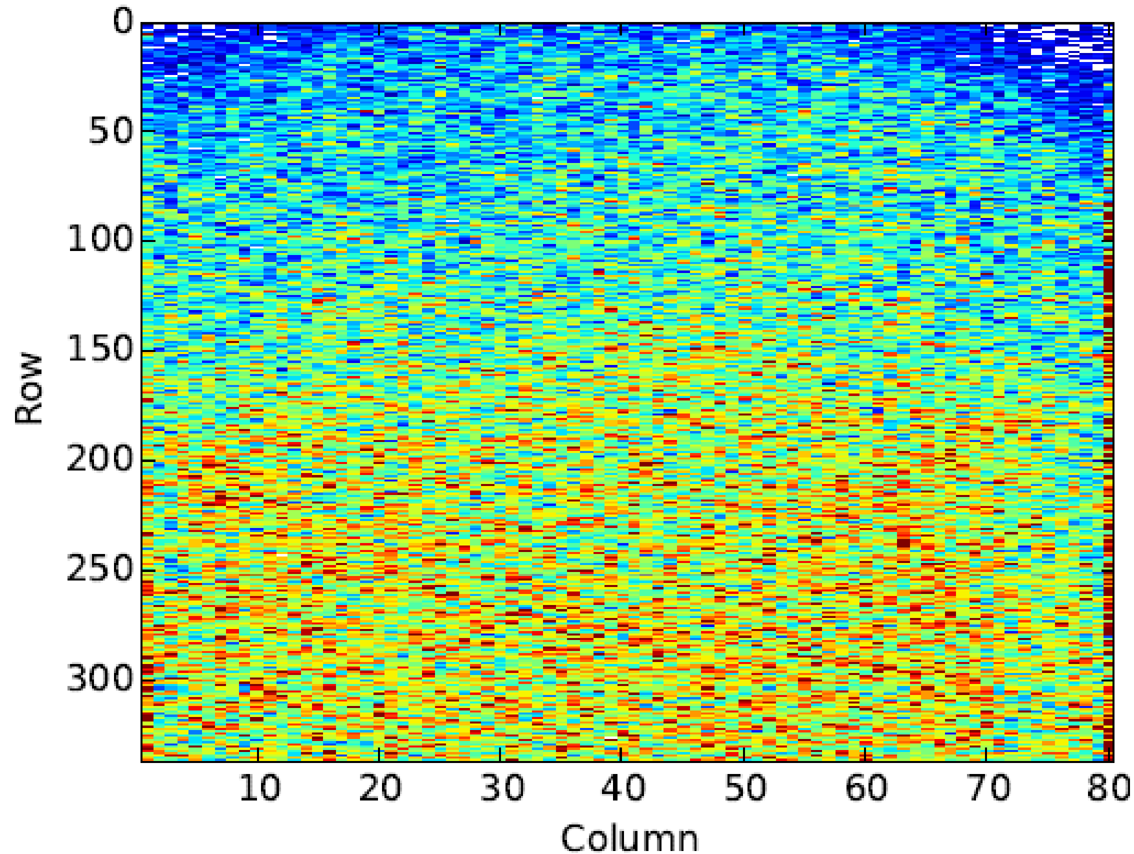




- Hit map two FE under Sr90 illumination
- Multiple module parallel readout with MMC3
- Current stave design prompted by absorption of flex components

Backside Illumination

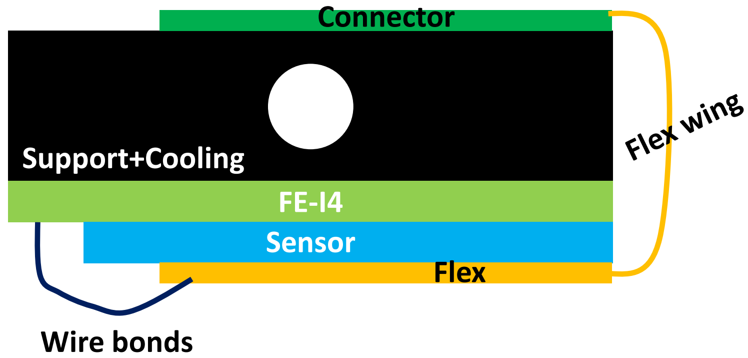


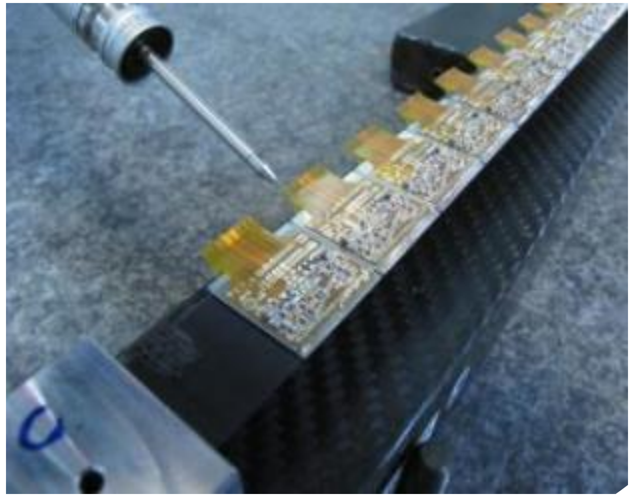


- Effect of components is eliminated by taking a source scan via backside (FE) illumination
- For BEAST, no material in front of the sensor; kapton running parallel to the modules

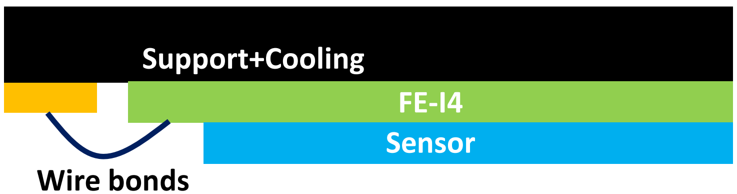
FANGS Stave Design Concept

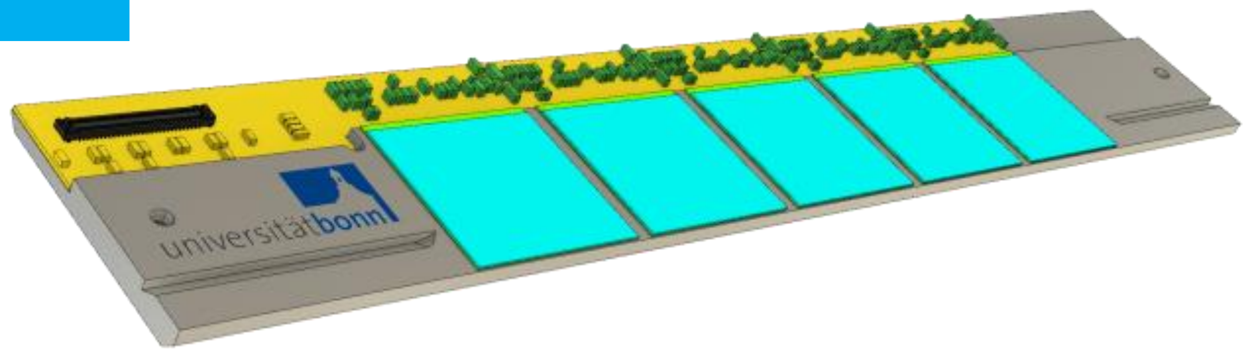
- Initial concept, following IBL stave design



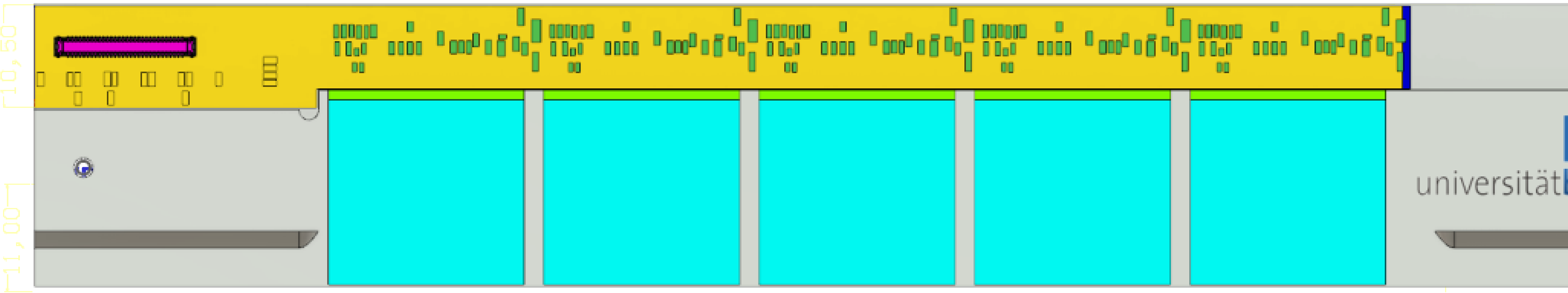


- Revised design, adapted to BEAST needs



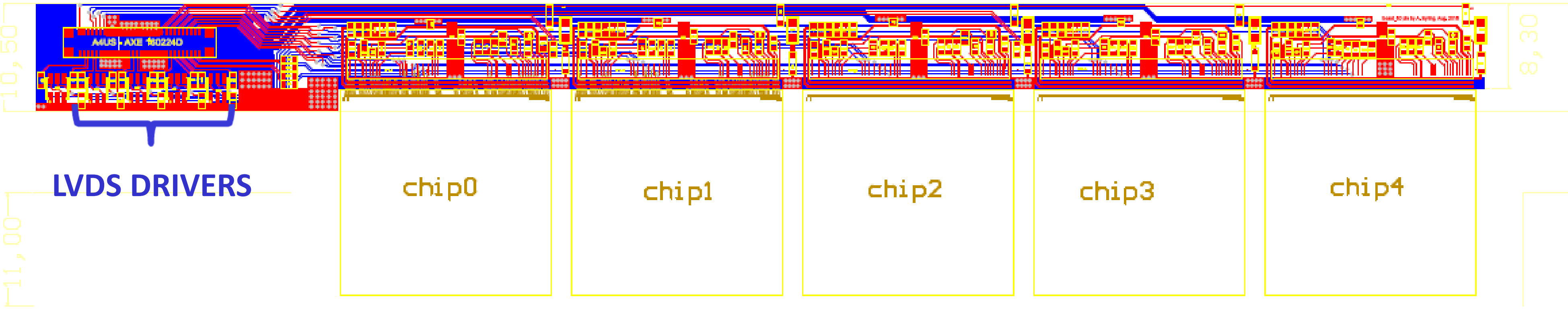


Kapton Design



- Flex design for a single stave of 5 FE-I4 chips
- LVDS drivers converting single ended HitOr signal to differential signal for propagation over long cables
- Drivers positioned in backward direction shielded from radiation behind the PXD cooling block
- Radiation hardness to be investigated

Kapton Design



- Flex design for a single stave of 5 FE-I4 chips
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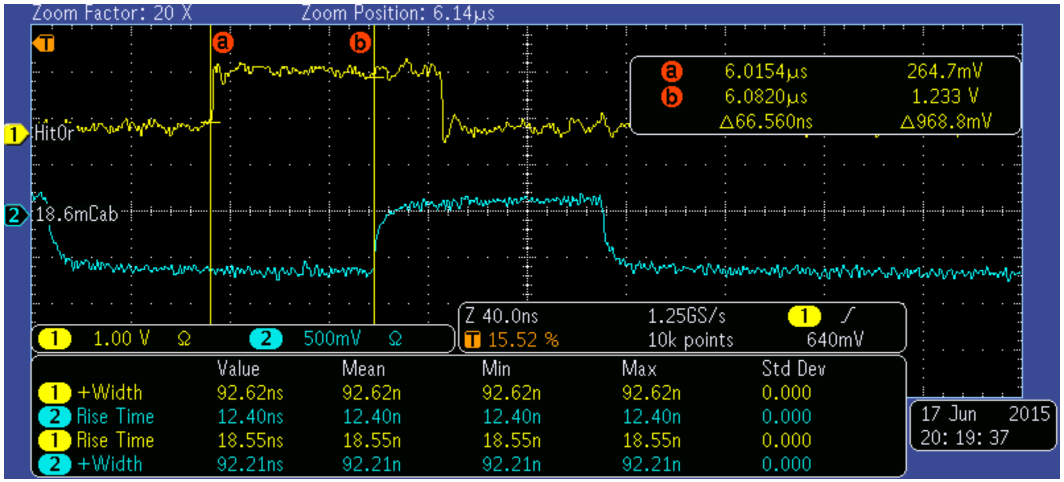
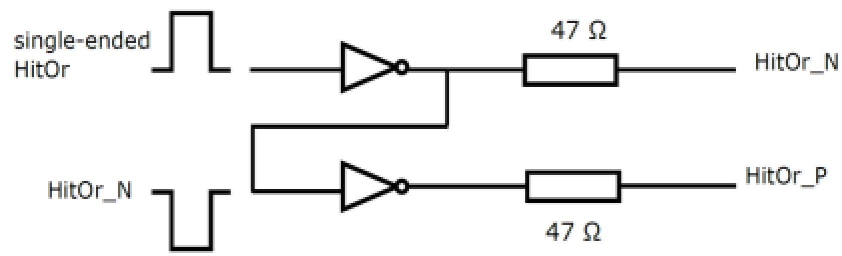
Hit Or Delay and Signal Quality Measurements

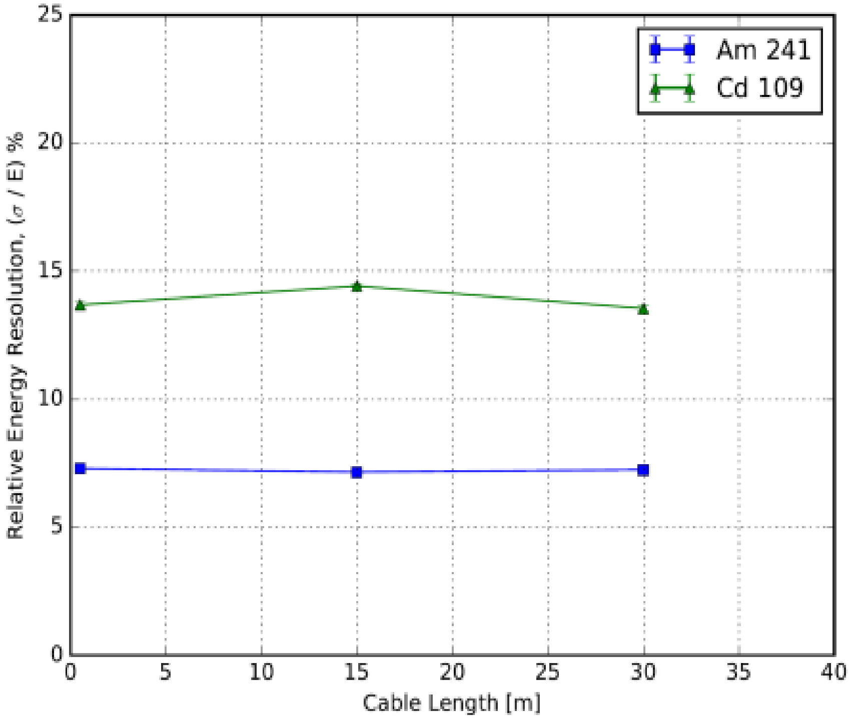


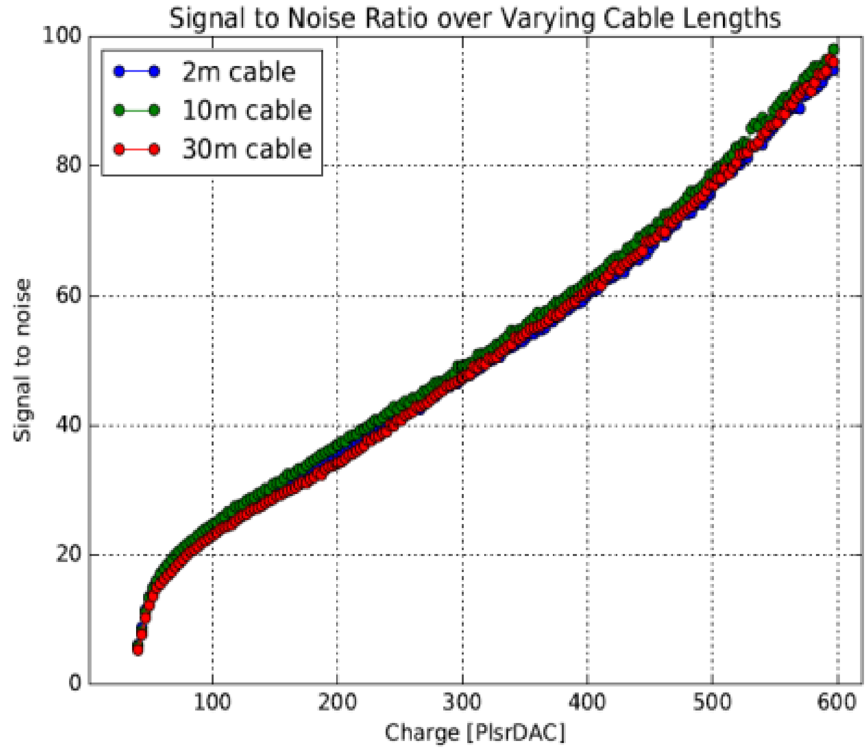


- Convert single ended HitOr to differential

- Propagation delay of HitOr over a 19 m CAT 7
- Signal integrity maintained with delay of ~60 ns
- Improvement pulse shape under investigation

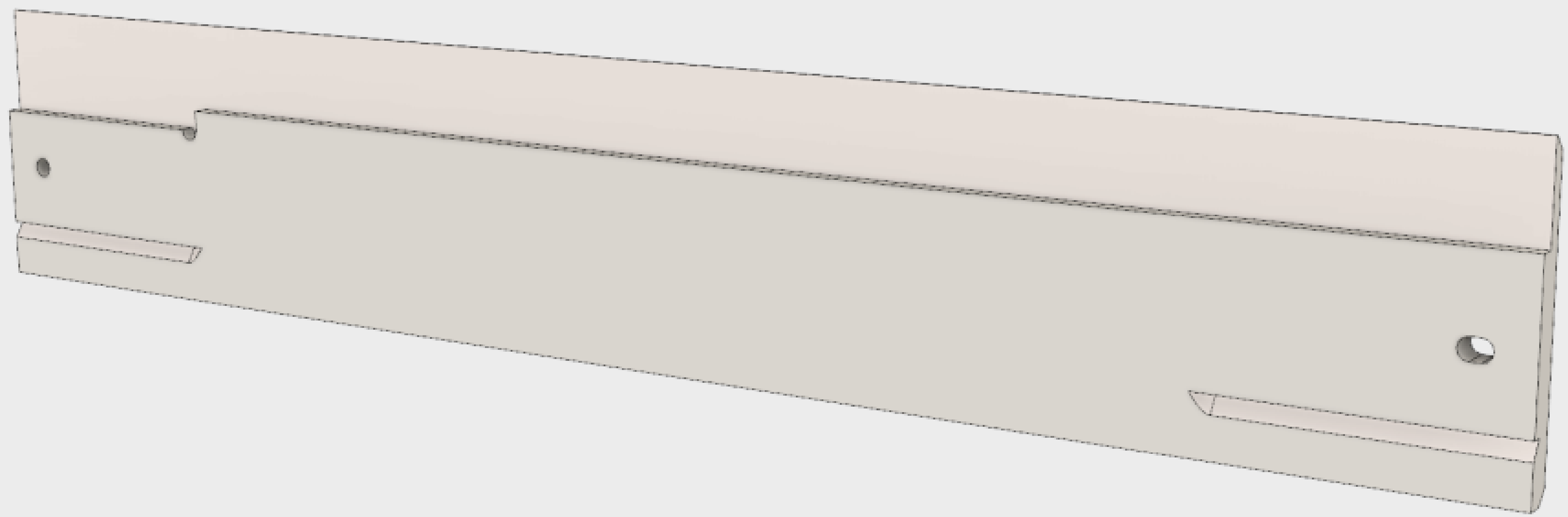
Signal Integrity



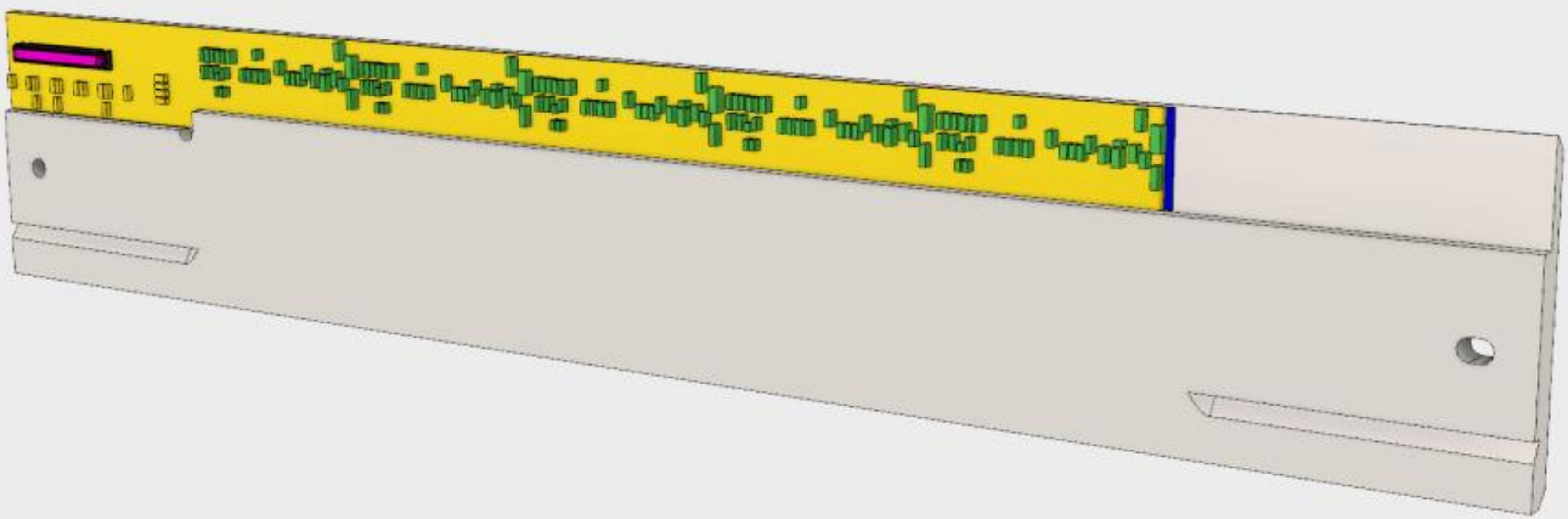


- Signal integrity maintained over 20 m cable
- Proper resolution over this range

FANGS Stave Assembly



FANGS Stave Assembly



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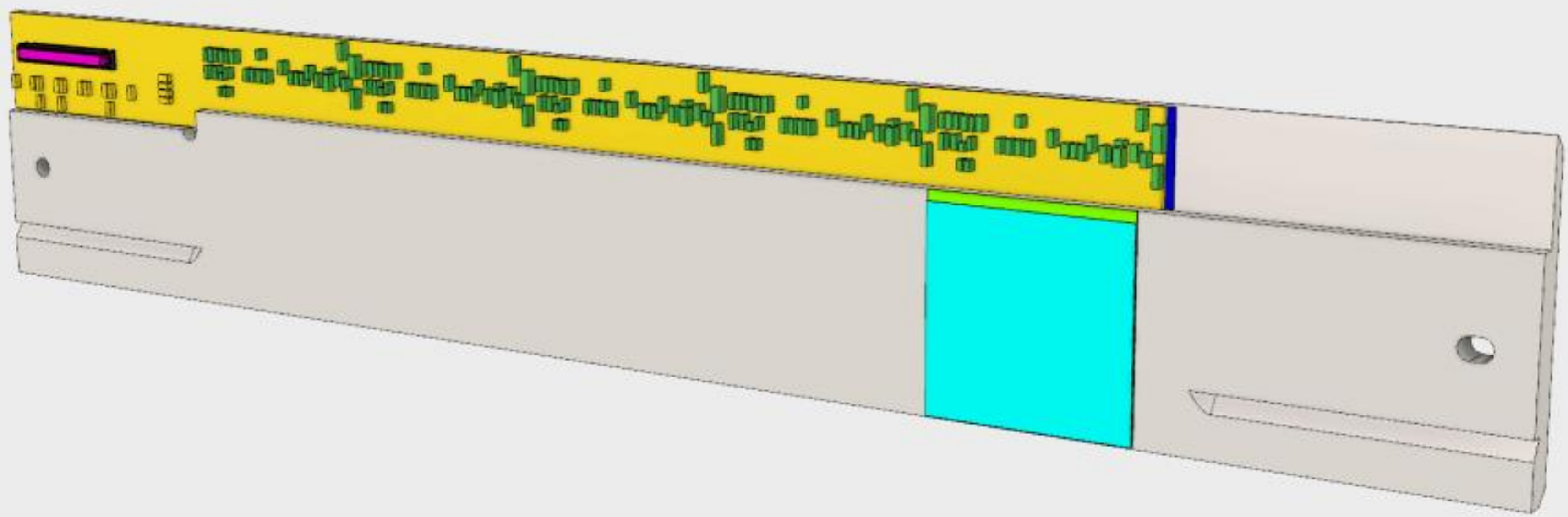
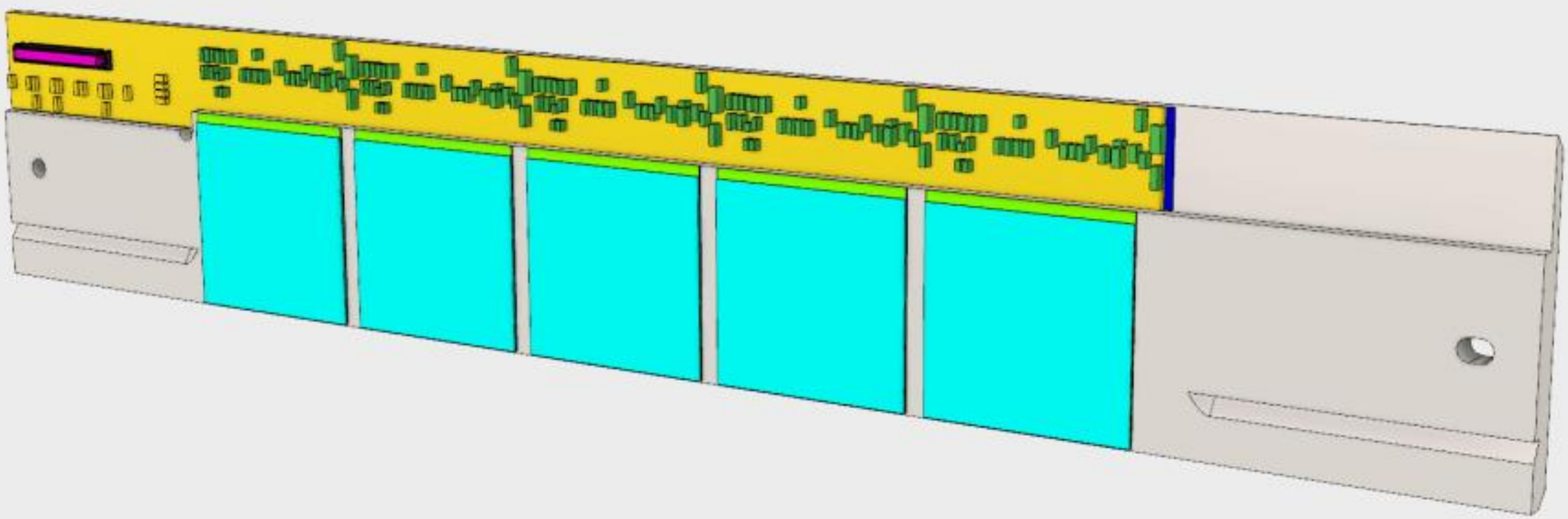
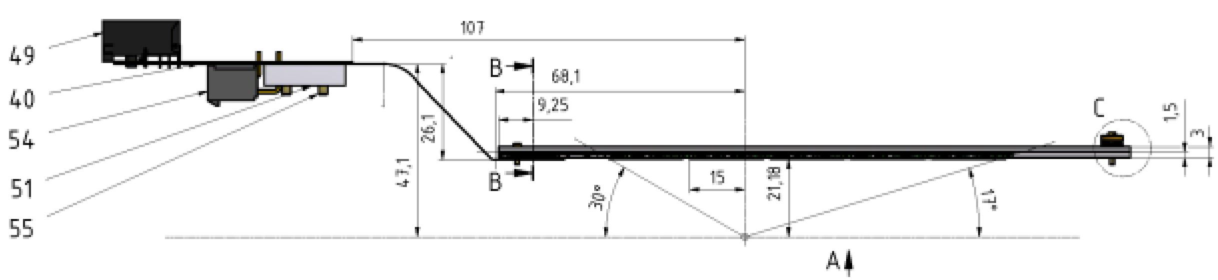
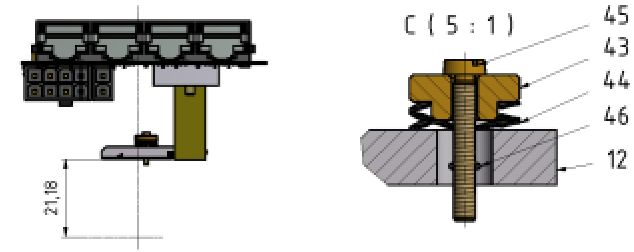


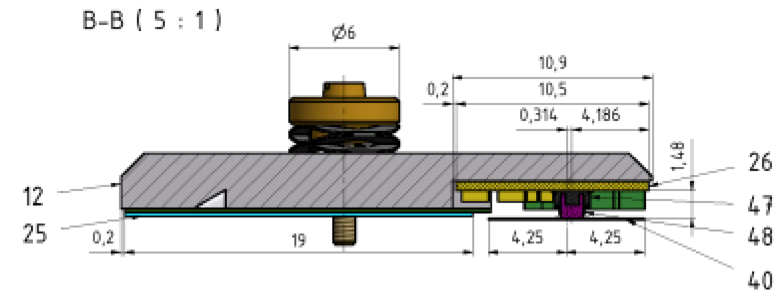
FANGS Stave Assembly

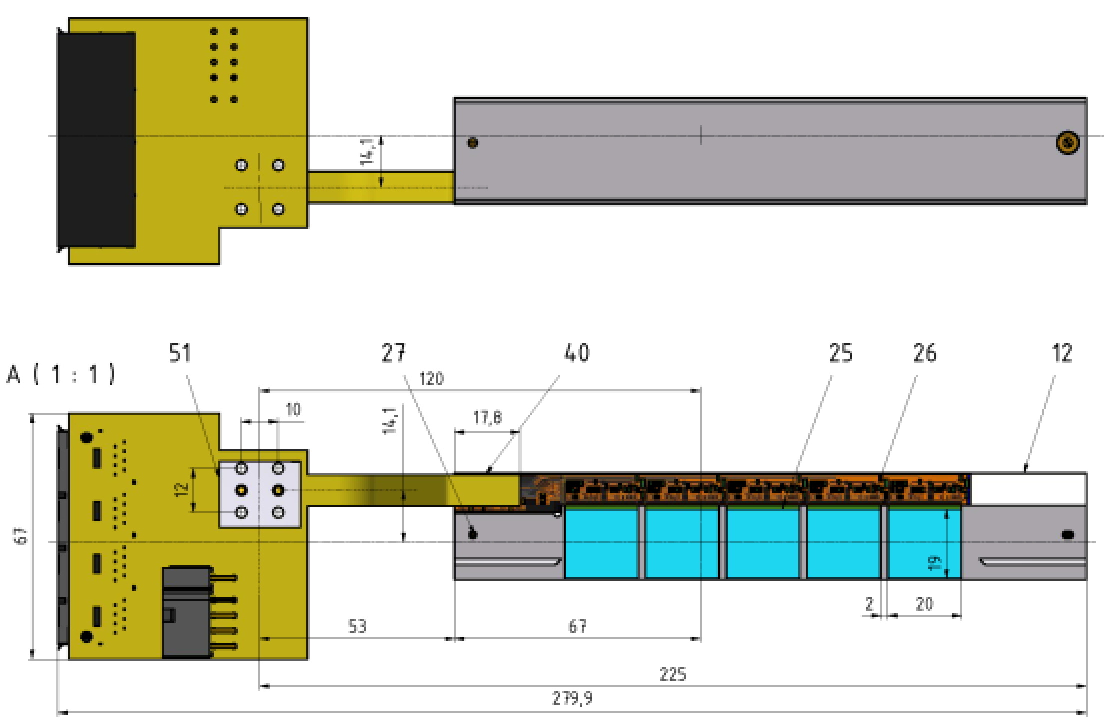


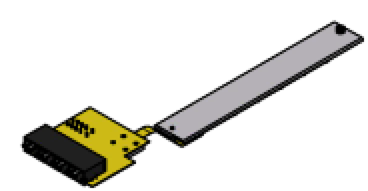
FANGS Stave Fully Equipped





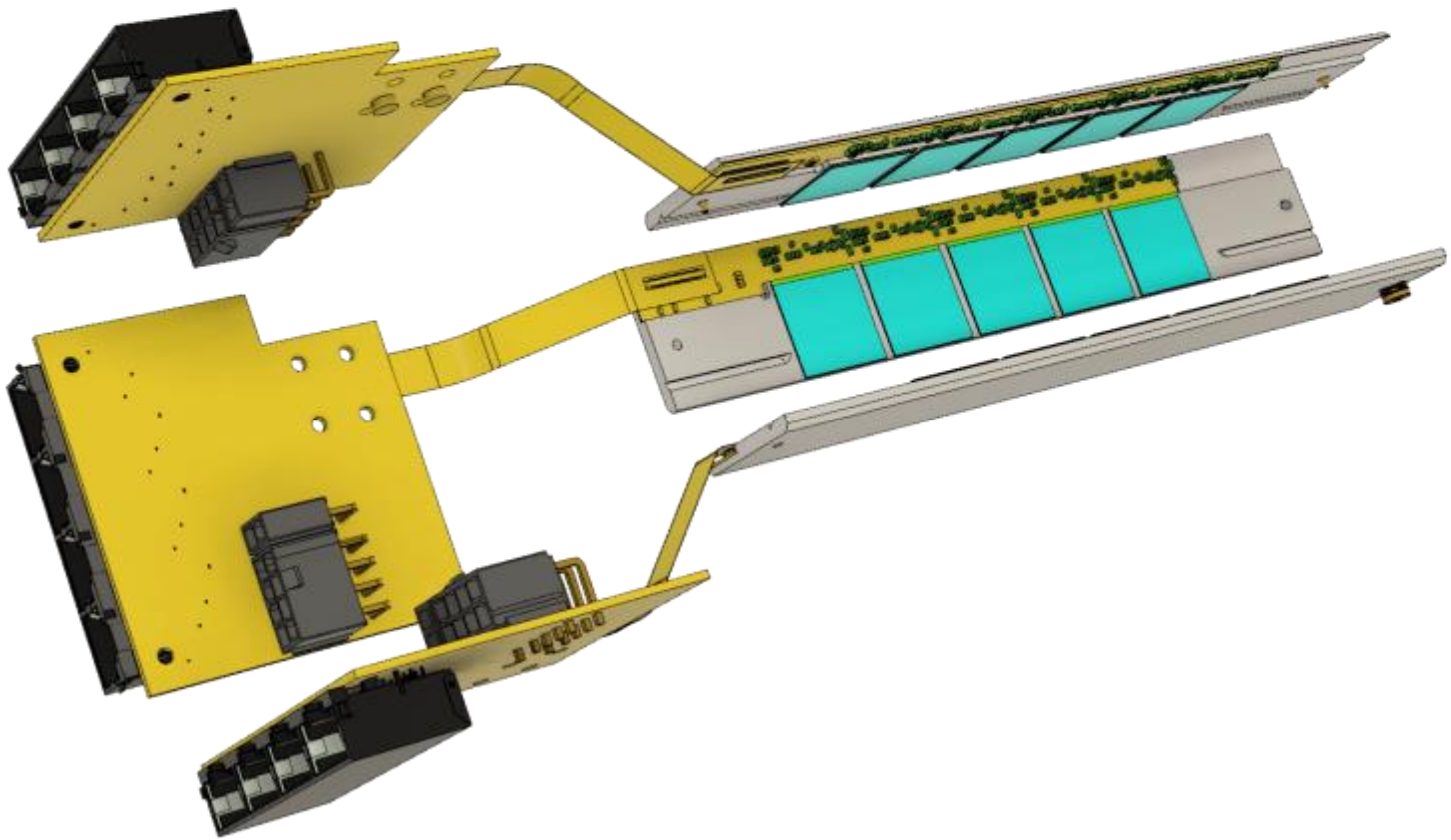




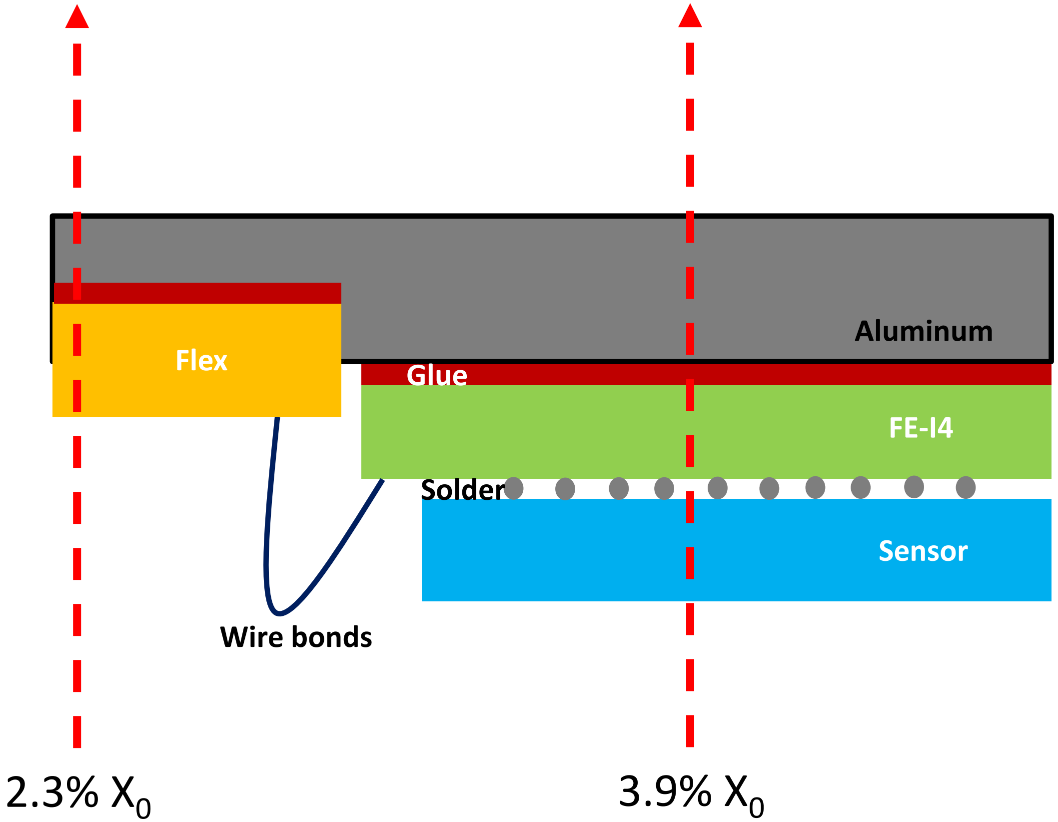


FANGS System

3 Staves: Covering 90º , 180º , 270º in ϕ, *full* acceptance in θ



Aluminum Stave Material Budget



- Support:
3 mm thick Aluminum → 3.4%X_0
- Glue:
50 µm thick Epoxy → 0.014%X_0
- FE-I4
150 µm thick Silicon → 0.16%X_0
- Sensor:
200 µm thick Silicon → 0.21%X_0
- Solder balls
25 µm thick SnAg → 0.17%X_0 (3.3% of the area)
- Flex
100 µm thick polymide → 0.035%X_0
70 µm Cu (2 layers) → 0.50%X_0
50 µm thick Epoxy → 0.014%X_0

Total$_{Max}$: 3.9% X_0

- Low and flat material budget distribution
- No impact in outer detectors
- Further reduction possible if strong physics arguments

Aluminum Stave Material Budget

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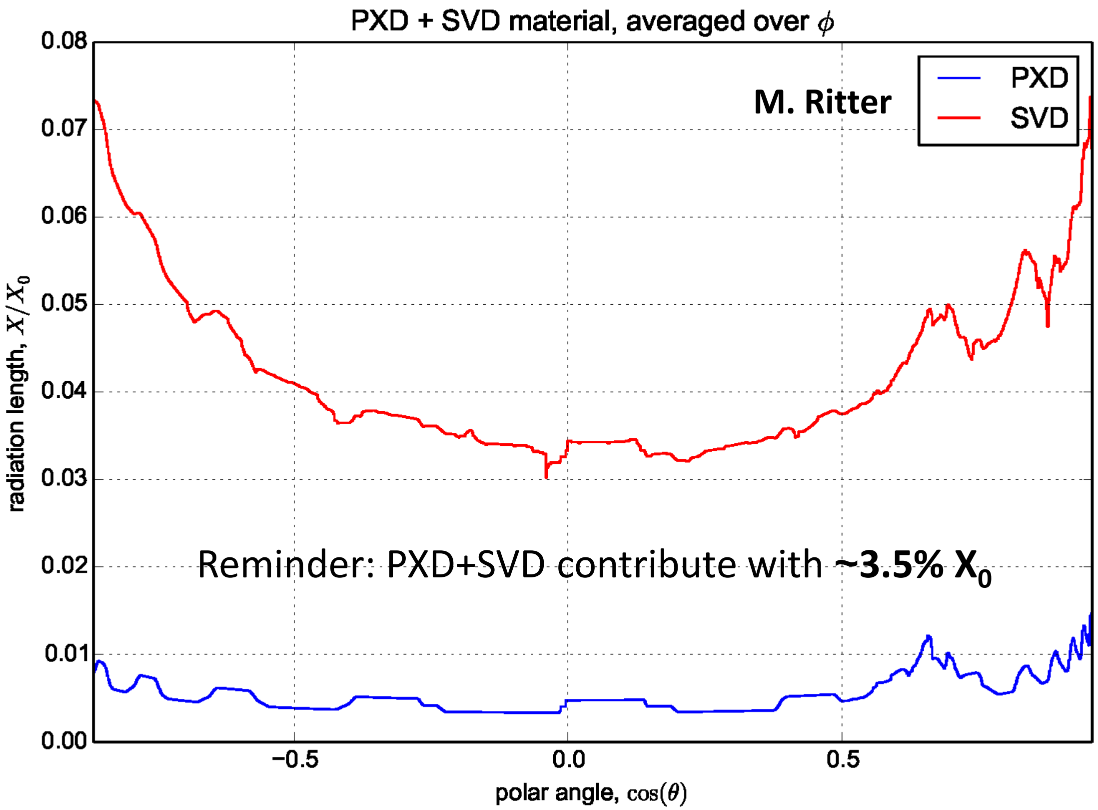


- Low and flat material budget distribution
- No impact in outer detectors

- Support:

3 mm thick Aluminum → 3.4%X_0

- Glue:

50 µm thick Epoxy → 0.014%X_0

- FE-I4

150 µm thick Silicon → 0.16%X_0

- Sensor:

200 µm thick Silicon → 0.21%X_0

- Solder balls

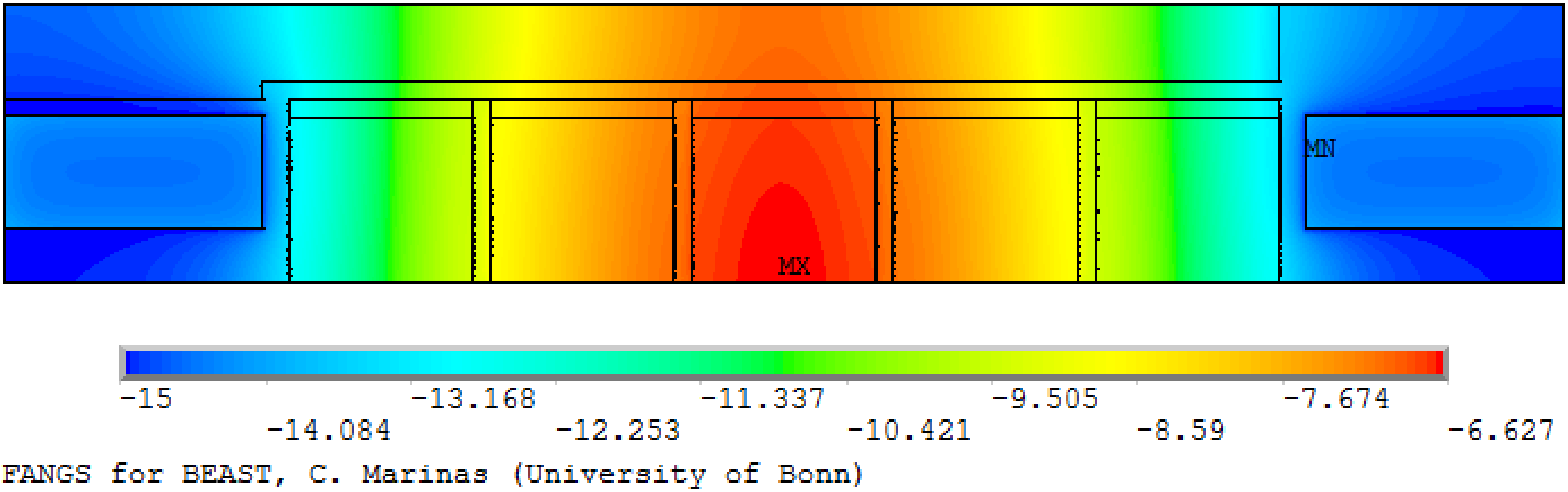
25 µm thick SnAg → 0.17%X_0 (3.3% of the area)

- Flex

66 µm thick polymide → 0.023%X_0
24 µm Cu (2 layers) → 0.17%X_0

Total$_{Max}$: 3.9% X_0

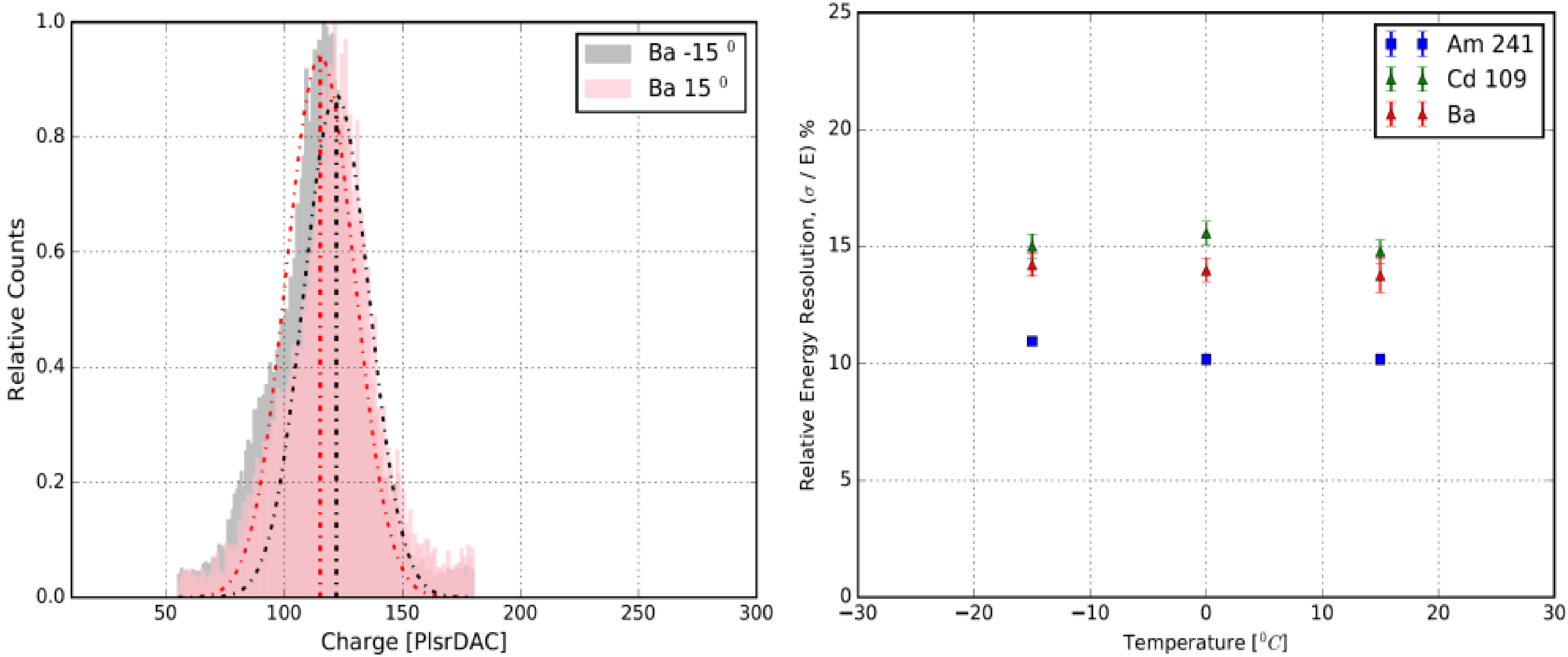
FEA of the FANGS Stave



- Maximum temperature = -7 ºC
- Maximum ΔT within one sensor = 5 ºC
- Power = 1.2 W each FE
- Cooling block = -15 ºC
- Environment = 20 ºC at 2 m/s

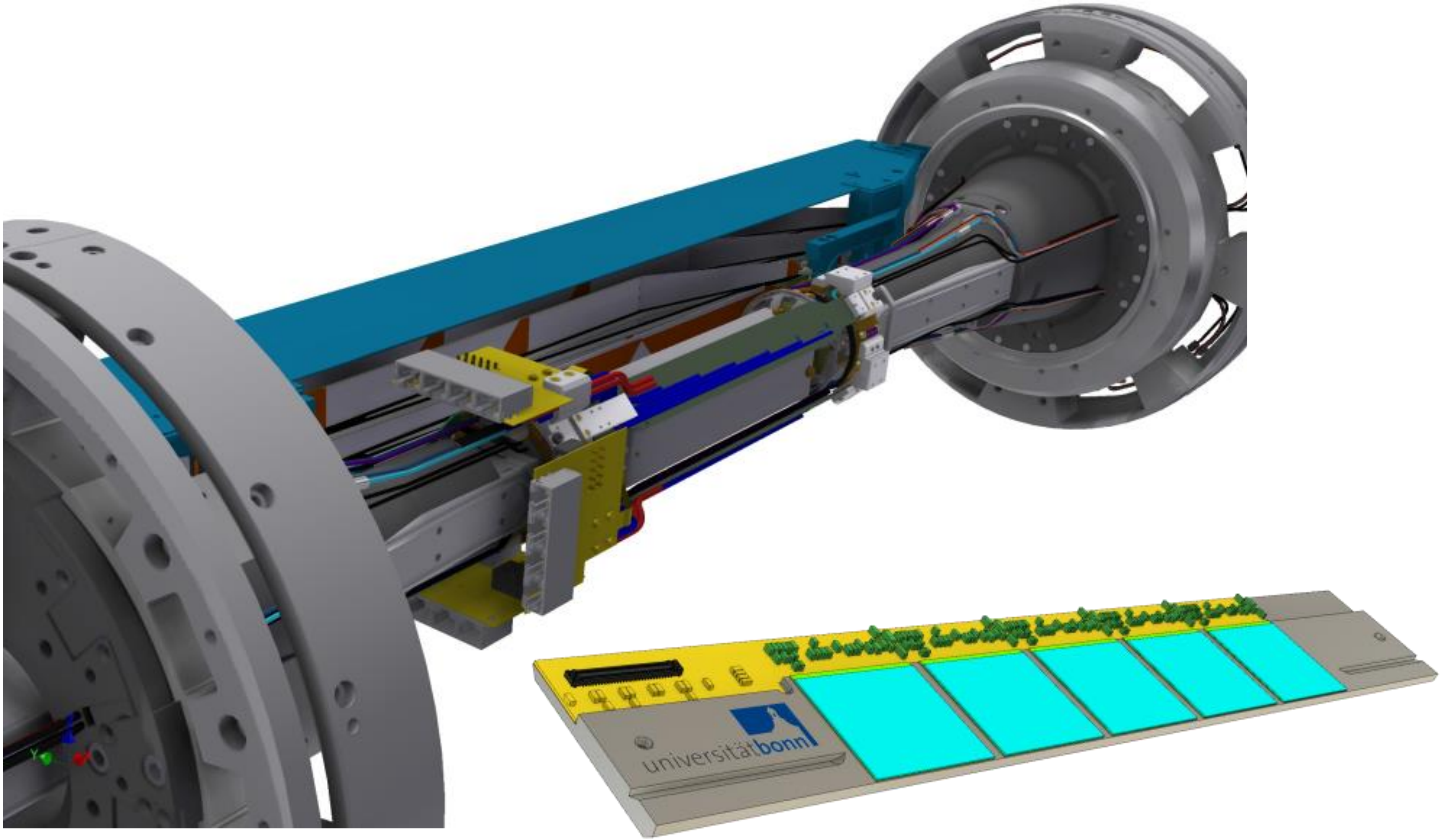
- Proper heat handling
- Low and flat temperature profile
- FOS integrated on the Al profile for temperature measurements

Energy Resolution with Temperature

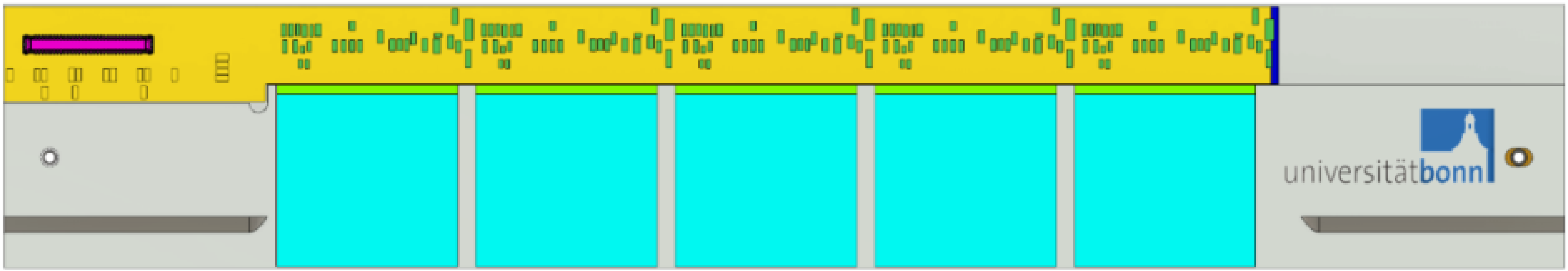


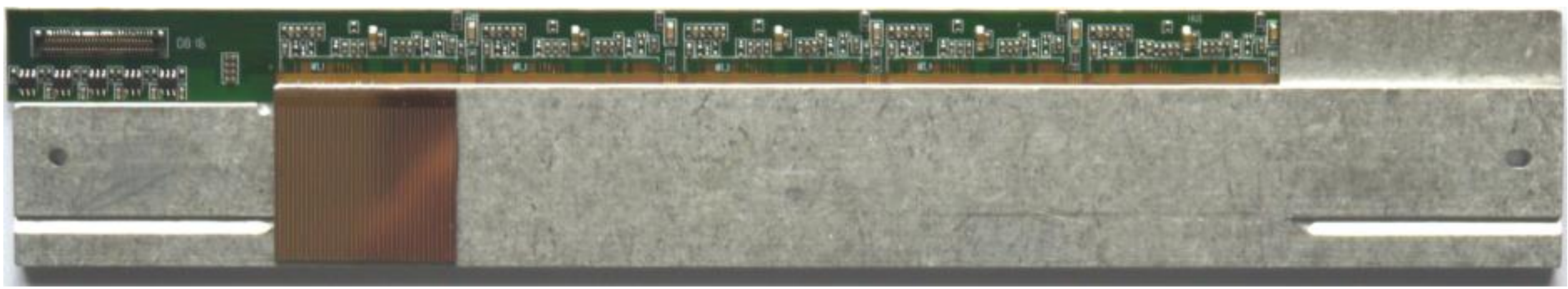
- No performance degradation is observed over the expected temperature range

FANGS Phase 2 Set Up



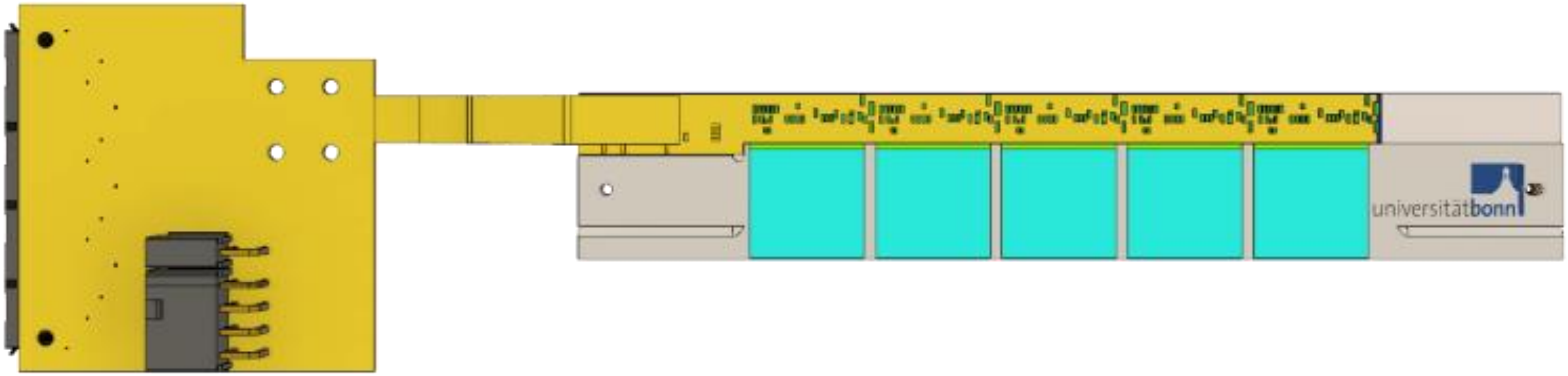
Stave Production

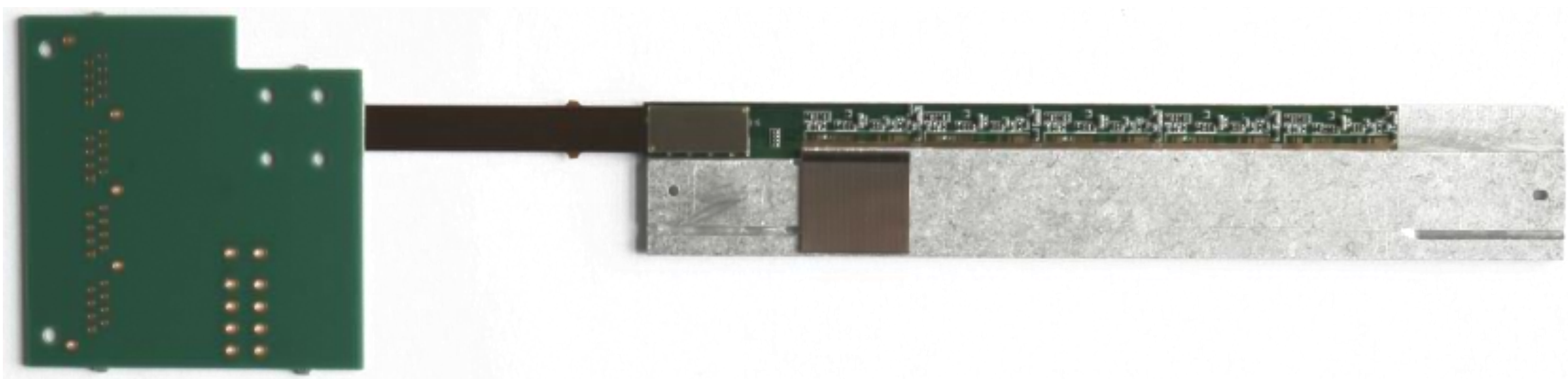




- First stave being produced
- All components in place (including FOS)

Stave Production





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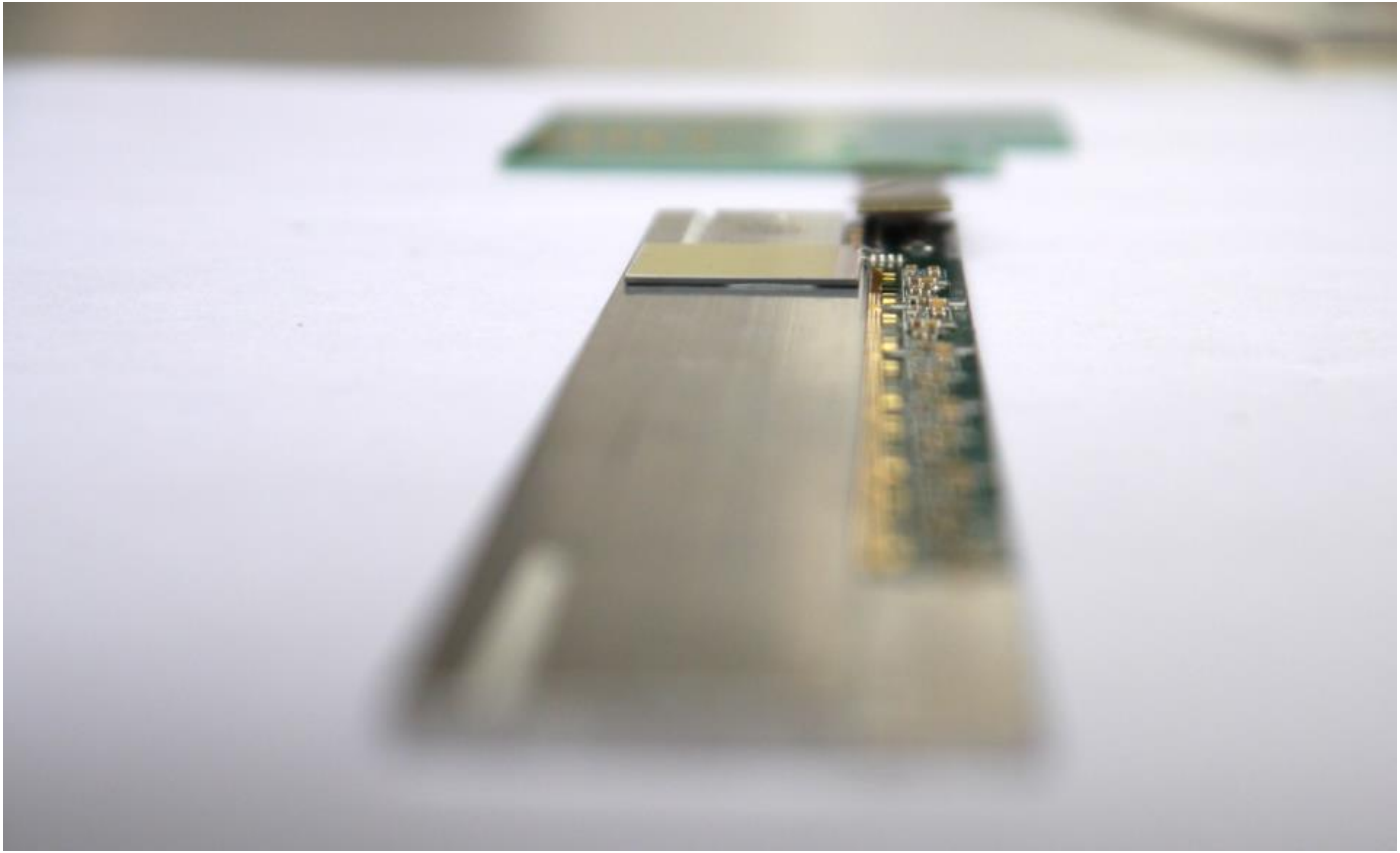
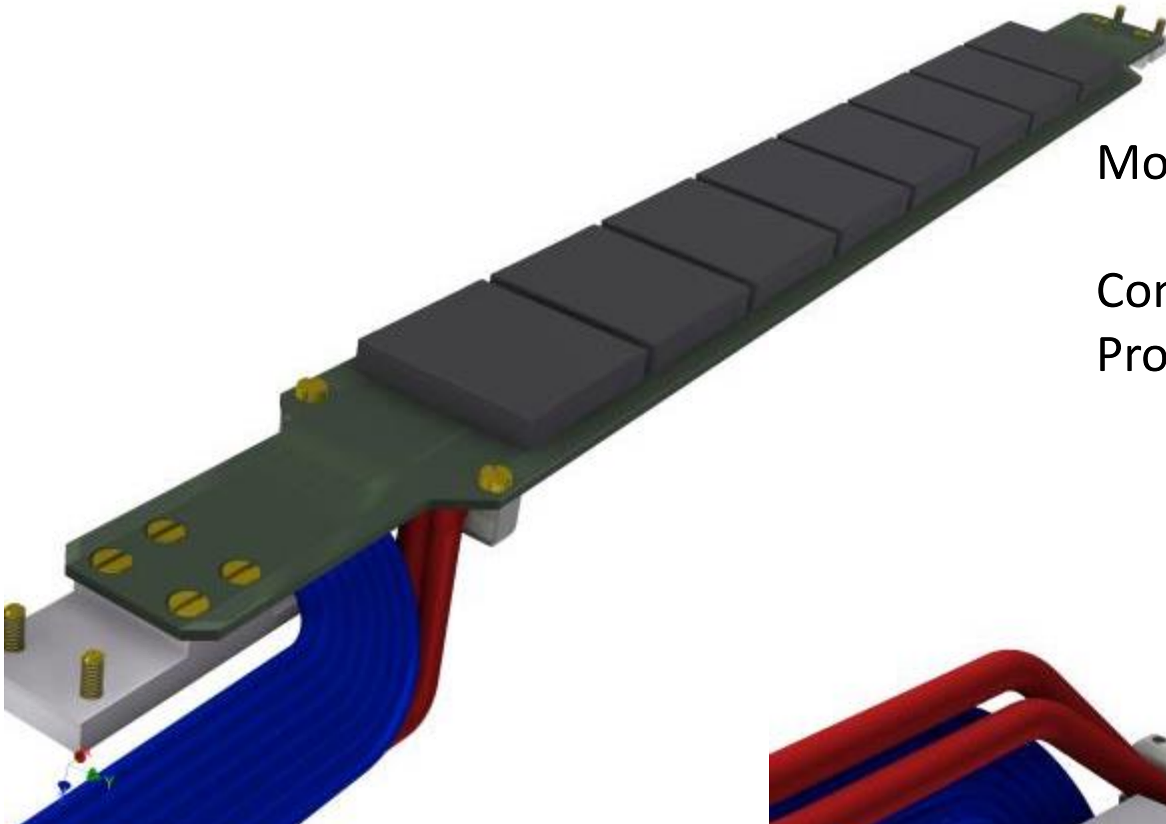
Stave Production

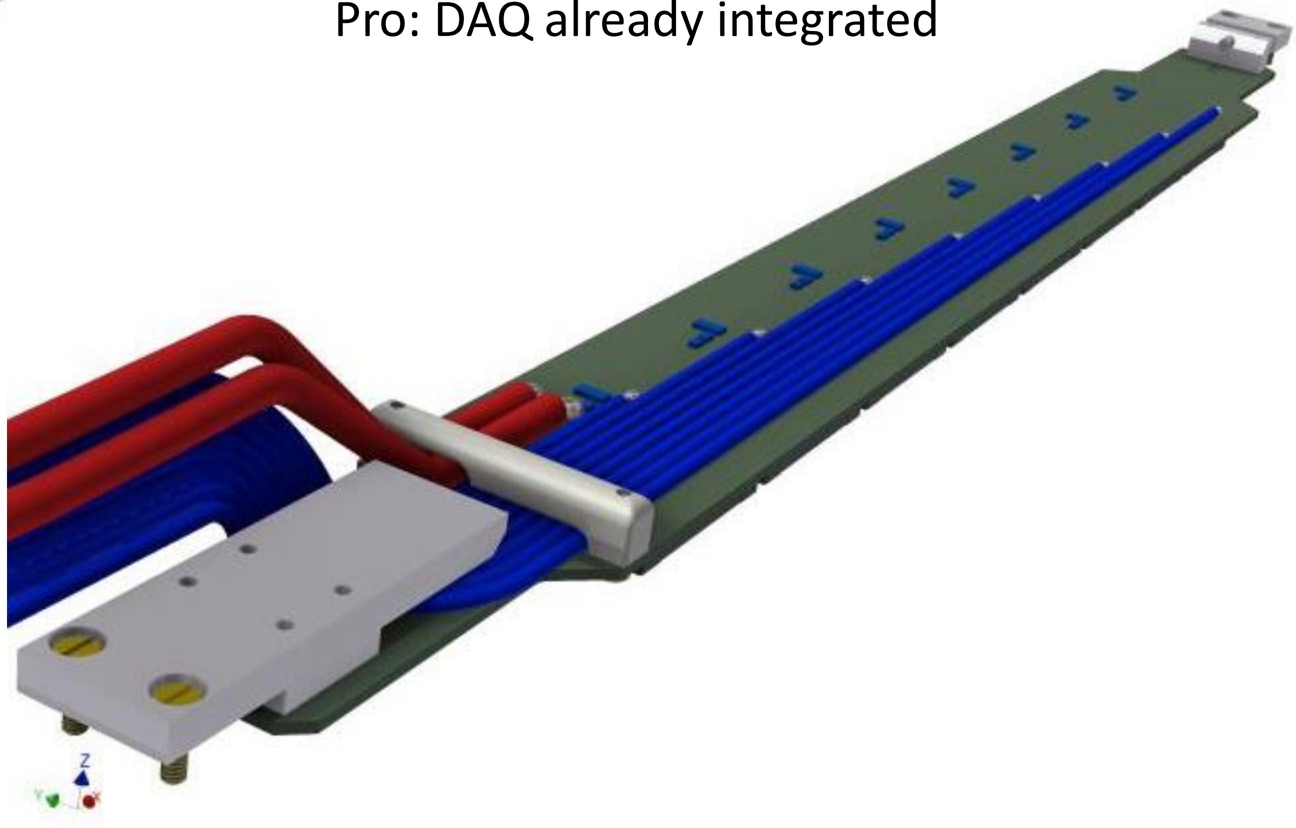


CLAWS Staves



Mostly focus on Phase 1

Con: Phase 2 development slightly delayed
Pro: DAQ already integrated



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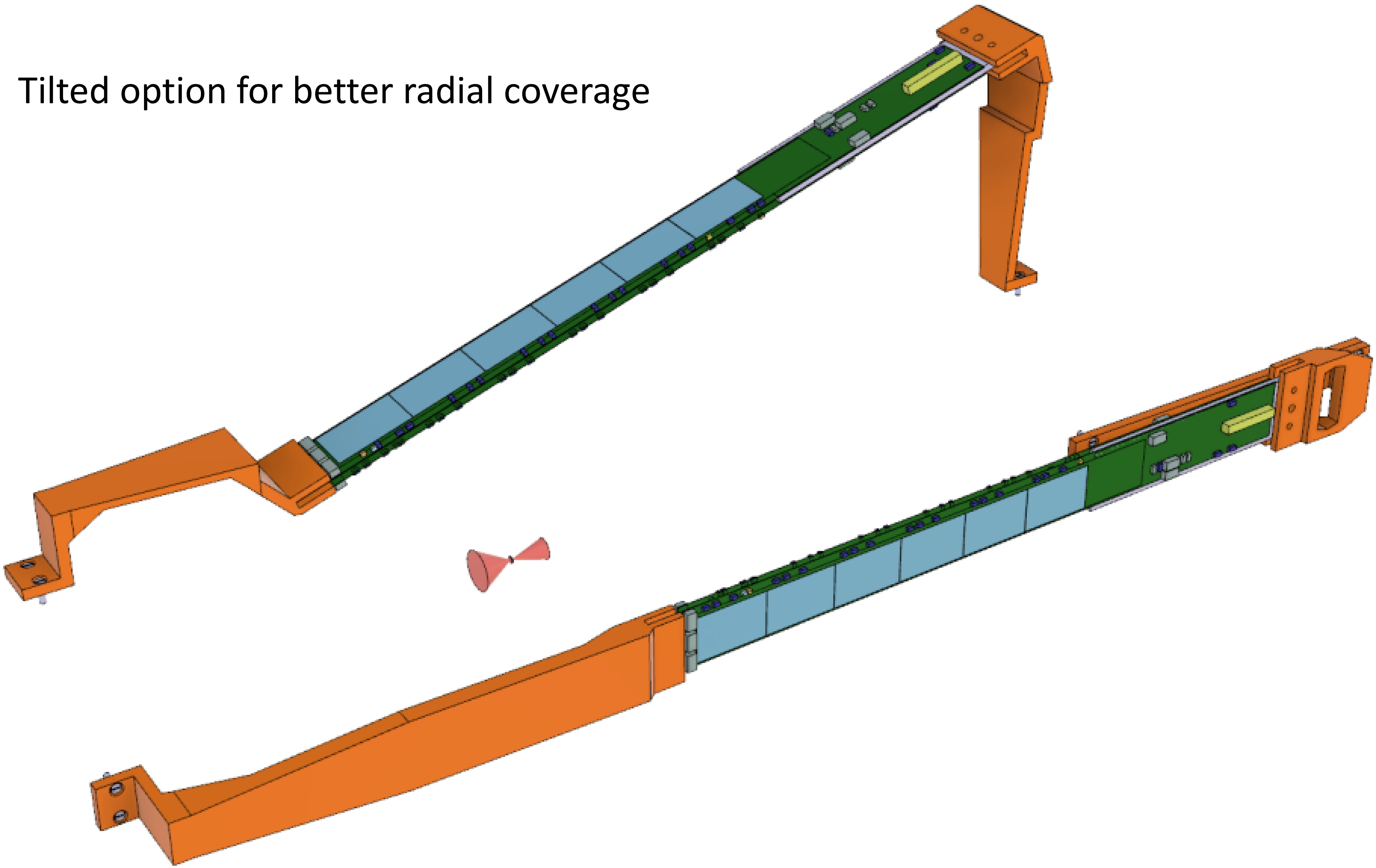
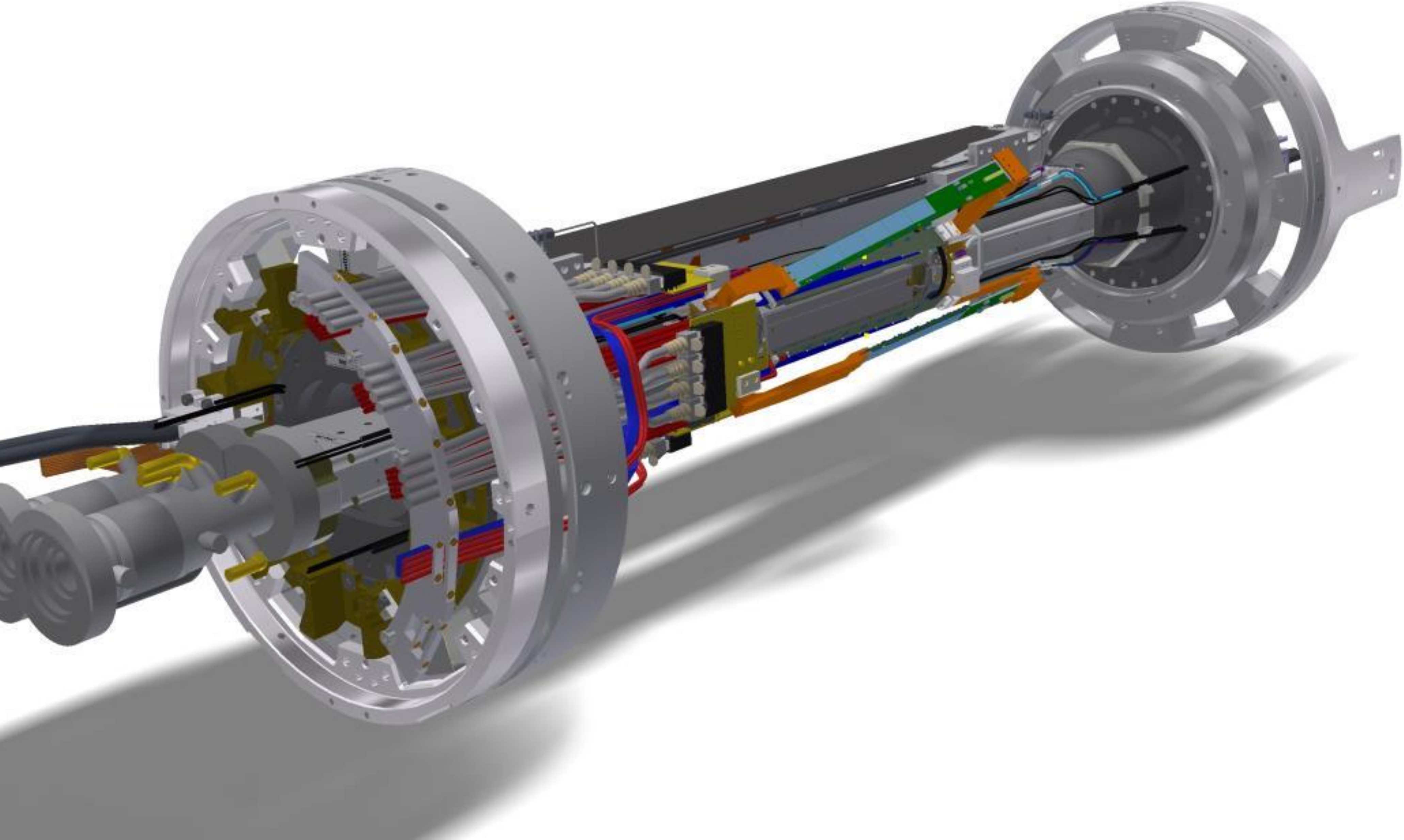
PLUME Staves

Tilted option for better radial coverage



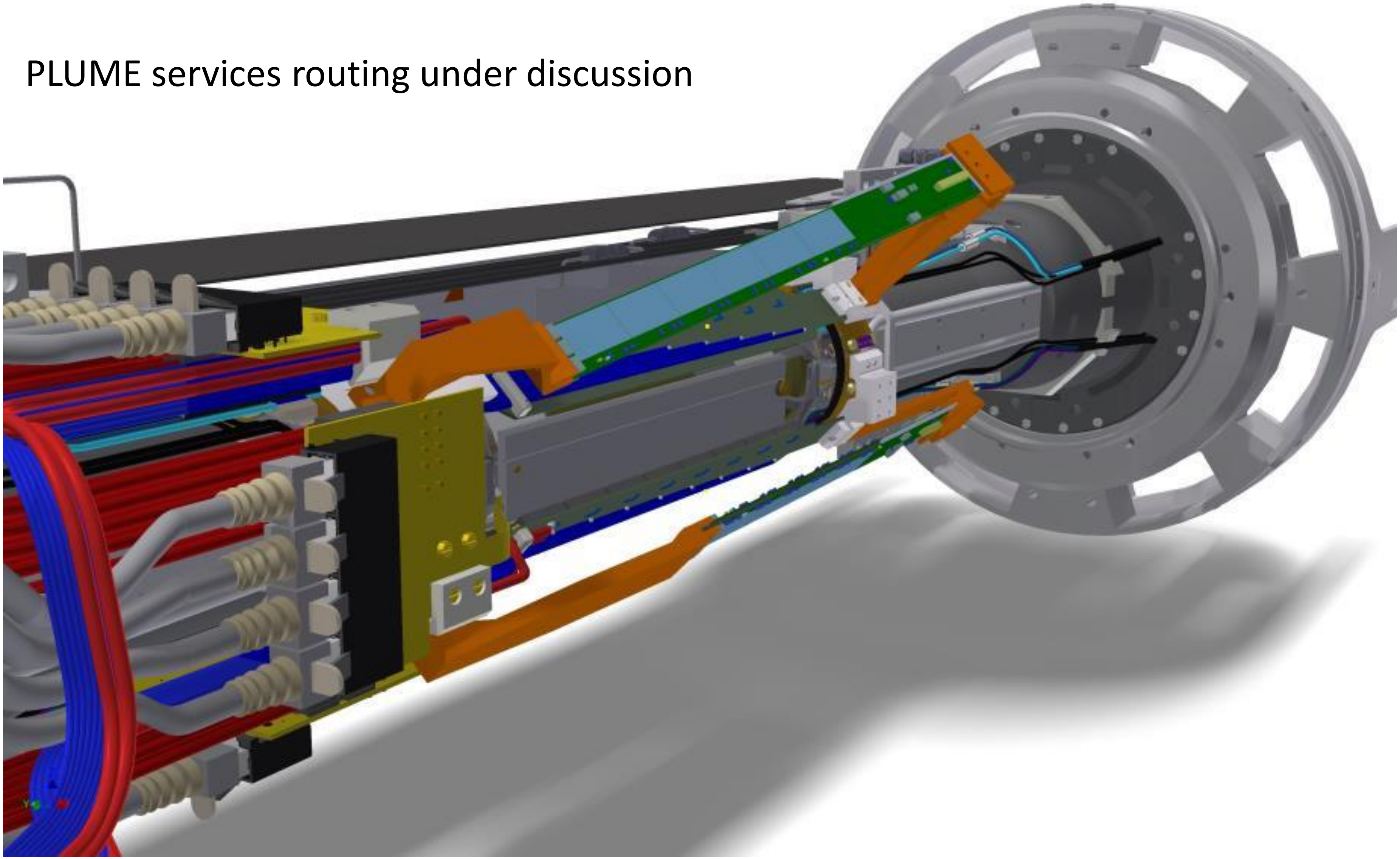
System Integration



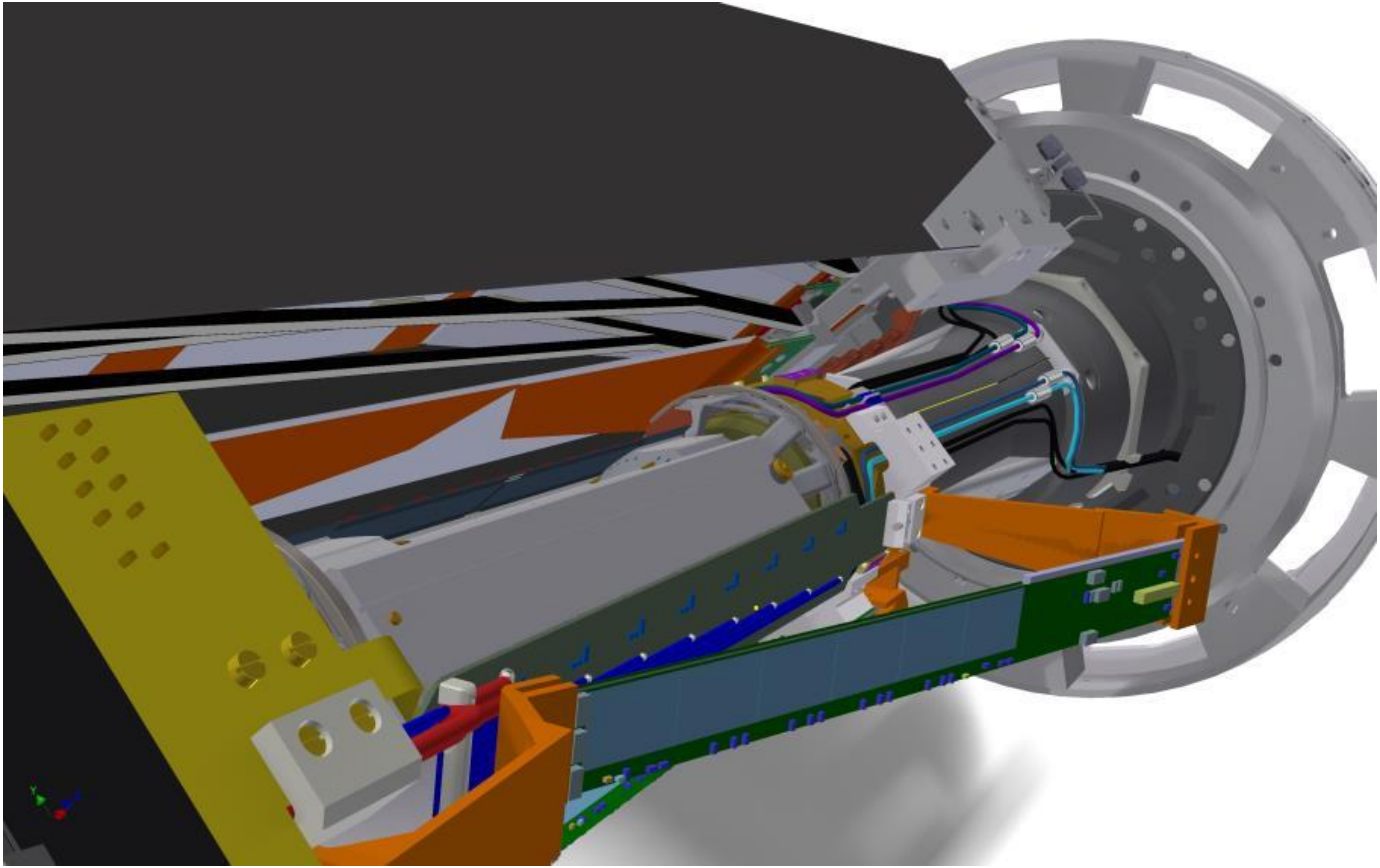
System Integration

universitätbonn

PLUME services routing under discussion



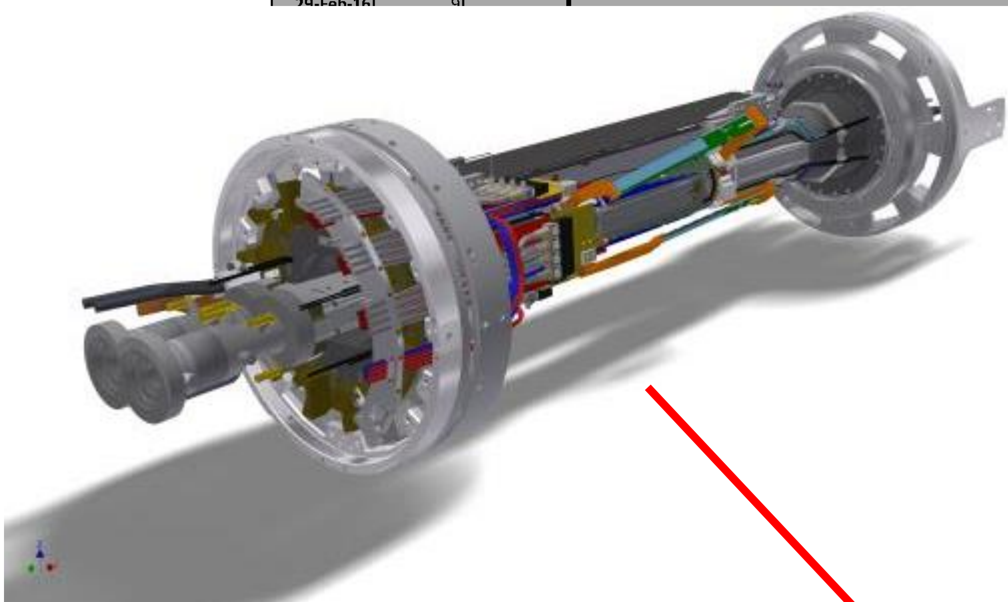
System Integration



Schedule 2016

DESY Testbeam Schedule 2016 - Version 8 - 27/04/2016

Ralf Diener, Norbert Meyners, Marcel Stanitzki - DESY Test Beam Coordinators

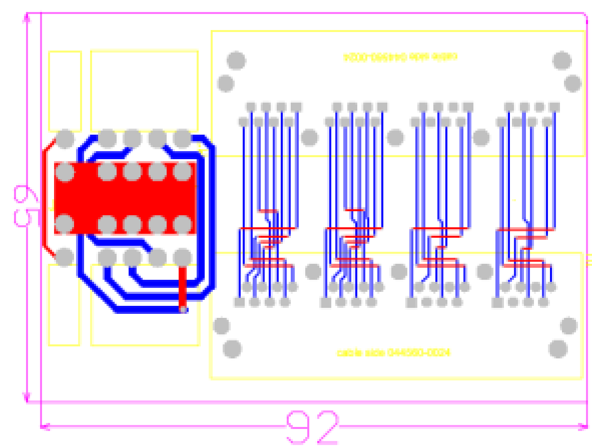


	Week		TB21		TB22		TB24/1		TB24	
			DATURA	none	DURANTA	none	Telescope in PCMAG	PCMAG	none	Announced
4-Jan-16	1		Shutdown							
11-Jan-16	2									
18-Jan-16	3									
25-Jan-16	4									
1-Feb-16	5									
8-Feb-16	6									
15-Feb-16	7									
22-Feb-16	8									
29-Feb-16	9									
						up	Startup		Startup	
							Belle-II			
						CALICE-AHCAL			SiPM	
						CALICE-AHCAL			SiPM	
									CMS-Pixel-Phase1	
						CALICE-AHCAL				
29-Aug-16	35								CBM-TRD	
5-Sep-16	36					VXD Dry Tests				
12-Sep-16	37									
19-Sep-16	38									
26-Sep-16	39									
3-Oct-16	40									
10-Oct-16	41									
17-Oct-16	42		CMS-Phase2-EPI							
24-Oct-16	43		CMS-Phase2-EPI		HEP for Teachers					
31-Oct-16	44									
7-Nov-16	45				Mu3e					
14-Nov-16	46					Phase 2 Dry Integration				
21-Nov-16	47									
28-Nov-16	48						Belle-II			
5-Dec-16	49									
12-Dec-16	50									
19-Dec-16	51	Beam till 23/12 0800								
26-Dec-16	52		Shutdown							

Conclusion

- Front end has been tuned to cover the expected energy range with sufficient **resolution** for Beast Phase 2
- **Multiple-FE DAQ** demonstrated
- **20 m long cables** tested
- Kapton flex and intermediate boards delivered
- **Mechanical** concept and **cooling** management finalized
- Stave production started
- FANGS to be ready by the end of the year for integration

NEXT:
- Patch panels (Docks design)
- Radiation hardness flex electrical components
- More realistic environment



Thank you

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