ASIC Optimization using DEPFET transistors as current source

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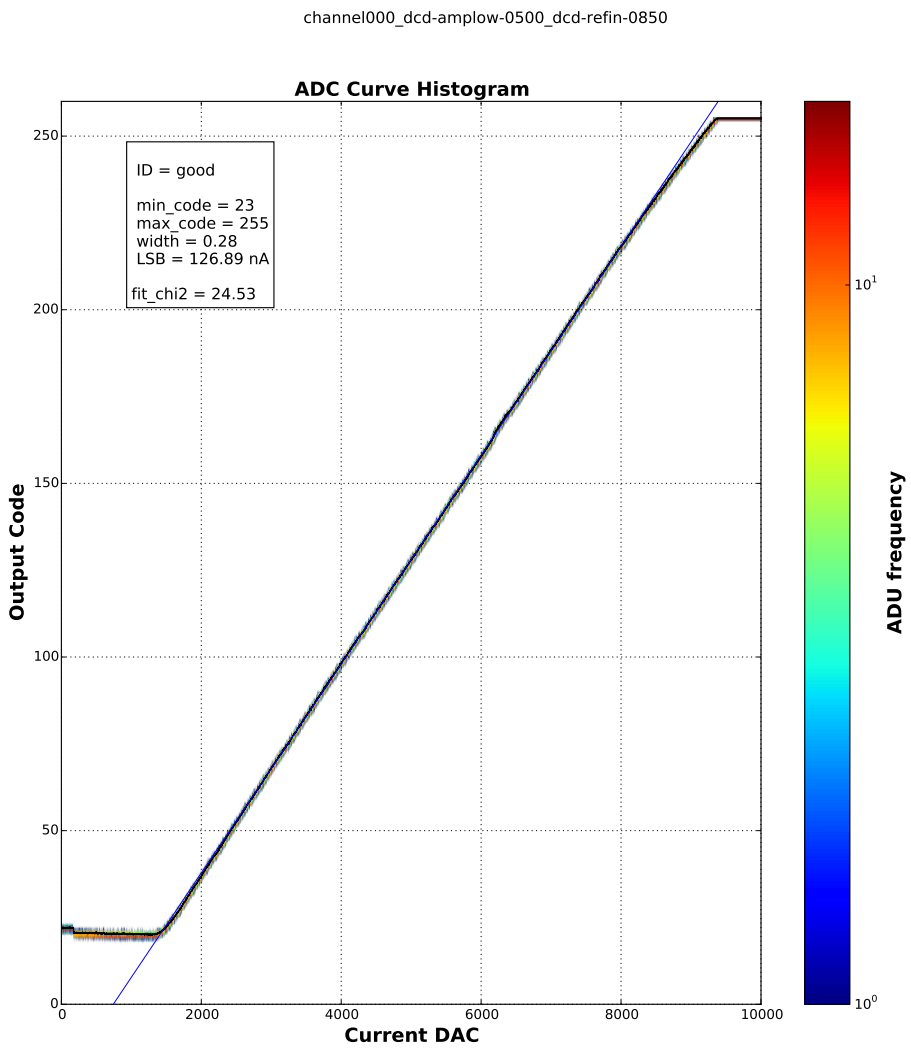
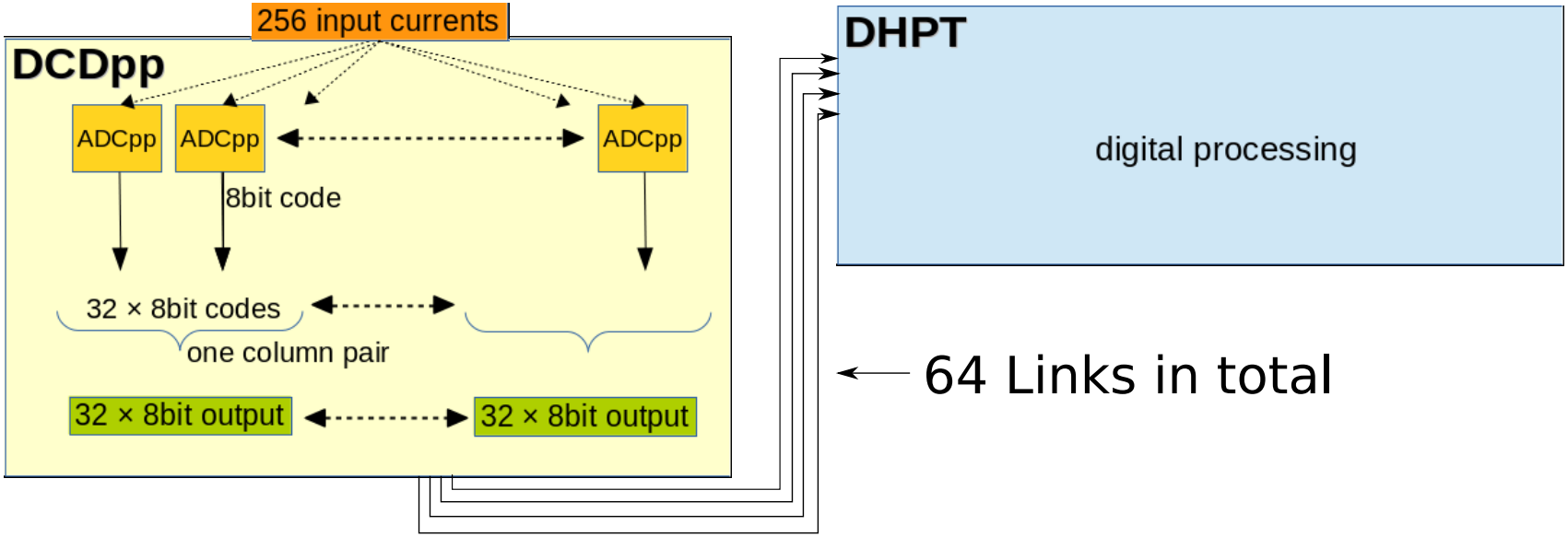
ADC Curves

- ADC curves can be used to identify various ASIC problems caused by false parameters and therefore are a useful tool for the optimization of the ASICS
- There are multiple tests for the ADC curves to identify several possible errors (long codes, bit errors, ...)



ADC Curves

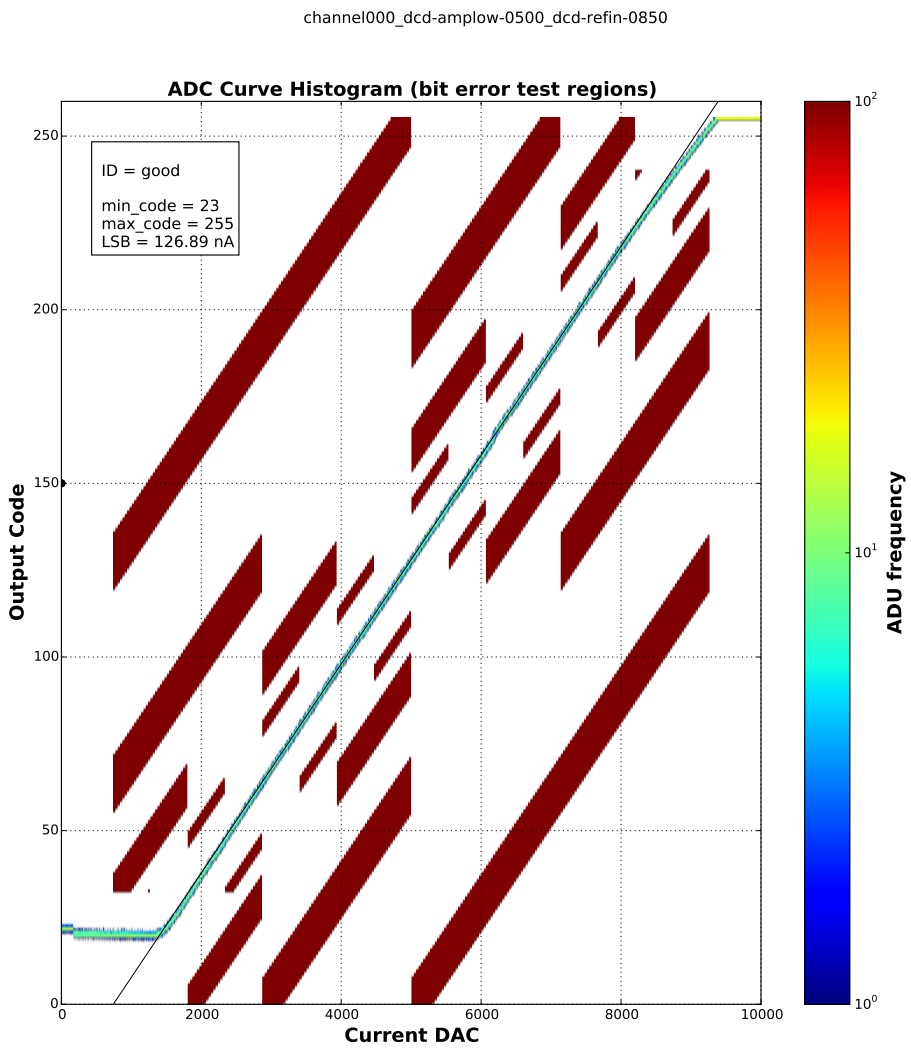
- A new test looks for wrong bits in the DCD output (Communication problem DCD-DHP)



Bit error test

DCD-DHP Bit Error Test:

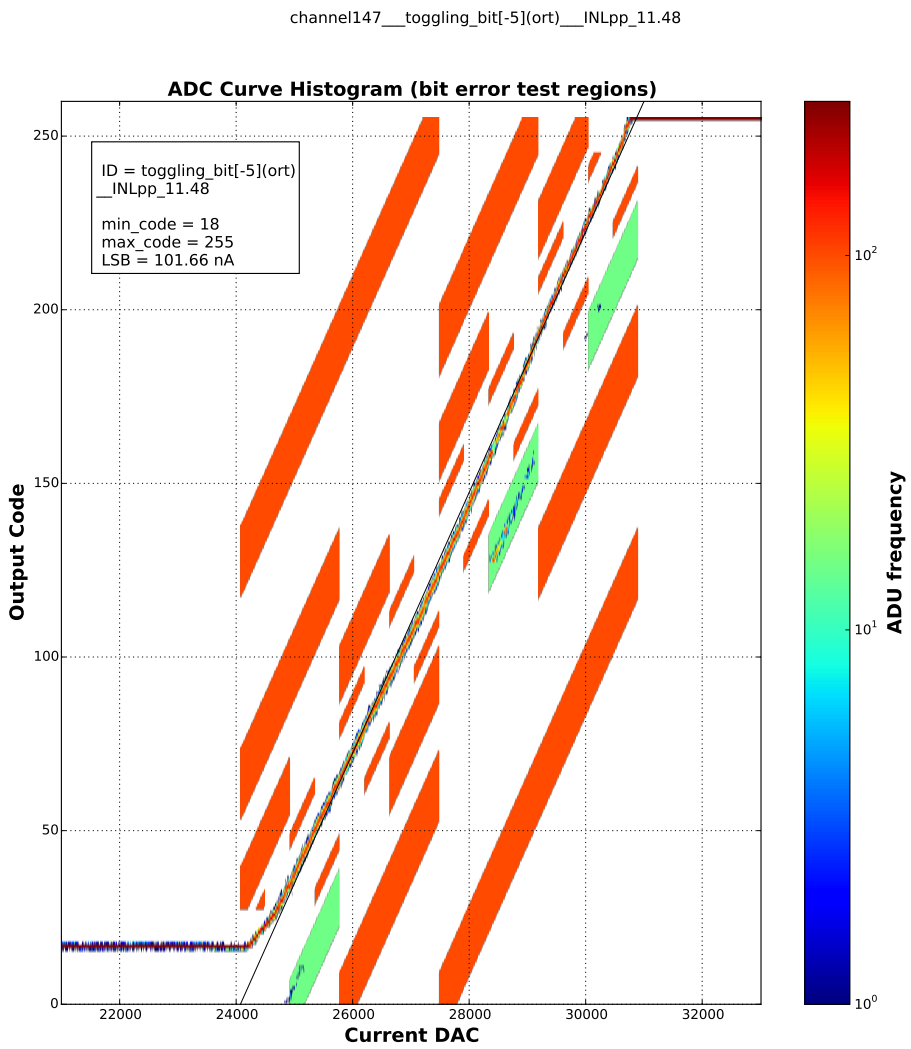
- Output of the DCD is a 8 Bit code
- If one Bit in the output code is wrong, the entry is shifted away from the curve
- From the fit of the curve 'Boxes' can be defined, in which these entries would lie
- 'Boxes' show the result of Bit 0,1,2,... being wrong
- If outliers are found in these 'Boxes' the error flag is set



Bit error test

DCD-DHP Bit Error Test:

- Output of the DCD is a 8 Bit code
- If one Bit in the output code is stuck, the entry is shifted away from the curve
- From the fit of the curve 'Boxes' can be defined, in which these entries would lie
- 'Boxes' show the result of Bit 0,1,2,... being stuck
- If outliers are found in these 'Boxes' the error flag is set



Optimization Strategy

- To optimize one module, the number of 'good' channels (i.e. channels with no errors) has to be maximised
  $\rightarrow$ Ideally the ADC curves of all 256 channels per DCD should be looked at

There are 3 ways to record an ADC curve:

- **DCD source**: Internal DCD current source (very slow)
- **DHE source**: External current source from DHE (faster, problematic noise with PXD9)
- **Gate-On source**: Depfet transistor as current source (potentially very fast and low noise)

Question: Does the existing analysis for ADC curves work with Gate-On measurements?

Gate-On Measurements

Idea: Use DEPFET drain current I_d as source

$$I_d = \frac{1}{2}\frac{W}{L}C'_{ox}\left(f\frac{q}{C_{ox}} + V_{gs} + V_{th}\right)^2$$

W/L = Width/Length of gate
q = Charge
f = Reduction factor
V_{gs} = Gate-Source voltage
V_{th} = Threshold voltage
C'_{ox} = Sheet capacitance
C_{ox} = Gate capacitance

$\Rightarrow$ Drain current can be steered with V_{gs}

Gate-On Measurements

- When the Gate-On voltage decreases, the drain current increases
- Gate-On voltages from -1500 mV to 0 mV are sufficient to cover the input range of the ADC
- During the measurement one matrix row is activated and a zero suppressed read-out is performed
- All channels can be measured simultaneously

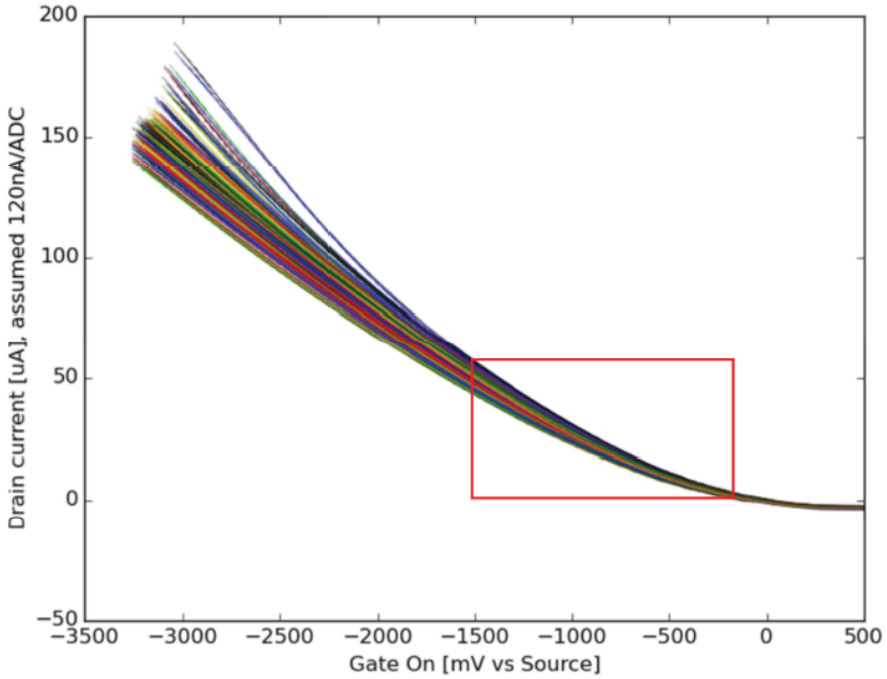


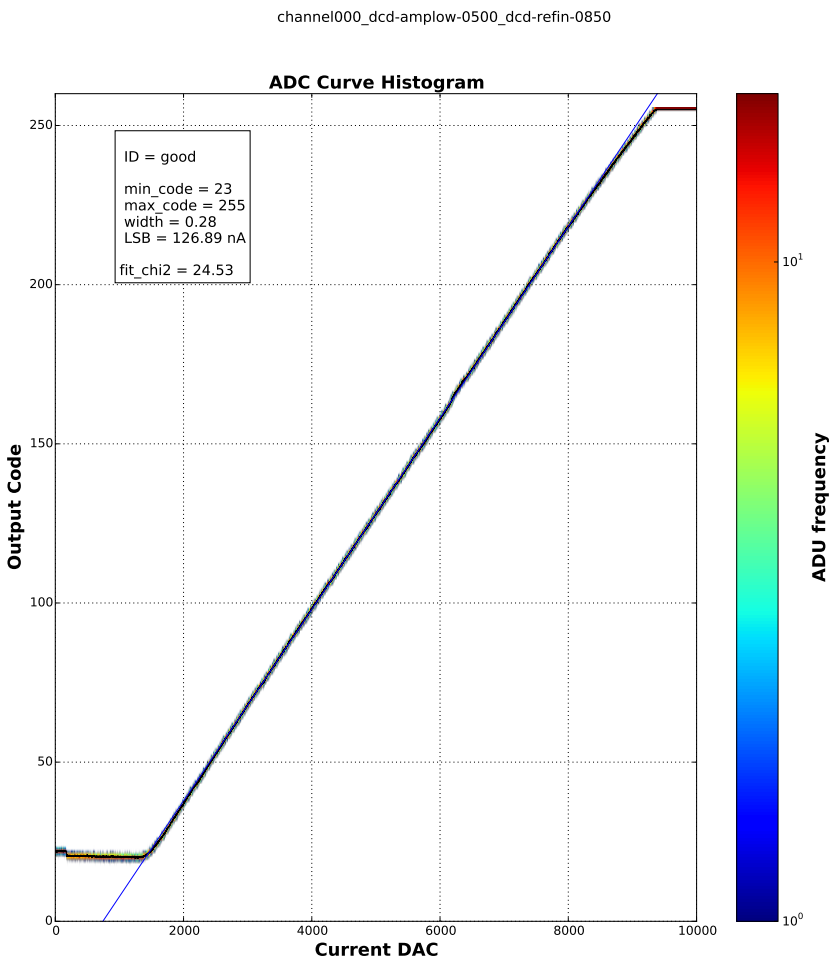
Figure: Plot by F. Lütticke

Gate-On measurement on Hybrib5

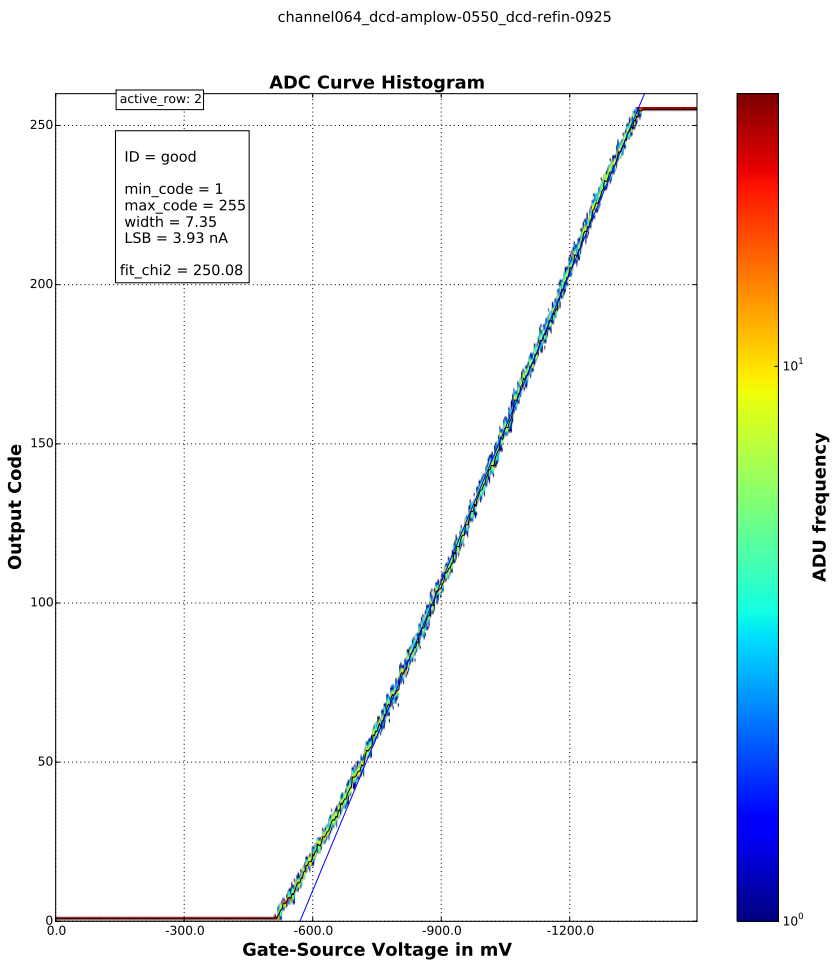
- For the measurement a Hybrid5 setup was used
- The system was configured with the ConfigDB instead of *.ini files (ASIC settings and PowerSupply voltages)
- Only two column pairs are connected to the matrix (channels 64-191)
- A 2-dimensional sweep over DCD-Amplow (200 mV to 550 mV) and DCD-Refin (700 mV to 1000 mV) was performed
- For comparison the sweep was also done using the DHE current source

DHE vs. Gate-On Measurements

DHE Measurement:

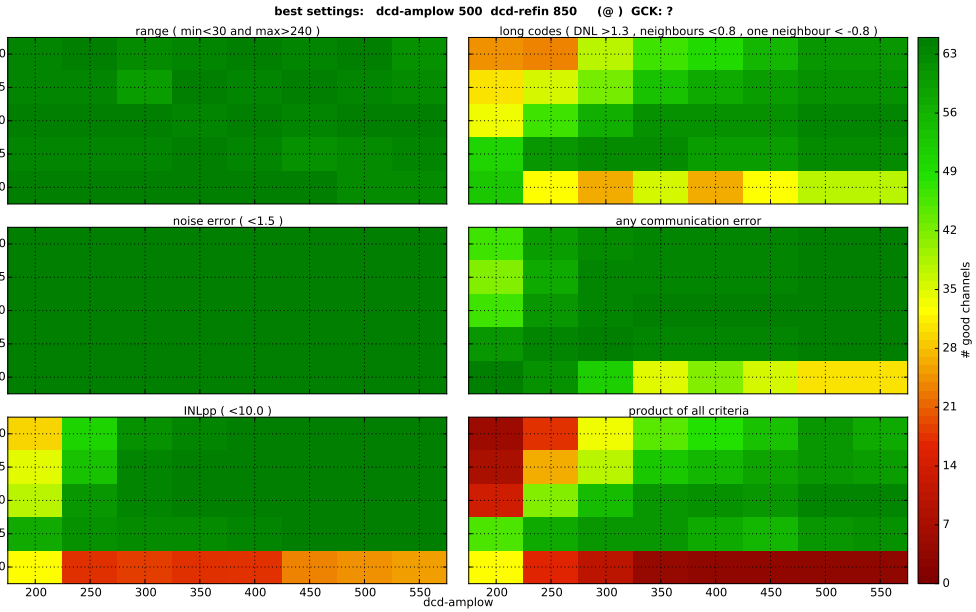


Gate-On Measurement:



DHE vs. Gate-On Measurements

Result of an Amplow-Refin sweep on a Hybrid5 system:



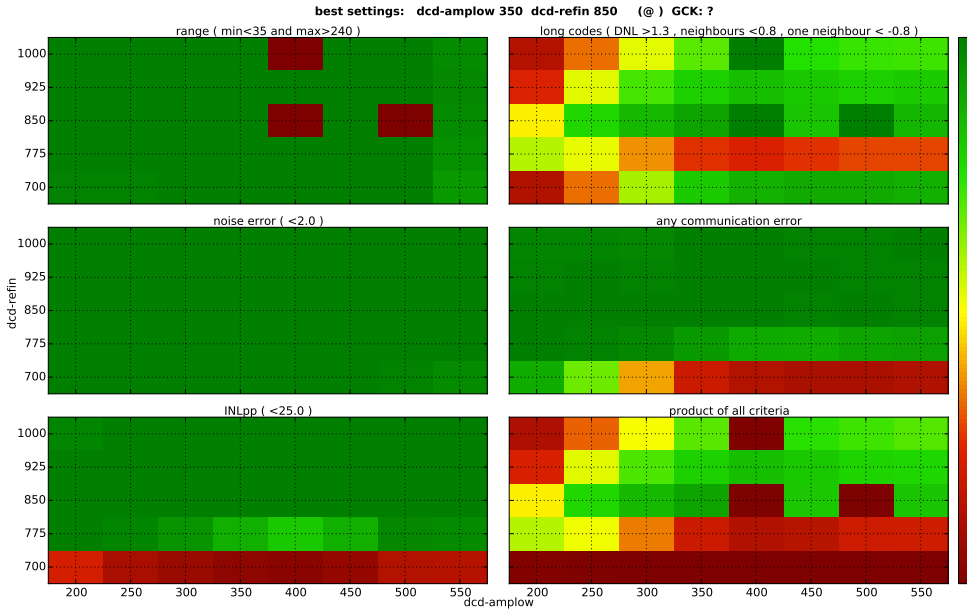


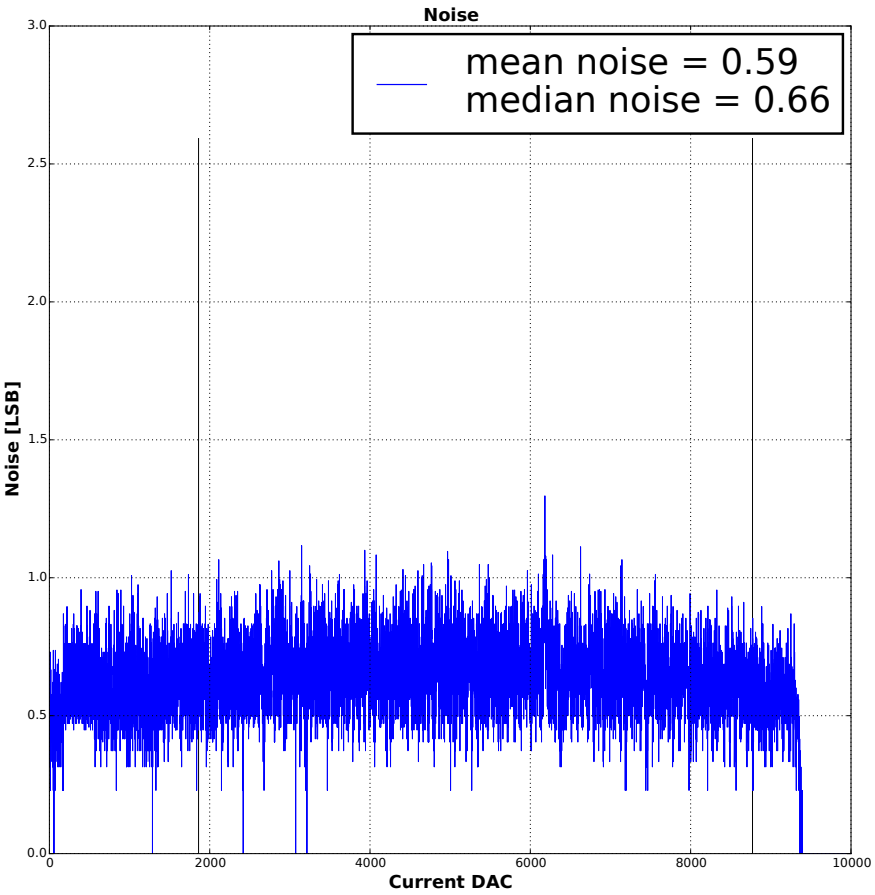
Figure: Summary Plots of an Amplow-Refin sweep for a DHE (left) and a Gate-On (right) measurement.

Best Working Point

DHE: Amplow 300-550, Refin 850

Gate: Amplow 300-550, Refin 850

DHE vs. Gate-On Measurements



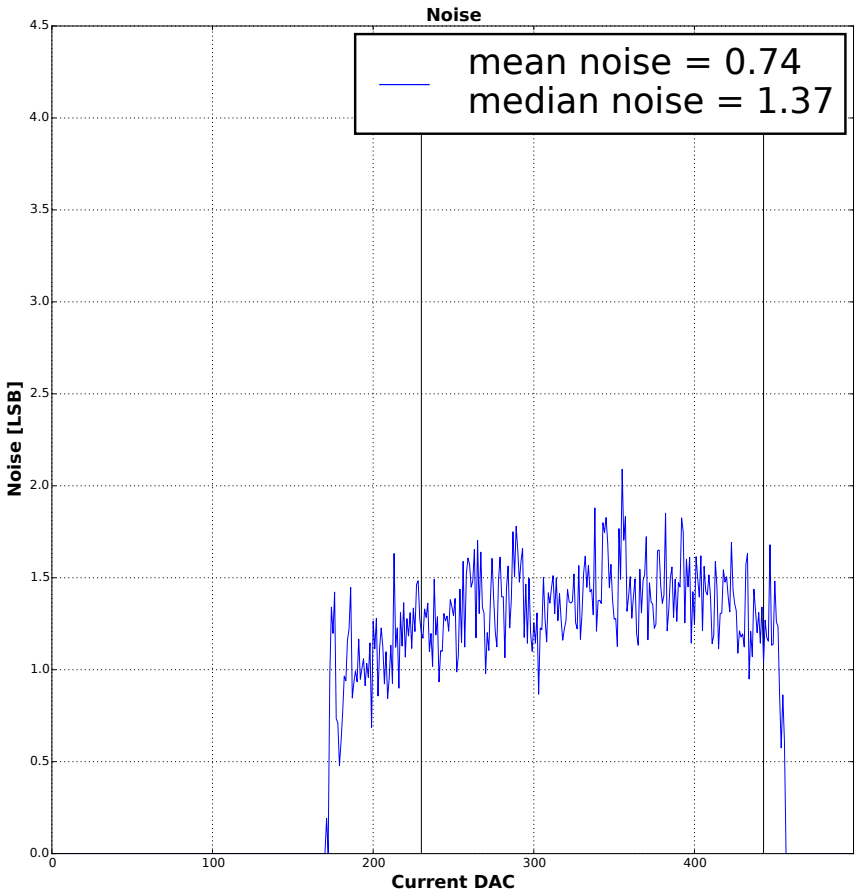


Figure: Comparison of the noise of the ADC curve for DHE (left) and Gate-On (right) measurement.

Gate-On measurement

Advantages

- All channels can be recorded simultaneously
- $\approx 2 - 3$ minutes per module (up to 1000 channels)
- DHE: ≈ 2 seconds per channel $\rightarrow \approx 33$ minutes for 1000 channel
  $\Rightarrow$ speed-up of factor $11 - 16$

Challenges

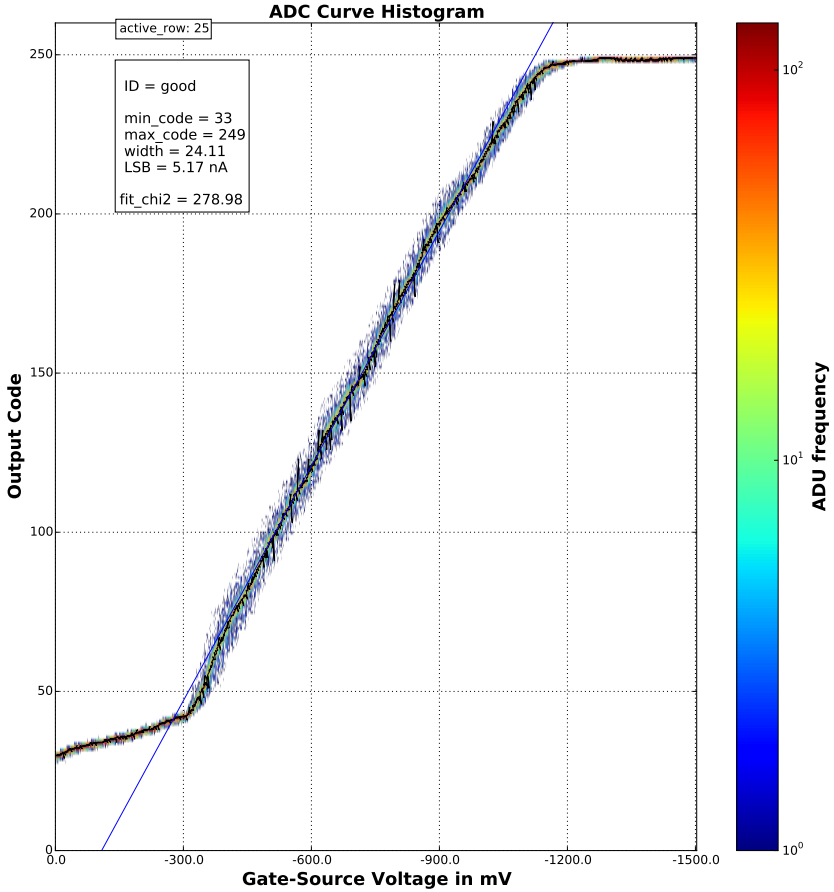
- Non-Linearity of transistor curve influences ADC curve
  $\rightarrow$ Some test criteria have to be adjusted

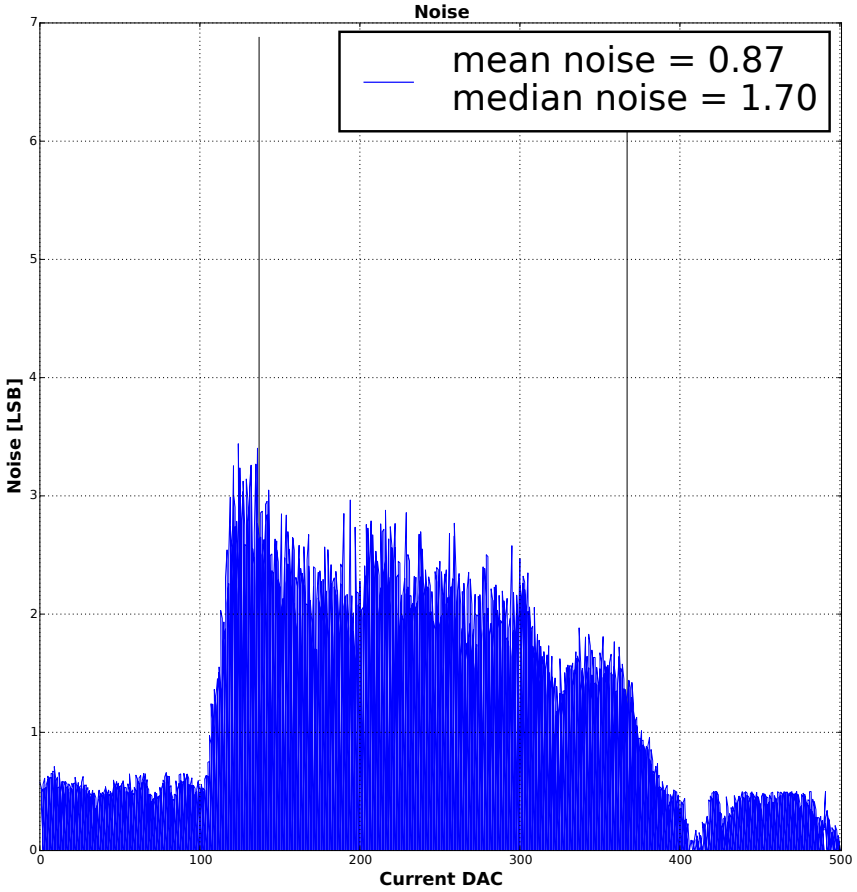
Results with Pilot Module

- Gate-On measurements have also been performed on PXD9 Pilot modules
- Data from all 4 ASIC pairs was taken (1000 channels)
- Initial measurements showed a noise problem

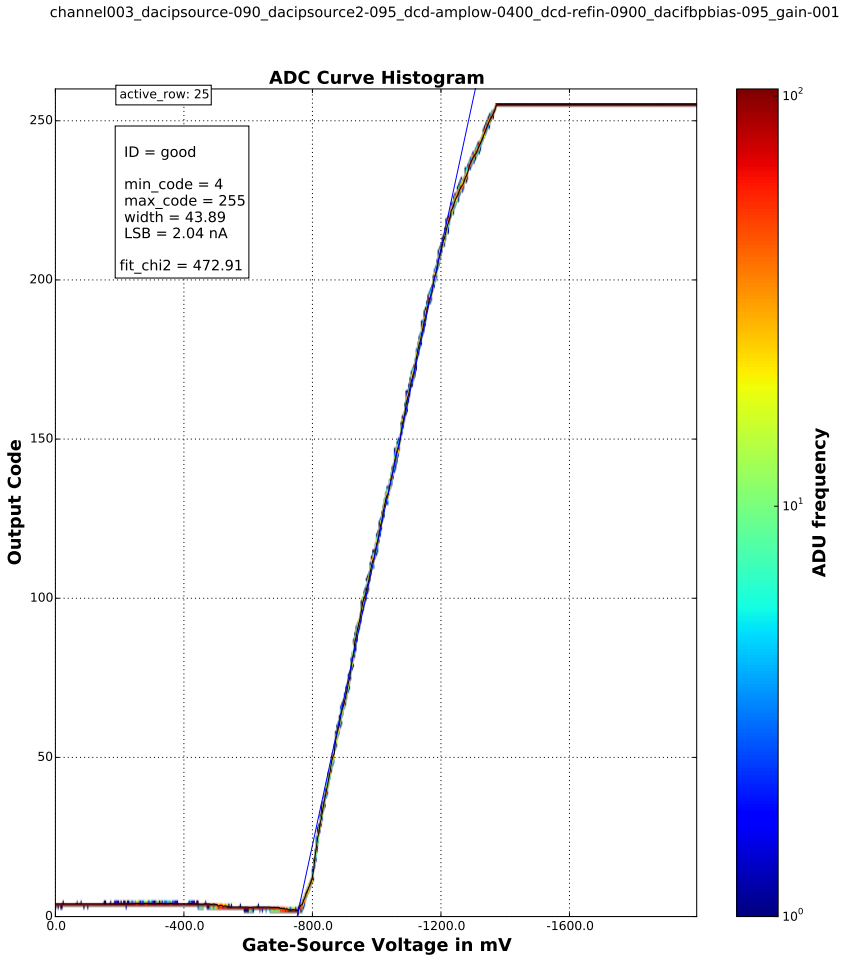
Results with Pilot Module

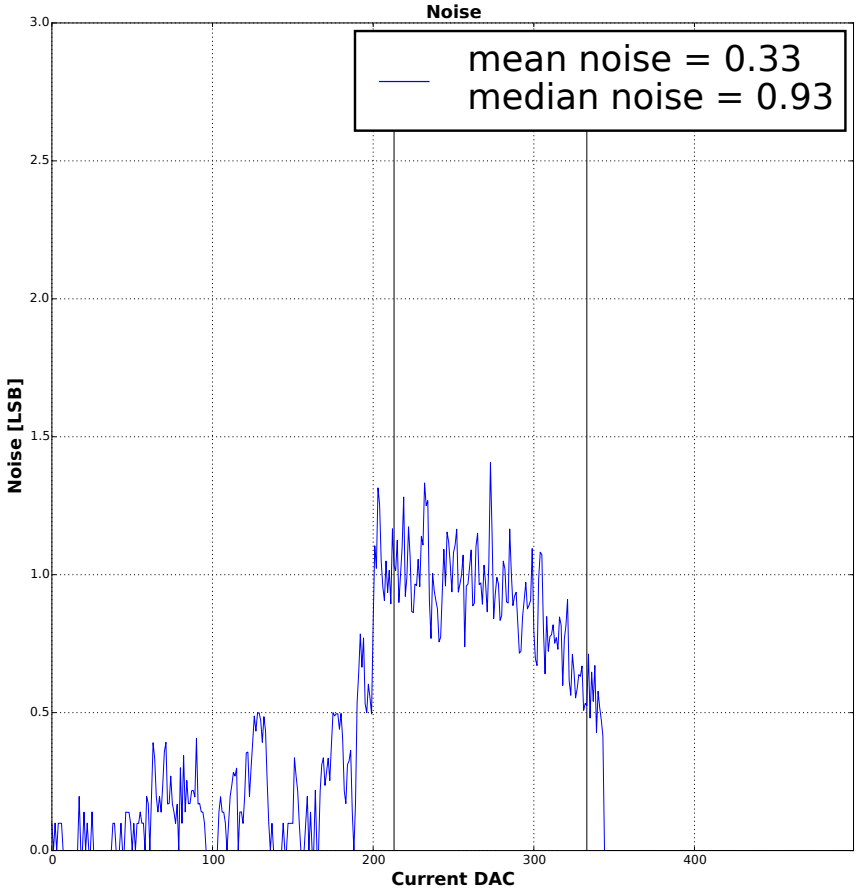
channel000_dacipsource-100_dacipsource2-090_dcd-amplow-0400_dcd-refin-0900_dacifbpbias-085_dacvnsubin-013_gain-001





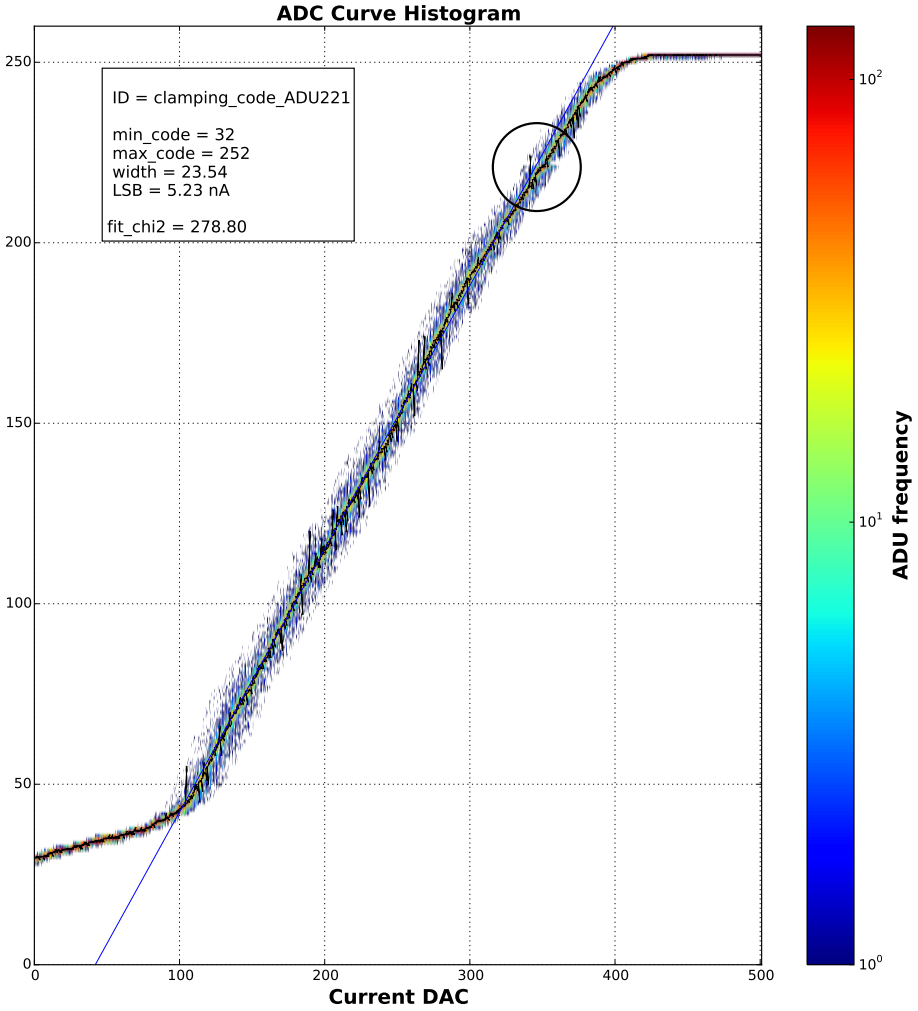
Results with Pilot Module

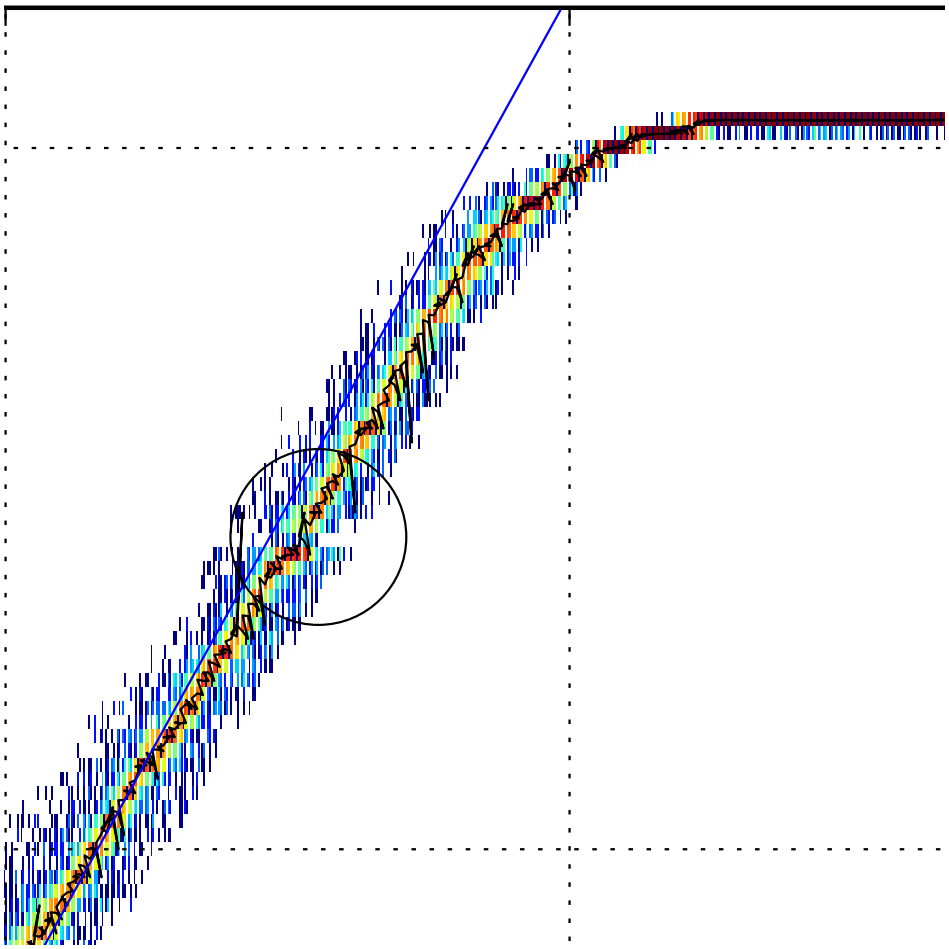




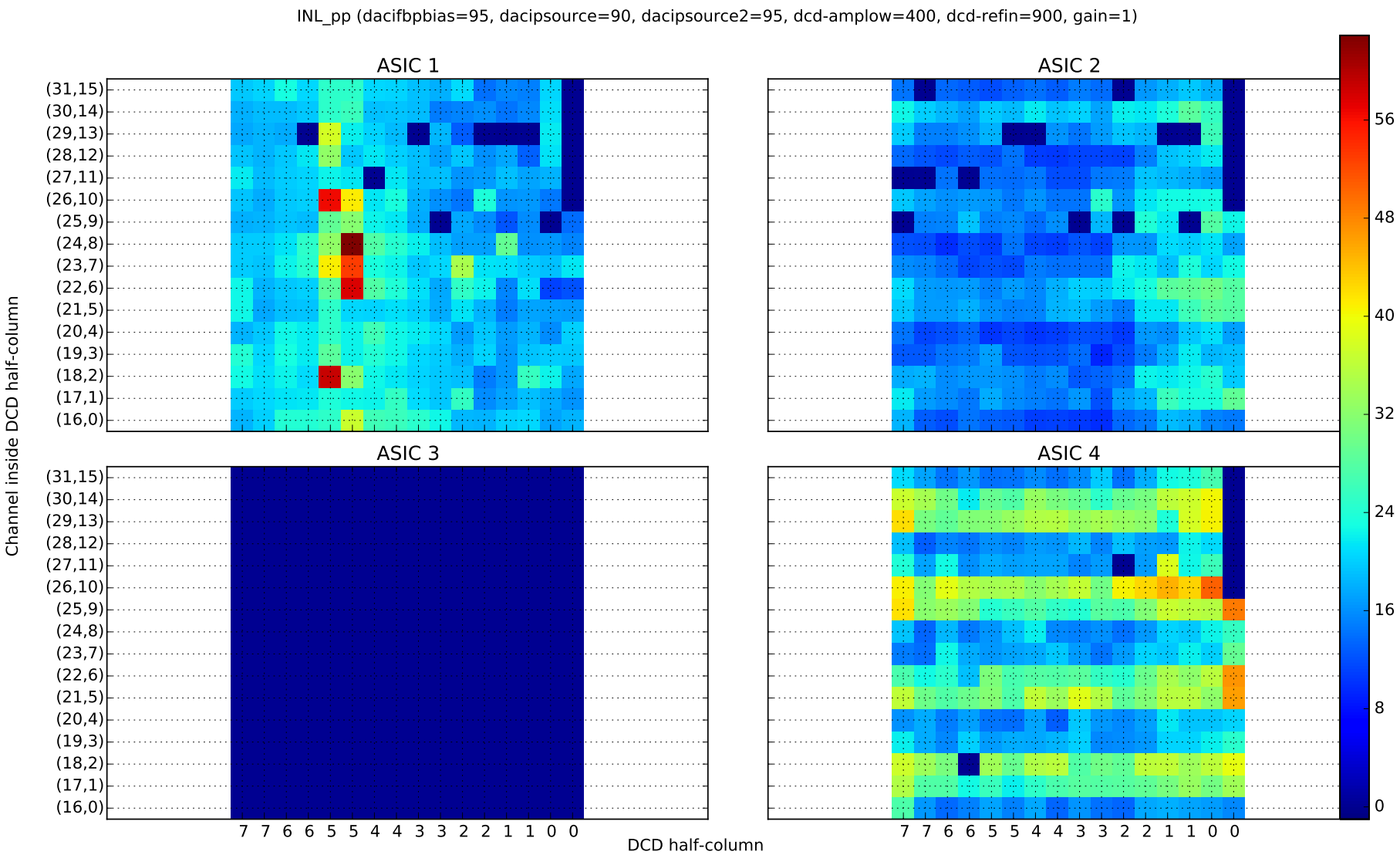
Clamping/Long Code

ource-100_dacipsource2-090_dcd-amplow-0400_dcd-refin-0900_dacifbpbias-085_dacvnsubin-013_gain-001___clam

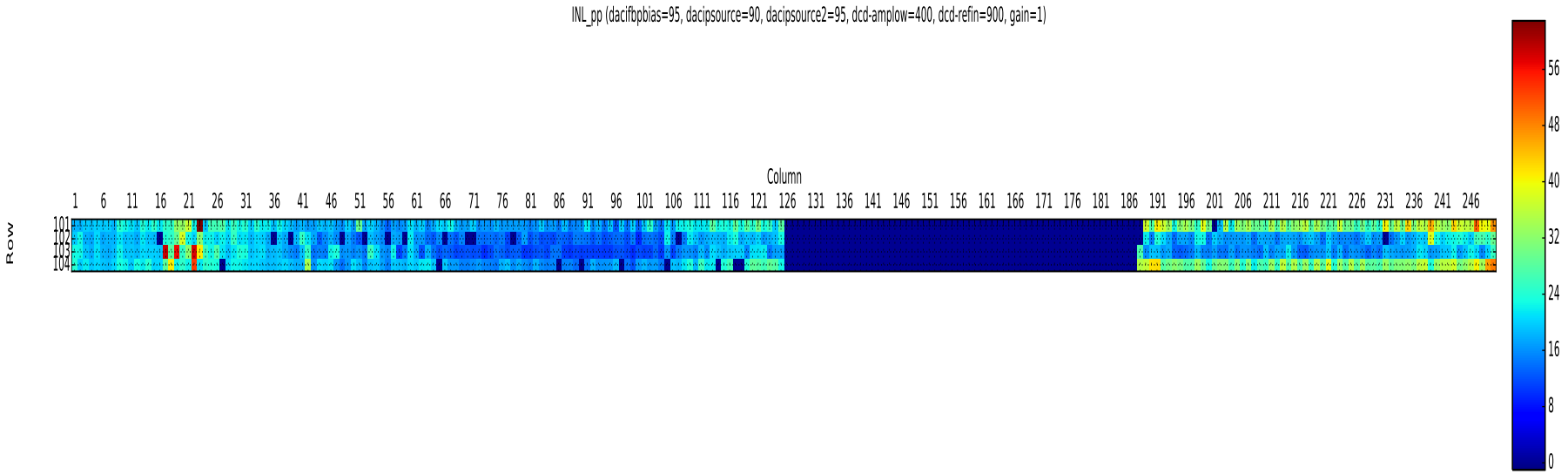




Results with Pilot Module



Results with Pilot Module



Summary

- Gate-On measurement is much faster than the DHE source measurement
- Existing analysis scripts work with Gate-On measurements
- Linearity of Gate-On measurement slightly worse
- Gate-On measurement most promising method for optimization of the final modules

Thank you for your attention