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Changes from DHPT 1.1 to DHPT 1.2

DEPFET Workshop, Kloster Seeon

Mai 11-14, 2016

Bugs fixed in DHPT 1.2

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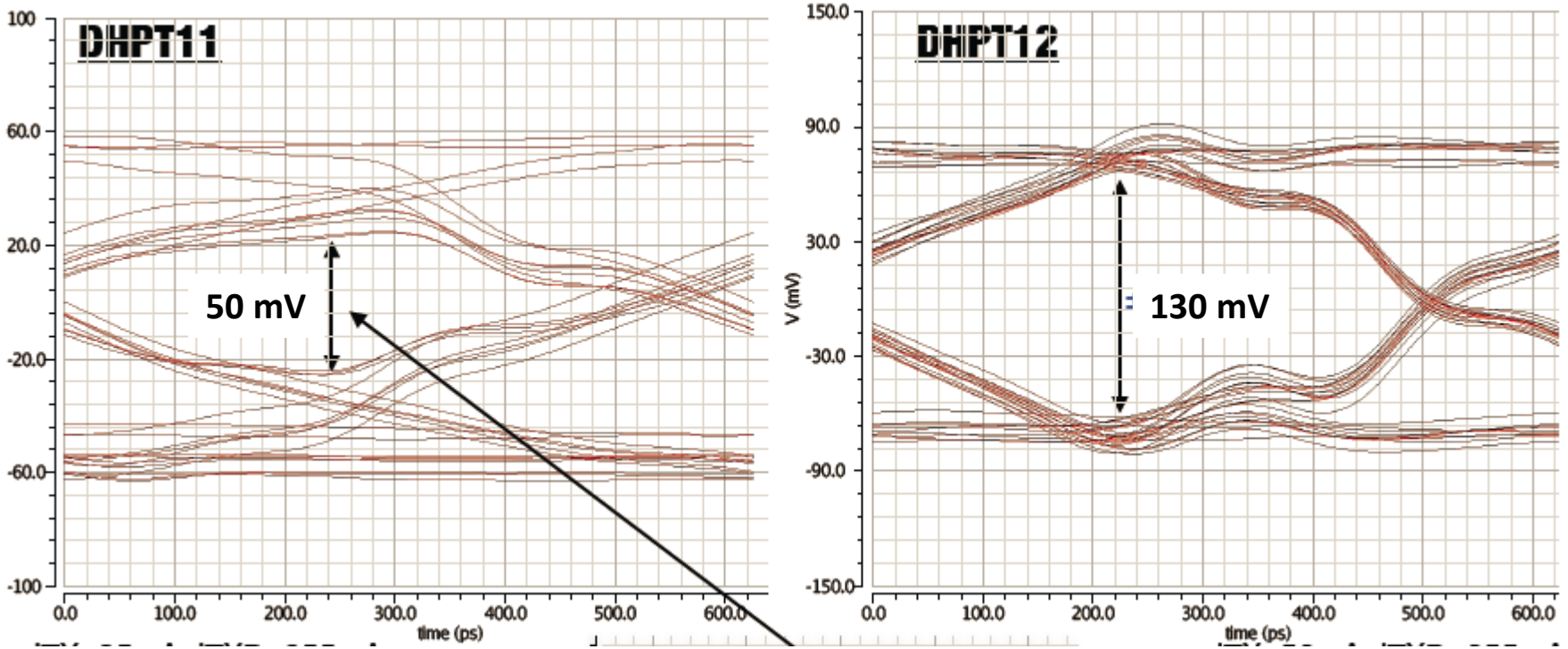
CML Driver

- CML driver power routing
  - Ground rail (VSS) had a too high wiring resistance (~30 Ohm), parasitic extraction did not spot this because of substrate model
  - Rerouting of power nets → $R_{VSS} < 0.2$ Ohm

- CML driver bias routing
  - Removed ESD resistor in bias connection and reduced parasitic resistance → increase of bias current, less sensitivity to voltage supply

CML Driver Performance Improvements

- Simulation setup
  - CML driver: fully extracted RC including bias and power routing, typical corner
  - Cable model: Extracted S-parameters of kapton + 2m TWP + 12m TWP including the patch panels



Bugs fixed in DHPT 1.2

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Digital core

- Mem dump
  - Data had some low probability to show corrupted values for the first few pixels when output was set to 800 MHz and clock compensation was on → fixed in HDL code
- Internal system clock phase
  - The core clock started with an arbitrary phase after power-on → added controlled reset (delayed GCK) to the internal clock divider
- Gated mode sequence put out first word twice
  - Fixed HDL code

Enhancements for DHPT 1.2

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Digital core

- JTAG USERID changed: allows recognition of DHPT version
- Gated mode: DATA_IN for the switcher can be selected to be controlled from either the *normal mode* sequence of the *gated mode* sequence (was *normal mode* only)
- Added the DHPT ID in the memory dump frame header
- Memory dump start address configurable
- Bias register for LVDS receivers has fixed minimum value

Summary & Outlook

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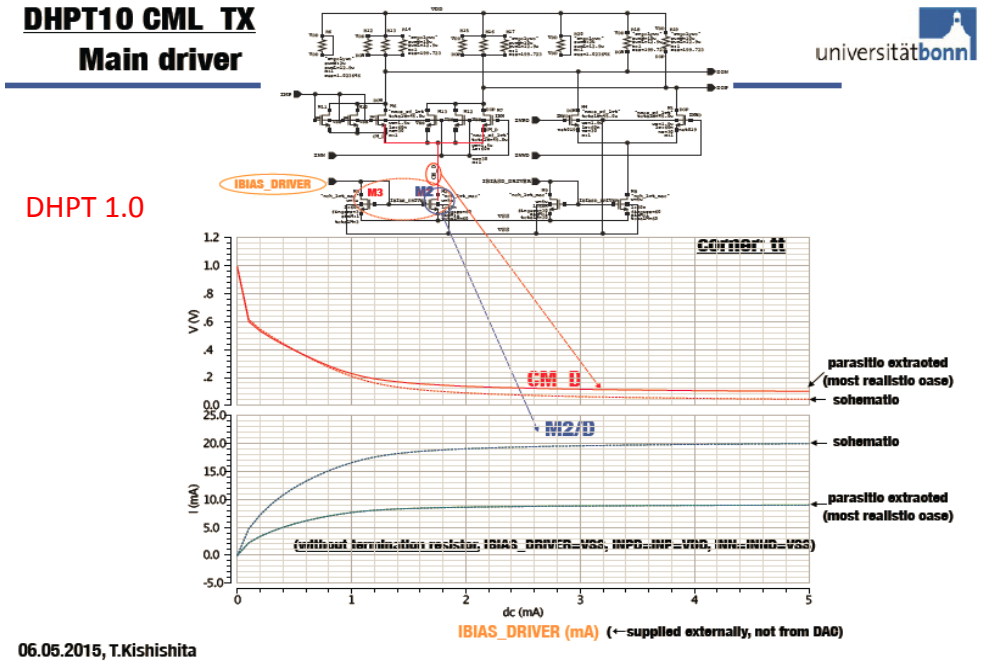
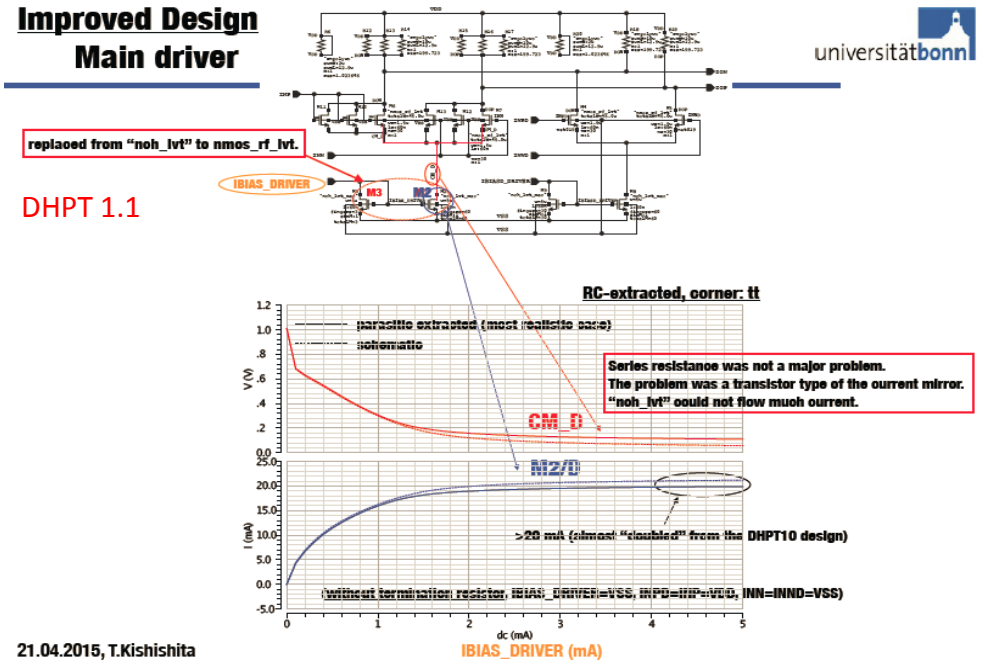
- DHPT 1.2 changes
  - Power routing if the CML driver fixed
  - Re-synthesized the digital core (bug fixes and enhancements)
- DHPT 1.2 production
  - Tape-out: April 27 (official deadline, production at TSMC starts ~ 2 weeks later)
  - Expected delivery (100 bumped chips): beginning of July
- Functional test
  - Functional test on probe station and hybrid 5
  - If functional tests are passed, immediately start to deliver tested chips for module production
- Mass production/testing
  - Decision for DHPT 1.2 as the production chip
  - Then: Order of 9 additional wafers (1000 chips in total)
  - Two new needle cards for probe station testing are available
  - Estimated testing throughput: ~50 chips per week

BACKUP

DHPT CML Driver

- Changes from DHPT1.0 to DHPT1.1

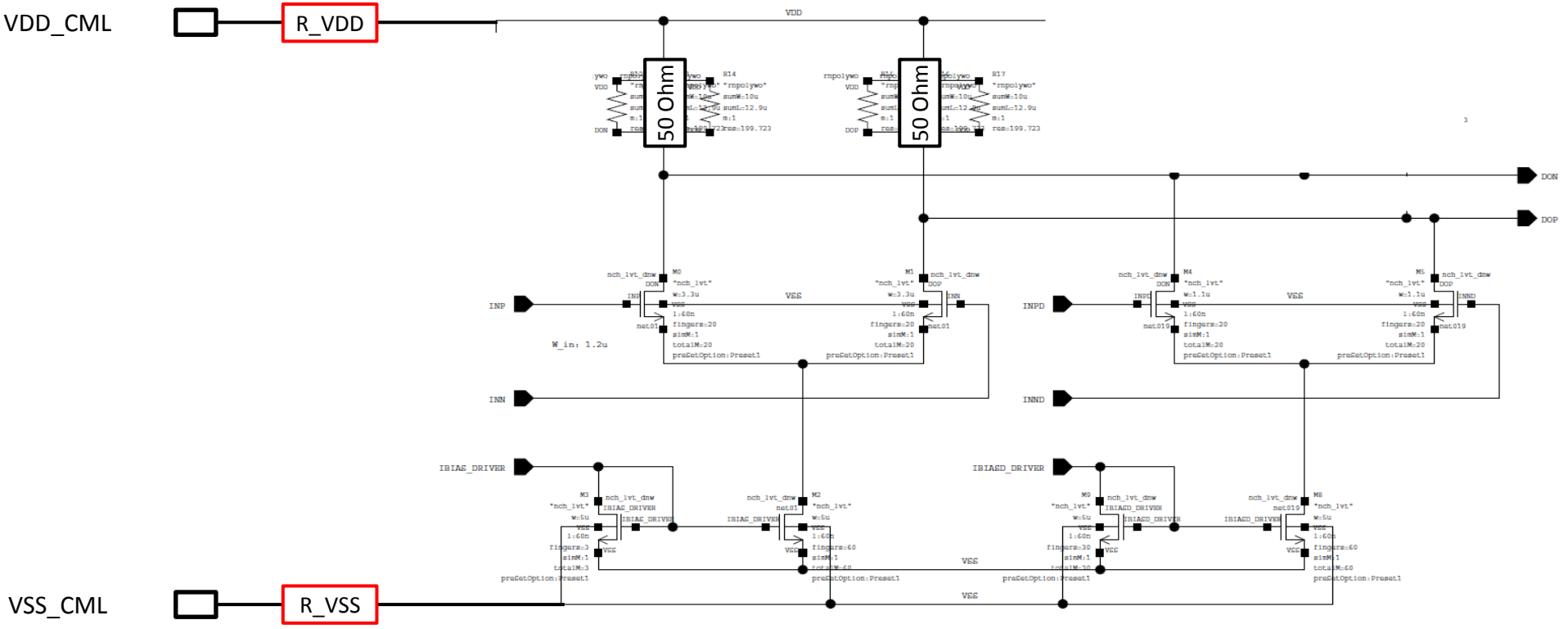




- Layout extracted with all parasitic elements
- Current in the main stage expected to be ~20mA after improvement of the transistor layout
- However measurements on DHPT 1.1 indicated ~10mA only

DHPT CML Driver

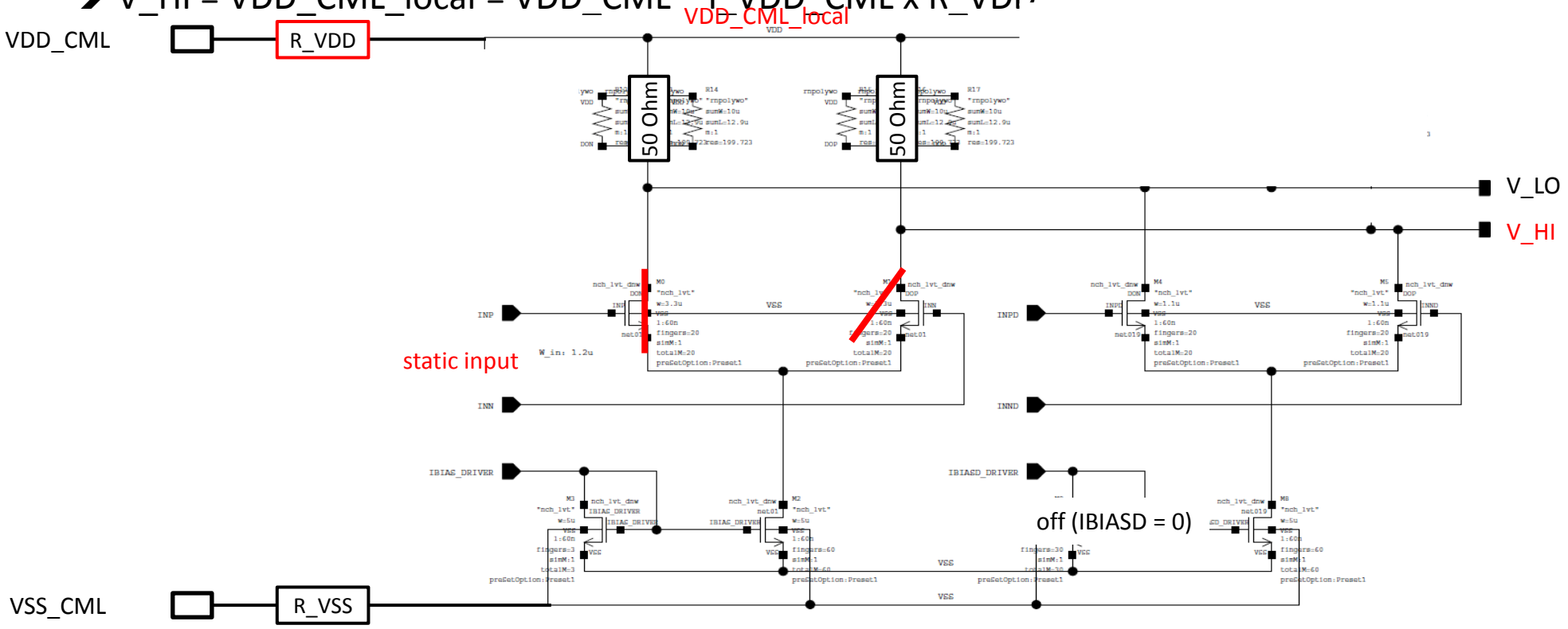
- Possible explanation: layout extraction underestimated the **parasitic** resistances R_VDD and R_VSS on the power lines



Measurement of the Parasitic Resistance R_VDD

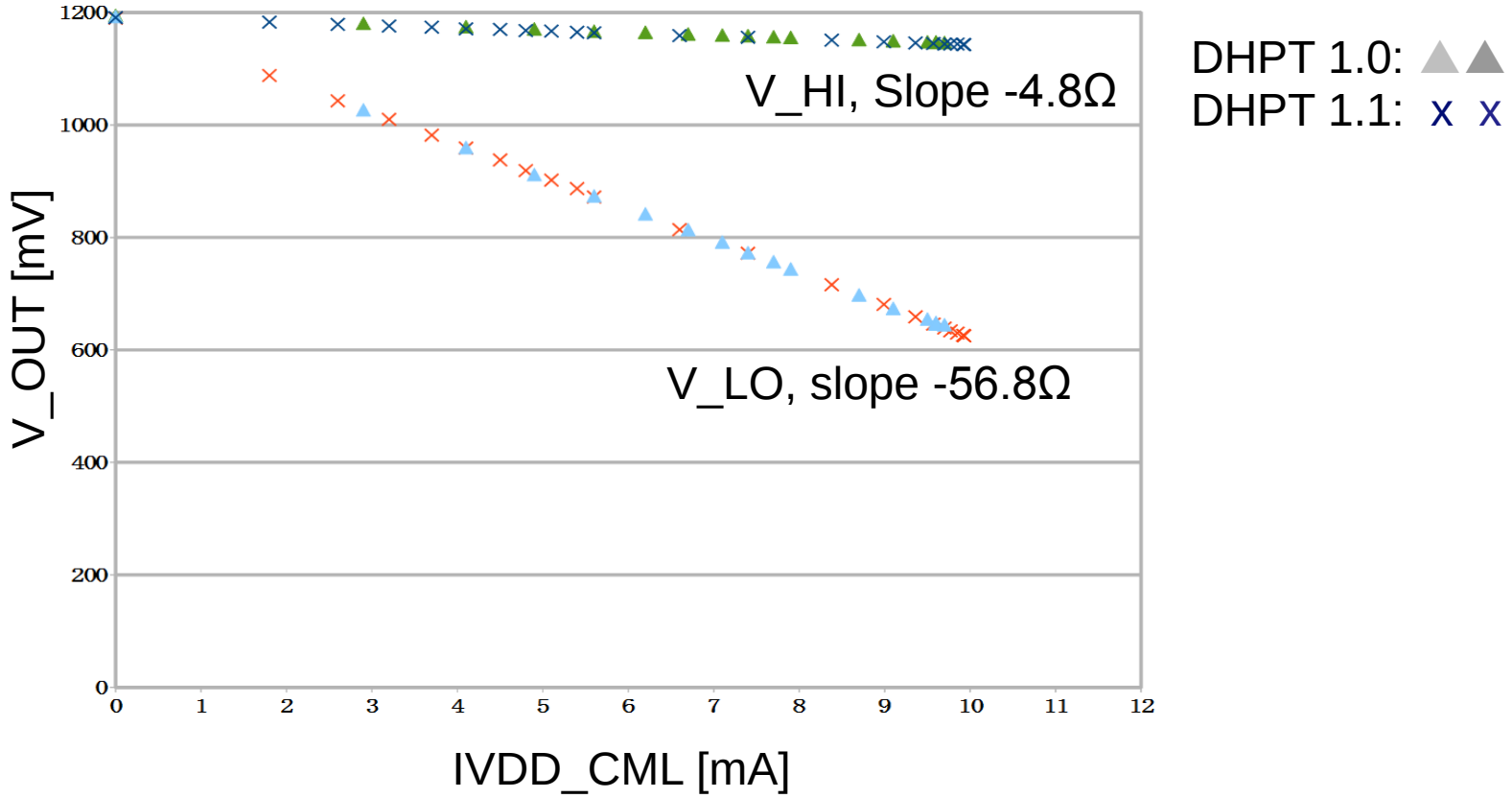
- Measure V_HI as a function of I_VDD_CML by changing IBIAS
  - no termination at driver output
  - no data line switching

➔ V_HI = VDD_CML_local = VDD_CML – I_VDD_CML x R_VDD



Measurement of the Parasitic Resistance R_VDD

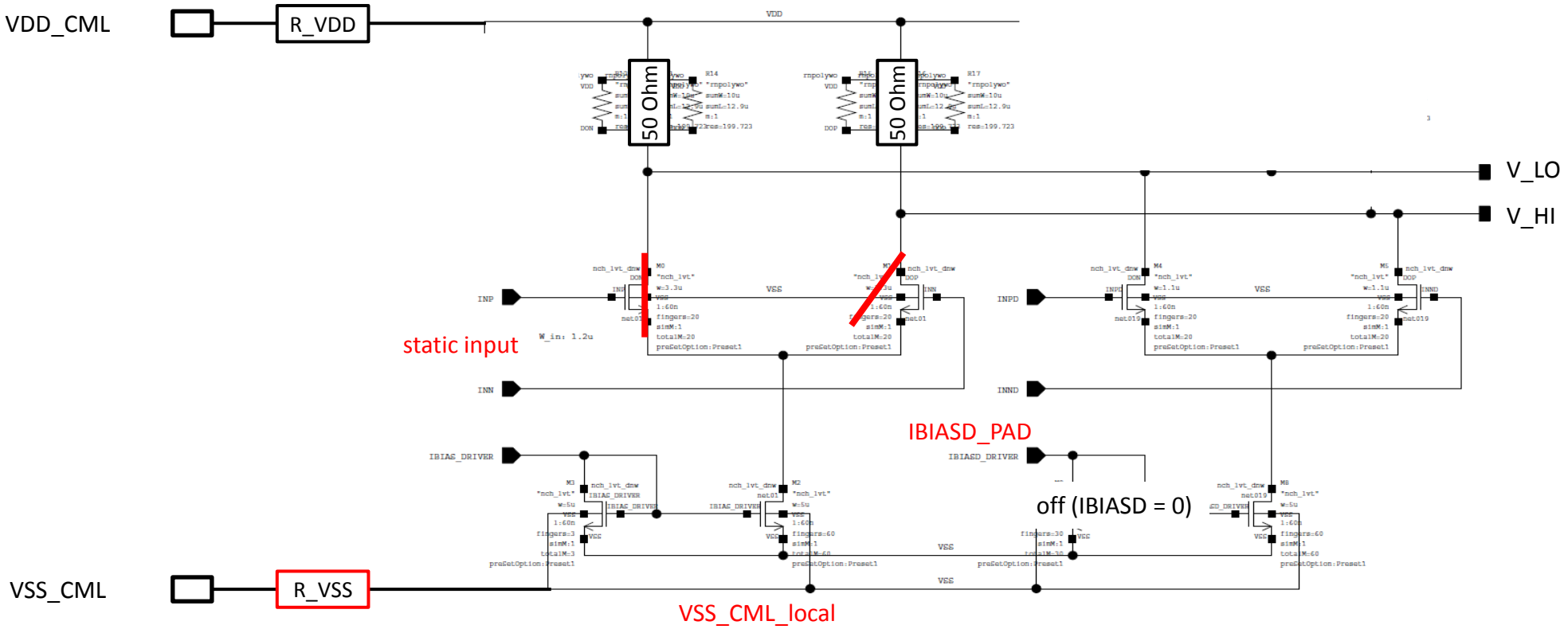
- Measurements indicate a parasitic resistance of about 5 Ohm in the VDD_CML line
- This is in agreement with the extraction of the parasitic elements of the layout, however this does not explain the loss of drive strength.



Measurement of the Parasitic Resistance R_VSS

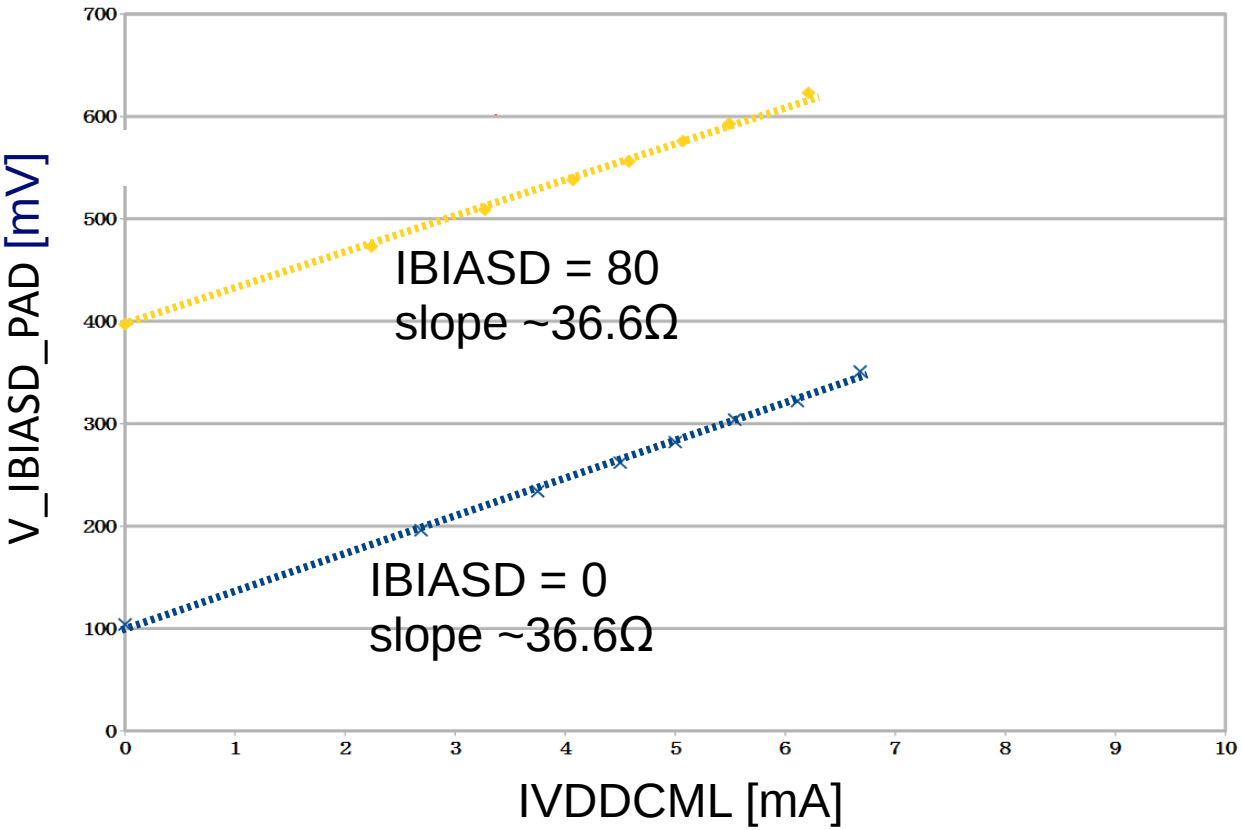
- Measure V_IBIASD_PAD as a function of I_VDD_CML by changing IBIAS, no termination at driver output

➔ V_IBIASD_PAD = VSS_CML_local + const = VSS_CML + I_VDD_CML x R_VSS



Measurement of the Parasitic Resistance R_VSS

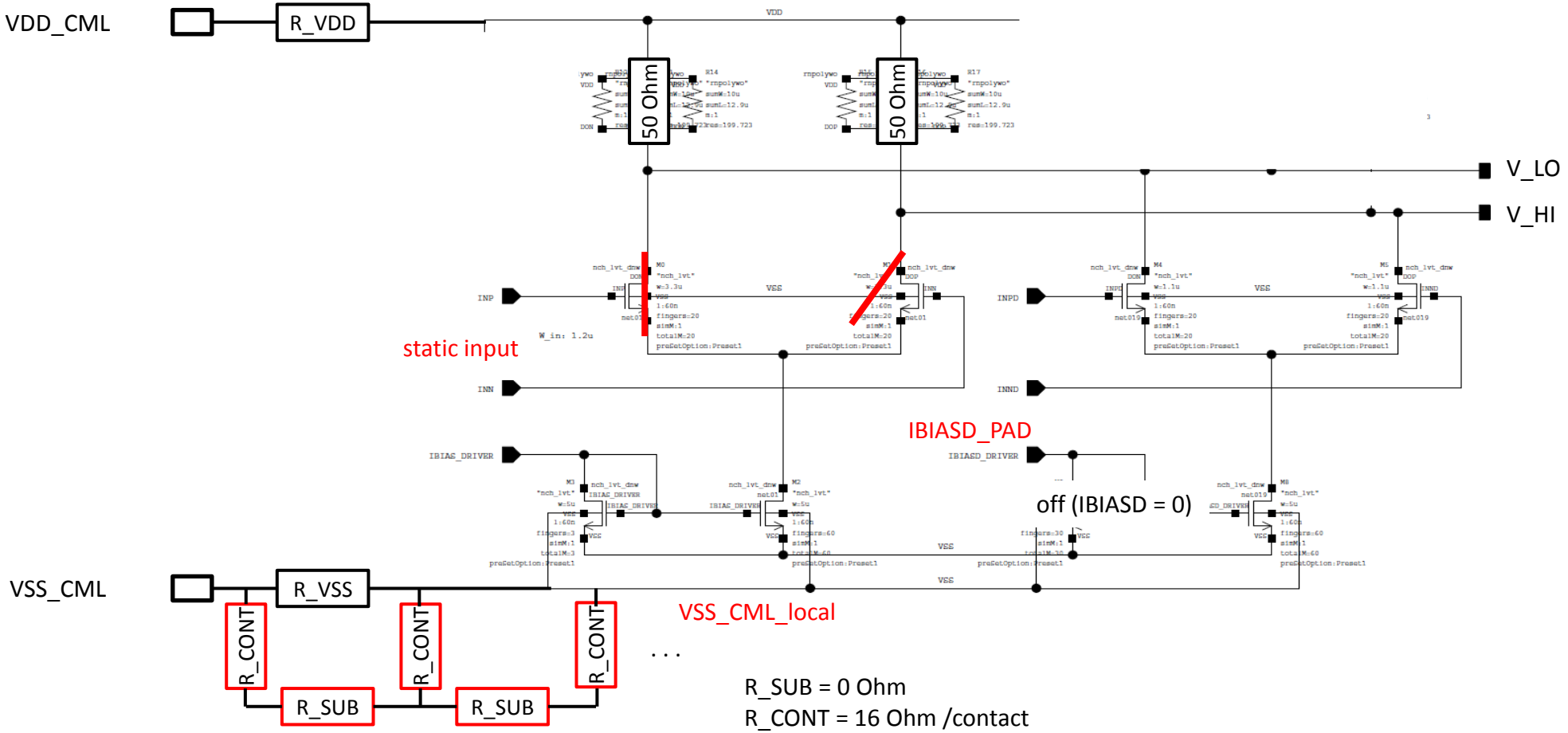
- Measurements indicate a parasitic resistance of about 36 Ohm in the VSS_CML line
- This is **not in agreement** with the simulation of the extracted layout which also shows ~5 Ohm parasitic resistance



Issue with the RC-extraction of the layout

- The extraction tool models the silicon substrate as a perfect conductor (R_SUB = 0 Ohm) and VSS_CML ins connected to the bulk with a lot of substrate contacts

➔ Underestimation of the resistance in VSS_CML

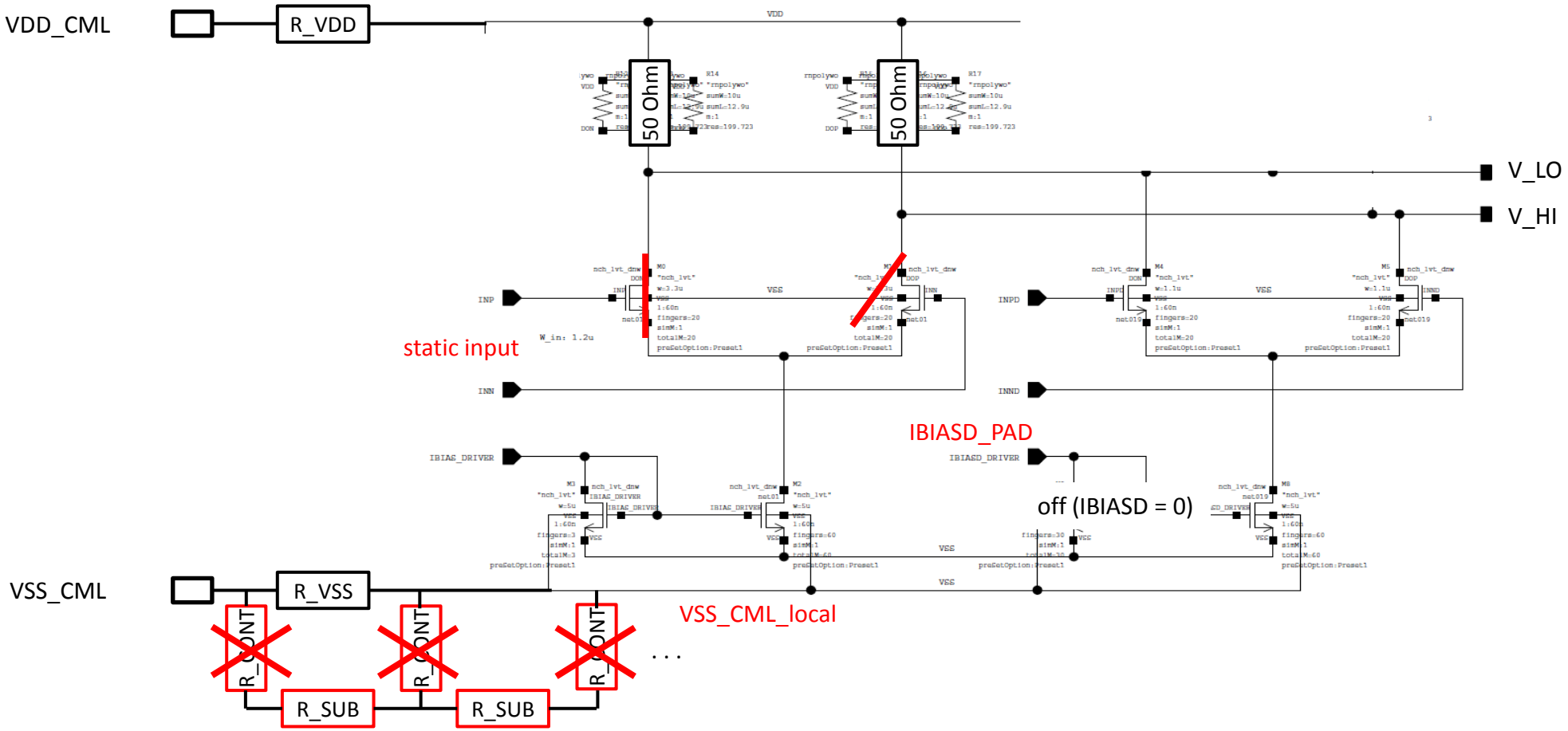


R_SUB = 0 Ohm
R_CONT = 16 Ohm /contact

Proof of the Explanation

- We removed the substrate contacts in the layout and extracted the parasitics again

➔ R_VSS_CML ~ 30 Ohm



CML_TX Layout toward DHPT12

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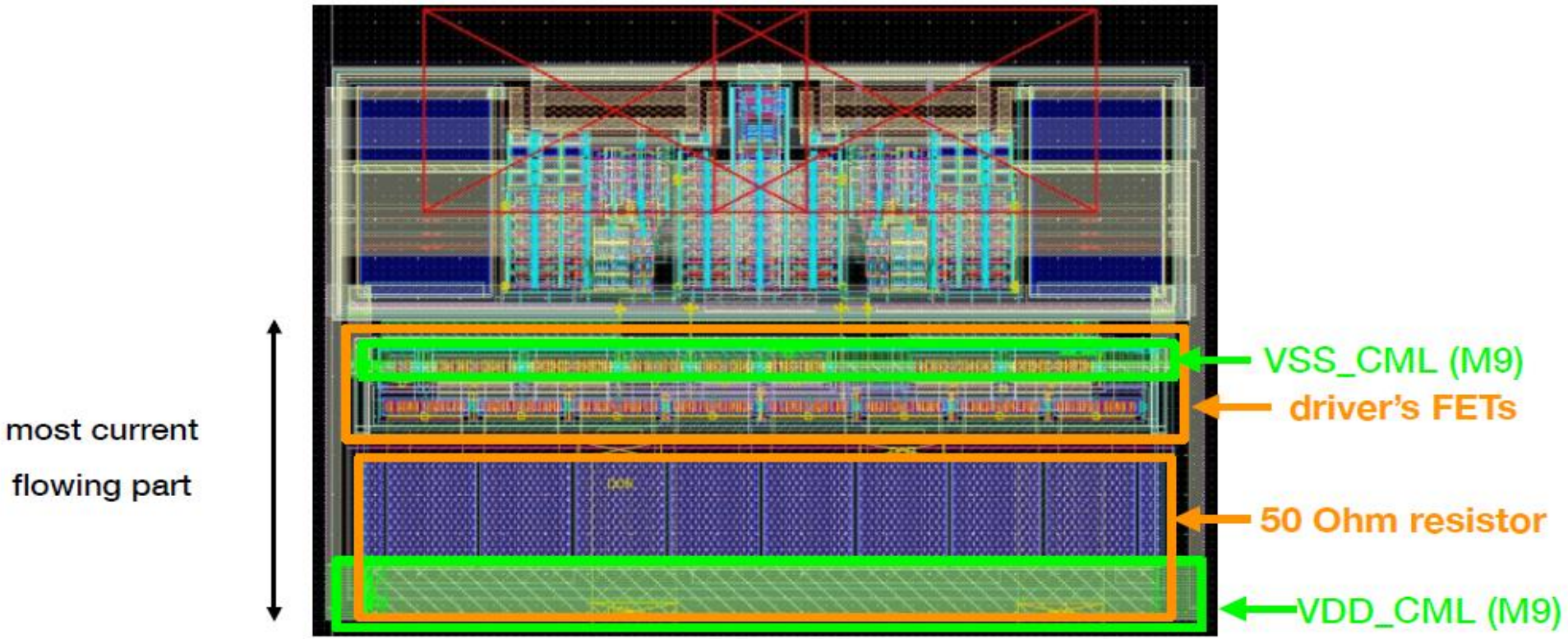
- vertical connection (M2→M9 for VDD_CML and M4→M9 for VSS_CML
- separate VSS and PSUB for Driver current mirror and switches
- avoid M1 connection between separate circuit blocks



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Serial-Resistance

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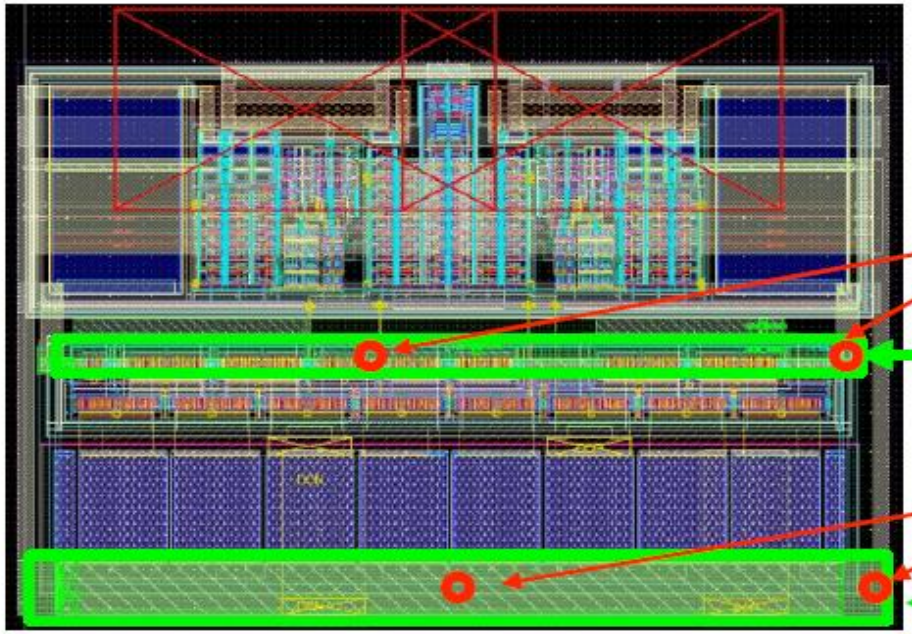

	Assura, typical	Assura, worst	Calibre, typical
VDD_CML	49.3 mΩ	66.5 mΩ	53.0 mΩ
VSS_CML	114.1 mΩ	151.4 mΩ	115.2 mΩ

ΔR_{serial}: ~30% corner dependence, and ~10% between Assura and Calibre

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