JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN

Belle II

ONSEN report on 2016 DESY Test Beam

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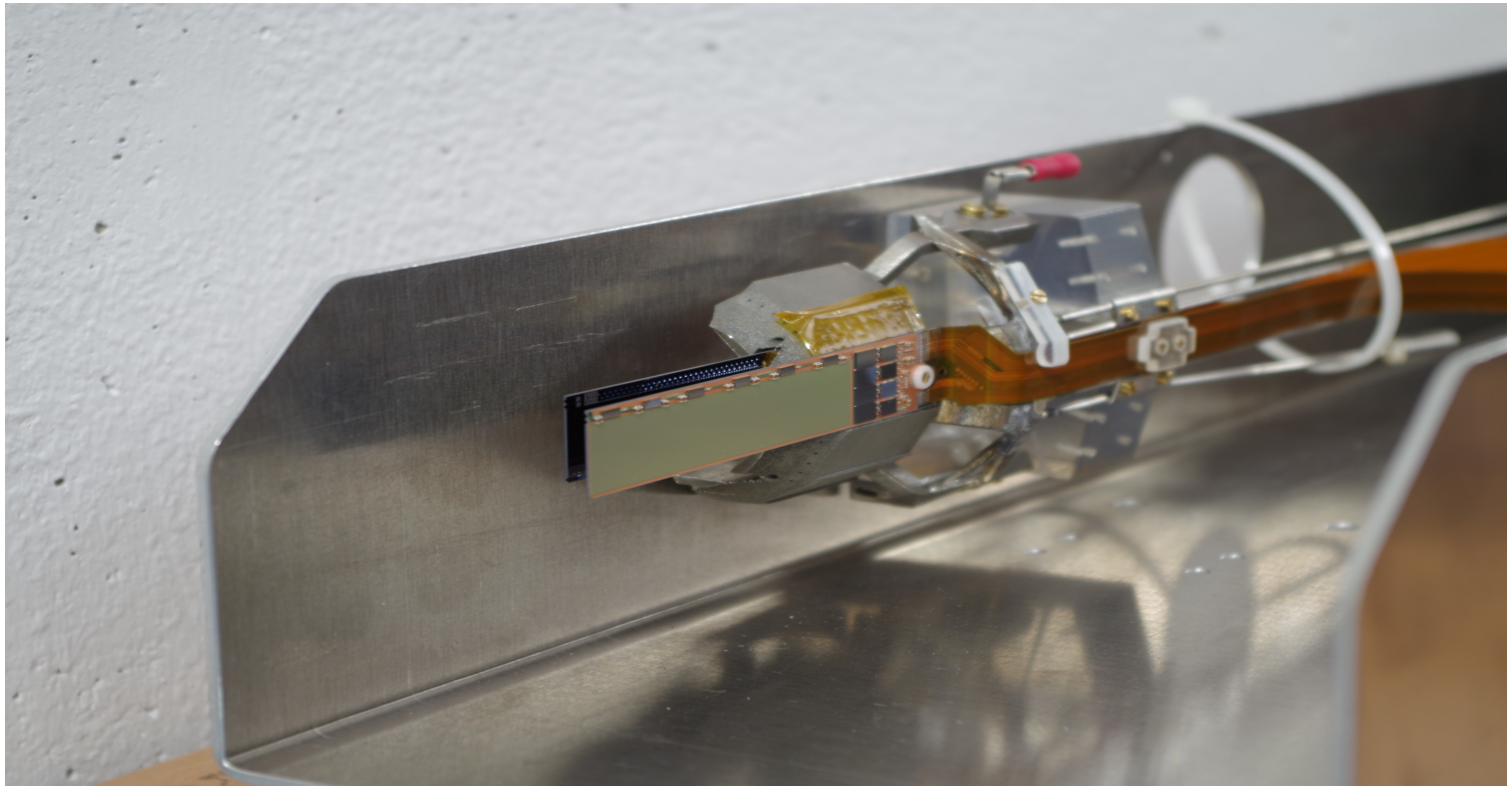
Detector

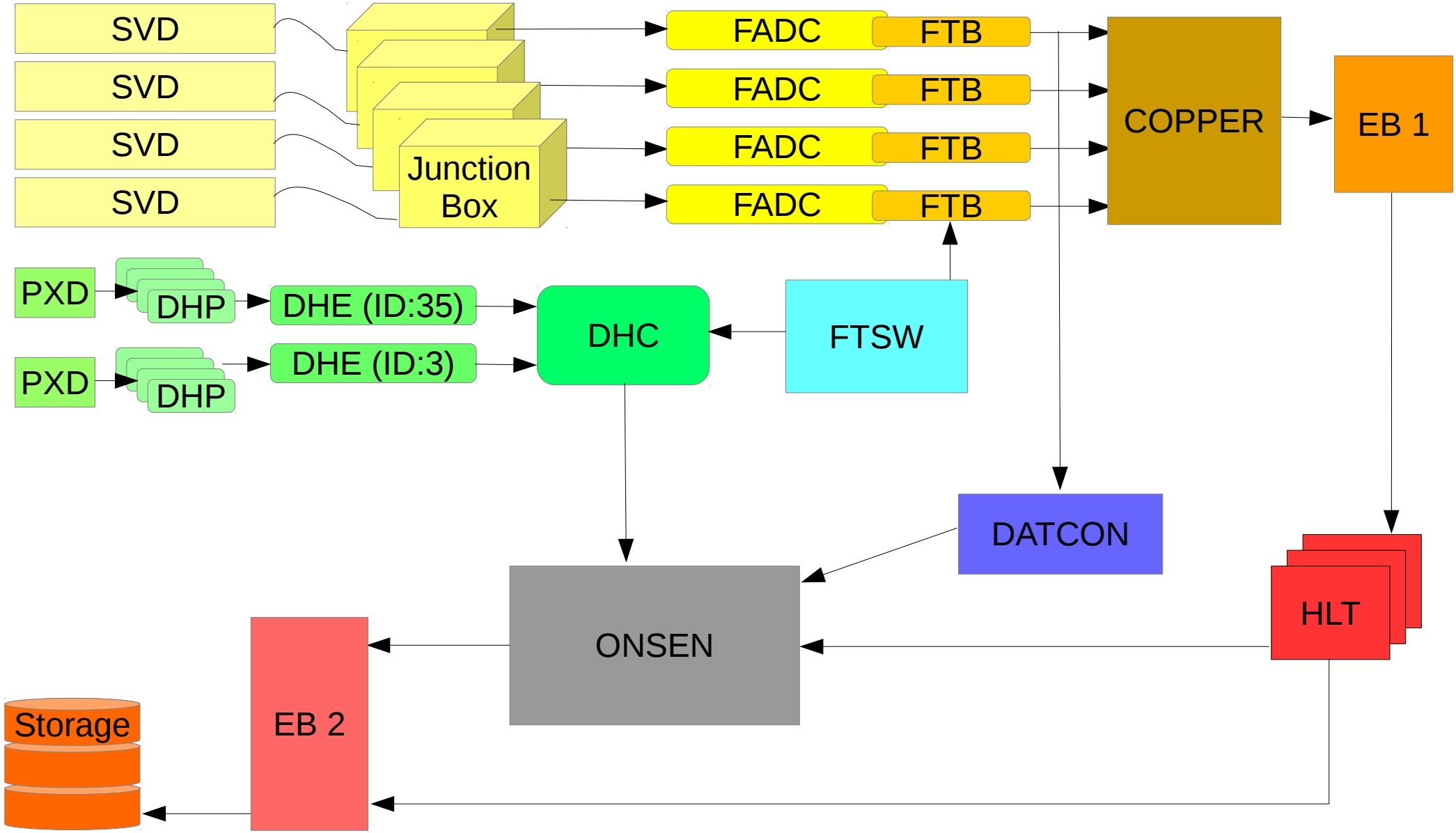
Whats new:

→ DESY TB 2014 only one PXD layer (no full sensor)
→ now 2 full PXD sensors, outer and inner backward (DHE ID 3 & 35)
→ 2 DHEs for readout of the half ladders, one DHC to combine them
→ All four SVD layers



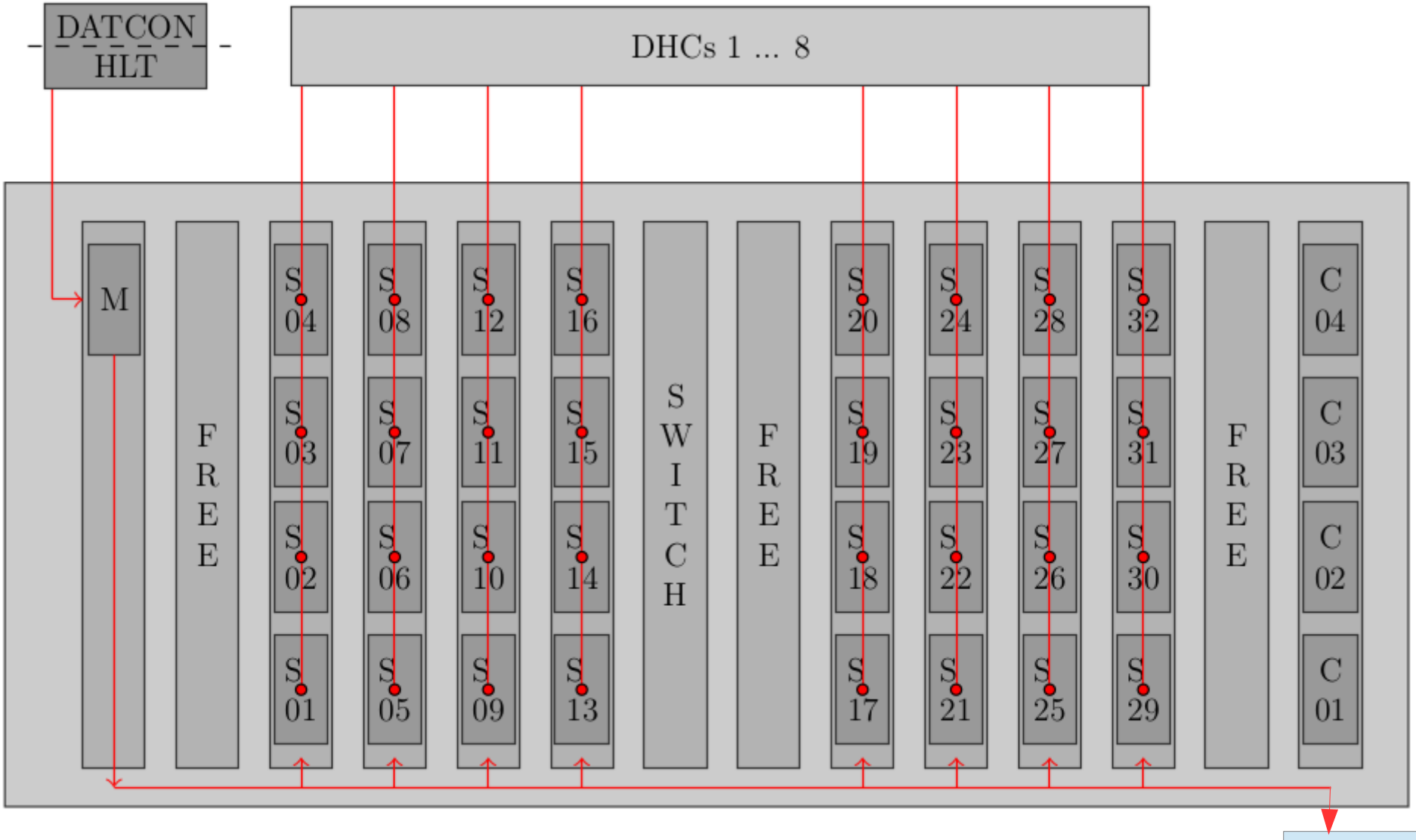
→ on April 28th full readout of all DHPs on both half ladders and all SVD layers
With ROI selection / tracking / magnetic field succeeded!!!

Hardware – Readout chain



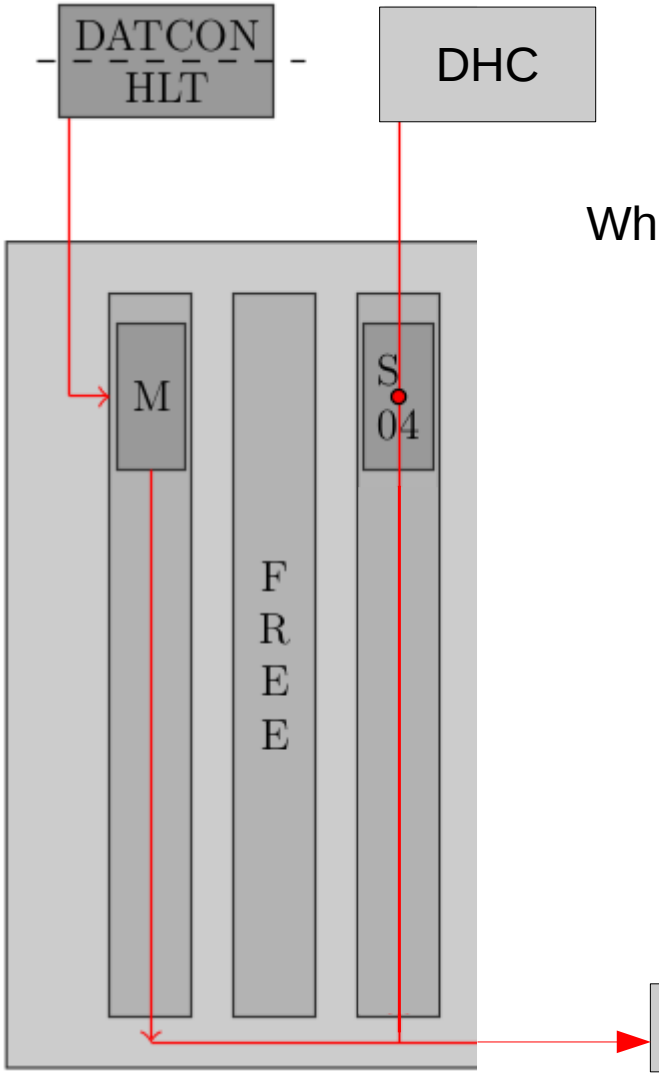
Hardware (ONSEN side)

- Reminder on full/final setup



Hardware (ONSEN side)

- Reduced DESY TB setup



What's new:

→ 2014 TB pocket ONSEN in µTCA shelf

→ ***now 2 slot ATCA shelf (pizza-shelf)***

→ ***2 additional FPGAs on carrier boards***

→ merger-carrier FPGA distributes ROIs to selector-carrier

→ selector-carrier FPGA distributes ROI to selector xFP card

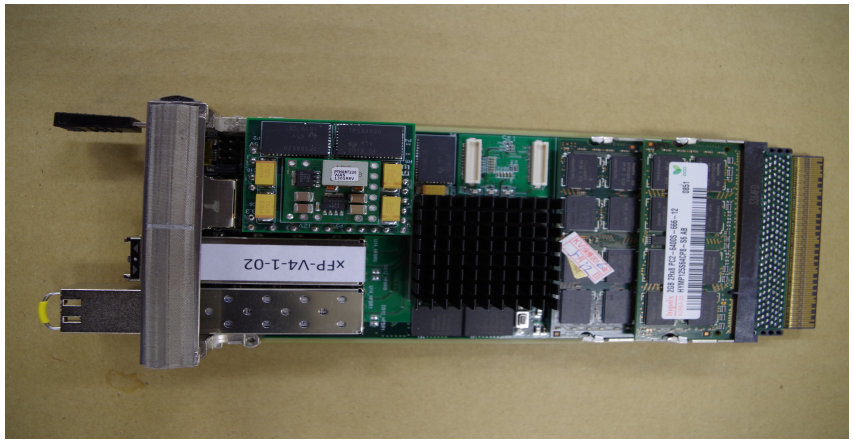
→ no 3rd / sender node

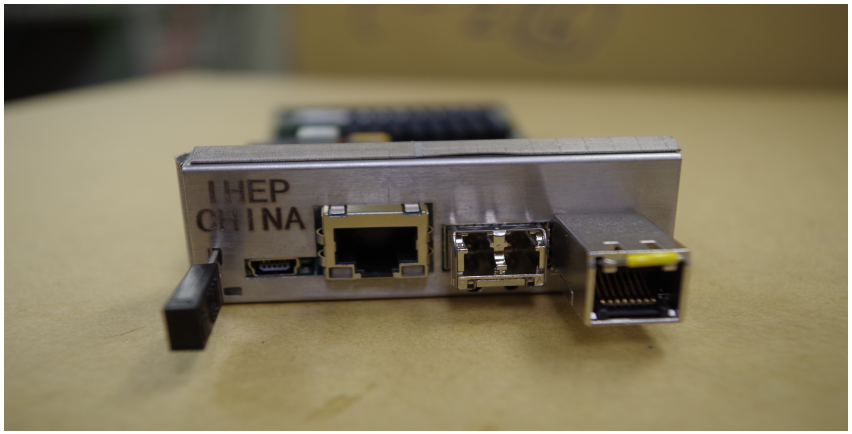
→ ***first time data transmission via backplane***

→ integration to slow- and run-control in EPICS / CSS

→ lots of fun with remapping … later more

Hardware (ONSEN side)





Firmware

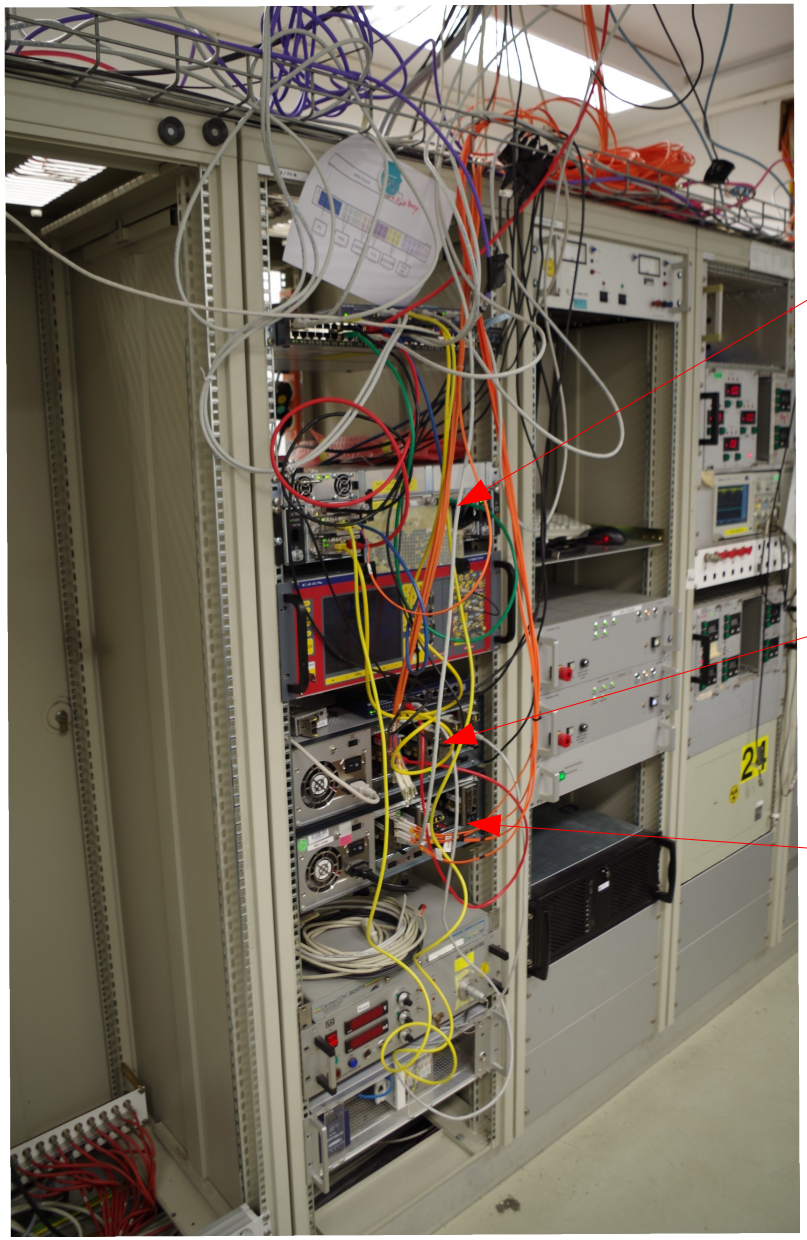
- Merger xFP
  - merge ROI's from DATCON and HLT
  - DATCON ROIs via AURORA, HLT via SiTCP
  - buffer management
    - store DATCON ROIs until HLT ROIs arrive
    - match ROIs according to trigger number, DHE ID and run number

- Merger-carrier
  - receives merged ROIs via backplane AURORA from xFP
  - distributes ROIs to selector-carrier

- Selector-carrier
  - receives merged ROIs via backplane AURORA from merger-carrier
  - distributes ROIs to selector xFP card

- Selector xFP
  - gets PXD data from DHC via optical link
  - data stored until merged ROIs arrive
    - → data read back from memory according to trigger number and DHE ID
  - PXD data reduced due to ROI selection
  - data further transmitted to EB2 via SiTCP

Setup at DESY



ONSEN pizza shelf

Pocket ONSEN backup (not used)

DATCON

Software

- PXDUnpacker
  → Unpacks ONSEN data stream on Express Reco level for DQM monitoring
  → Unpacks *.sroot files for offline analysis (UnpackFromSeqroot.py)

- ROIPayloadAssembler – for HLT
  → calculates lengths and places Header on HLT ROI frames
  → running in HLT script

- ROIGenerator – for HLT
  → running in HLT script
  → ROI sizes where fixed due to remapping

- Changes made for DESY TB
  → check if DHE IDs arrive in ascending order in PXDUnpacker
  (otherwise no hits on inner layer)
  → remapping in PXDUnpacker and ROIGenerator

Remapping

- New mapping on PXD sensors

- Unfortunately not known before TB
  → remapping in Firmware not possible during TB time
  → ROIs and Pixels had to be remapped in software (basf2)
    → in Unpacker and ROI assembler

- In final setup remapping will be done on DHE
  → send out pixel coordinates in geometrical final coordinate system as u_cellID, v_cellID

- Remapping depends on inner / outer as well as forward and backward orientation of the modules
  → inner forward and outer backward modules have the same remapping

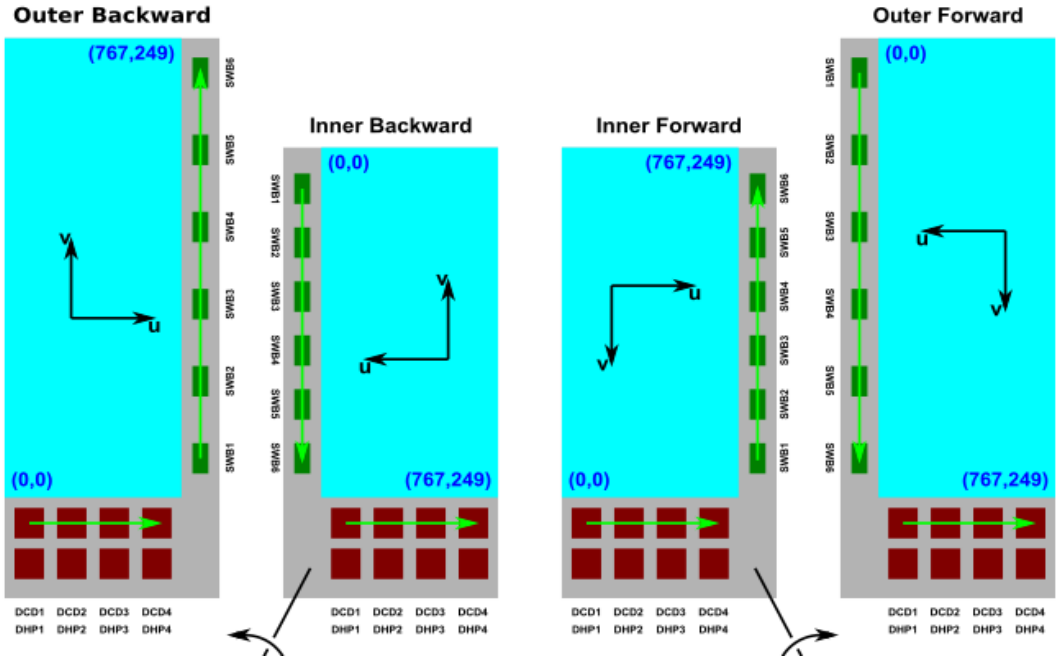
- Due to remapping the smallest ROI size was fixed to Gate*DHP (4 rows * 62 columns)

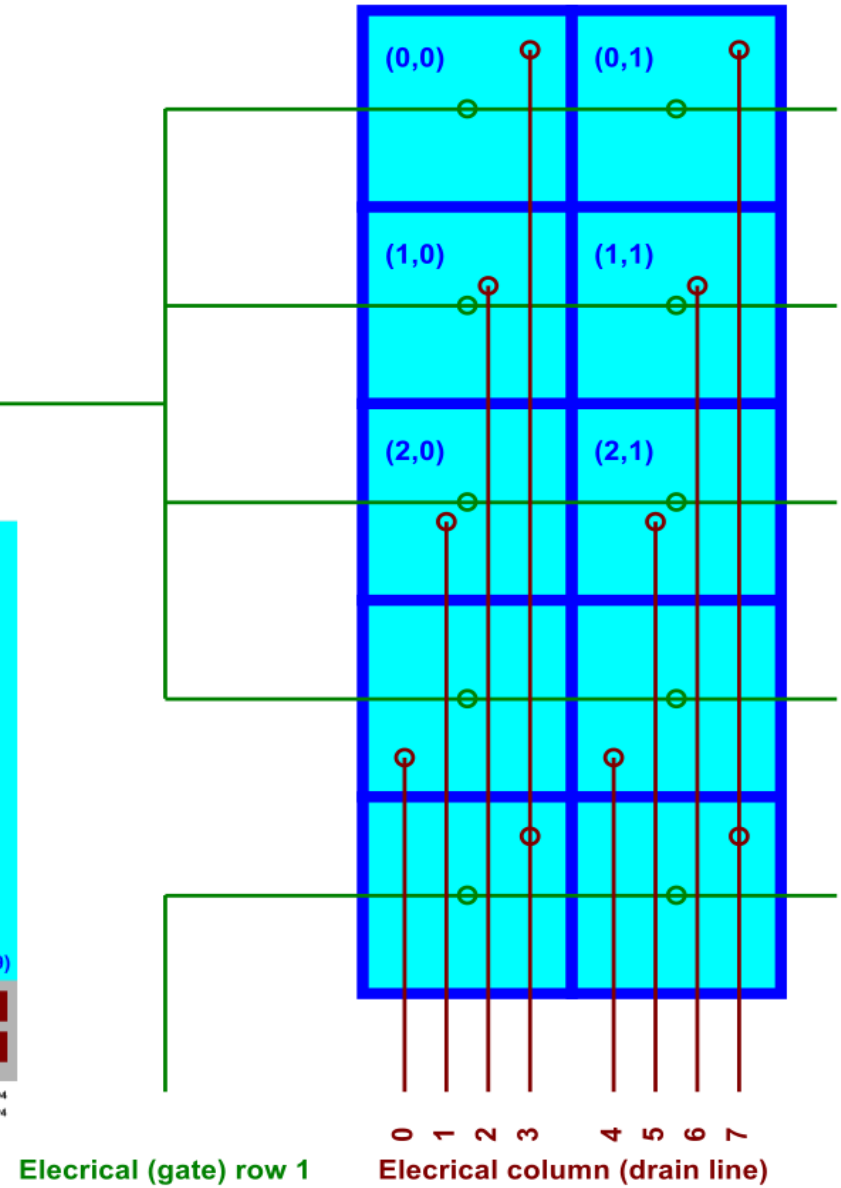
Remapping

- 3 different coordinate systems
  → Chip system (DHP_col, DHP_row)

  2 LUTs and 4 calculation steps

  → geometrical system (col, row)



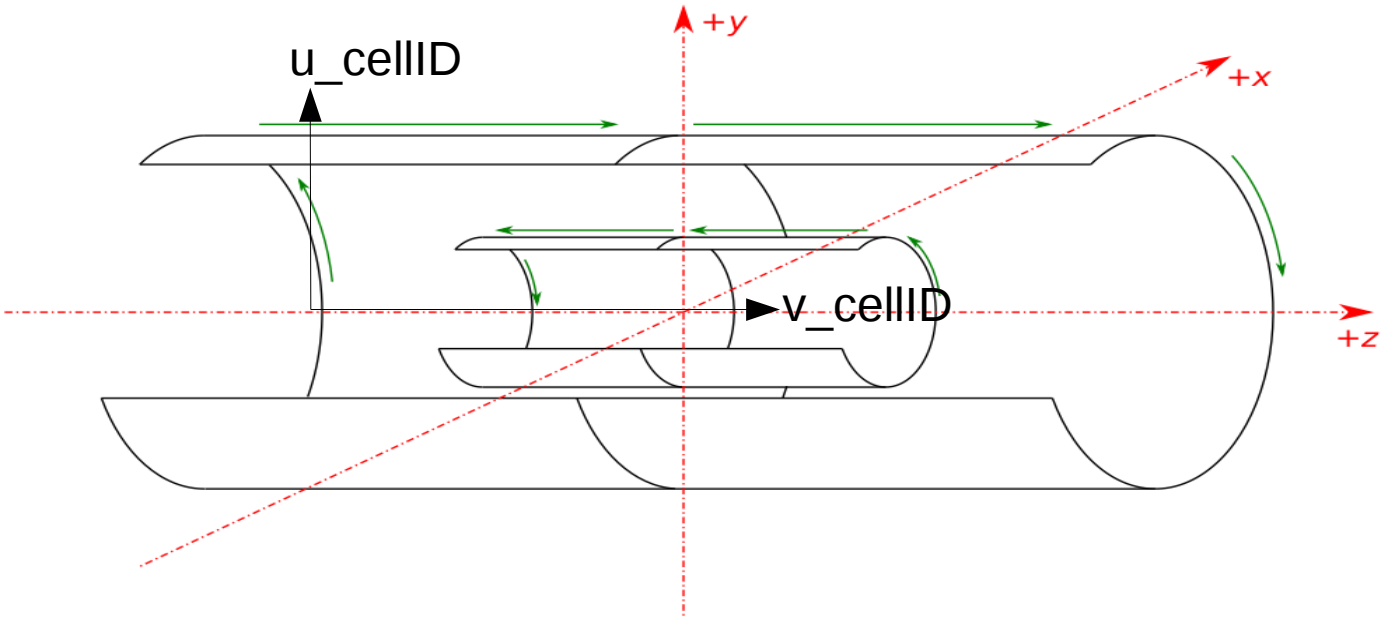


Remapping

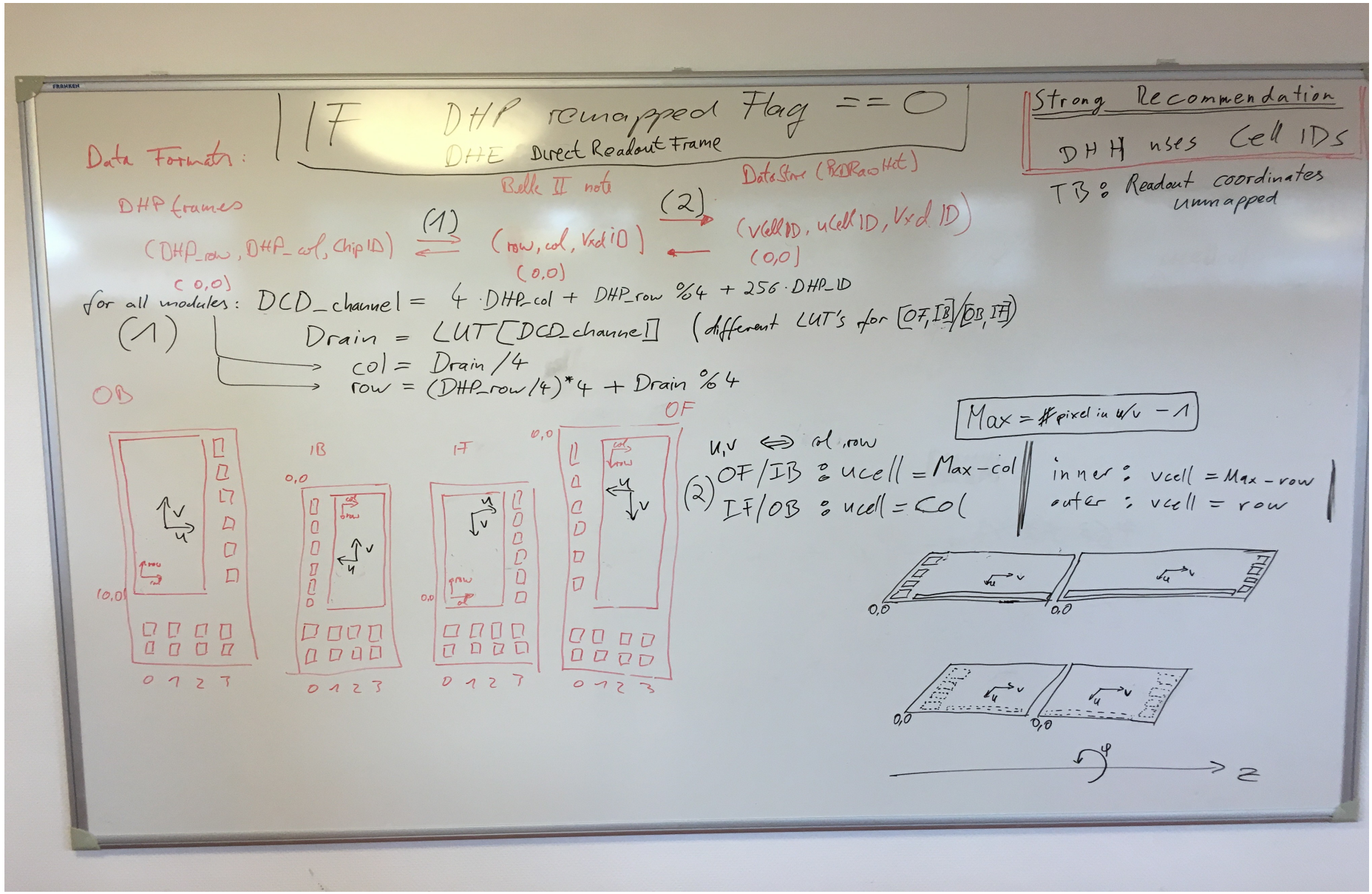
→ geometrical system (col, row)

Mirroring col/row according to layer
Orientation in respect to the beam

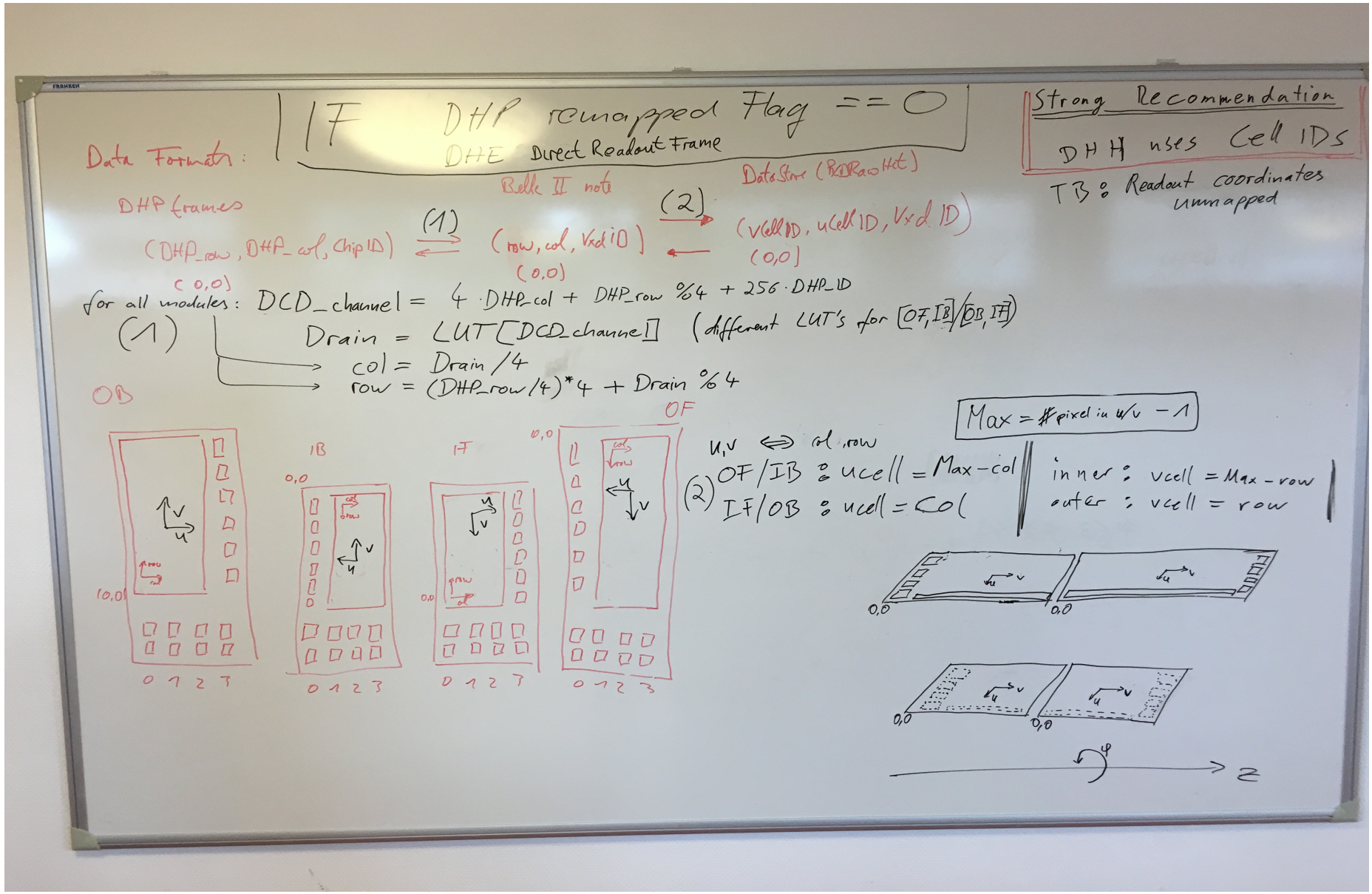
→ global coordinate system (u_cellID, v_cellID)
- → defied in basf2
- → u_cellID runs along positive R-Phi-direction
- → v_vellID runs along positive z-direction



Remapping


IF DHP remapped Flag == 0
DHE Direct Readout Frame
Strong Recommendation
DHH uses Cell IDs
TB: Readout coordinates unmapped
Data Formats:
Belle II note
DataStore (RawHit)
DHP frames
(DHP_row, DHP_col, Chip ID)
(row, col, Vxd ID)
(vCellID, uCellID, Vxd ID)
(0,0)
for all modules: DCD_channel = 4 · DHP_col + DHP_row %4 + 256 · DHP_ID
(1)
Drain = LUT[DCD_channel] (different LUT's for [OF, IB]/[OB, IF])
col = Drain /4
row = (DHP_row /4)*4 + Drain %4
OB
IB
IF
OF
Max = #pixel in u/v − 1
u,v ⇔ col, row
(2) OF/IB : ucell = Max − col
IF/OB : ucell = col
inner : vcell = Max − row
outer : vcell = row
z

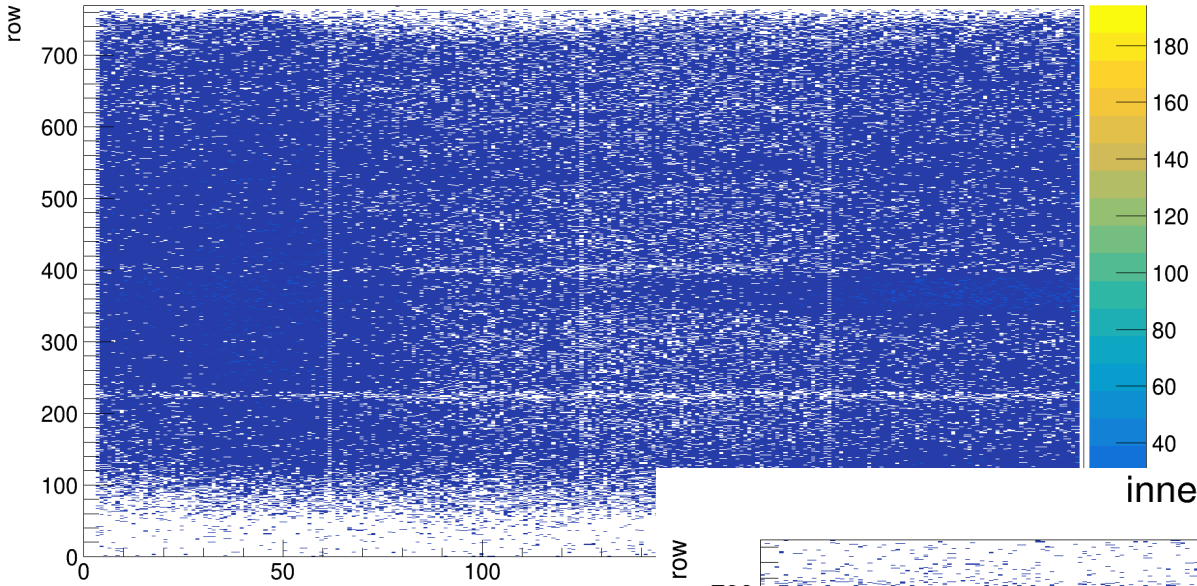
Remapping



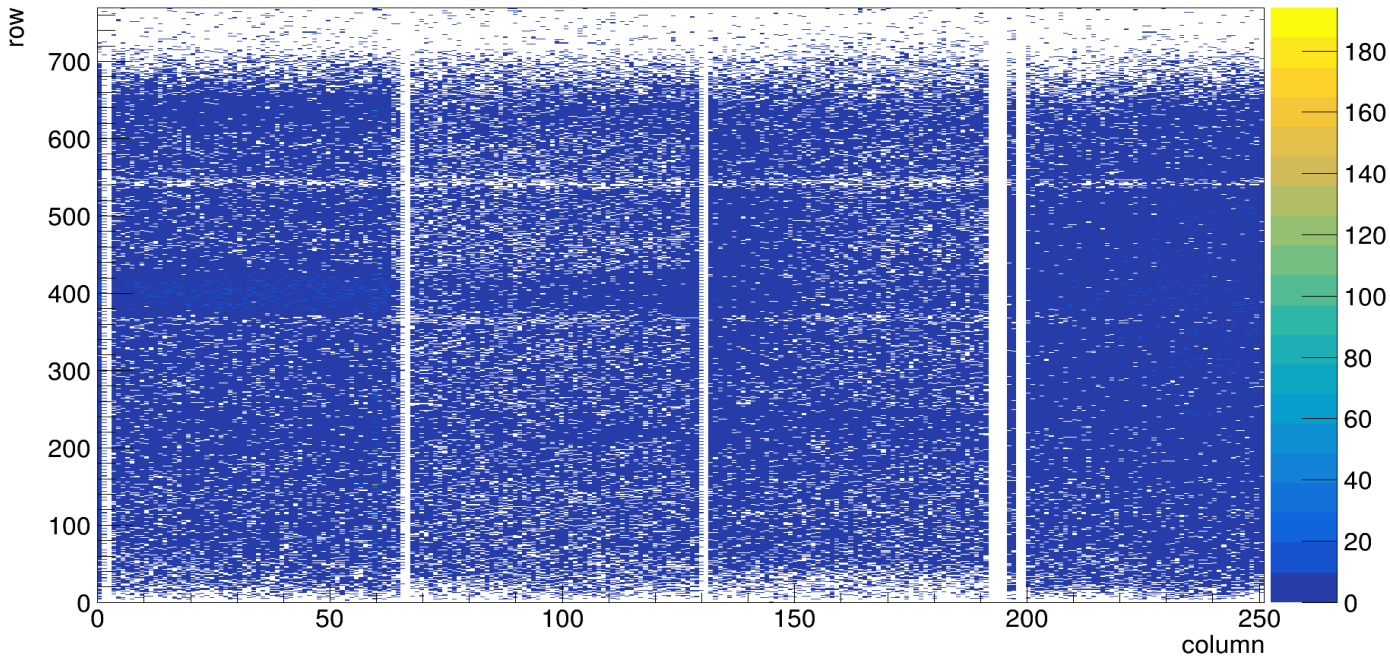
documented in Belle2 Note 10 by Manfred Valentan

Remapping

inner layer with remapping



inner layer w/o remapping

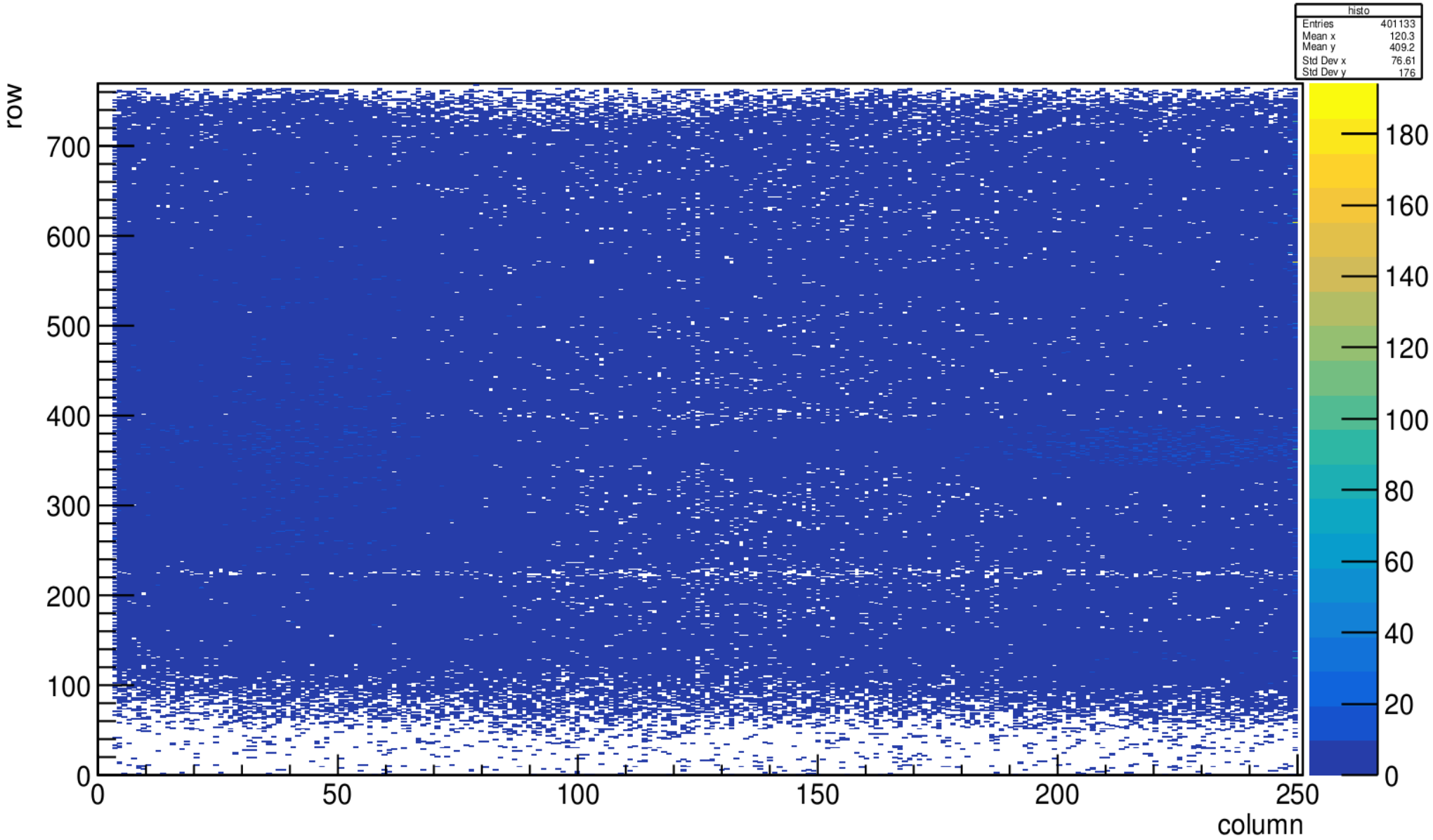


Hardware (ONSEN side)

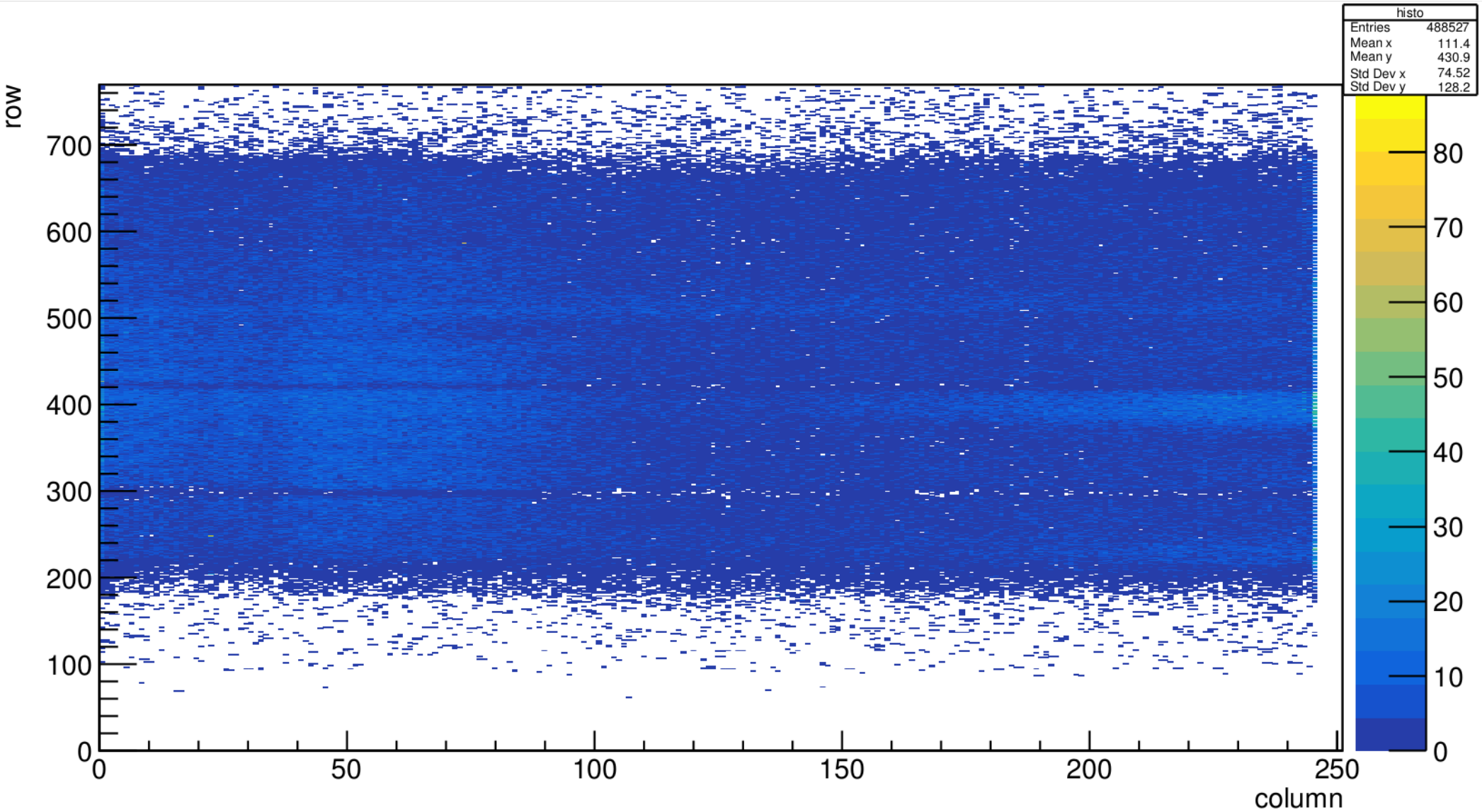
- Preperations and pre-tests
  - → starting on 03/29 (2 weeks before arrival of PXD), tests with DHH and DATCON
  - → new: HLT emulator
    - → random ROIs, but matched trigger number send by UDP from DHC
  - → 8kHz achieve with FTSW+DHC+HLT (tracking switched off)
  - → 10kHz achieved with FTSW+DHC+HLT emulator

- Achievements with beam
  - → 2kHz run 279 “golden run” (w/o DATCON)
    - → 1.152.046 triggers
    - → 889.660 pixel hits
    - → 892.977 ROIs (=> some ROIs w/o Pixels) → to be explored

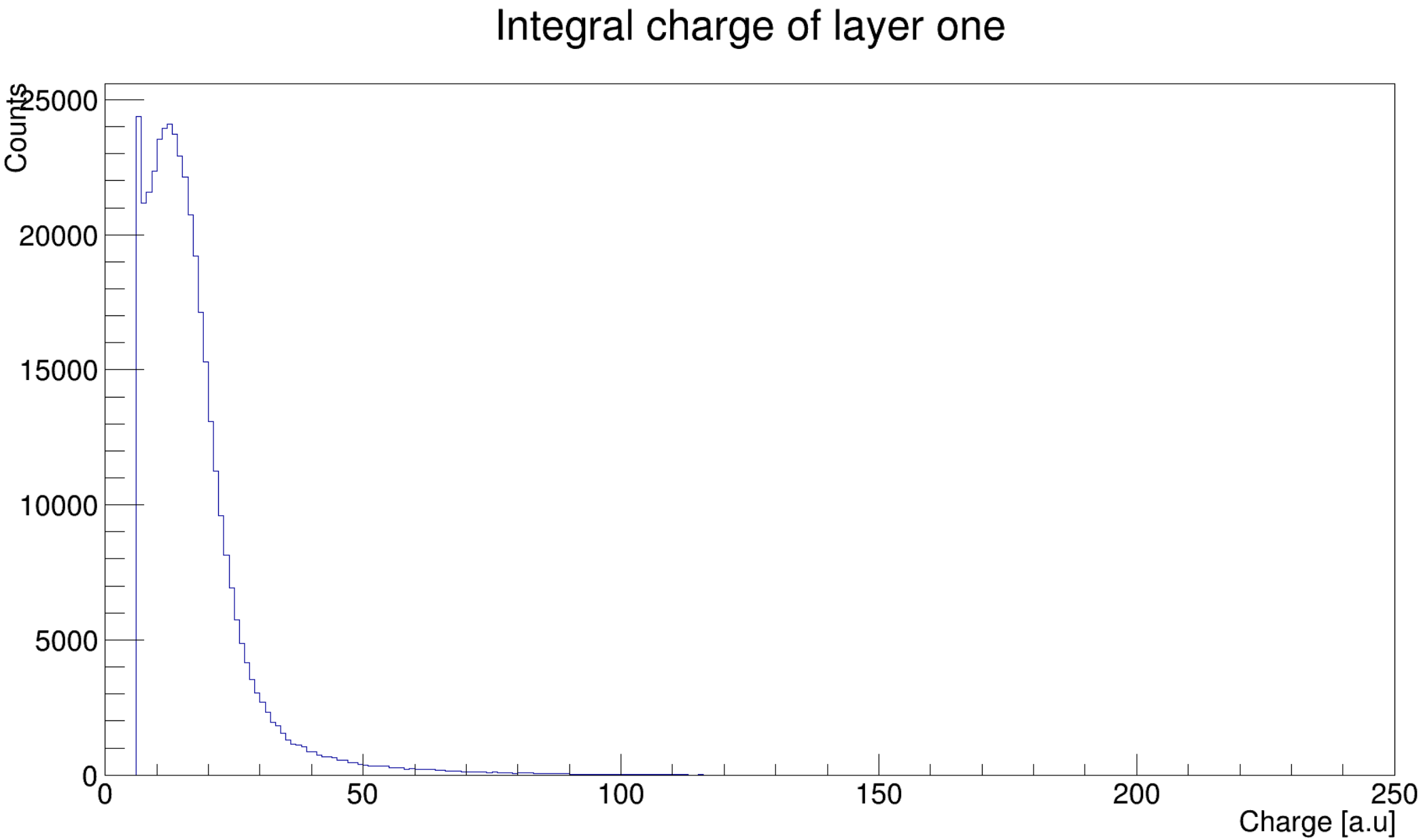
Hitmap Layer 1 run 279



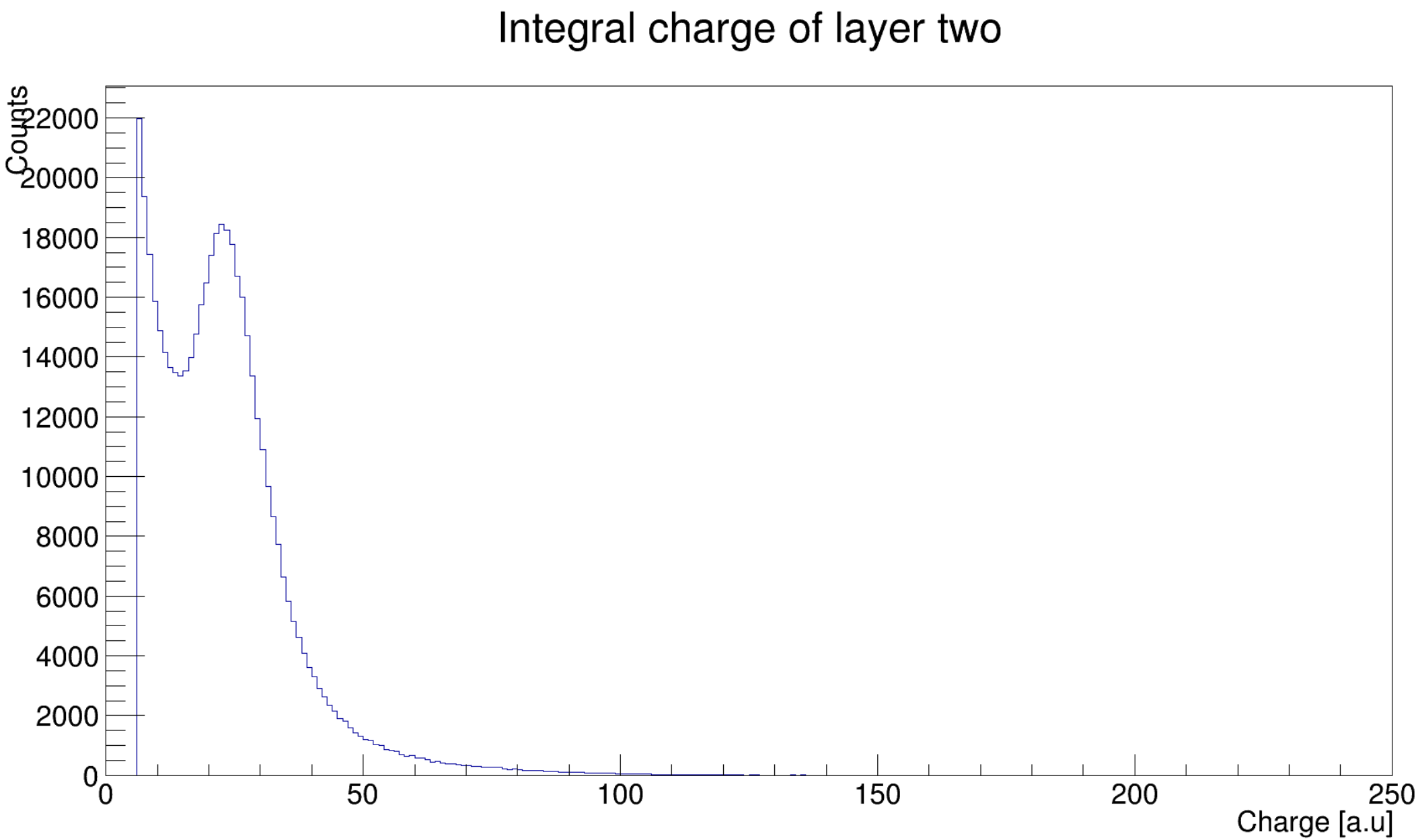
Hitmap Layer 2 run 279



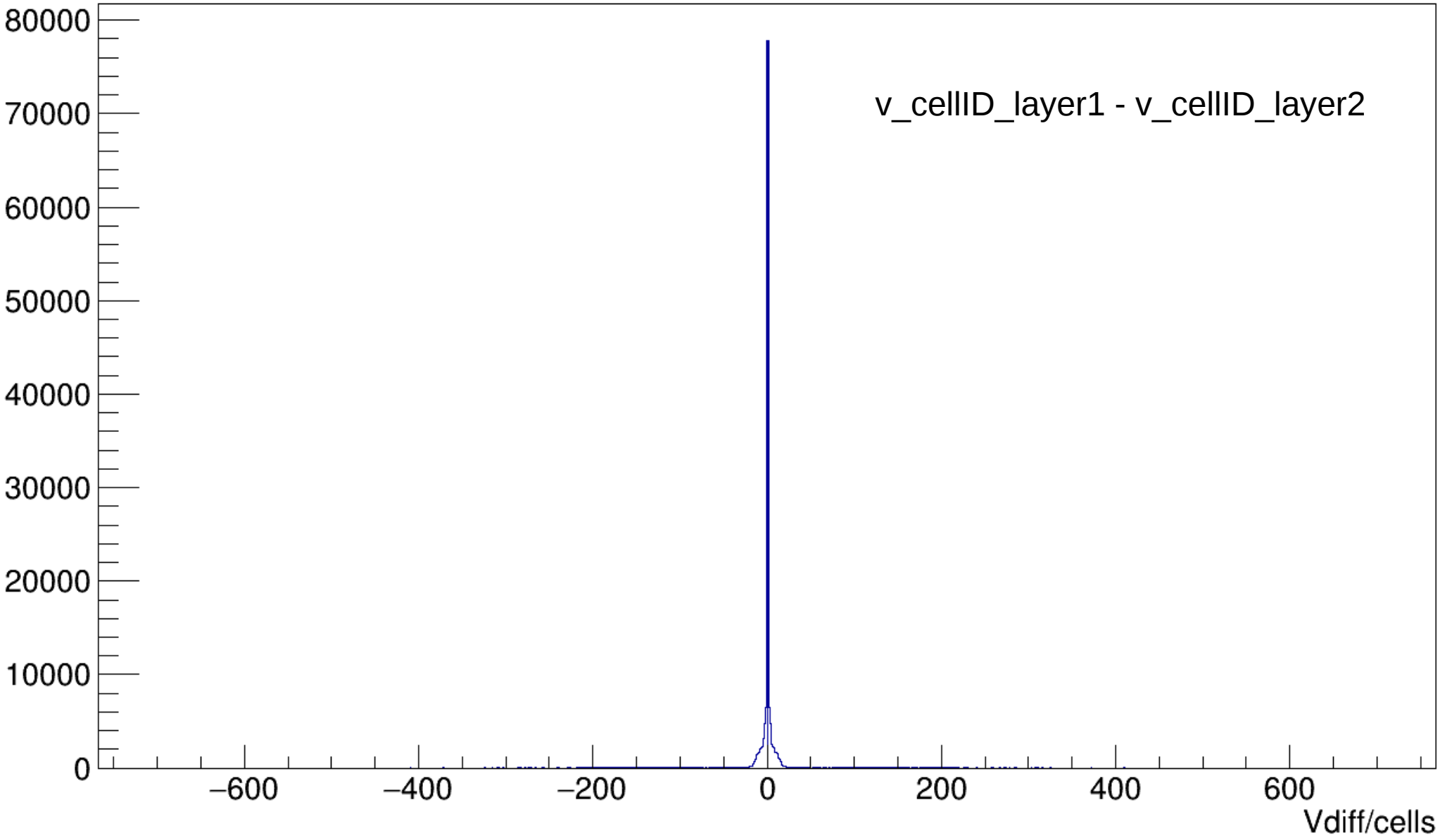
Charge in Layer 1 for run 279



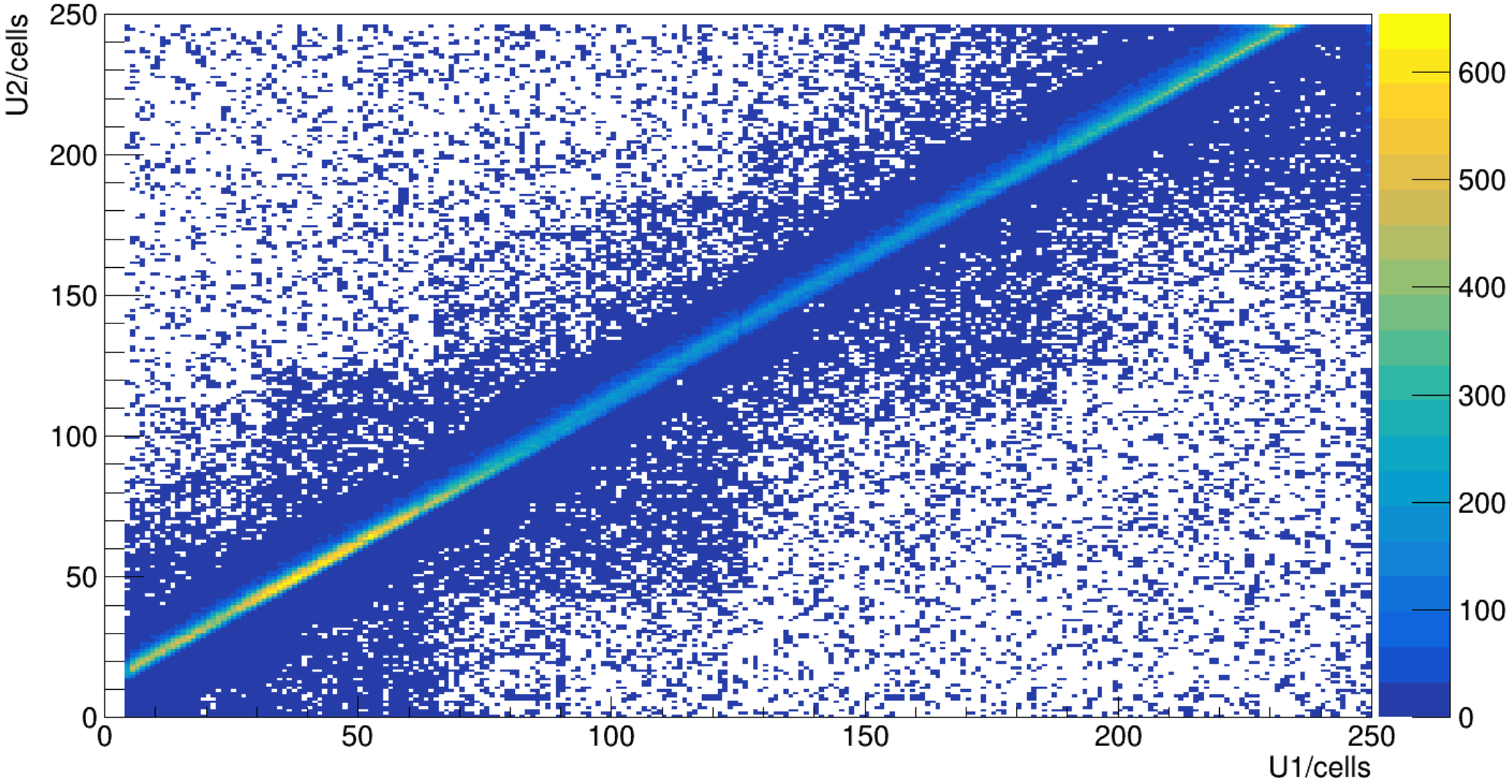
Charge in Layer 2 for run 279



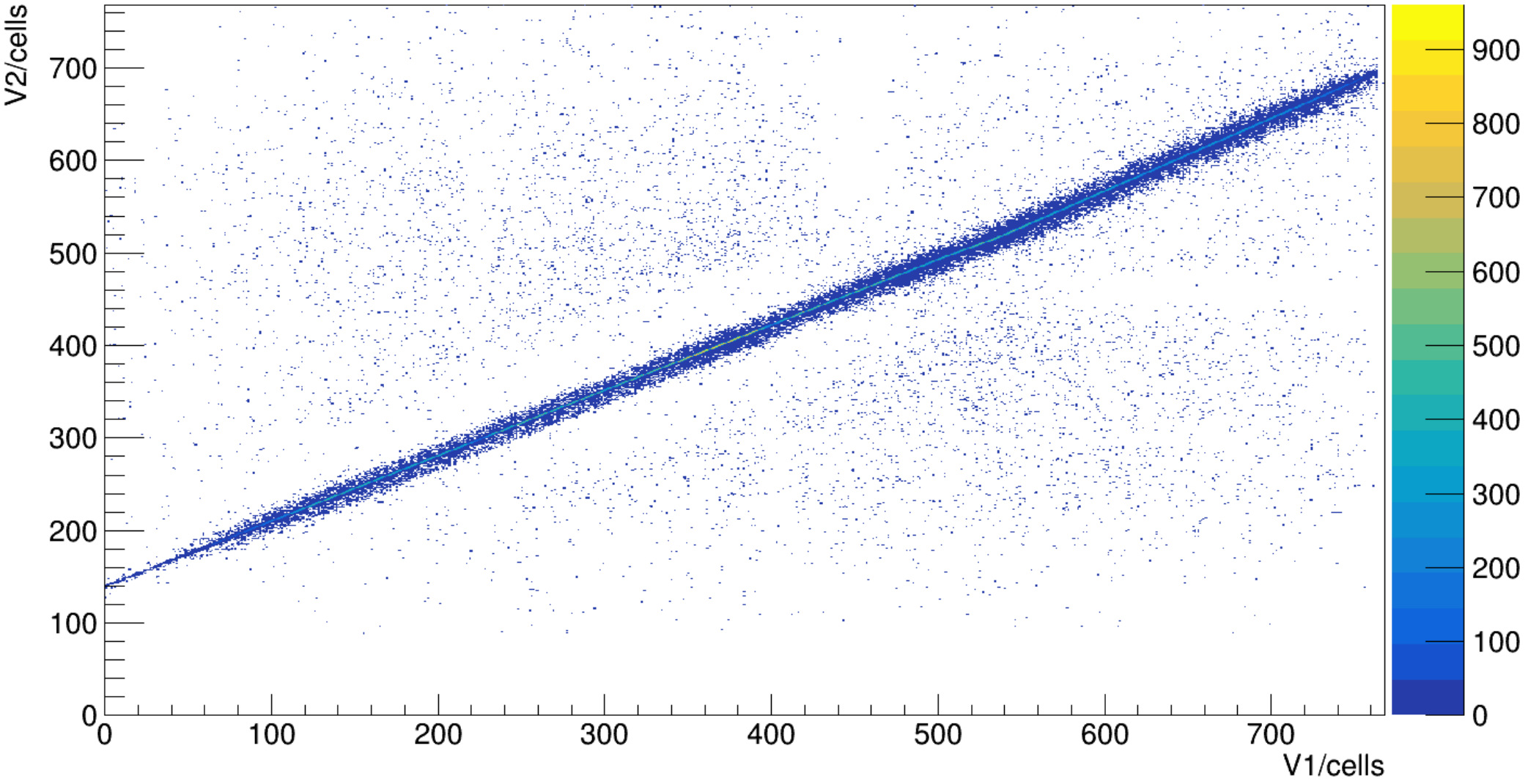
Residual Plot on V run 279



Correlation Plot in U direction run 279



Correlation Plot in V direction run 279

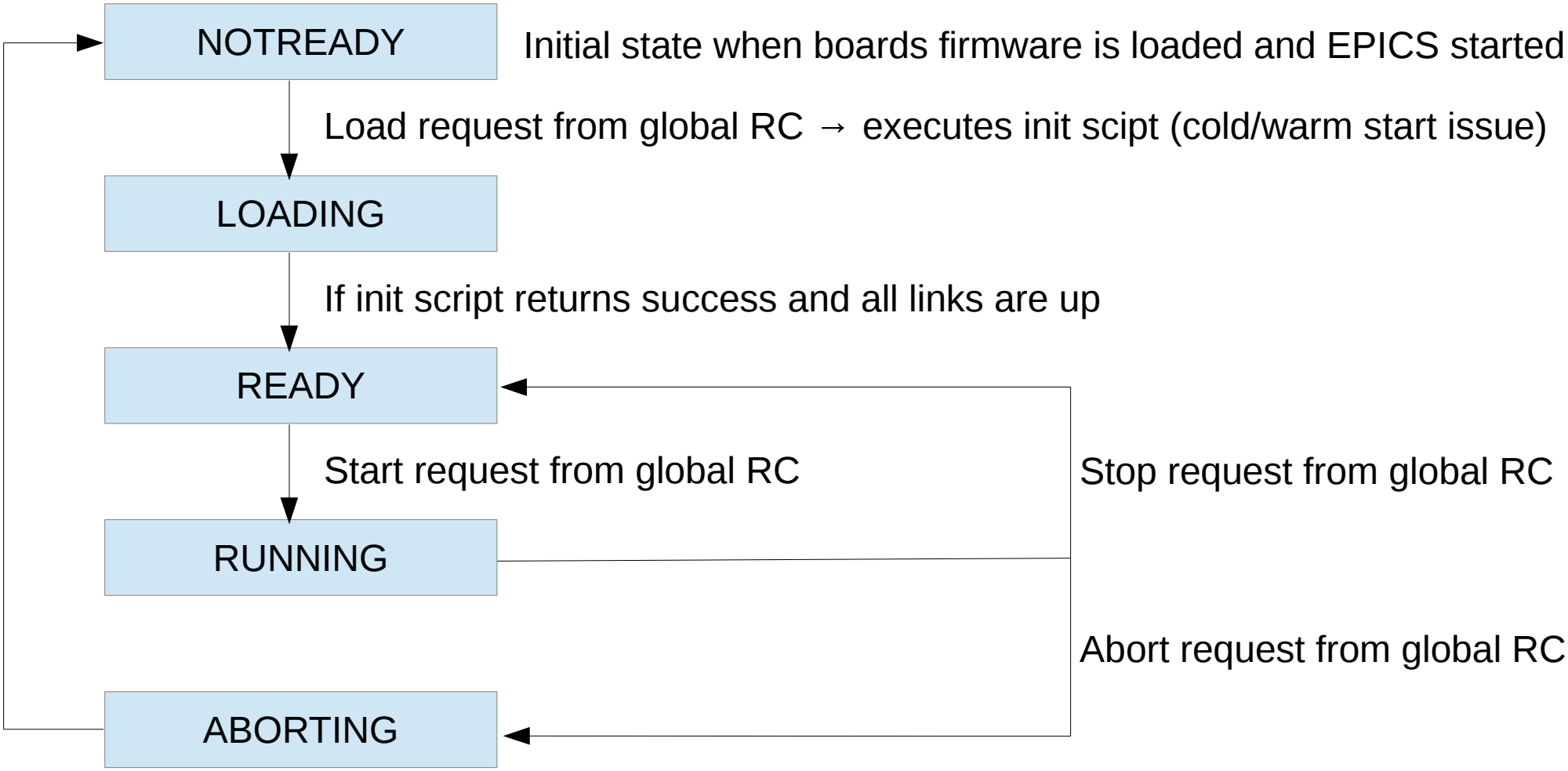


Slow control of pizza ONSEN

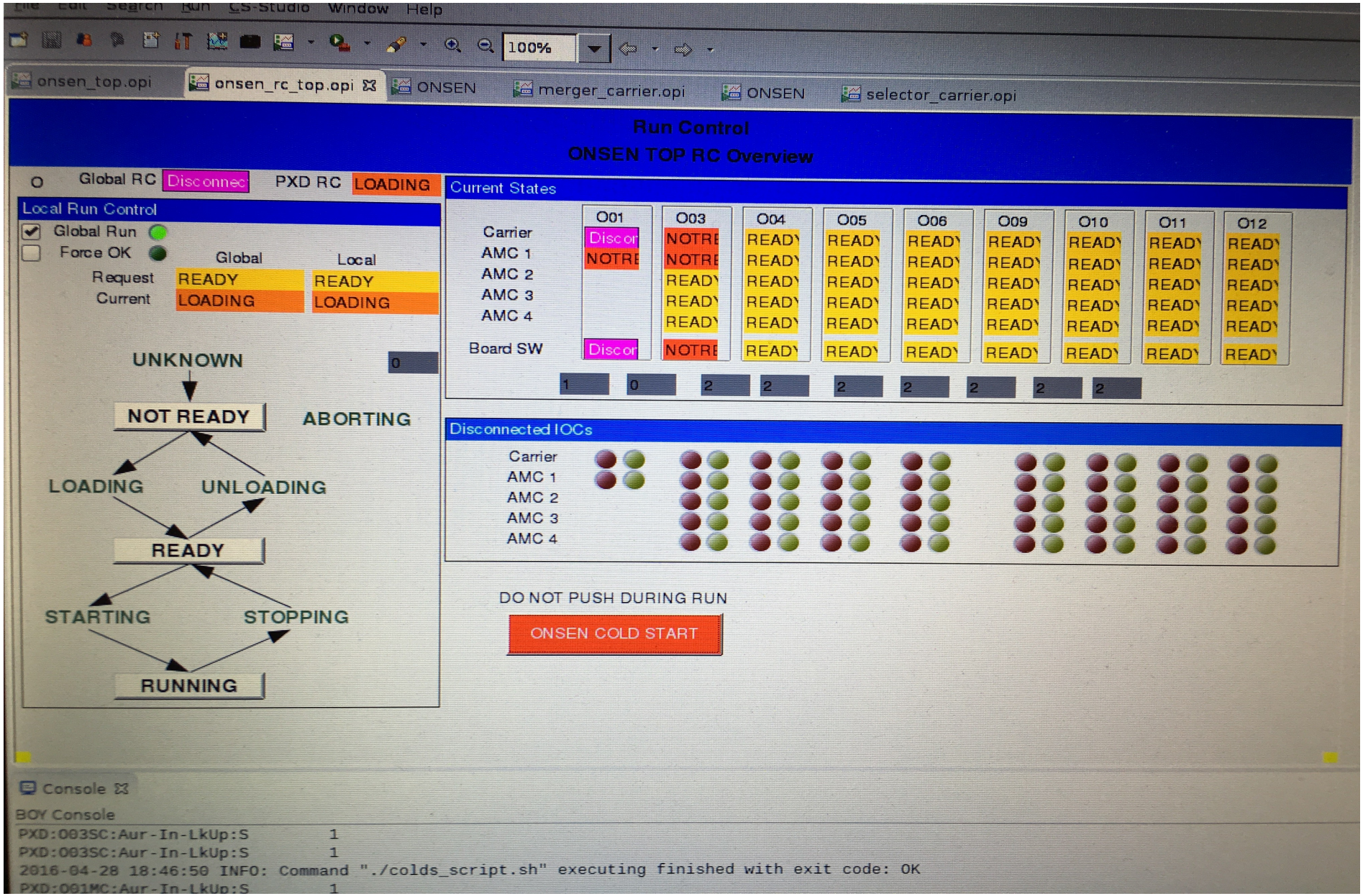
- EPICS can be started on the FPGA's power pc (linux)
- Registers that can be read out by PVs were implemented in firmware
- .db files access these registers and provide PVs fot readout and control
- Some Interrupts are provided but still need improvement
  - → AURORA link up
  - → SiTCP link up
  - → LUT write error (when entry in LUT gets overwritten)

Run control of pizza ONSEN

- Run control IOC provided by B. Spruck
- Receives requests from global run control (Konno-san)



Run control of pizza ONSEN



Issues on ONSEN side

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  → Problem traced back to delay time on the link between xFP card and carrier

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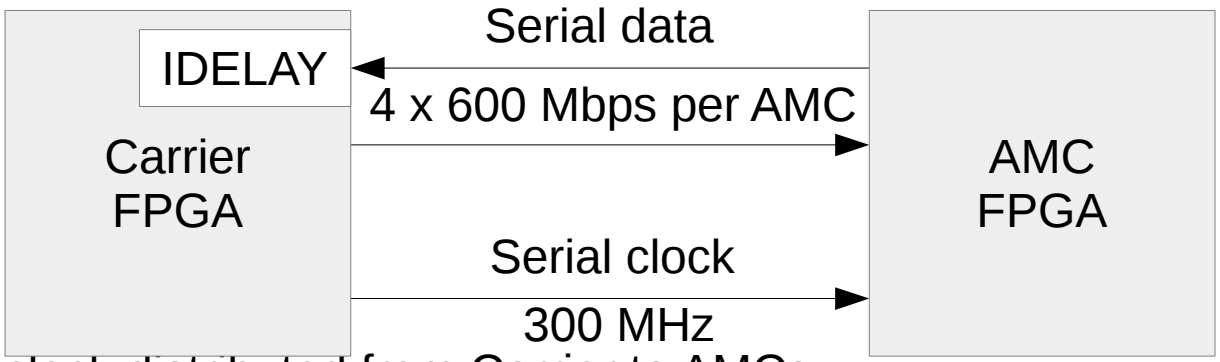

  → Serial clock distributed from Carrier to AMCs
  → Data received on Carrier has **phase shift** relative to Carrier clock
    → Compensate with a **fixed delay**, determined by tuning
  → Problem: One (!) carrier shows a **temperature dependency** of the delay
    → new delay value for warm FPGA and raise temperature in E-Hut

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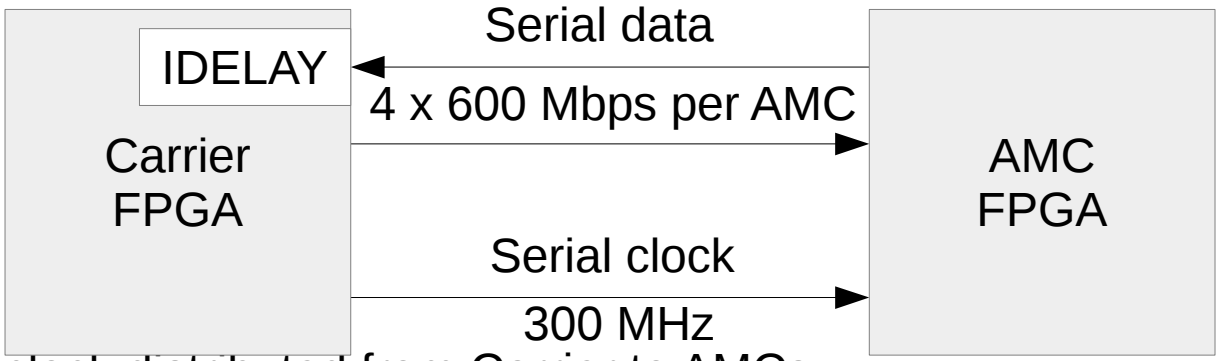

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  → new delay value for warm FPGA and raise temperature in E-Hut
    → ***everyone is a big ONSEN fan now***
    → ***this is not a feature***

Issues on ONSEN side

- ONSEN cold start issue
  - → after suspending a run ONSEN needs to have a “cold start”
    - → load firmware, initialize system
  - → hot start (just send data again) and warm start (only initialize the boards) lead to corrupted data on EB2 (trigger number mismatch between HLT and DHC frame)
  - → init script does not work properly / still HLT packets in SiTCP buffer which corrupts data

- Interrupt handler does not work properly for the time being
  - → interrupts e.g. for channel up should run in separate a program setting status of PV
  - → for now no interrupts but polling on registers (PVs) to display

Results

- The whole DAQ chain was tested with up to 2kHz (improvement of factor 20 to TB 14)
- ROI selection on ONSEN worked with fixed ROI sizes required due to remapping problem
- Correlations were seen in ALL detector layers (PXD & SVD)
- Long time stability tested for 8h at 2kHz
- Everything stably watched by run and slow control


THANK YOU!