edet: Depfet Movie Chip
(DMC) Status

20th International Workshop on DEPFET Detectors and Applications

11.-14.05.2014 Kloster Seeon

DMC keypoints

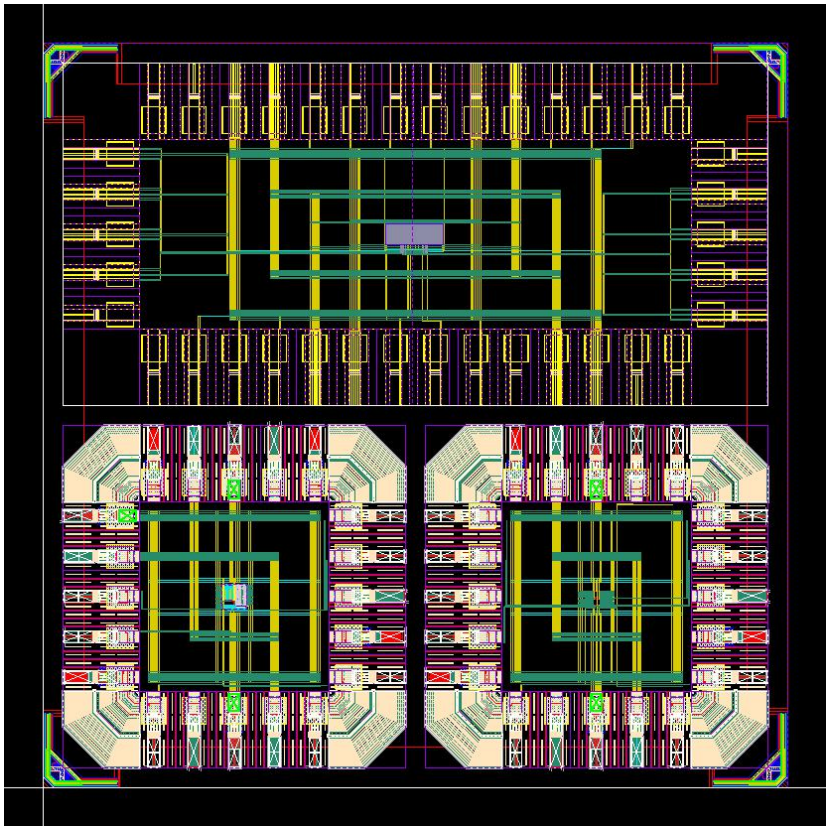
- Capturing up to 100 full pictures (512x64x100x8bit = 26Mbit) implemented via single port SRAM IP (TSMC)
- footprint compatible to DHP (new pins located in the not assigned pin area)

  → TSMC 40nm technology → reuse of DHP IP not possible

- 6 „slow“ serial downlinks with 200Mbit (for edet only 4 will be used)

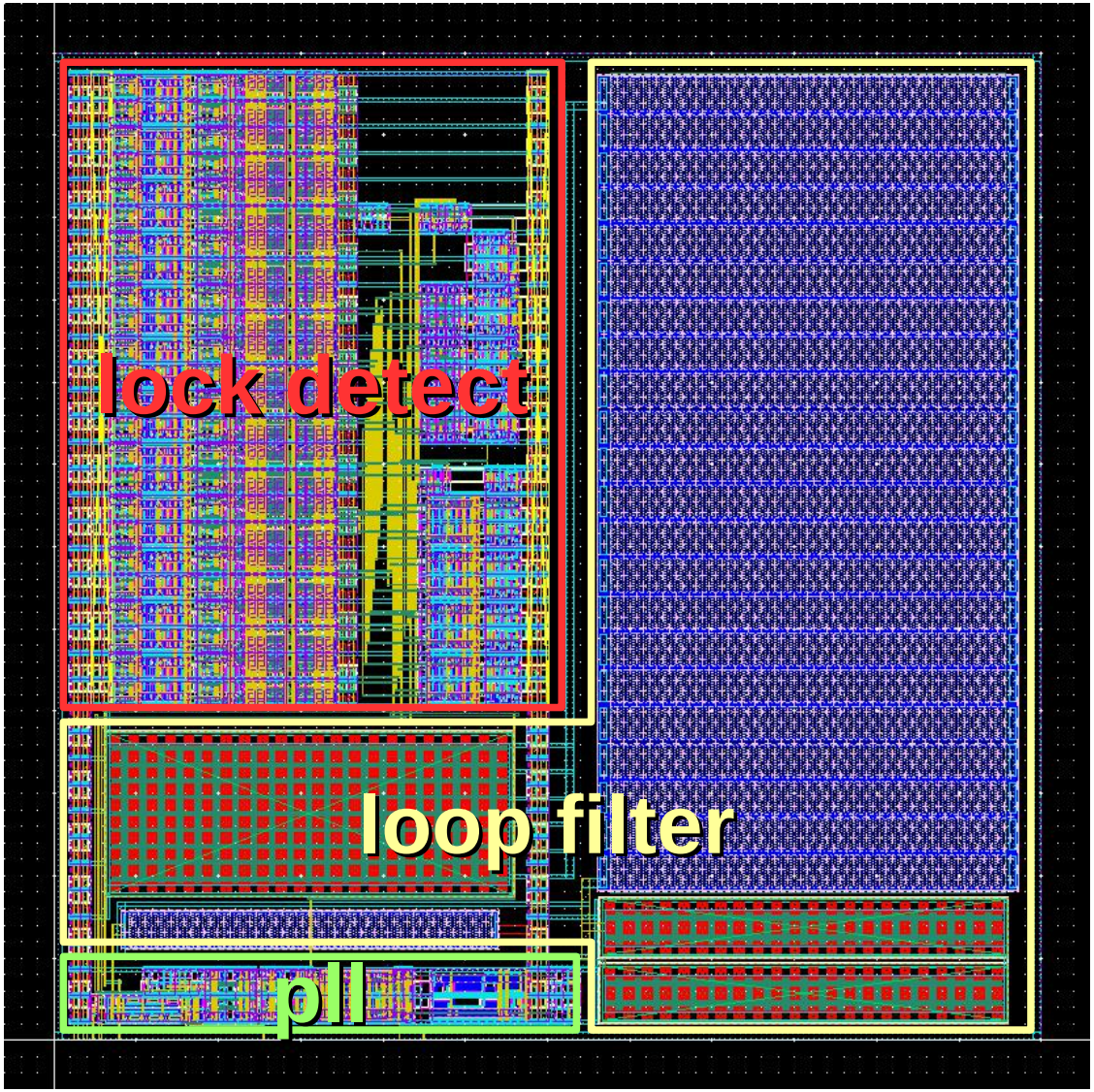
Technology test chip submission

- DMC:
  - v0.1 submitted via miniasic run, 3 subasic's
    - optimized 1:4 PLL for 320MHz generation and digital lock detection
    - io-delay subcircuit for adaption of the different wire length on the module (128 steps)
    - dual port memory for verification of the ip integration flow
    - bond pitch 100µm with 63x60µm standard lib bond pad
    - these miniasic run was already very helpful for establishing the whole tech. dependent design flow (IP integration..



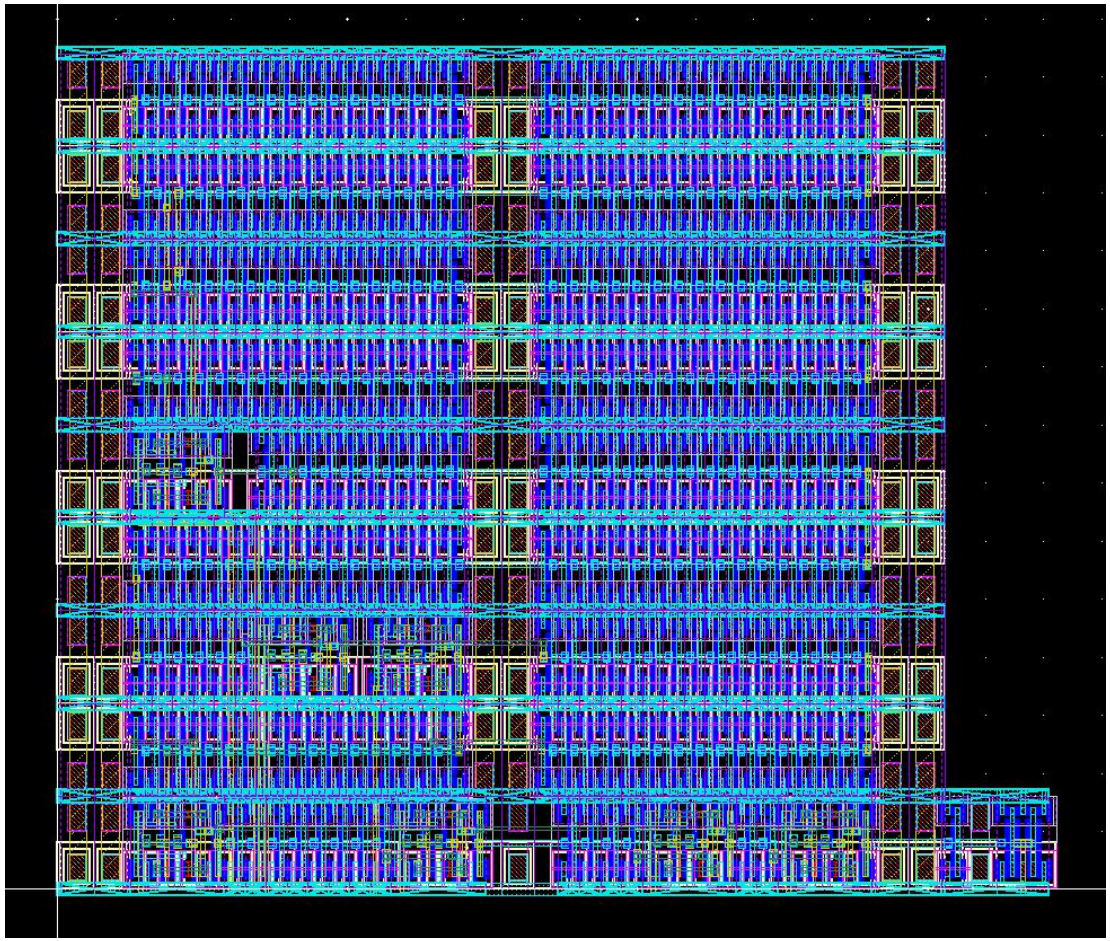
1:4 pll

- 60x60 mm^2
- vco up to 2GHz
- dynamic circuit technique for high speed flipflops in internal clock divider and phase detector
- digital lock detect
- ~2µs lock time (2,5 day for single simulation with extracted parasitic's)



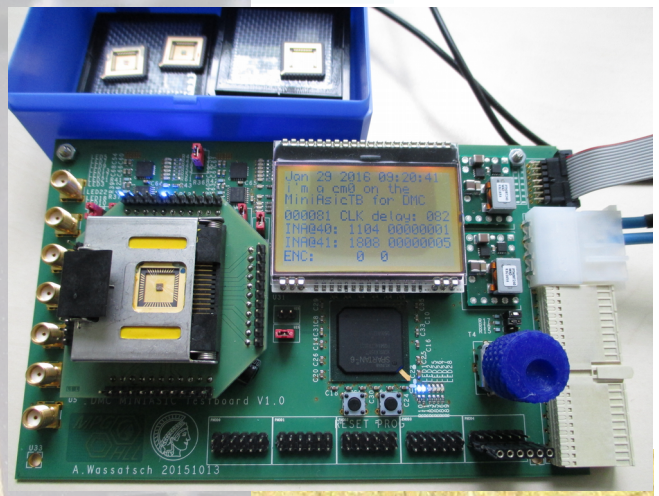
delay7

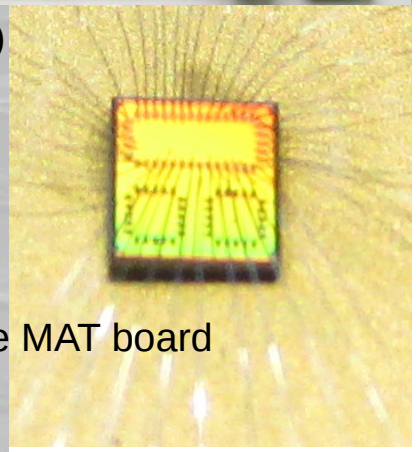
- 128 steps (~65ps)
- signal duty cycle 48-52%
- 30x30µm^2
- integration between core and io padring



DMC MiniAsic test

- Done via the MAT board
- 80→320MHz clk pll working
  - jitter slightly higher as aspected from simulation
  - standard io cells with 320MHz on the edge of the spec
- Delay unit working
  - Width freq range tested, stable delay (range up to 4.2ns in 128 steps)
  - Balanced duty cycle of the output signal
- memory
  - 1k * 4bit dual port configuration tested
  - Working as aspected in the speed range given by the limitations of the MAT board



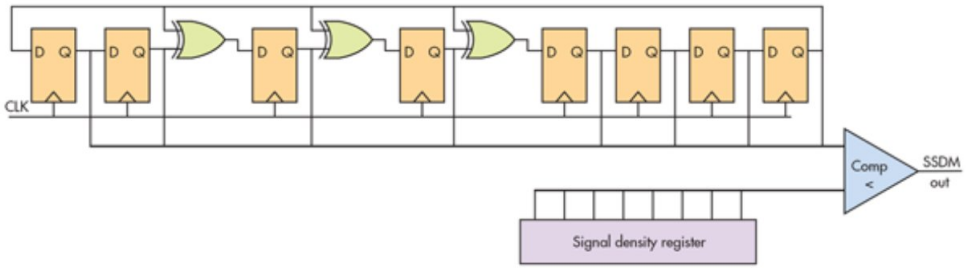


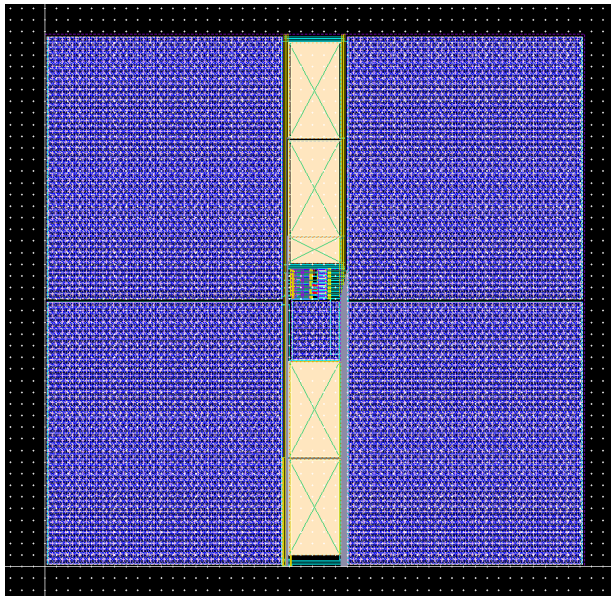
→ all subchips on the DMC miniasic v0.1 are working

→ results of the time consuming parasitic simulation fits in Range >95% to the measurements

design inputs from the DHP tests

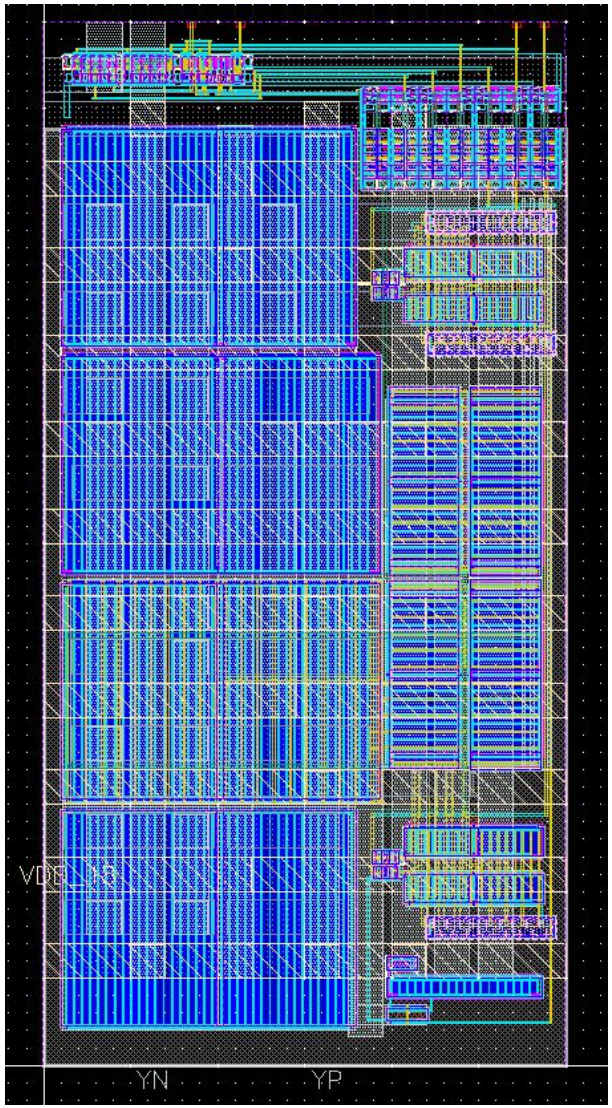
- more but shorter JTAG user chains for improved accessibility of controll regs
- improved low voltage swing io cells for DCD communication with dual mode
  operation (also usable as standard LVDS cell)
  - SSDM based DAC for JTAG controlled adjustment of the DCD common
    mode voltage (230x230µm^2)





current and short term next topic's

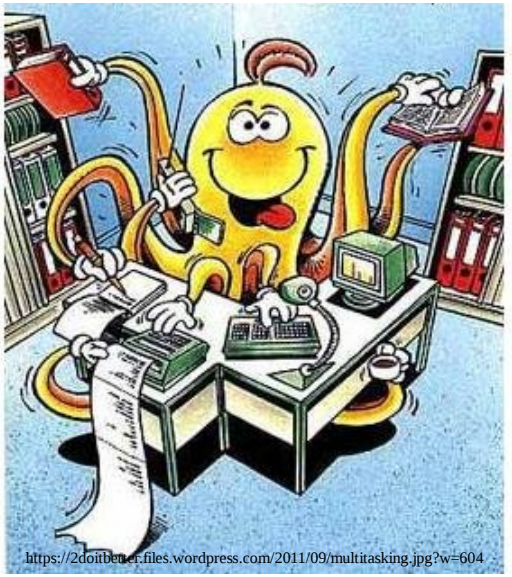
- cell layout of the low voltage swing cells
  - directly attached to the standard analog io cell
  - verification together with the related DCD circuits with full parasitics and line model
- Integration of the LVDS cell into the synthesis flow
- finalization of the DMC VHDL model and system verification



timeline estimate

- „LVDS“ io layout and integration into the „empty“ analog io cells with esd structures (3MW)
  - integration of the custom layout cells into the synthesis flow (characterisation, lef,def-definition) (2-?MW)
- finalization of the digital system and verification against the external models (dcd, switcher, jtag, …) (6-8MW)
- logic synthesis (optimization for speed and power goals) (2-3MW)
- layout synthesis (extensive power and clock verification) (4-6MW)
- final chip assembly (3-4MW)
  - standard io pads for testing in the io ring in parallel to the bump balls
  - full chip drc, lvs and extraction, metal fill , …. (2+...MW)
  - final verification of the extracted circuit (4+...MW)

best case 26MW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Thank you