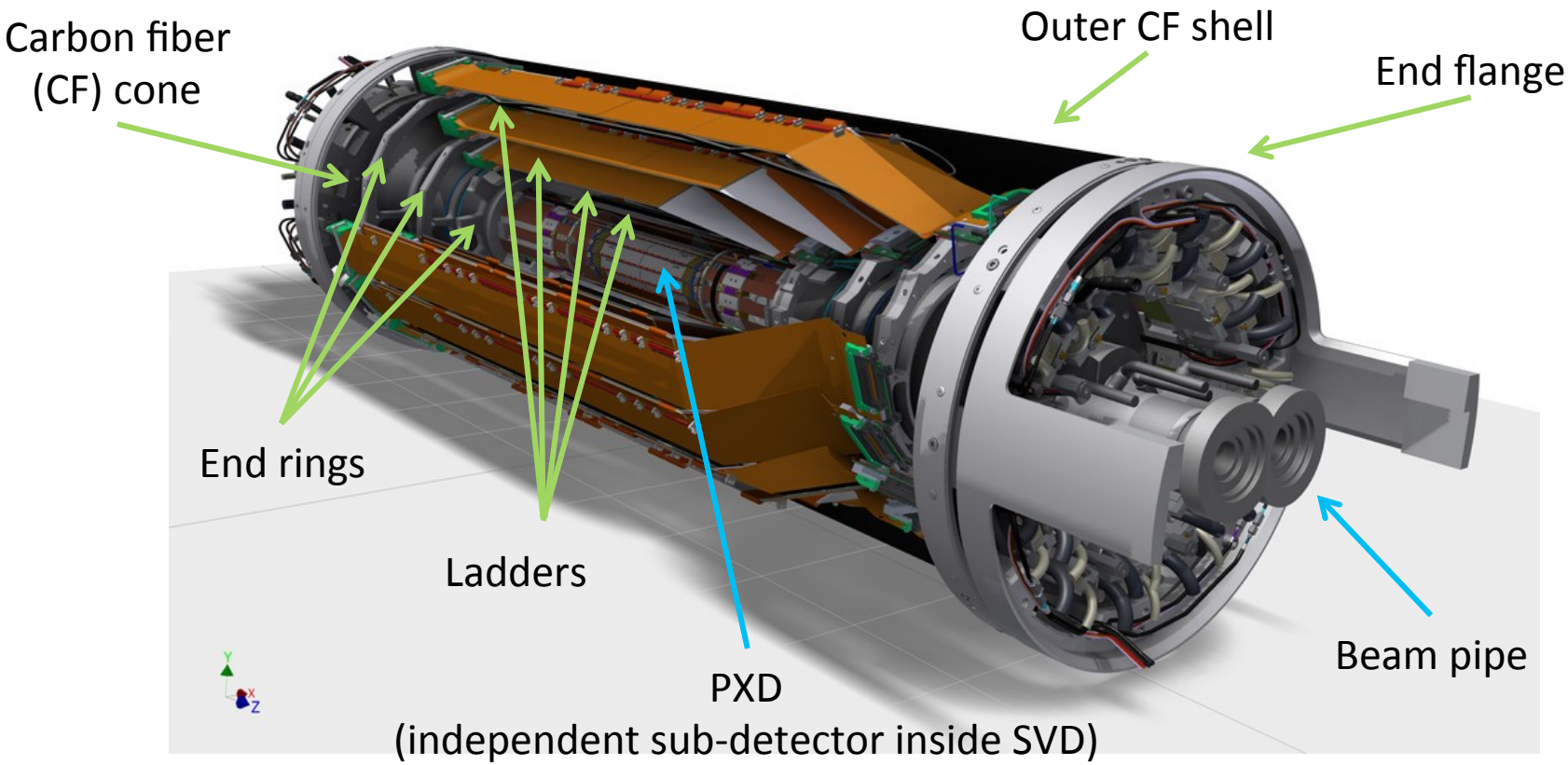
Status of SVD Production
SVD Parallel Summary

Christoph Schwanda (HEPHY Vienna)
For the Belle II SVD group

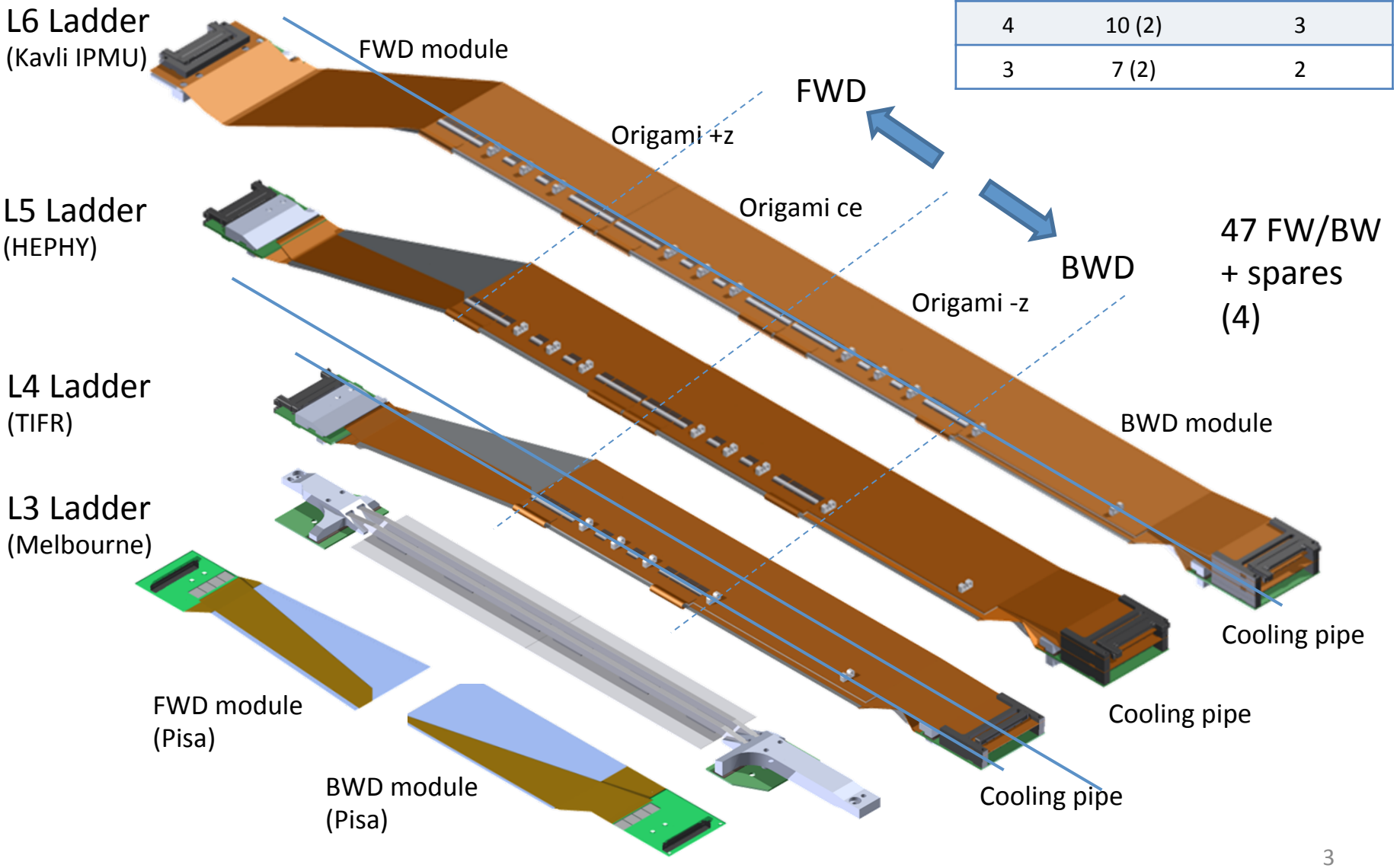
10th VXD Belle II Workshop
September 14-16, 2016, Santander, Spain

Components of the Belle II SVD



SVD ladders

Layer	Ladders (spares)	DSSDs / ladder
6	16 (4)	5
5	12 (3)	4
4	10 (2)	3
3	7 (2)	2

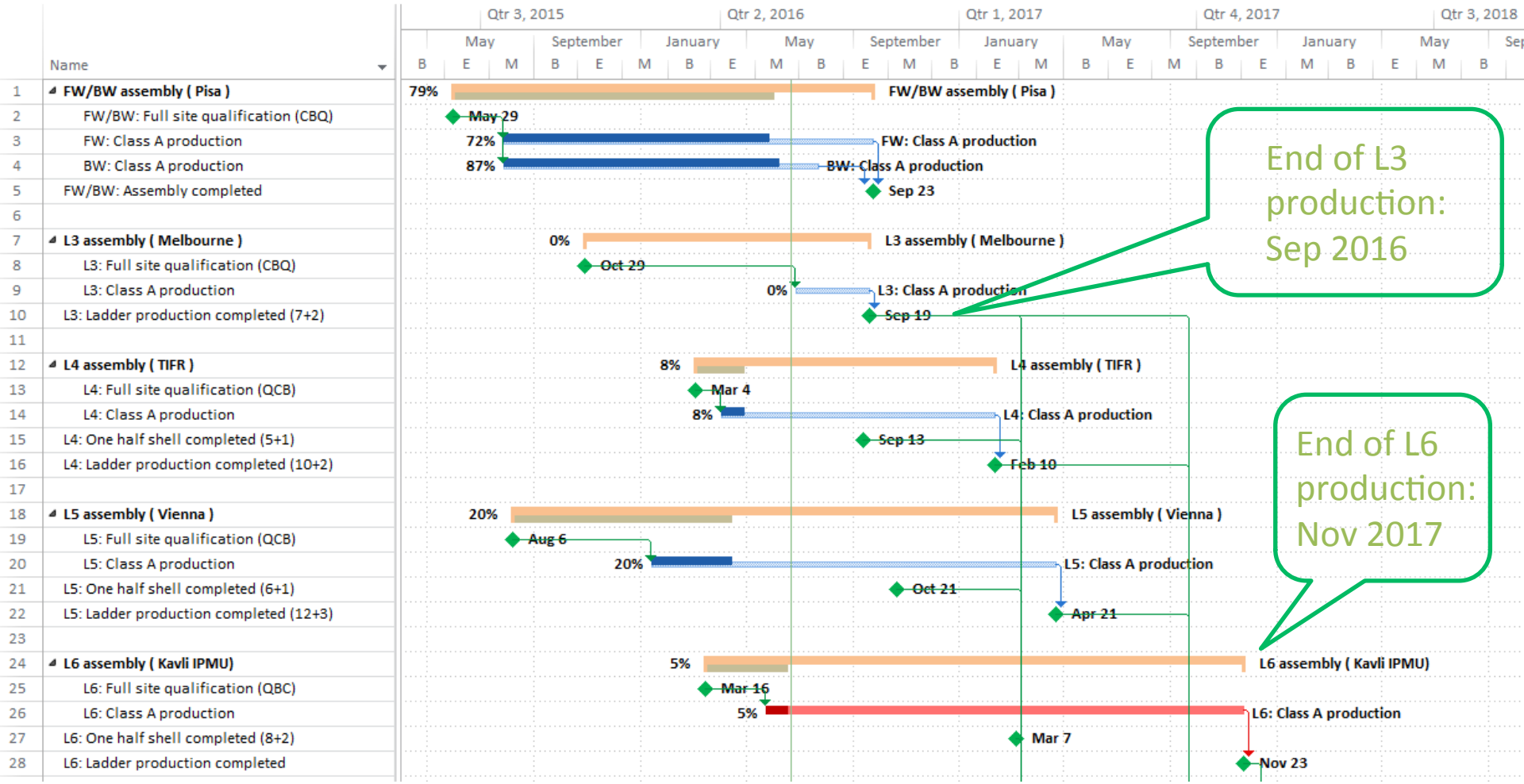


SVD ladder production status (as of September 12, 2016)

- Pisa (FW/BW) 100% (85%*) of the backward (forward) subassemblies completed
- Melbourne (L3) 5 out of 7+2 ladders completed
- TIFR (L4) 3 out of now 10+2 ladders completed
- HEPHY (L5) 4 out of 12+3 ladders completed
- Kavli IPMU (L6) 3 out of 16+4 ladders completed

* as of end of August

Ladder production schedule



To be updated

SVD parallel on Wednesday

Welcome	*Dr. Christoph SCHWANDA*	
Santander	09:30 - 09:35	
Origami status and shipment plans	*Dr. Koji HARA*	
Santander	09:35 - 09:55	
Report from VXD mechanics meeting @ Munich	*Dr. Markus FRIEDL*	
Santander	09:55 - 10:15	
Experience with the open CO2 system @ KEK	*Mr. Katsuro NAKAMURA*	
Santander	10:15 - 10:30	

Reports

SVD slow control and network configuration	*Mr. Christian IRMLER*	
Santander	11:00 - 11:20	
FADC slow/run control software	*Mr. Hao YIN*	
Santander	11:20 - 11:35	
Monitors -- slow control integration, interlocks	*Prof. Livio LANCERI*	
Santander	11:35 - 11:50	
SVD network layout, cable routing	*Mr. Katsuro NAKAMURA*	
Santander	11:50 - 12:05	
Discussion about SVD slow control (definition of the system, layout, responsabilities, schedule)		
Santander	12:05 - 12:45	

SVD SC discussion

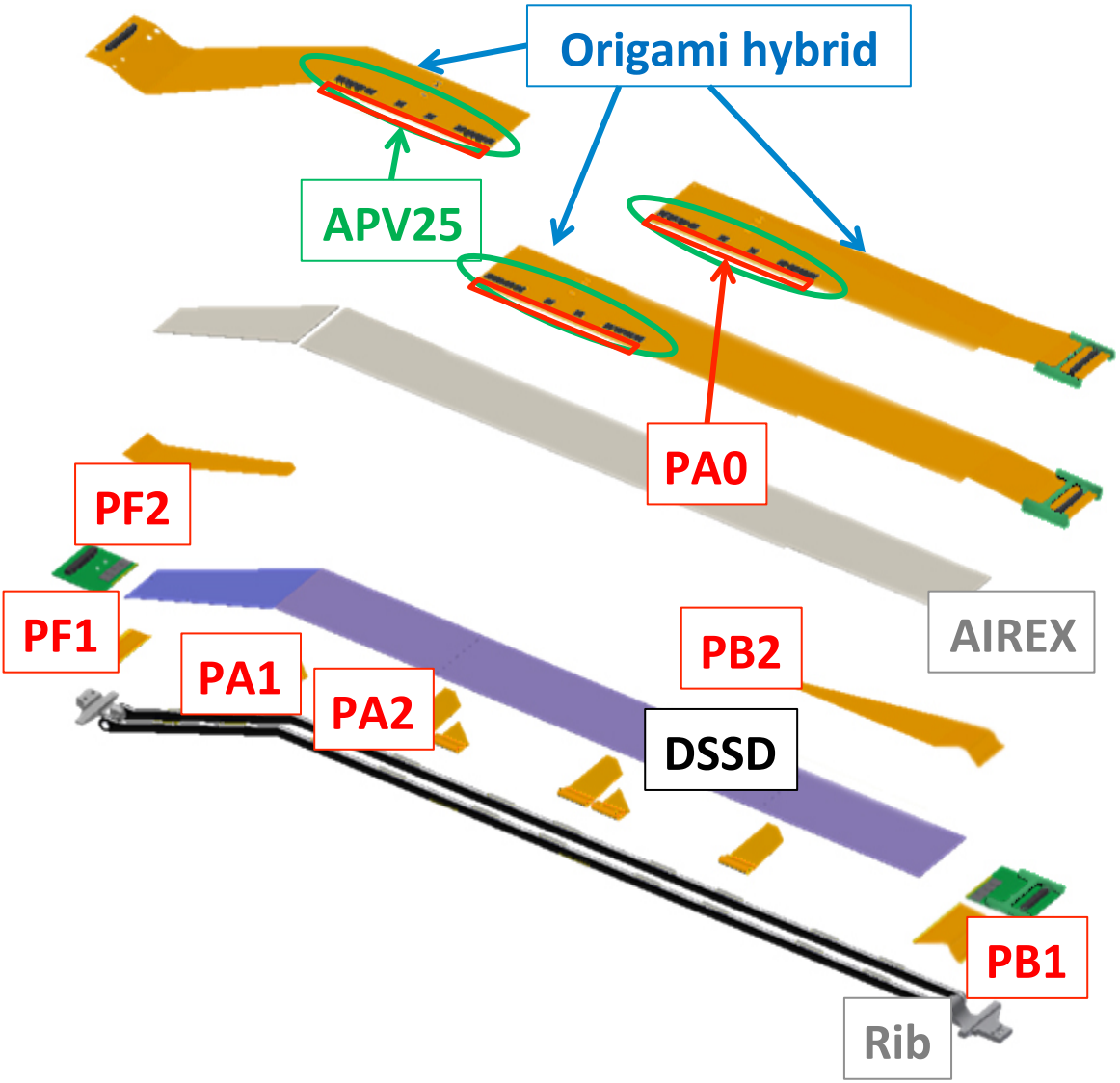
FADC hardware/firmware status	*Richard THALMEIER*	
Santander	14:30 - 14:50	
CAEN PS interface, patch pannel requirements	*Francesco FORTI*	
Santander	14:50 - 15:05	
SVD DAQ status	*Mr. Katsuro NAKAMURA*	
Santander	15:05 - 15:20	
Discussion on SVD DAQ integration (system layout, responsabilites, schedule)		
Santander	15:20 - 16:00	

SVD DAQ discussion

SVD/VXD alignment status	*Jakub KANDRA*	
Santander	16:30 - 16:50	
Two side clusters correlaton	*Andrzej BOZEK*	
Santander	16:50 - 17:10	

SVD software

Ladder Anatomy (L6 ladder)



DSSDs
- 2 small rectangular (L3)
- 2-4 large rectangular (L4-6)
- 1 trapezoidal (L4-6)

Origami hybrid
Flexible circuit to transmit detector signals to the ladder ends

APV25
Readout ASIC of the strips

FlexPA (PA/PF/PB)
Flexible circuit to transmit detector signals to the APV25

PA0
Flexible circuit glued on the Origami hybrid to transmit *n*-side detector signals to the APV25

AIREX
Thermal insulator between the DSSD and APV25

Koji Hara

Origami Status

- 80 assembled, inspected so far
  - 30 O-Z : 25 class A, 5 e-test fail
  - 27 OCE : 22* class A, 4 e-test fail, 1 e-test fail but repaired
    * include 12 OCEs with APV3 ch0 noise ~ 2
  - 23 O+Z : 18 class A, 3 e-test fail, 2 OK but minor issue**
    ** 1 wires bent, 1 soldering to be reworked
- 63 will be assembled with new DISCO thinned chips + chips thinned as a whole wafer
  - 36 O-Z
  - 22 OCE
  - 5 O+Z

Koji Hara

Electrical failures in assembled Origami

- Whole analog dead (all 128 chs are bad) : 6.3% (5/80)
  - O-Z130 APV6 (N0), no crack, LV normal
  - O+Z118 APV9 (N3), crack observed, LV low cur.
  - OCE122 APV3 (P3), crack observed, LV low cur.
  - OCE123 APV6 (N0), power OK on chip, LV normal
  - O-Z107 APV5 (P5), discon. at soldered pad, LV low cur.
- A part of chs dead : 10.0% (8/80) (1 repaired)
  - O-Z 3/30 before|after our inspection: 2/17 | 1/13
  - OCE 3/27 before|after our inspection: 3/15 | 0/12
  - O+Z 2/23 before|after our inspection: 0/8 | 2/15
  - Total 8/80 before|after our inspection: 5/40| 3/40
- Short on PA0 (1 on each)
  - O-Z 4 (117,121,123,146) → to be assembled

Expected Origami readiness at KEK

Koji Hara

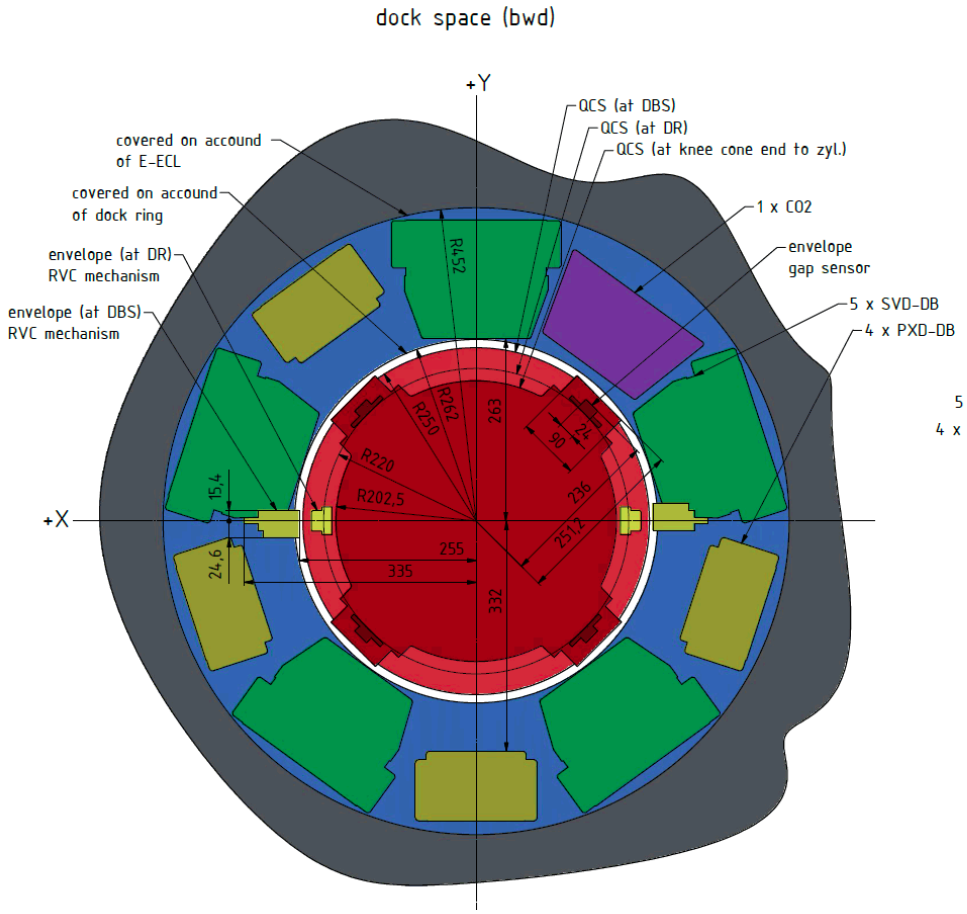
week		O+Z ready@KEK	OCE ready@KEK	O-Z ready@KEK
2016/9/5		18 (3 shipped)	22 (8 shipped)	25 (12 shipped)
2016/9/12	VXD workshop			
2016/9/19	"Silver week"			
2016/9/26				
2016/10/3				
2016/10/10				
2016/10/17	B2GM			+13
2016/10/24				
2016/10/31			+10	
2016/11/7				
2016/11/14				+12
2016/11/21				
2016/11/28				+11
2016/12/5				
2016/12/12				
2016/12/19		+4 +1	+11 +1	
2016/12/26				
2017/1/2	New Year			
2017/1/9				

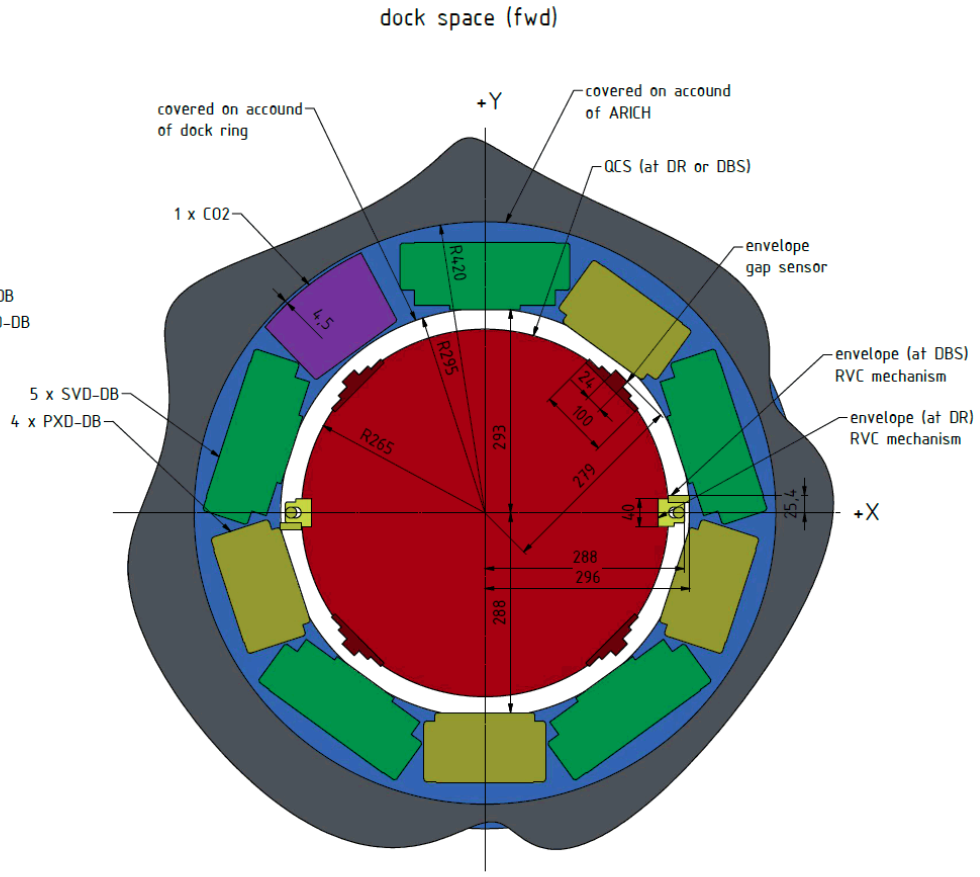
Numbers in future are before acceptance inspection at KEK
Assumed to resume APV gluing on Sep. 26

Markus Friedl

Space Around DOCK

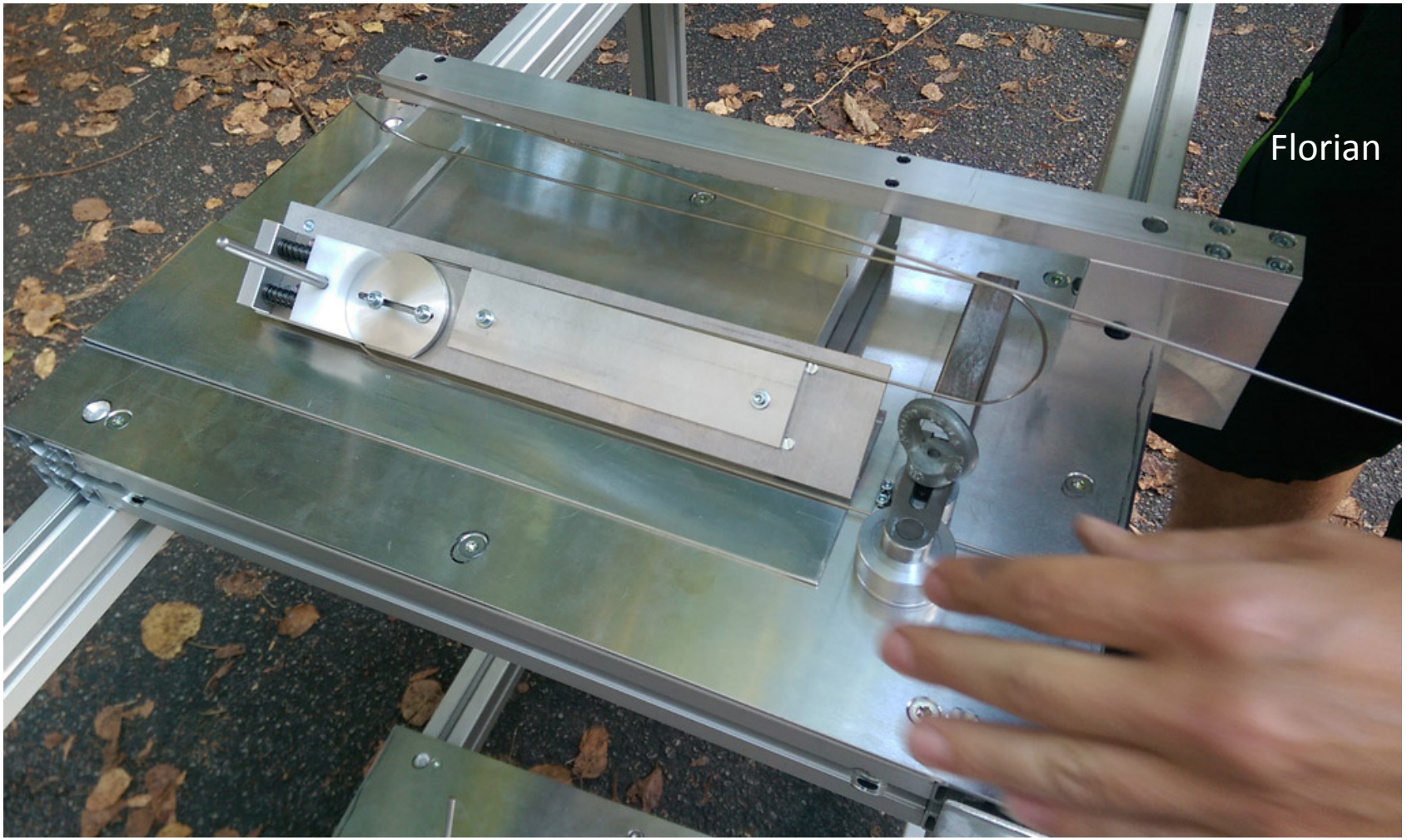
- Latest Drawing by Tscharlie





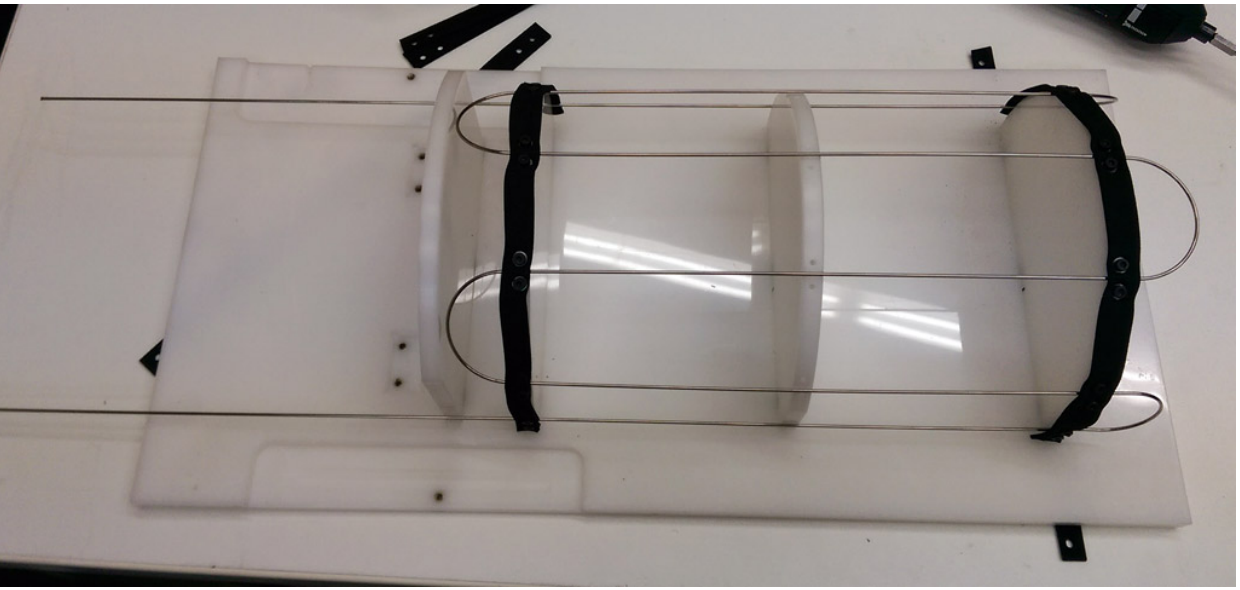
Markus Friedl

L4 Origami Pipe 3D Bending



Markus Friedl

Result



- Left: after 3D bending
- Right: after inlet/outlet bending (manual) and cutting
  - Needs more practicing…

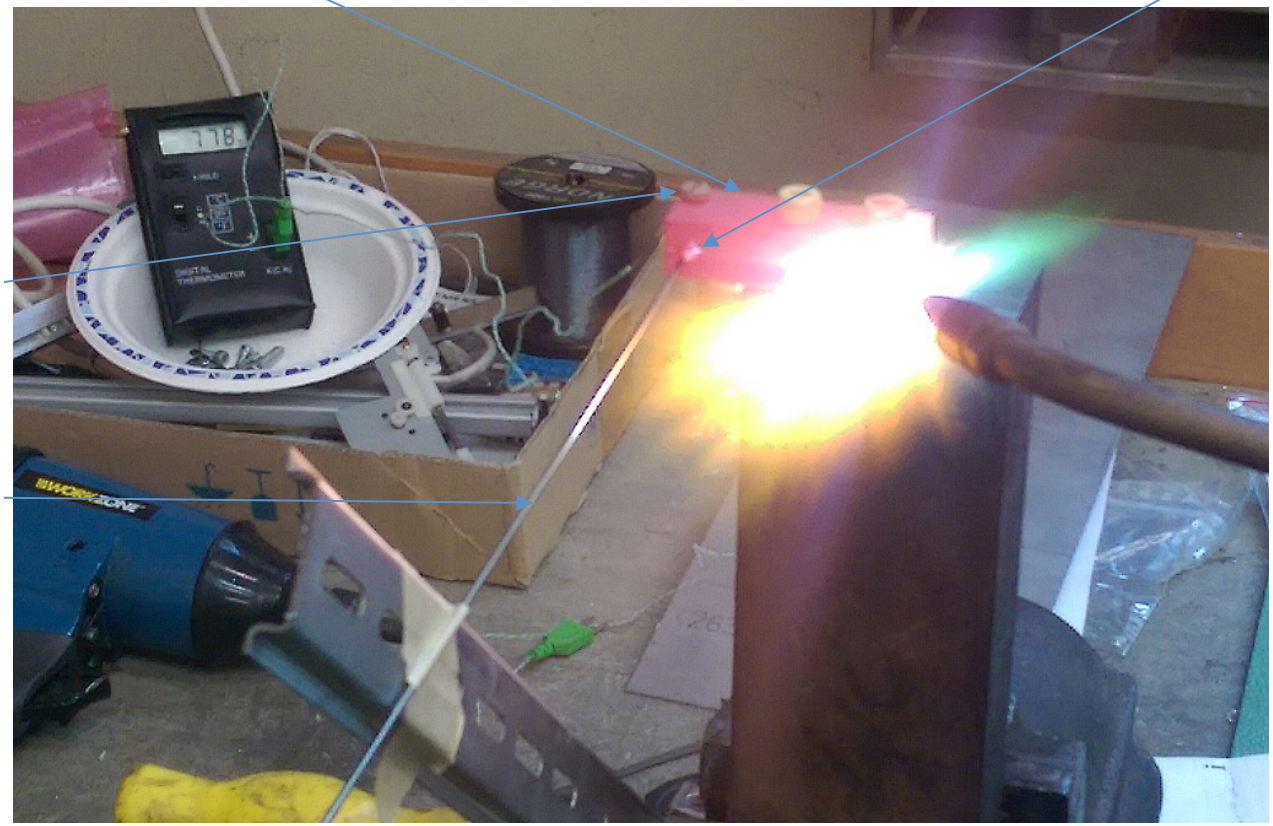
Markus Friedl

Preparation Test for Brazing

- We can achieve homogeneous heat for (dummy) Streuli using a copper block and acetylene/oxygen burner

778°C measured here

Pipe



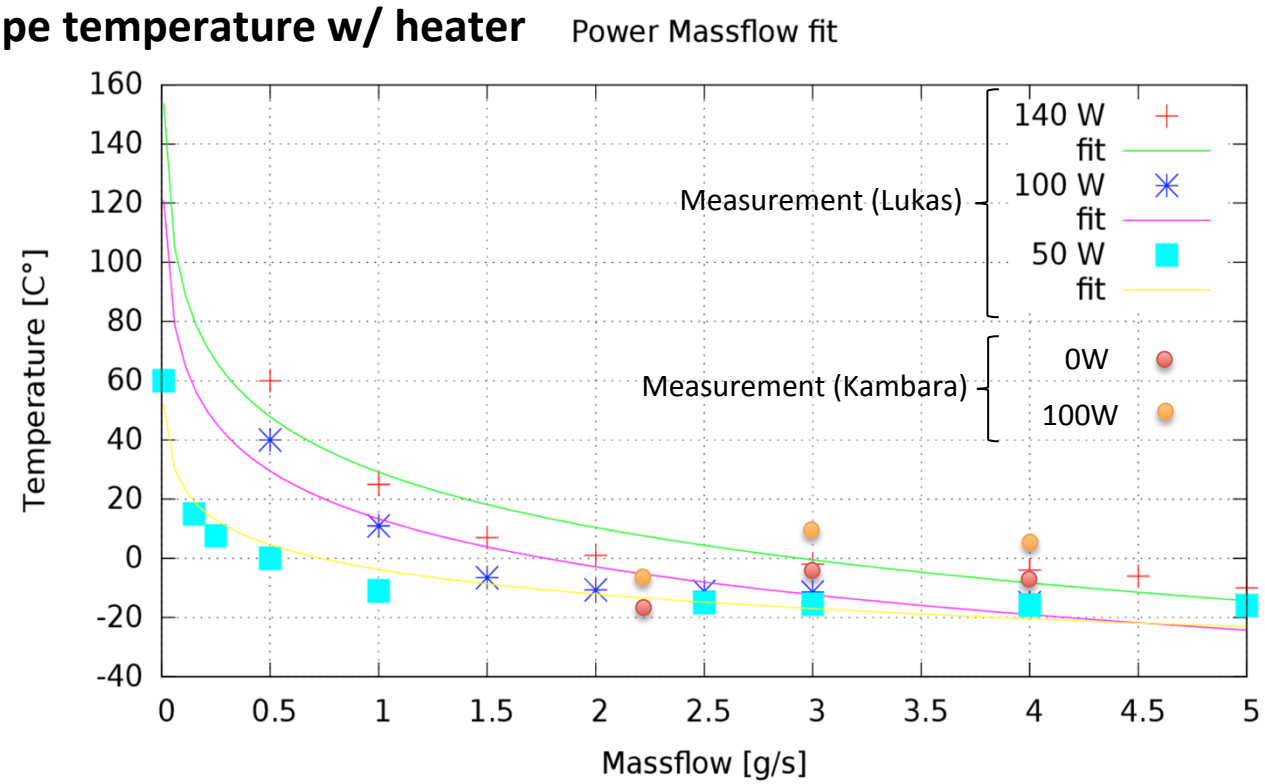
Katsuro Nakamura

CO2 cooling system setup at KEK B1

- From 1 CO2 bottle, about 20kg CO2 is available for the CO2 system
  - (actual amount of CO2 inside the bottle is 30kg).
- Currently, once one CO2 bottle gets empty, we have to switch off the CO2 cooling system, connect to another bottle, and then restart the CO2 system.
- In future, we will implement switching valves, which enable us continuous switching the bottles without stop of the system.

Katsuro Nakamura

Comparison the results with before shipment

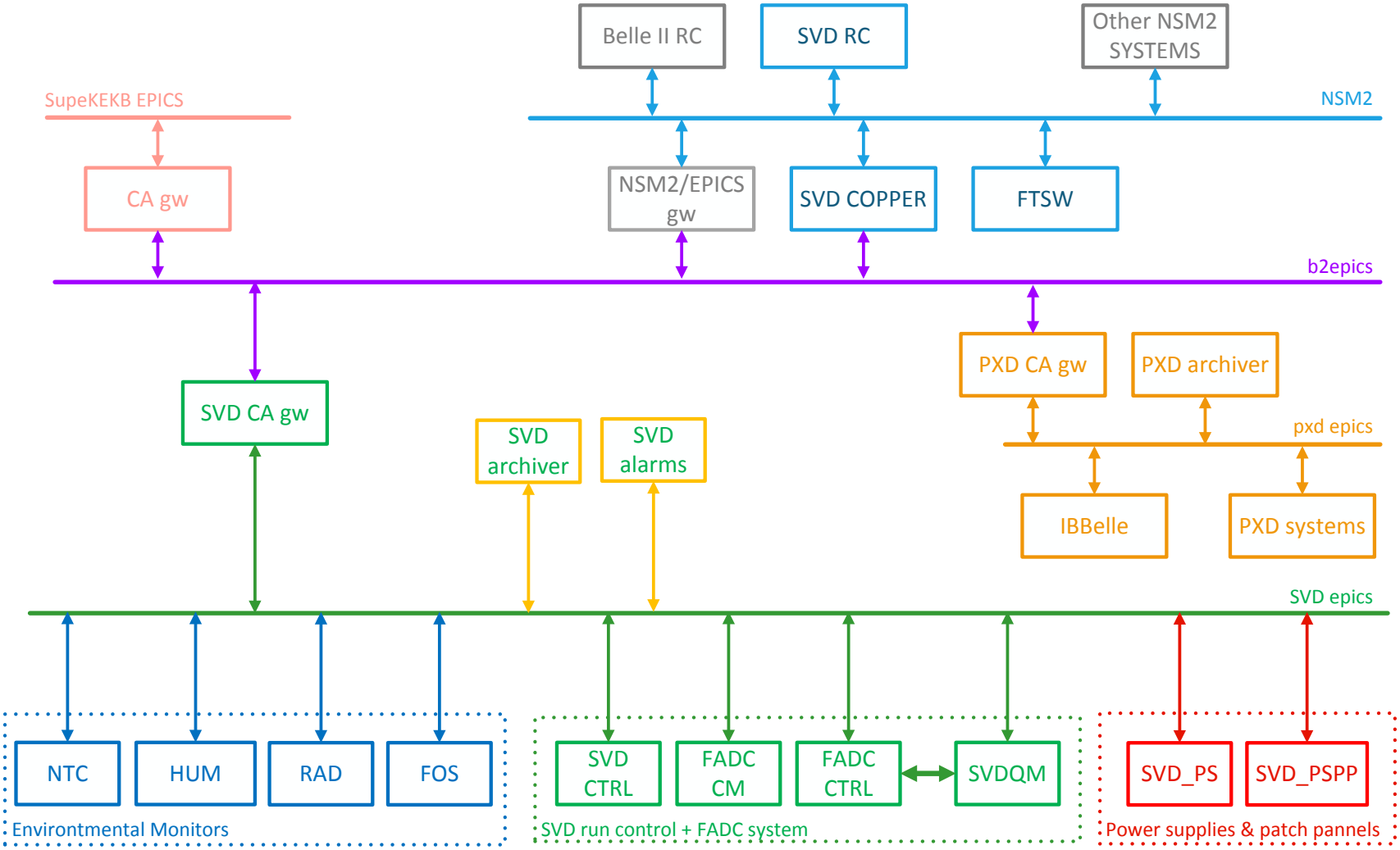


- Results in 2.2 g/s shows good consistency with Lukas's measurement and a enough cooling power for 100W load.
- But, Results in 3 g/s and 4 g/s are higher temperature than Lukas's measurement and our 2.2 g/s result.
  - They looks inconsistent with our 2.2 g/s result.

SVD SC

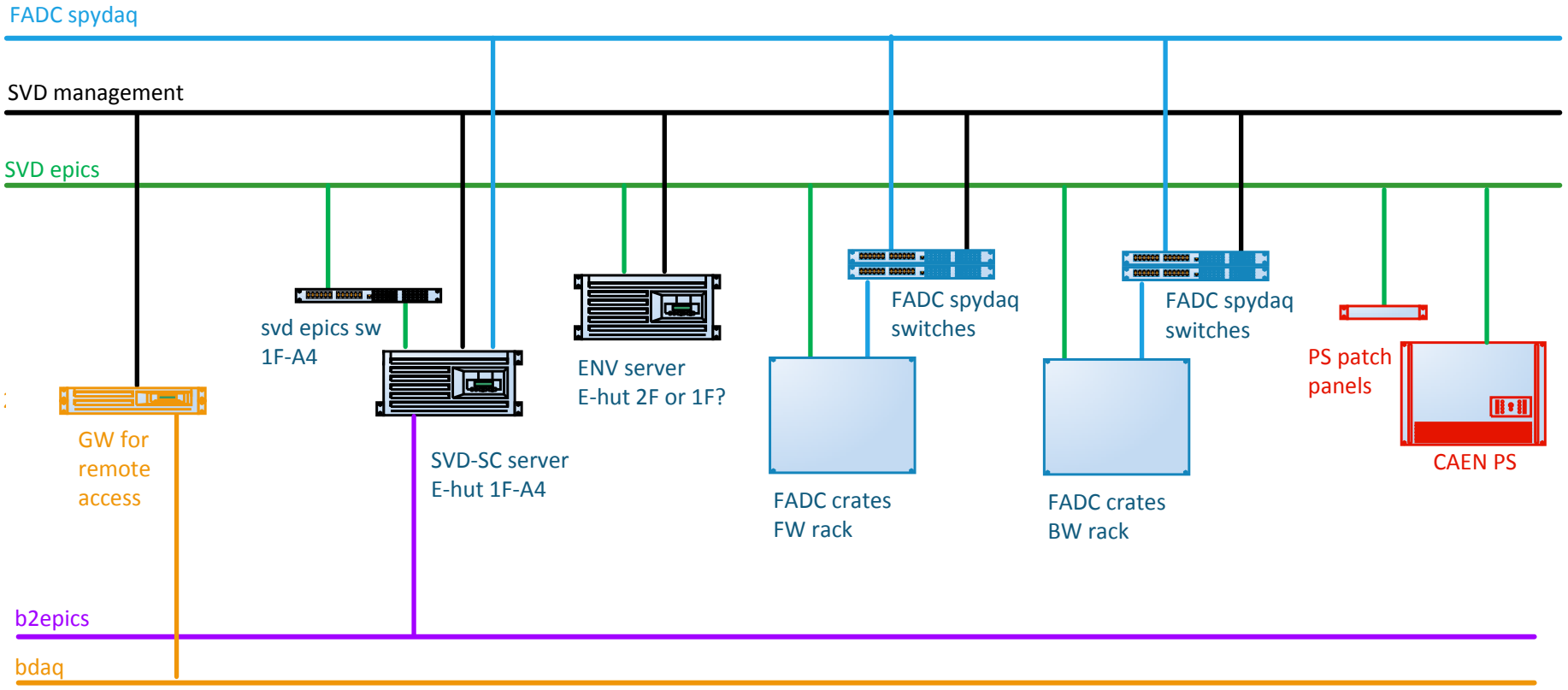
Christian Irmler

SVD Slow Control System Overview



Christian Irmler

Network Configuration (Draft)



- First draft, assuming that IOCs are distributed among 2 servers
  - One for FADC related IOCs and a second for the rest (PS, environment, etc.)
- To be discussed
- Remote connection to our machines via bdaq and access gateway

Christian Irmler

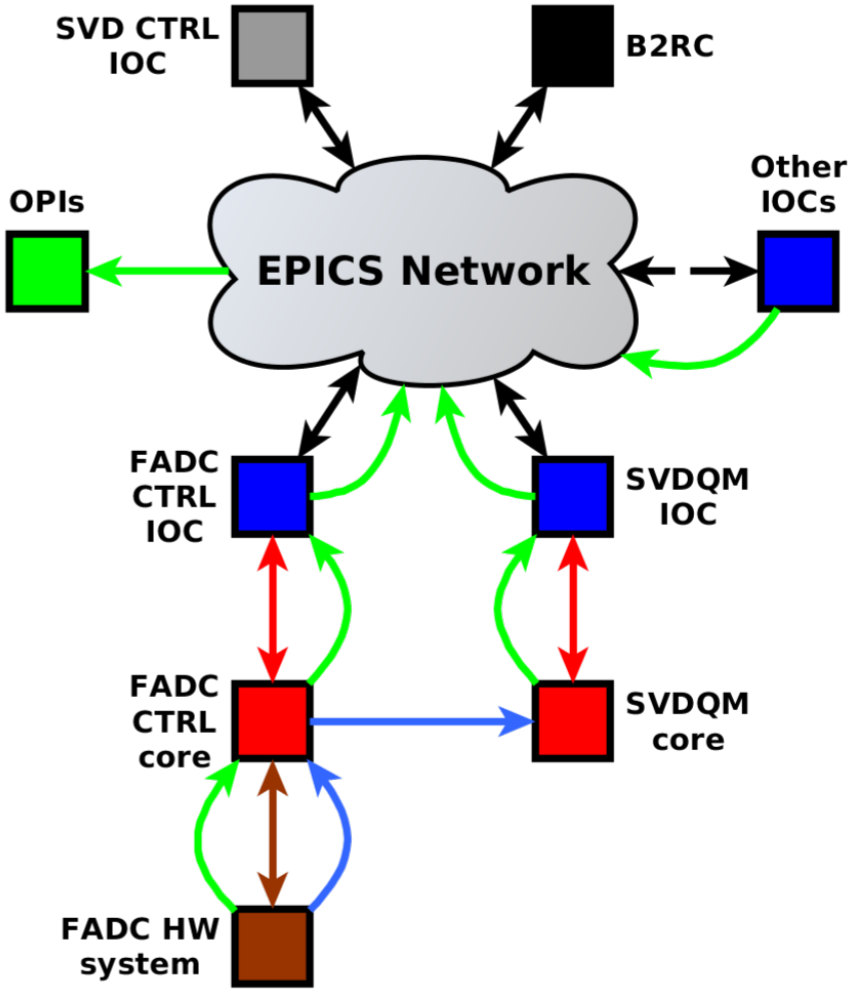
Poorly Covered Tasks

- The following tasks and subsystems are not or just poorly covered
- FOS
  - Same system as PXD, but can we also share IOC?
  - Suppose we can use same IOC, but should run on SVD server
  - Need to implement SVD specific CSS
- Coordination of SC activities → SC group management
  - So far, partly done by myself
  - Will be busy with L5 assembly until summer 2017
- Databases, archiver, gateways, system and network architecture

Overview

SVD slow control

Hao Yin



- **OPI/CSS:** Presents data from the epics network to the user.
- **Epics Net.:** Contains data from all connected IOCs.
- **Epics IOC:** Provides/broadcasts data for the epics network (PVs).
- **C++ Interfaces:** Provides IOCs with updates and processes the given request.

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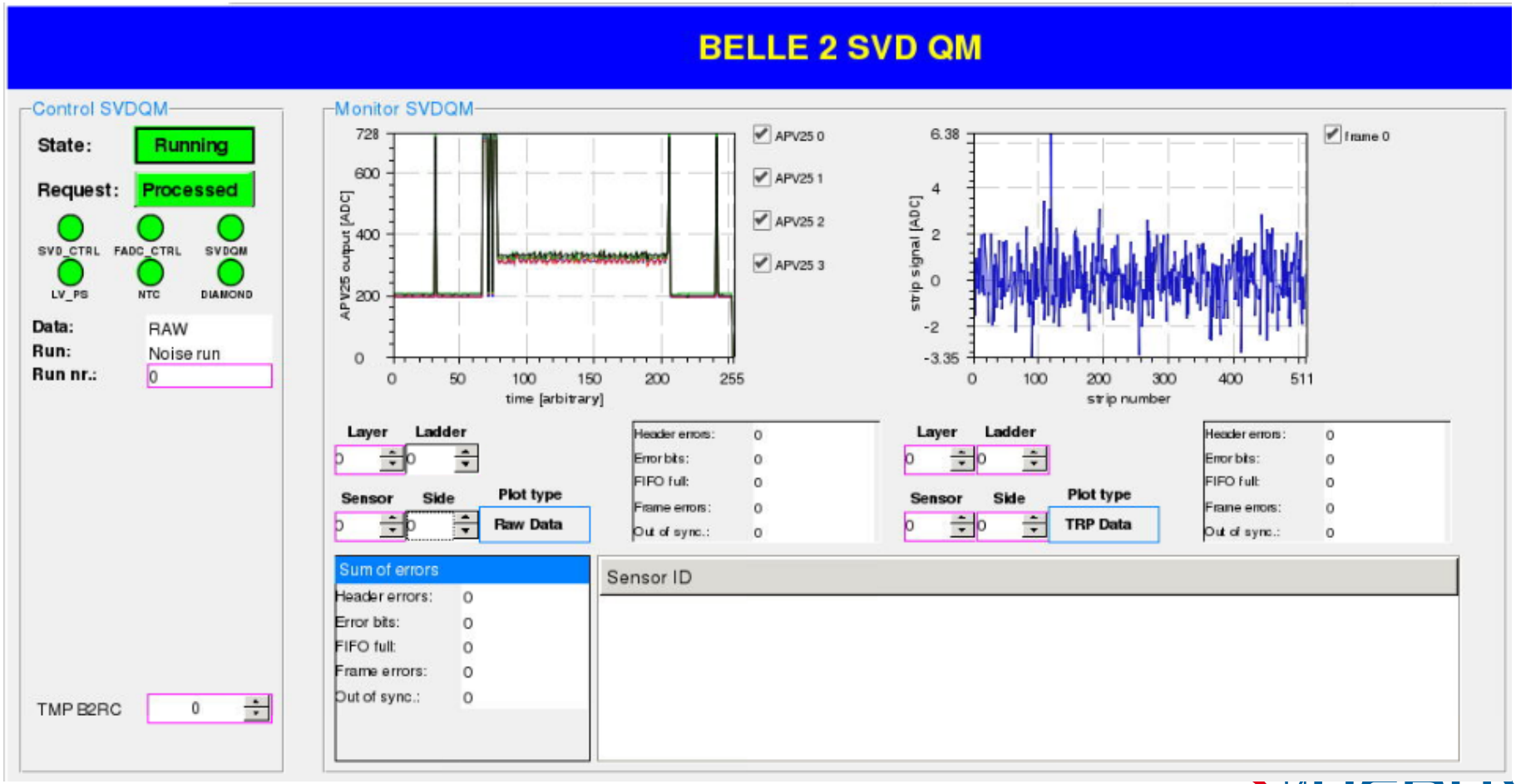
OPI - Preliminary buld!

SVDQM

Hao Yin



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Todos and time line

Hao Yin

Last B2GM:

- Debugging the DESY build (**on going...**)
- Refactoring the DESY build (**end of August**)
  - Core implementation of SVD QM (80% finished, 1-2 week)
  - Core implementation of FADC CTRL
  - Adapting SNL codes.
- Updating / rewriting OPIs (**end of September, mid October**)
- Forwarding warning and error msg to Belle II RC. Internal interface is already implemented. (If there is an interface on Belle II RC side, few days...)
- Configuration databases (**unknown need discussion**)

Current state

- **Finished** debugging DESY build.
- **Finished** refectoring C++ implementations, few minor tweak left (configuration)...
- **Finished** msg logging to CSS, using the C++ implementation provided by M. Ritzert.
- Implementing BOY widget for specific tasks needed by SVDQM and FADC CTRL OPI (**ongoing, end of october**).
- Move local file bases configurations to database (**not started yet**).
- Implement alarm system, need responsibility definition between Slow Control and Belle II DAQ. (**not yet started**)

A discussion important point: What kinds of plots do you expect to see on SVDQM (shifter and/or expert interface)?

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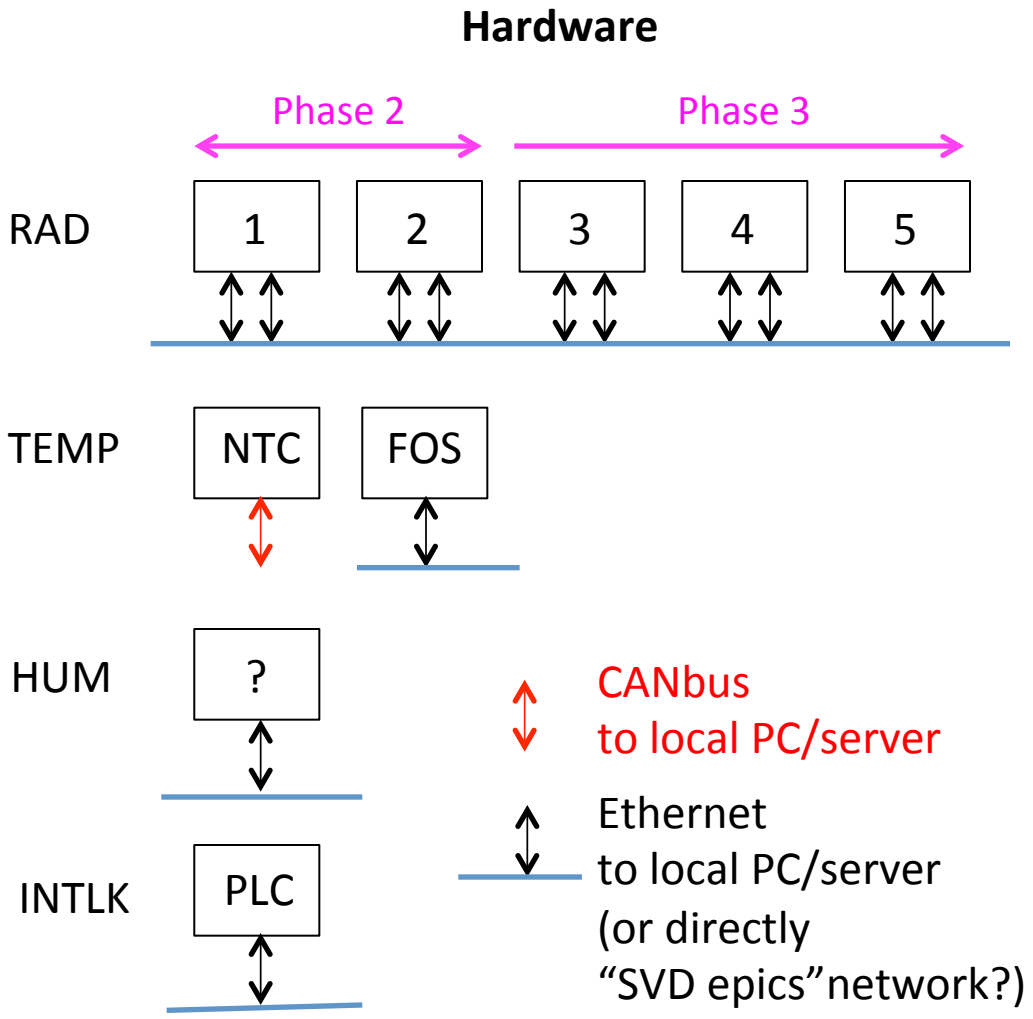
Mon./Intlk. Integration in Slow Control

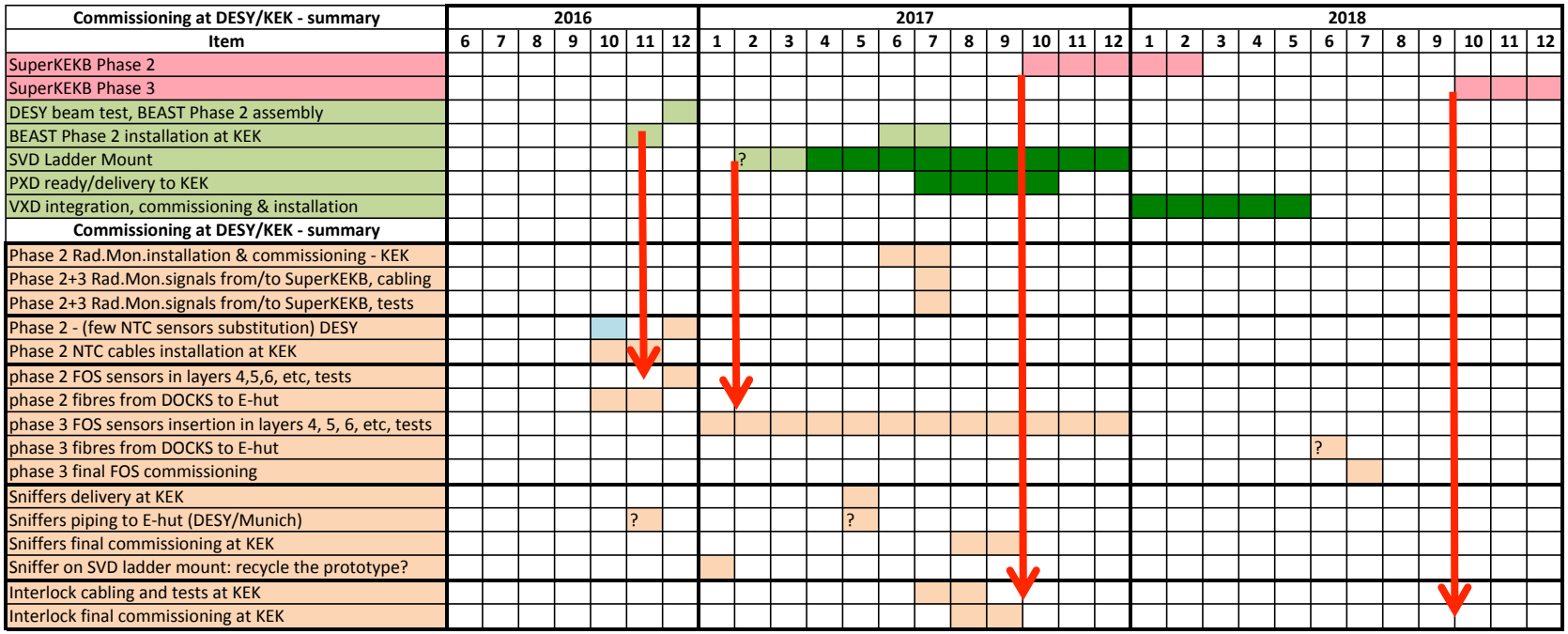
Livio Lanceri



	Software IOC	Manpower	Schedule
RAD	not yet	S.B. + …	1st sem. 2017
TEMP	Yes prototypes	S.B. + …	"now"
HUM	not yet	S.B. + …	1st sem. 2017
INTLK	Yes test	S.B. + …	"now"

Summary of commissioning at KEK

Livio Lanceri



Lab activities at INFN Trieste
Installation and commissioning at DESY or KEK

Driving deadlines:

2016, November, DESY Beam Test & Phase 2 VXD Assembly

2017, February, beginning of SVD Ladder Mount

2017, October, beginning of Phase 2

2018, October, beginning of Phase 3

Ideal presence at KEK in 2017

Livio Lanceri

settim.tot.	Nome	1				2				3				4				5				6				7				8				9				10				11				12			
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48
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4	Giuressi (Elettra)																											2	3								3	3											
102																																																	
21	B2GM + BPAC																							?	?														?	?										
22	VXD workshop			?																																?												
23	Physics, computing workshops																						?															?											

First rough exercise on the ideally required presence from Trieste at KEK in 2017
(see list of activities and their ID numbers in the next slide)

Our INFN travel budget (under discussion) will probably cover about 50% of this
We will have to identify the most critical periods and contributions
(Sensor testing periods during installation, for instance)

Comment

- I think we need a broader discussion to finalize the interlocks
- Maybe we can foresee time for this at the October B2GM

SVD DAQ

FADC System

Radiation: ~ 10 Mrad, Magnet.: 1.6T

Front-end hybrids with 1748x APV25-chips, 128 analog channels each, on 172 sensors.

~2.5m copper cable

8x Junction boxes with rad-hard DC/DC-converters

copper cables, ~13m, time multiplexed analog voltages

48x FADC in 4 crates.

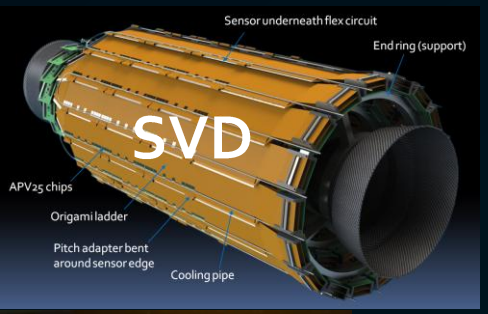
48x FTB

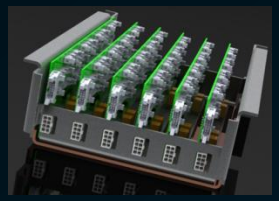
48x Optical data Links (>20m)

Data Acquisition (DAQ)

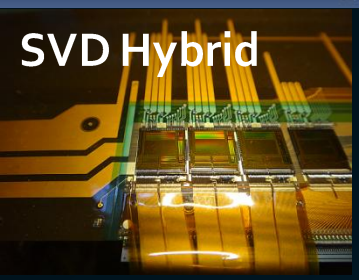
Power Supplies

Pixel Detector (DATCON)

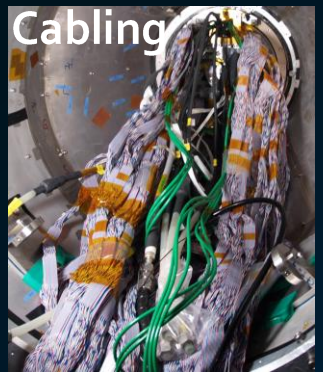




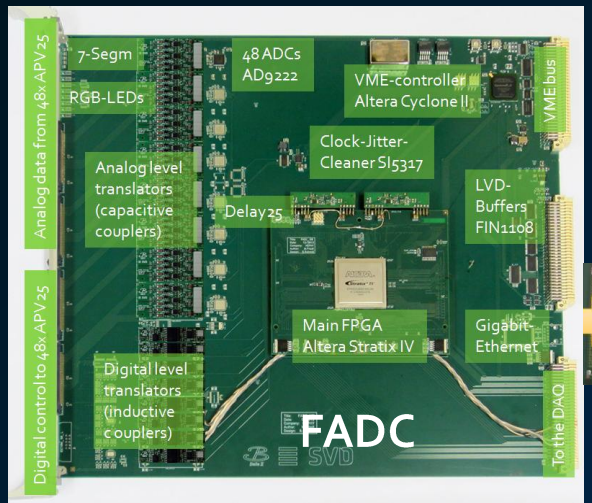
Junction Box



SVD Hybrid



Cabling



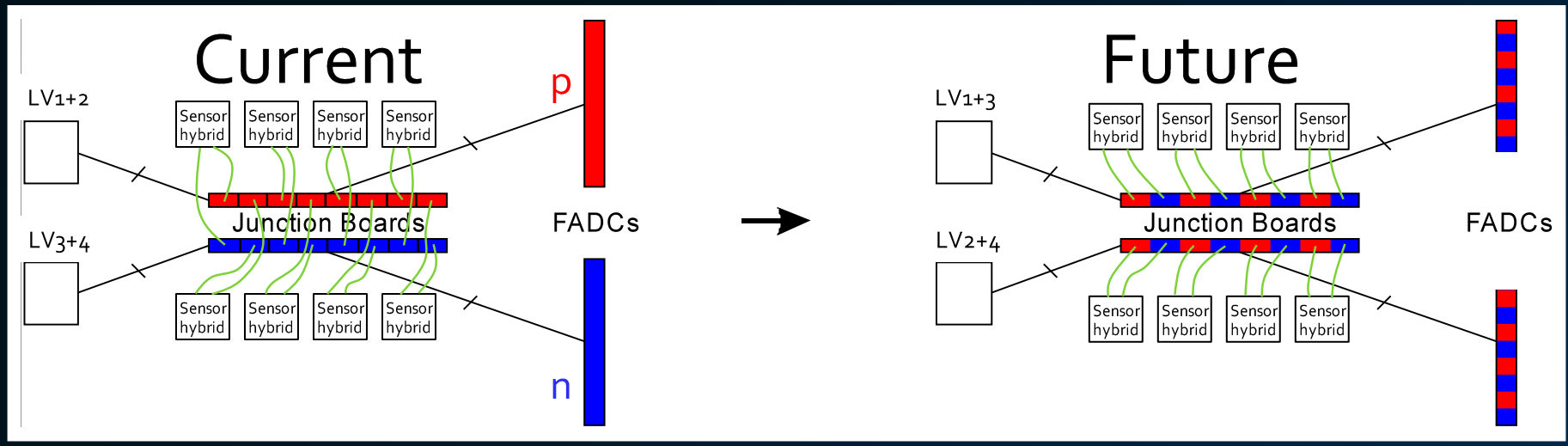
FTB

COPPER

DATCON

Realization

- Use only one LV cable for p and n, and connect it to one Dock Box PCB, which has 24 p and 24 n on-board. So, one sensor is connected to only one Dock-Box-PCB, not to two of them. Each Dock-Box-PCB is connected to only one FADC, not to two or more. Each FADC then also has 24 n and 24 p inputs.
  - Implies redesign of the Dock Box PCBs, changes to the FADCs (HV islands, V/I-measurement, DC/DC-Control), and HV/SepV-Cabling
  - No more loops due to individual cables to power supplies, FADCs, etc…
  - No more distinguishing between p and n PCBs (Dock Box, FADCs)



Schedule

- July to August 2015: Schematics V3 by Hephy — Done
- End of December 2015: Schematics P-Cad→Mentor by a company, Verification by Hephy, and Layout V3 by a company — Done
- Mid of February 2016: Manufacturing and Equipment of 2 PCBs V3 by the company; FADC Firmware migration to V3 by Hephy — Done
- February / March 2016: Testing and Debugging of V3 by Hephy — Done
- April 2016: **Beam test at DESY using V3**; — Done
- May to October 2016: Development of V4 hardware schematics (FADC, Junction_board), remaining Firmware (Cyclone with Stratix-Flasher, Gigabit, HitTime-finding, etc…) (and VXD workshop, TWEPP, B2GM, ~~PhD-work~~, ~~Vacation~~ Vacation, …) — WiP
- November: FADC V4 Layout, probably by company, maybe by Hephy? — ToDo
- December: DESY testbeam using FADC V3 (Long-Term-test)
- January 2017: Production of V4 FADC & Junction_board prototypes
- March 2017: Tests of V4 at Hephy, DESY testbeam using FADC V4 (Long-Term-test)
- April 2017: Decision which way to go: V3 or V4 way.
- May to July 2017: **"Mass production" (58 pcs) of V4.1** including Optical and Electrical testing by the company; In-System-Test at Hephy
- All the other components (FADC Controllers, Buffer Boards, Dock Boxes, VME-Backplanes, cables, etc…) are being built in parallel at Hephy.

CAEN Boards: all delivered

Note: all channels are fully floating, but the polarity is defined by wiring

A2519A LV Board 5-15V/10A; 8 ch/board; 12 boards + 3 spares

A1519B HV Board 250V/1mA; 12 ch/board; 4 boards + 1 spare

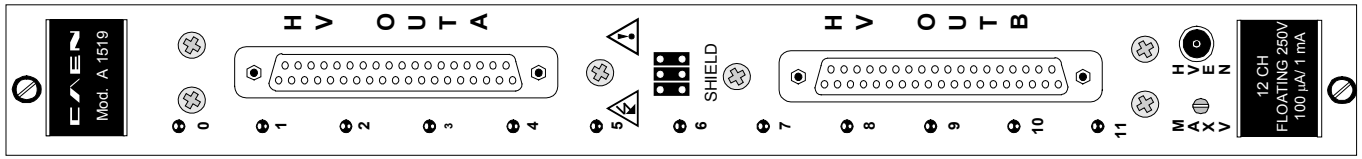


Fig. 1.1 - Mod. A 1519B front panel

A1510 VSEP Board 100V/10mA; 12 ch/board; 4 boards + 1 spare

One problematic board replaced by CAEN under warranty

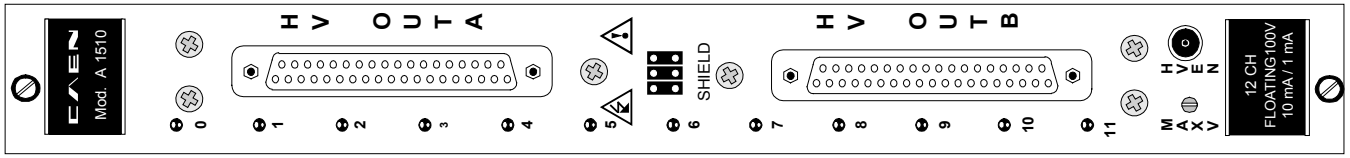
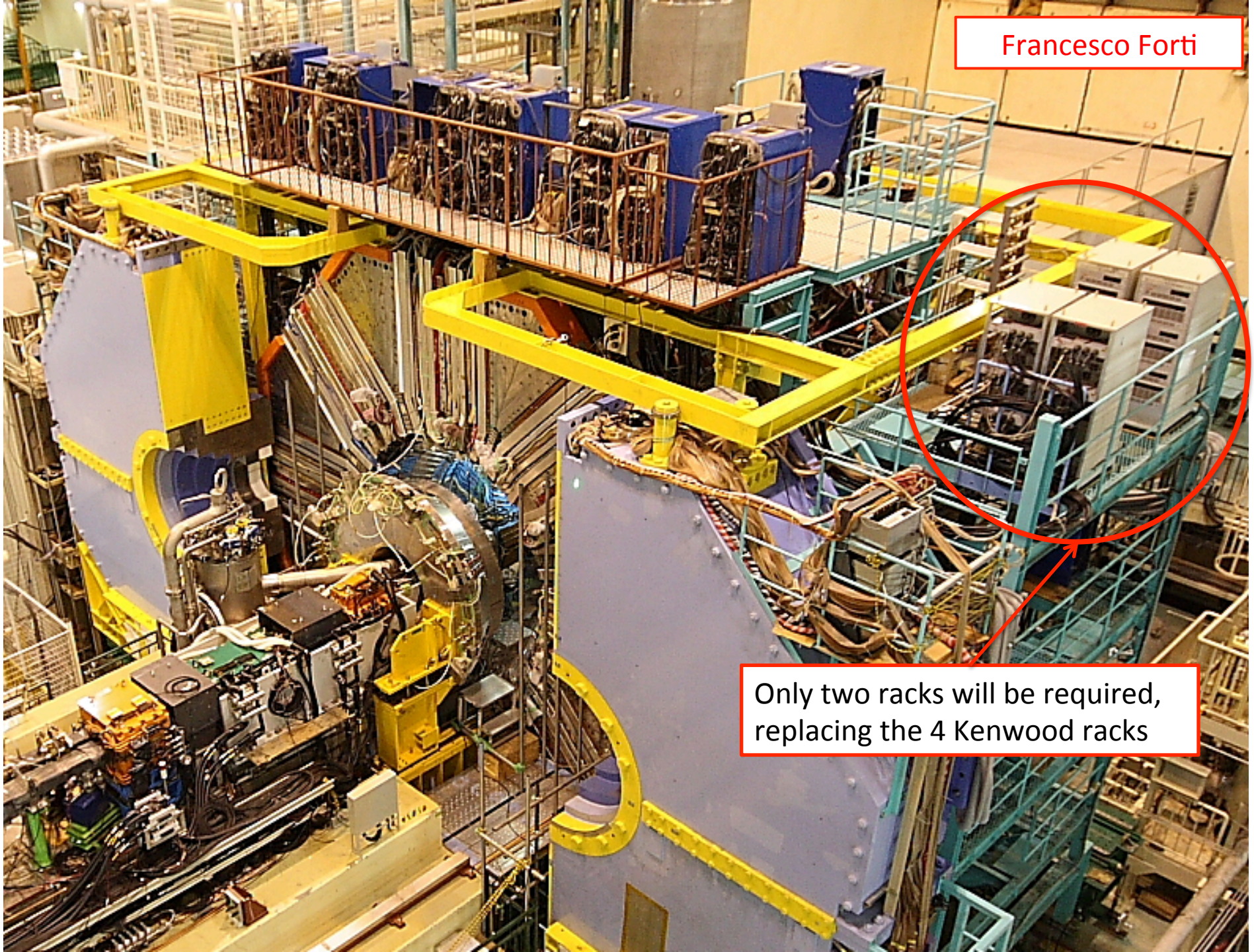


Fig. 1.1 - Mod. A 1510 front panel

ense	tatus	nable
YES	YES	YES
NO	NO	YES
NO	NO	YES

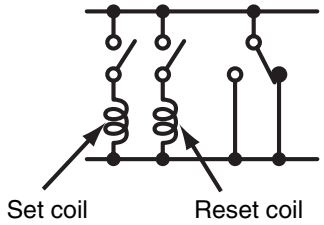

Francesco Forti
Only two racks will be required,
replacing the 4 Kenwood racks

Francesco Forti

Power distribution panel interface

- The only programmable part of the power distribution panel is the VSEP polarity select
  - The rest is only signal distribution, although the LVEnable/ HVEnable requires will require active components.
- Requirements
  - EPICS interface
  - Functionality choices:
  - Maintain polarity select across power cycles, or require reprogramming ?
    - Proposal to use latching relays
  - Include relay status monitoring ?
    - Of course you will be able to read back the digital signal status controlling the relay. The question is whether to use 3-pole relay where one pole is used to monitor the actual switching of the relay.

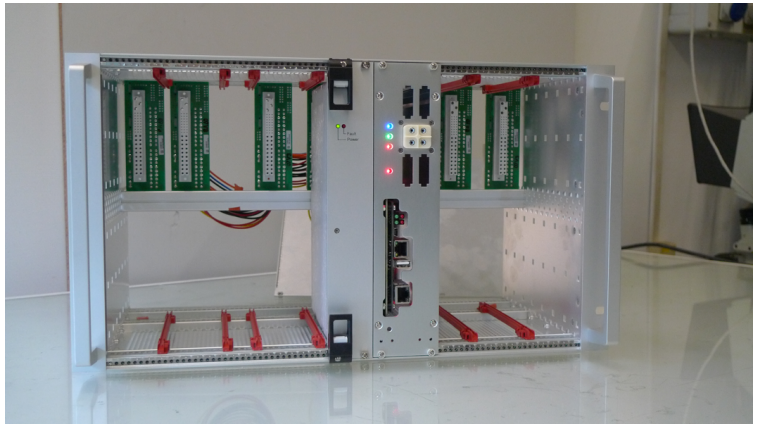
· **Latching Relays (Bistable Relays)**
The contact turns ON or OFF when input signal is received and maintain that status even if the input signal is cut.

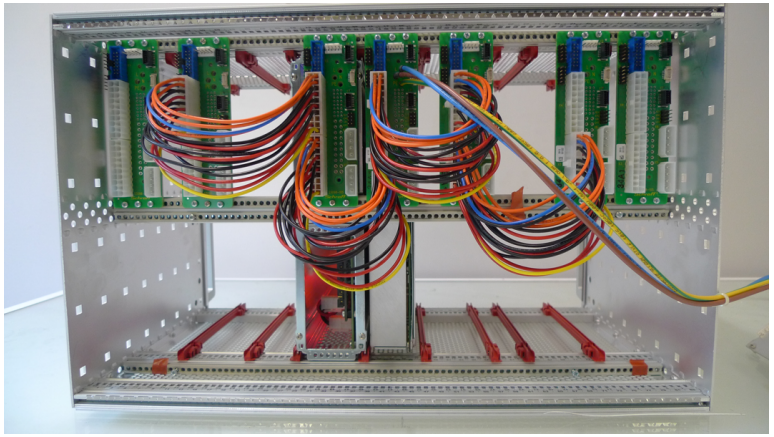


Francesco Forti

Final system ?

- Proposal: use the USOP system (from ECL) to provide local intelligence and control





- Advantage: developed in Naples, easy to use and powerful, with epics drivers (see slides attached to agenda)
- Disadvantage: relatively expensive and not funded at this time (working on this)
- Each USOP crate requires 2 ethernet lines: one for remote control over IP, the other for normal data operation (epics PV)
- Other solutions:
  - other systems with I/O capability, possibly already used in Belle2 ?
  - Use just one uSOP for all PDP crates ?
  - Need to decide soon

Katsuro Nakamura

Firmware Preparation Status

- Basically, minimum set of firmwares for data taking are already prepared.
  - They work good in the previous DESY beam test.
- However, still some necessary functions for the physics run are missing and further development are required.

Katsuro Nakamura

Remaining Tasks in Firmware Development

High priority: (necessary for physics run)

- APV pipe-line address emulator (in FADC-Ctrl)
  - the event order mismatch on FADC can be detected.
- APV FIFO emulator (in master FTSW)
  - prevents APV FIFO full which causes data corruption.
- Improvement on common-mode correction (CMC) function. (in FADC)
  - Currently 128-strips wise, but will be changed to 32-strips wise for more accurate common-mode noise reduction.
- GbE data link for SVD local data taking (in FADC)
  - For faster local data taking.
- Remote FPGA configuration through VME access (in FADC)
- Improvement on data format of FTB-DATCON link (in FTB)
  - in order to increase the data size of the clock counter (currently 24-bits).

Middle priority: (not mandatory, but better to have)

- Fake-hit filter (in FADC)
- Zero-suppressed + Hit timing extraction mode (in FADC)
  - The last data format for further data size suppression.
- Function of event-by-event switching btw. 3- and 6-samples depending on trigger types. (in FADC-Ctrl + FADC)
  - Necessary only for operation with about 30kHz or higher trigger rate.
- New FTB data format (in FTB)
  - w/ more useful information.

Katsuro Nakamura

Global Schedule

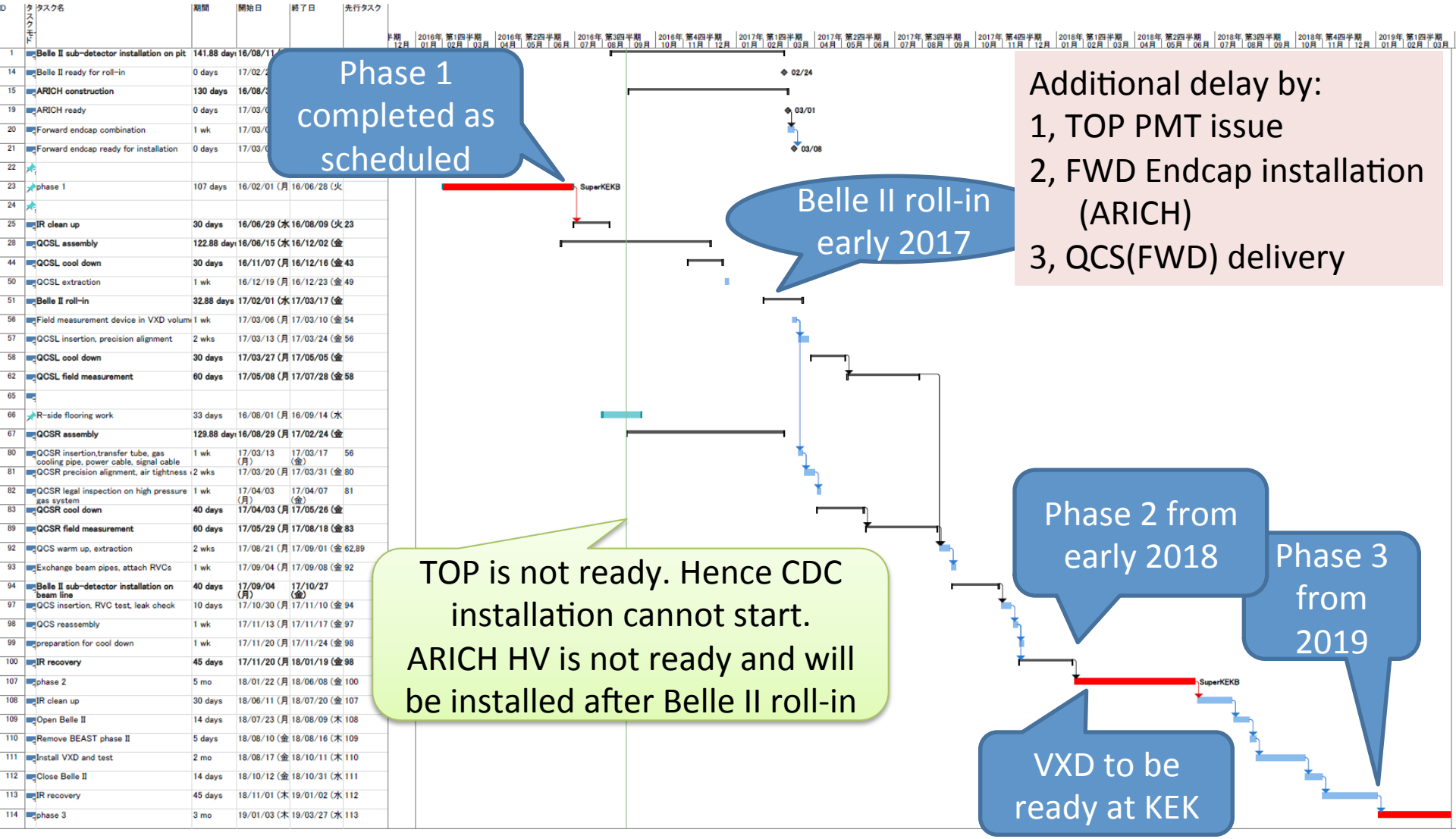
- Dec. 2016: 3rd DESY beam test campaign
  - We will use FADC ver.3 boards for this beam test.
- End of Feb. 2017: Start SVD ladder mount
  - We will use FADC ver.2 boards for electrical test during the ladder mount.
- Jan. 2017: FADC ver.4/Junction boards test production
- Mar. 2017: Test of FADC ver.4 in HEPHY and DESY
  - Noise performance will be tested with permanent setup at DESY
- Apr. 2017: Decision whether ver.3 or ver.4
- May.-Jul. 2017: FADC ver.4/Junction board mass production
- From the end of 2017:
  - Phase-2: A partial VXD system will be installed for phase-2 commissioning.
  - Cosmic-ray commissioning: In parallel to phase-2, full VXD will be assembled and tested with
  - Full sets of FADC system and power supply are necessary by this point.
- From the end of 2018: Phase-3 experiment
  - Full VXD installation and operation

- PS schedule must be included here.

SUMMARY

Schedule

(Recently shown by Yutaka, but it will be decided in next B2GM)



ID	タスク名	期間	開始日	終了日	先行タスク
1	**Belle II sub-detector installation on pit**	141.88 days	16/08/11		
14	Belle II ready for roll-in	0 days	17/02/2		
15	**ARICH construction**	130 days	16/08/3		
19	ARICH ready	0 days	17/03/0		
20	Forward endcap combination	1 wk	17/03/0		
21	Forward endcap ready for installation	0 days	17/03/0		
22					
23	phase 1	107 days	16/02/01 (月	16/06/28 (火	
24					
25	**IR clean up**	30 days	16/06/29 (水	16/08/09 (火	23
28	**QCSL assembly**	122.88 days	16/06/15 (水	16/12/02 (金	
44	**QCSL cool down**	30 days	16/11/07 (月	16/12/16 (金	43
50	QCSL extraction	1 wk	16/12/19 (月	16/12/23 (金	49
51	**Belle II roll-in**	32.88 days	17/02/01 (水	17/03/17 (金	
56	Field measurement device in VXD volum	1 wk	17/03/06 (月	17/03/10 (金	54
57	QCSL insertion, precision alignment	2 wks	17/03/13 (月	17/03/24 (金	56
58	**QCSL cool down**	30 days	17/03/27 (月	17/05/05 (金	
62	**QCSL field measurement**	60 days	17/05/08 (月	17/07/28 (金	58
65					
66	R-side flooring work	33 days	16/08/01 (月	16/09/14 (水	
67	**QCSR assembly**	129.88 days	16/08/29 (月	17/02/24 (金	
80	QCSR insertion,transfer tube, gas cooling pipe, power cable, signal cable	1 wk	17/03/13 (月)	17/03/17 (金)	56
81	QCSR precision alignment, air tightness	2 wks	17/03/20 (月	17/03/31 (金	80
82	QCSR legal inspection on high pressure gas system	1 wk	17/04/03 (月)	17/04/07 (金)	81
83	**QCSR cool down**	40 days	17/04/03 (月	17/05/26 (金	
89	**QCSR field measurement**	60 days	17/05/29 (月	17/08/18 (金	83
92	QCS warm up, extraction	2 wks	17/08/21 (月	17/09/01 (金	62,89
93	Exchange beam pipes, attach RVCs	1 wk	17/09/04 (月	17/09/08 (金	92
94	**Belle II sub-detector installation on beam line**	40 days	17/09/04 (月)	17/10/27 (金)	
97	QCS insertion, RVC test, leak check	10 days	17/10/30 (月	17/11/10 (金	94
98	QCS reassembly	1 wk	17/11/13 (月	17/11/17 (金	97
99	preparation for cool down	1 wk	17/11/20 (月	17/11/24 (金	98
100	**IR recovery**	45 days	17/11/20 (月	18/01/19 (金	98
107	phase 2	5 mo	18/01/22 (月	18/06/08 (金	100
108	IR clean up	30 days	18/06/11 (月	18/07/20 (金	107
109	Open Belle II	14 days	18/07/23 (月	18/08/09 (木	108
110	Remove BEAST phase II	5 days	18/08/10 (金	18/08/16 (木	109
111	Install VXD and test	2 mo	18/08/17 (金	18/10/11 (木	110
112	Close Belle II	14 days	18/10/12 (金	18/10/31 (木	111
113	IR recovery	45 days	18/11/01 (木	19/01/02 (水	112
114	phase 3	3 mo	19/01/03 (木	19/03/27 (水	113

Summary

- Ladders
  - Ladder assembly is in full swing
  - We expect to meet the global schedule
- Main topics @ this meeting: slow control and DAQ
  - Especially the SC effort needs to ramped up
  - The system is better defined after this meeting
  - Manpower/schedule needs to be clarfied
  - Broader discussion for interlocks

BACKUP