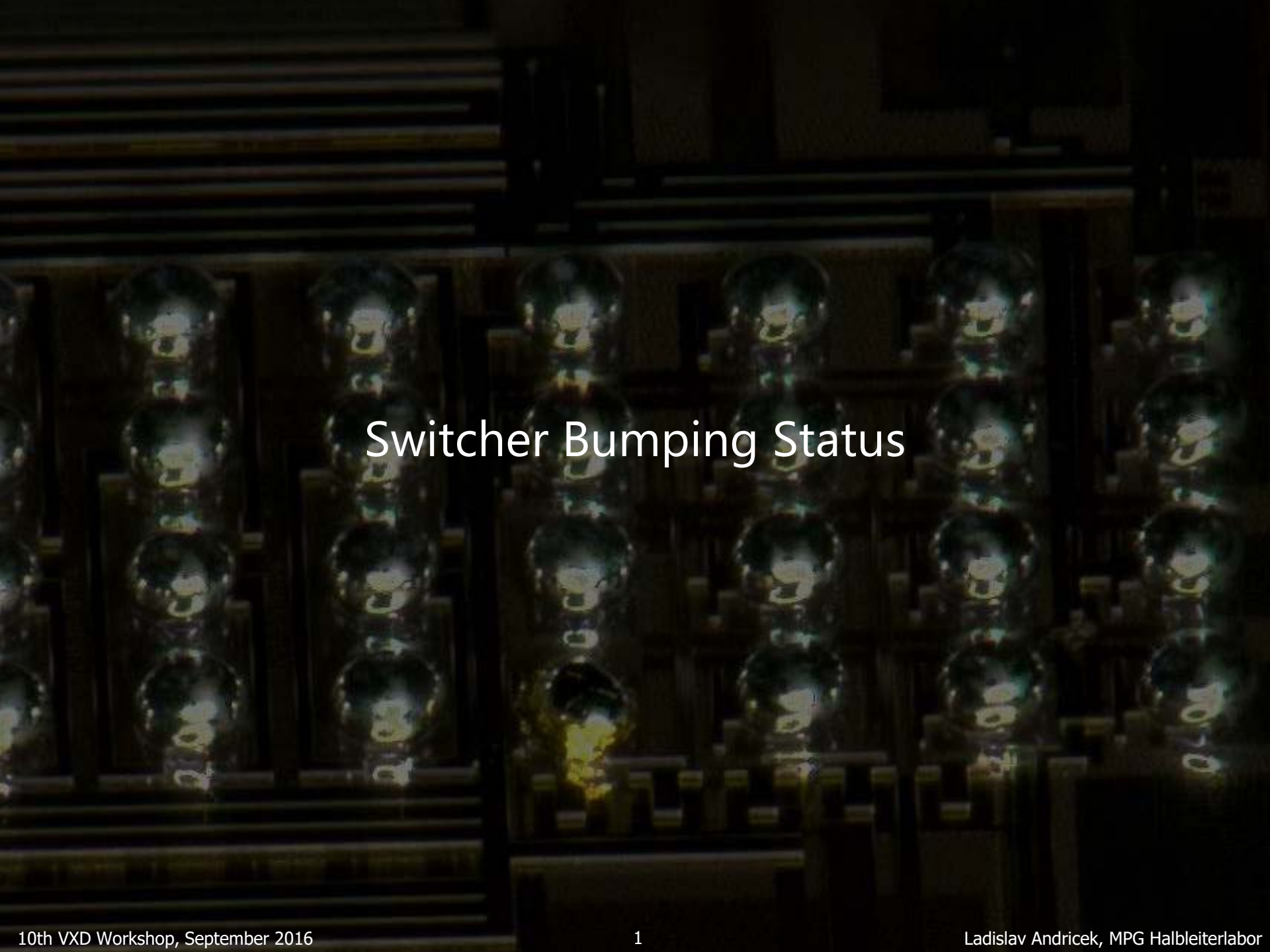
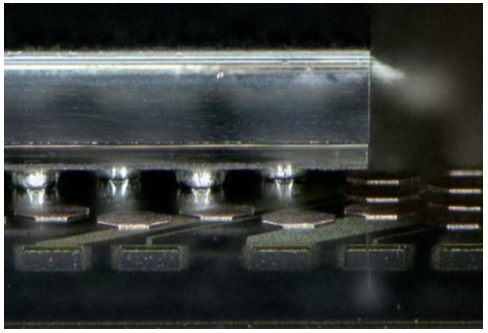


Switcher Bumping Status

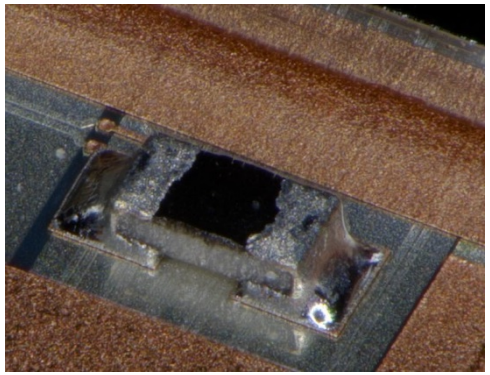
Flip Chip of ASICs (~240°C):

- Bumped ASICs have the solder balls (SAC305 and AgSn)
  - ↳ DHP bumping at TSMC, DCD bumping via Europractice
  - ↳ **SWB bumping on chip level at PacTech (????)**
- Flip Chip of PXD modules at IZM Berlin



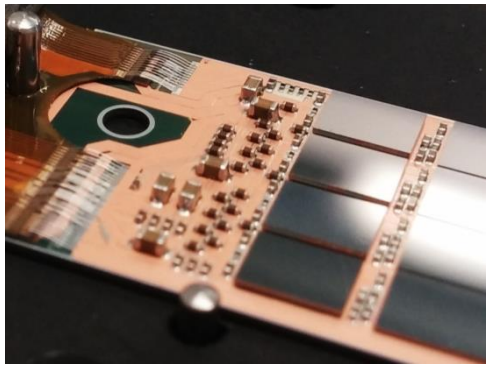
SMD placement (~200°C):

- Passive components (termination resistors, decoupling caps)
- Dispense solder paste/jetting of solder balls, pick, place and reflow
  - ↳ PbSn 37/63 solder



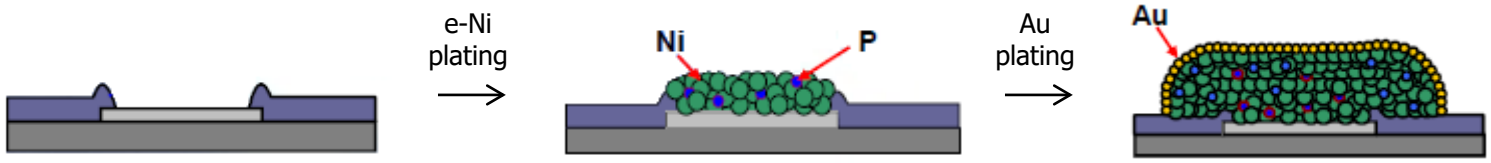
Kapton attachment (~170°C), wire bonding:

- Solder paste printing on kapton,
  - ↳ SnBi solder
- Wire-bond, wedge-wedge, 32 µm Al bond wires

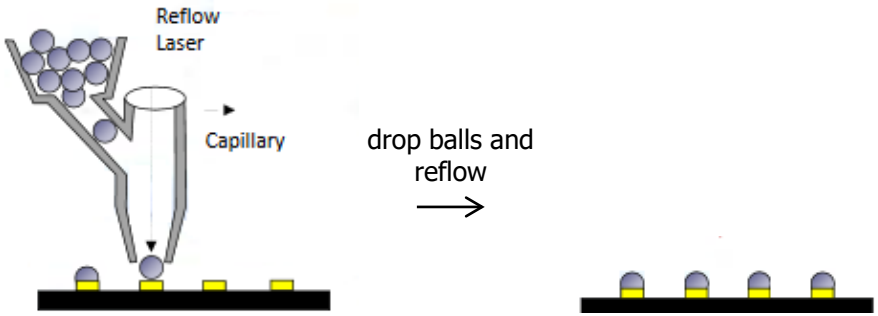


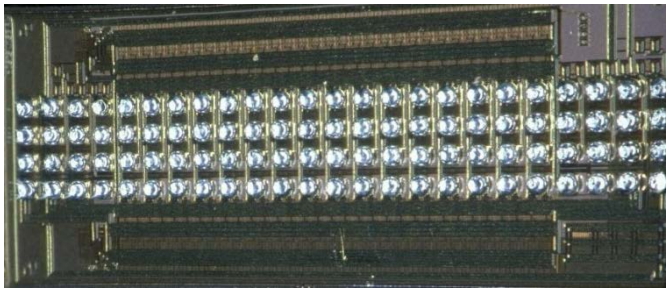
Bumping at PacTech

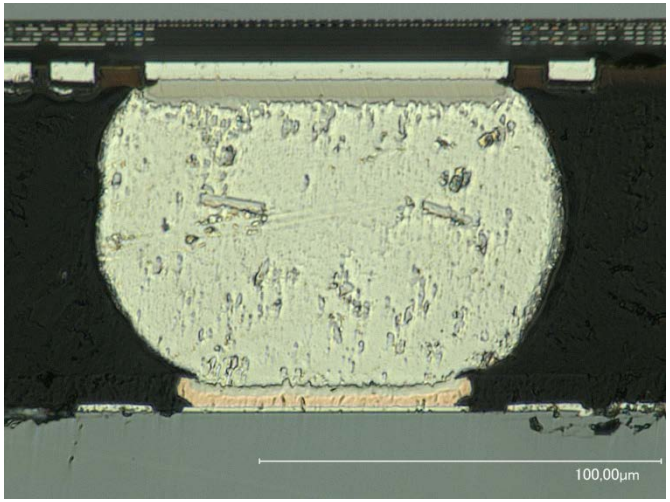
- ENIG process: Electroless Nickel Immersion Gold → UBM



- Solder ball jetting







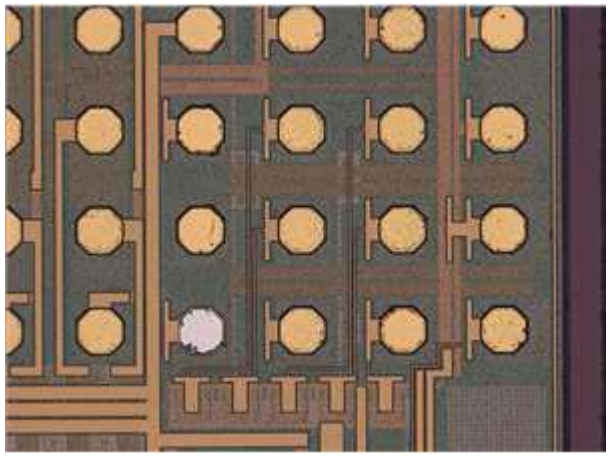
- Fully Qualified with SwitcherB18v2.0
  - ↳ Test production
  - ↳ X-sections, shear tests, test assemblies … all ok!
  - ↳ Assembly of EMCMs, pilot modules, Desy test..

The new SwitcherB18v2.1

- Bumping (UBM process) causes problems with the new Switcher

- On one pad – the substrate pad – and only on this pad
  - Very little or no Nickel deposition

- Main difference to old Switcher
  - Chip is wider…
  - Different passivation (1µm Nitride/Oxide <-> PI)
  - Guard ring of the chip exposed, connected to bulk

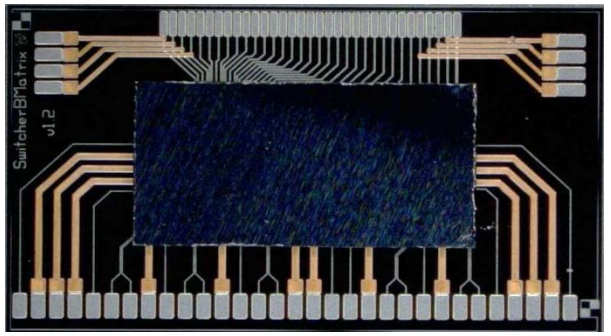


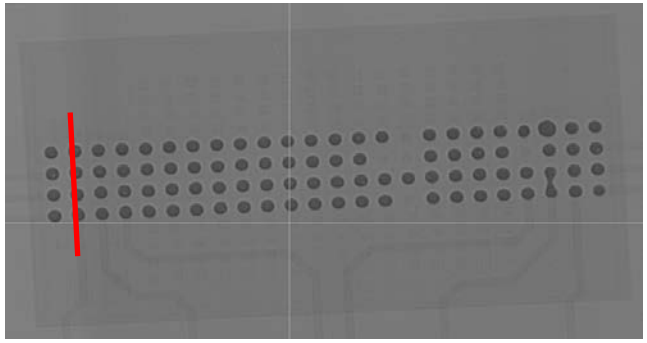
→ Different electrochemical potential causes reduced Ni growth on substrate

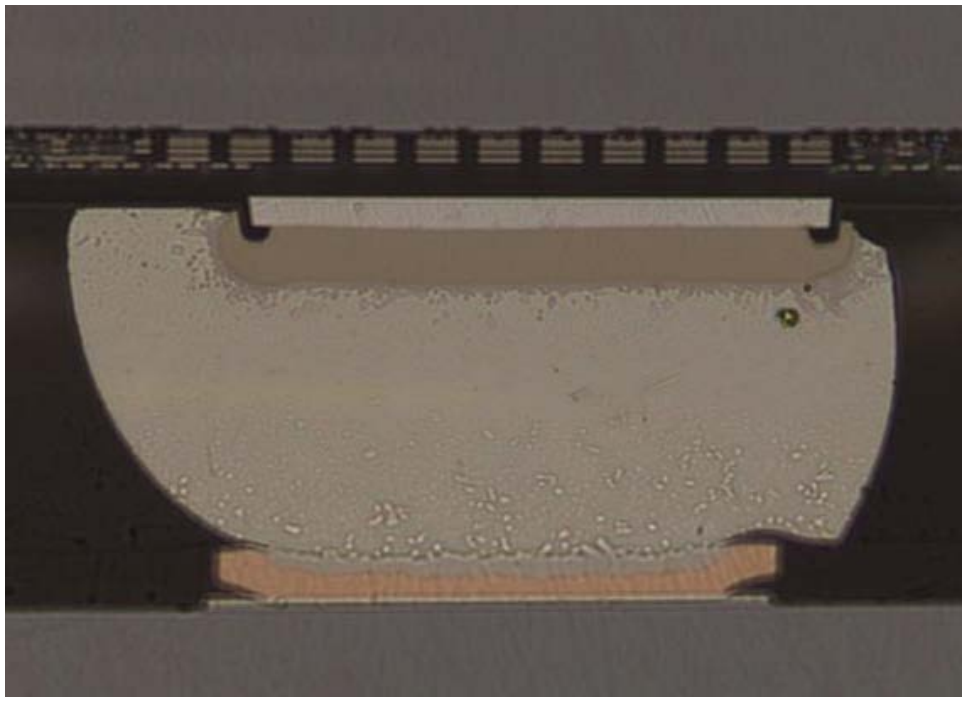
→ Solution: isolate chip edge! First trials by manual coating chip by chip …
  → **Successful but very time consuming process with bad yield**

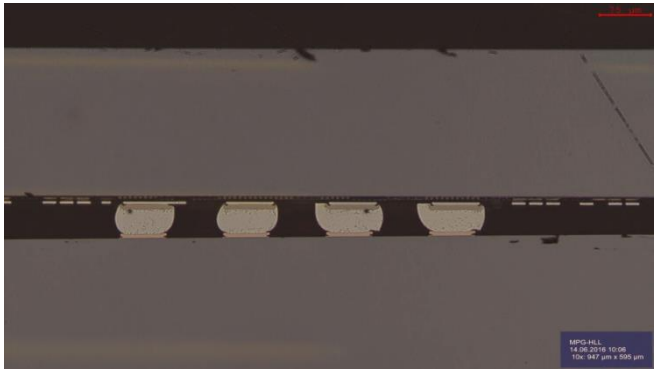
Test Assembly of SWBs to bond adapter

- Adapters assembled for SWB testing on hybrid level
  - Three adapters assembled
  - One assembly done with bad chip (bumping problems)
- Cross-section





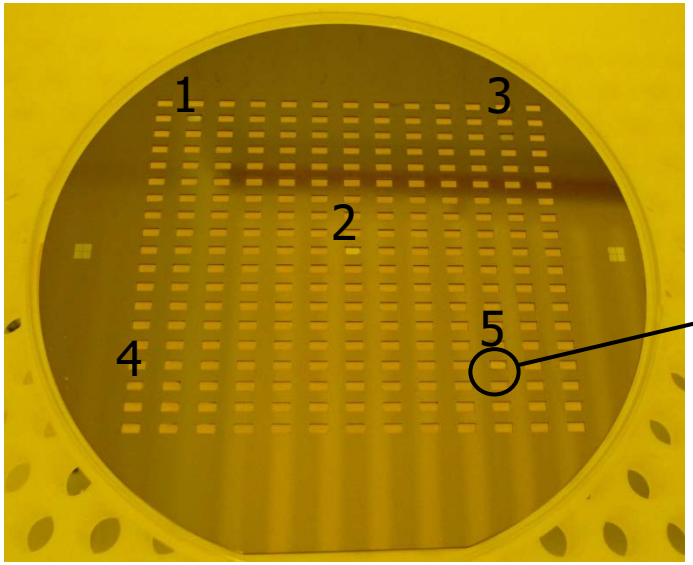


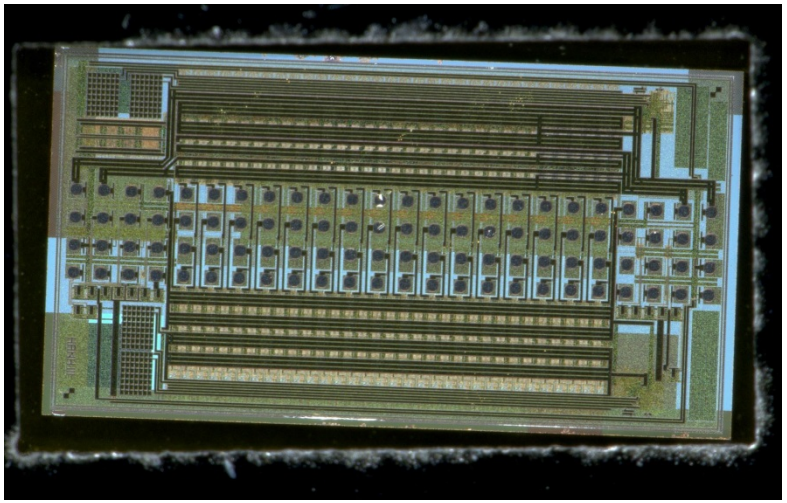


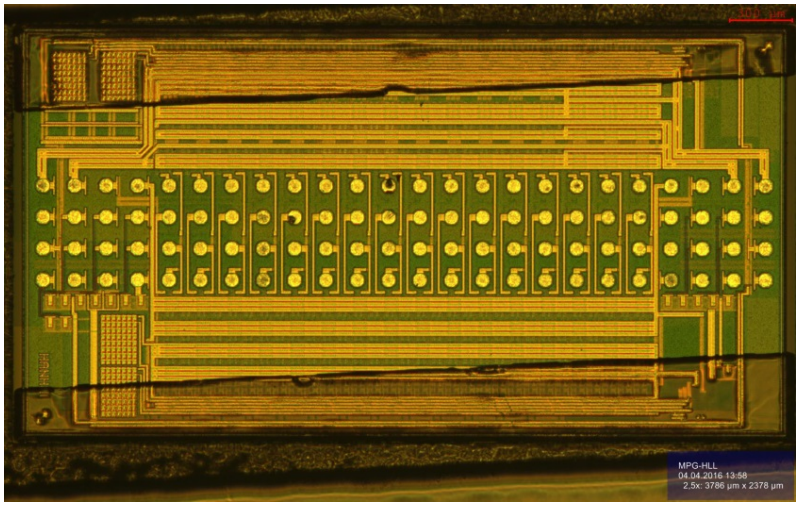
- Too much solder ….

Assembling a wafer

- After successful single chip coating by hand with miserable yield, trial to make it a batch process
- Re-assembly of a “wafer”



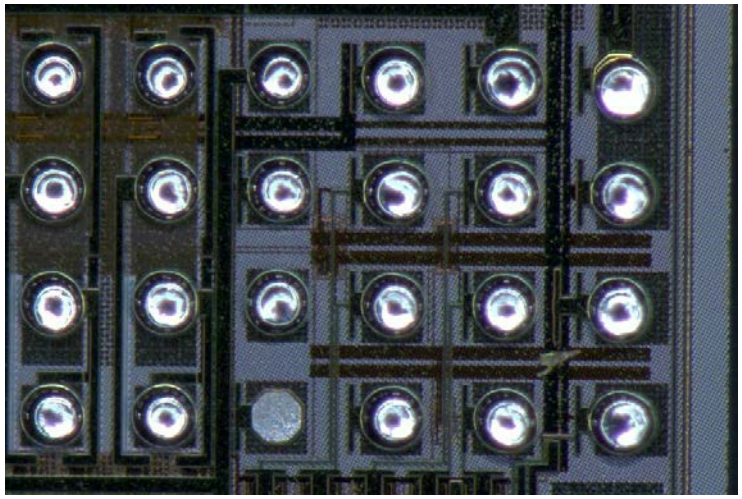




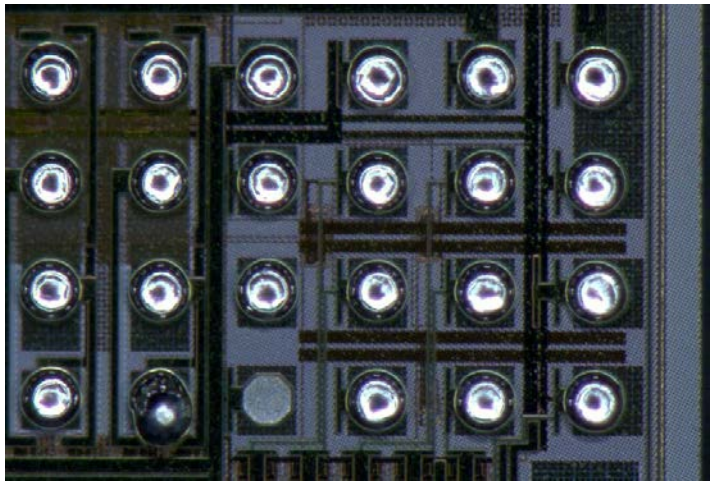
- Test successful
  - UBM successful on test wafer with five SWB
  - Balling was okay
  - Shear tests passed

First larger batch process

- "wafer" assembled with 29/100 remaining unbumped chips
- Sent to PacTech for bumping
  - Agreed to use smaller solder balls (70 µm and 60 µm instead of 80 µm now)
- **Failed!**
  - **Almost on all chips, the UBM was not deposited**



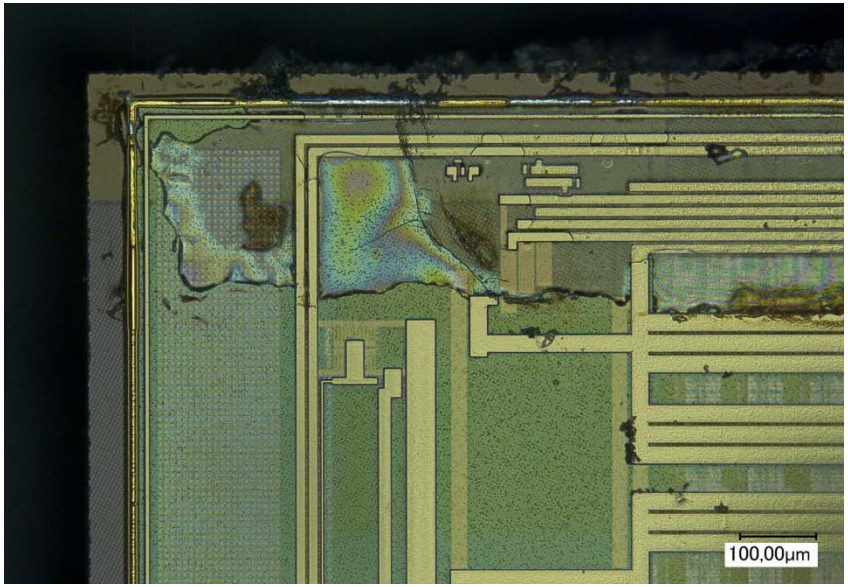
Bad UBM → no ball

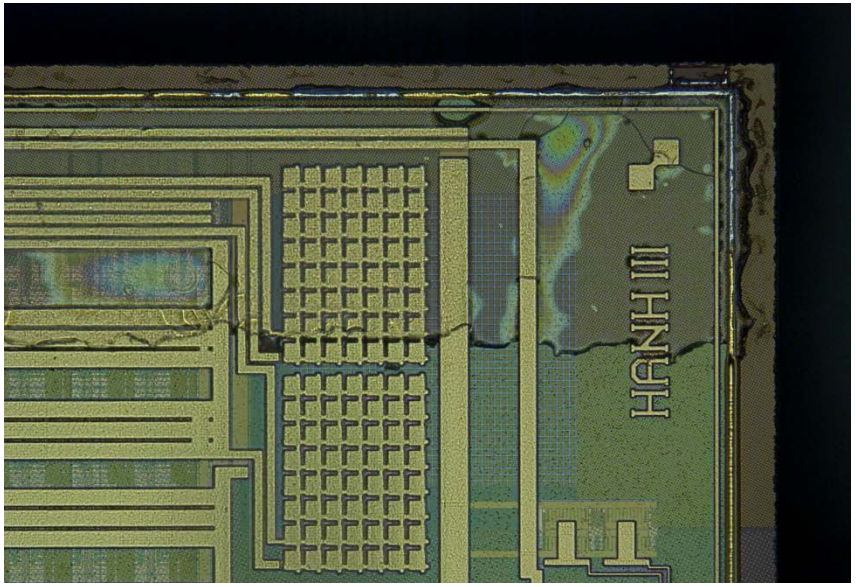


Bad UBM → no ball and double ball on neighbour

Why did it fail?

- According to PacTech, the chemistry for the UBM is very aggressive (with little control over it) and attacks the photo resist ("occasionally")
- Isolation of the edge is compromised

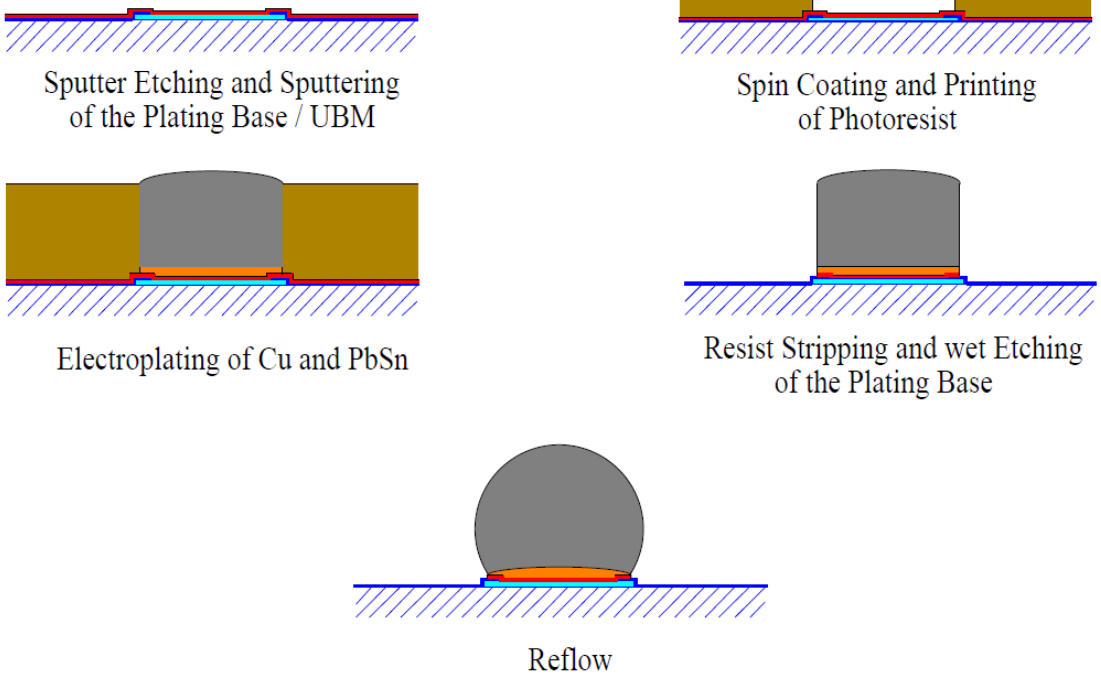




- Process is unstable, may work after some more trials (different PR …)
- But because of manual single chip handling (wafer assembly, PR removal ..) high loss expected

Bumping on “wafer level” at IZM

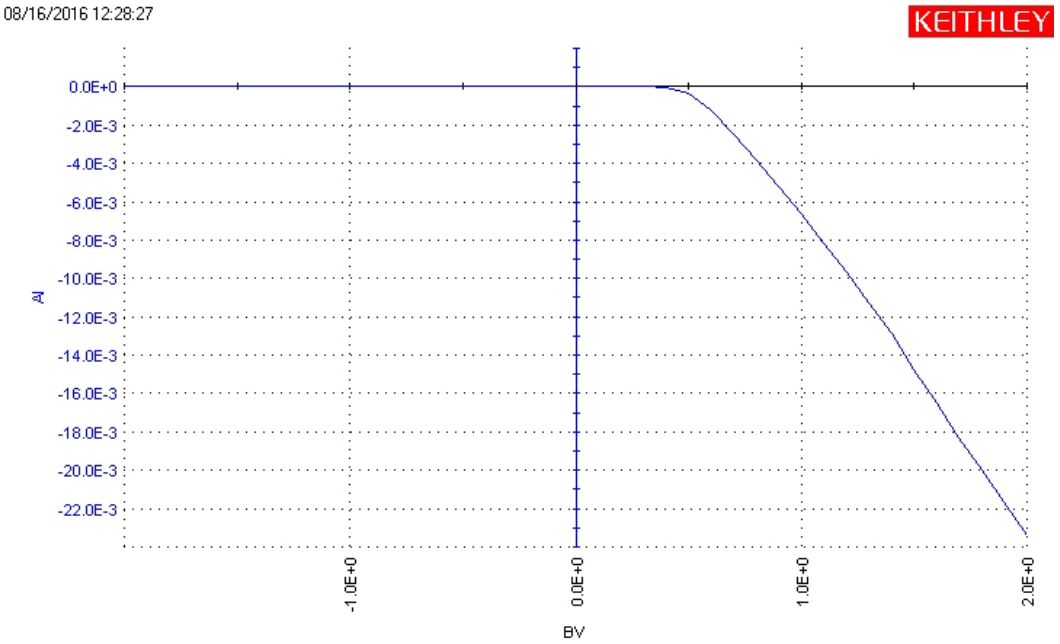
- Assemble a “wafer” by pick-and-place of Switchers to support with alignment marks
  - Accuracy ~few microns, subsequent wafer level lithography possible
  - Possibility to apply standard technology bumping by electro-plating



- Tests at IZM are ongoing … litho processes to be done this week

How to rescue the Switchers?

- Provide V_{sub} via backplane of the chip
  - Would be the most straight-forward solution
  - Unfortunately did not work (bad contact and diode structure between backplane and V_{sub})

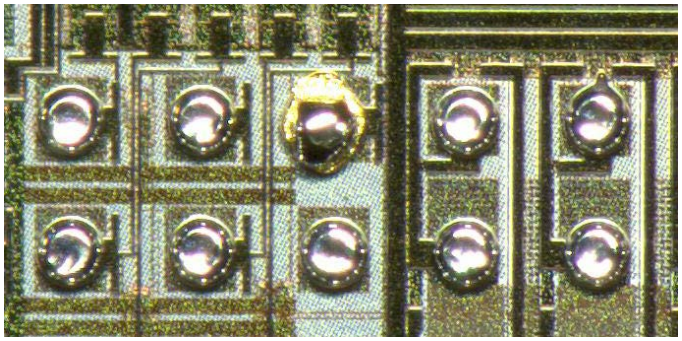


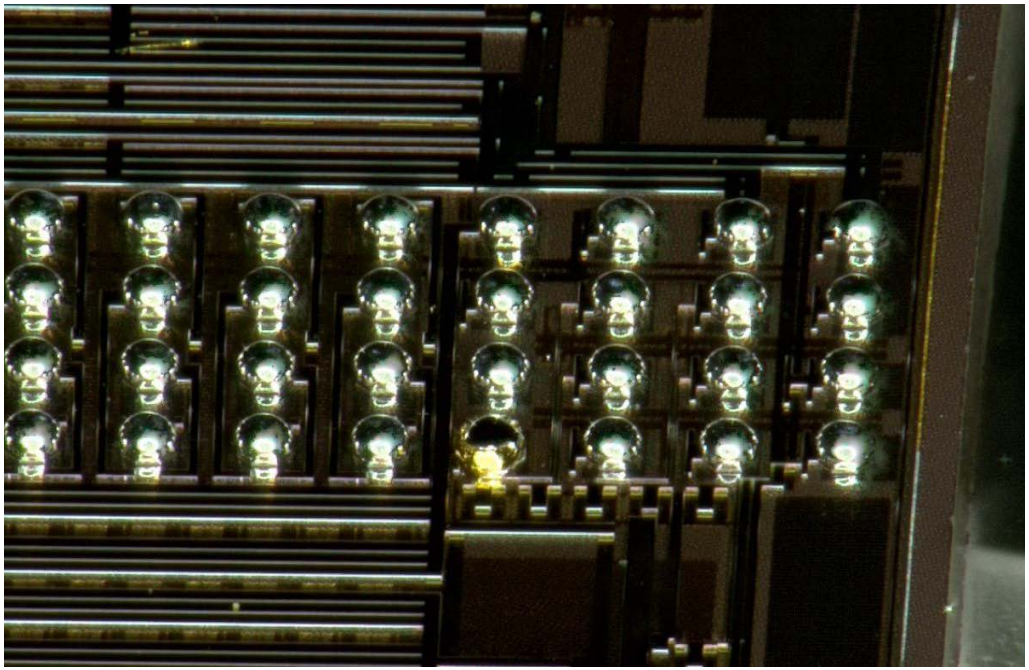
I(V) between Vsub and backplane, GND on back

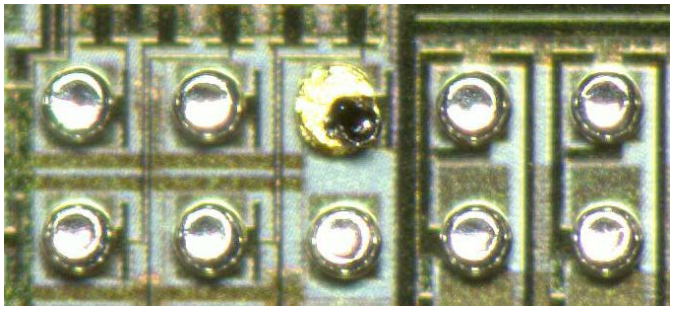
- Place Au stud on missing UBM pad and deposit small solder ball on it
  - Au stud at HLL, solder ball jetting at PacTech

Single pad balling

- Selected optically good chips
- It worked – sort of…







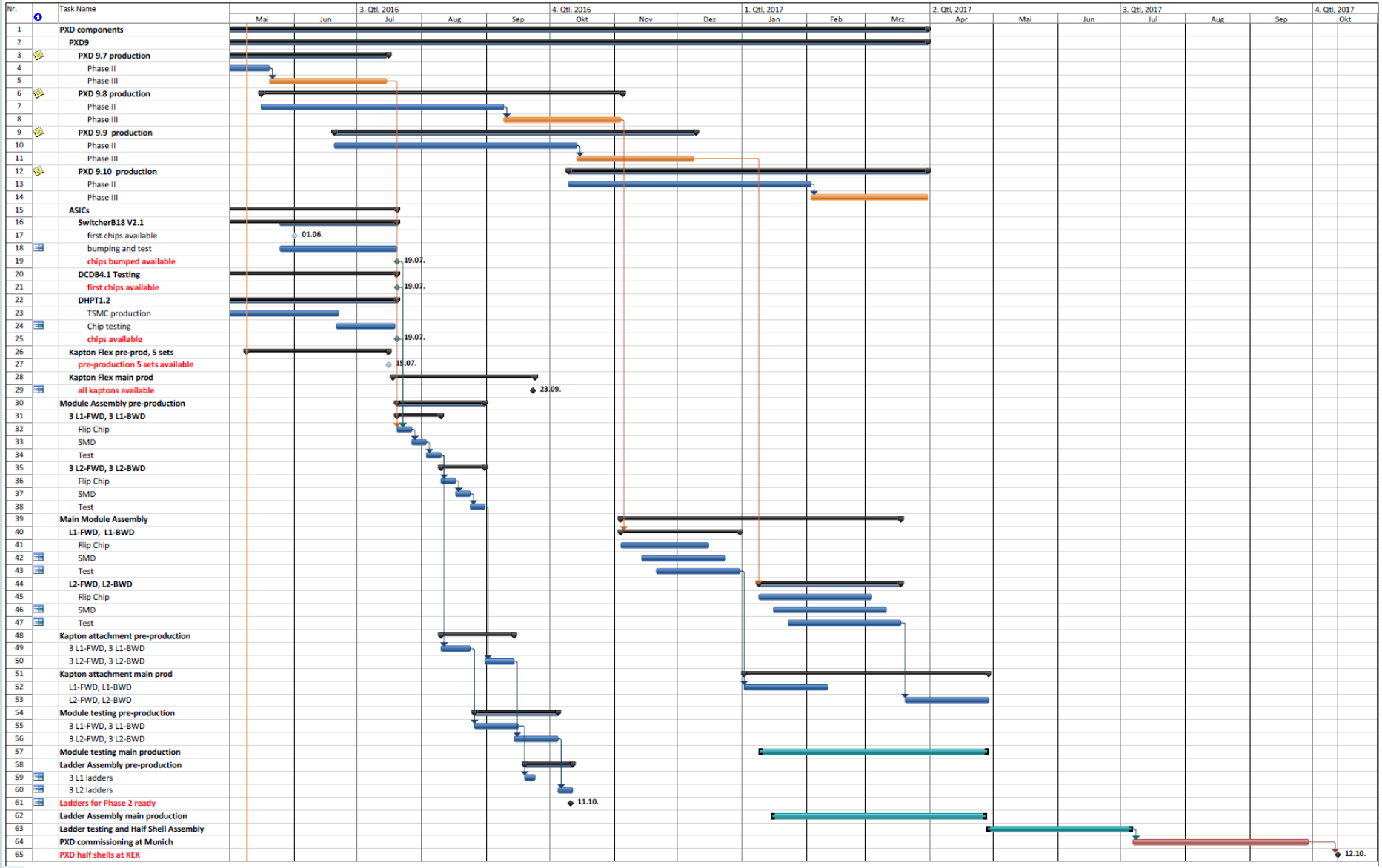
- Balls are all about 40-50 µm, as the others
- Mostly central ….
- Need for testing → KIT
- Have now: 16 Au-stud chips, 12 from first batch w/ manual PR coating

Summary

- Bumping on chip level is difficult!!
- PacTech bumping worked on SWB2.0 but failed for 2.1 (passivation)
  - Work around done small number of chips
  - If tests positive, assembly of phase 2 modules can start …
- Exploring new technique at IZM, seems feasible but remains to be shown
- To be on the safe side: order more switchers?? Engineering run??? Time scale???

backup

schedule – spring 2016



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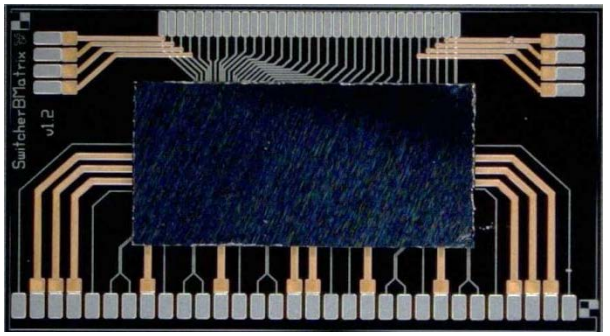

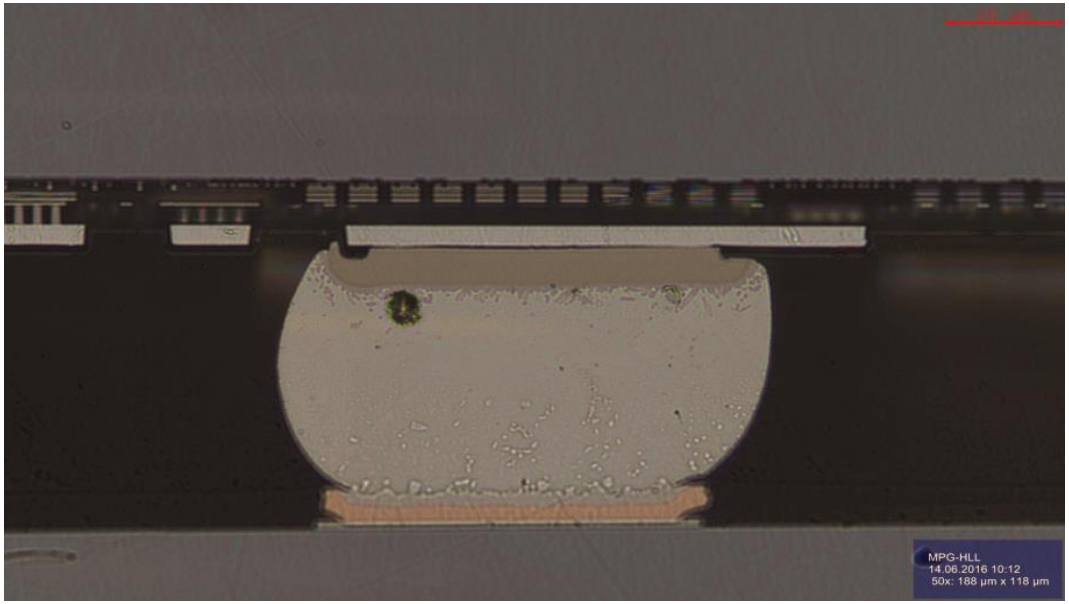

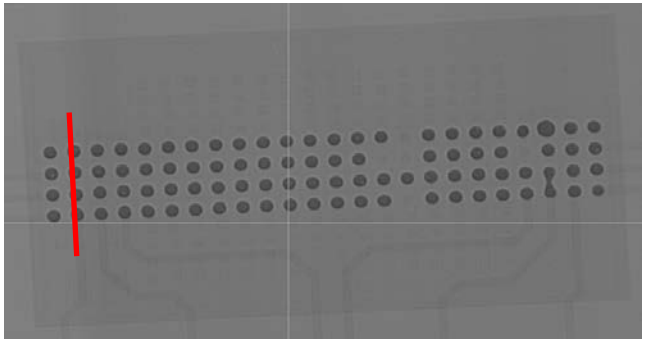

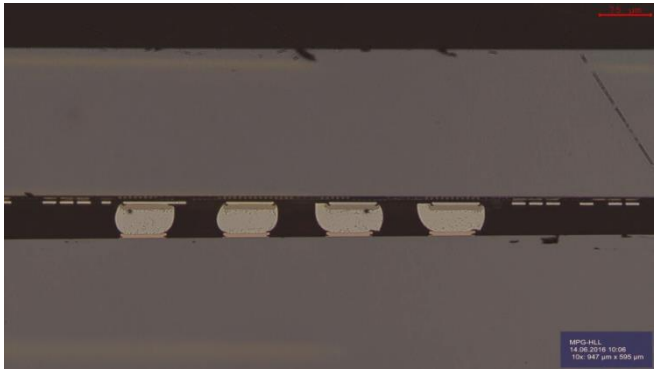

- Delamination between SWB Alu and Ni?