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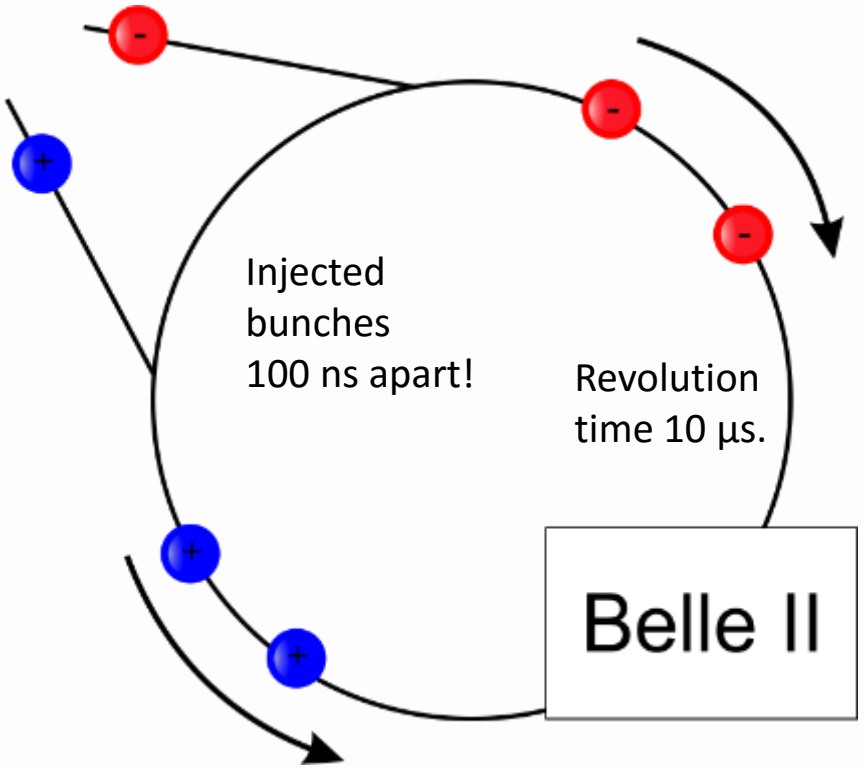
Gated Mode Operation

J. Dingfelder, L. Germic, T. Hemperek,
Jan Cedric Hönig, H. Krüger, F. Lütticke, C. Marinas,
B. Paschen, N. Wermes

Gated Mode operation



- Continuous refill of bunches (50 Hz)
- Newly injected bunches need some time to cool down

- Revolution time of 10 µs, while detector integration time is 20 µs

  → Noise created by refilled bunches flying through the detector

Gated Mode:

- Mechanism to make the detector 'blind' to passing noisy bunches!

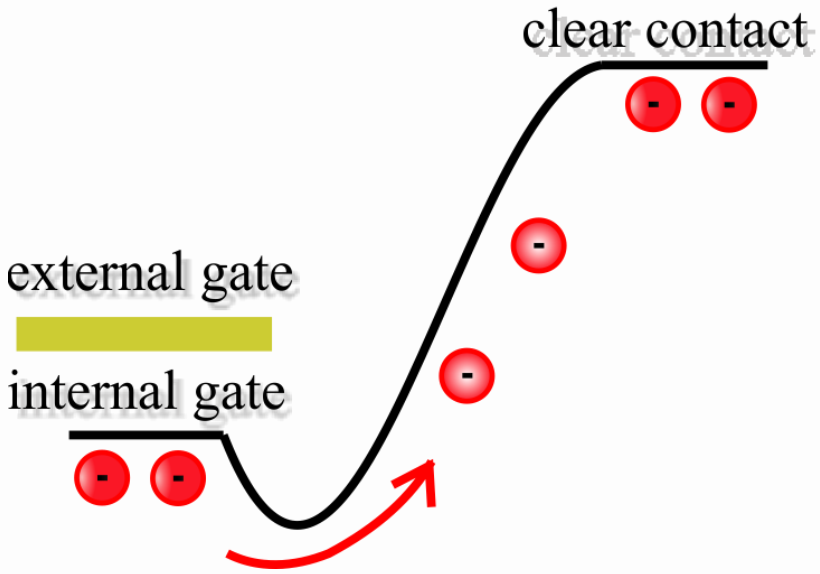
- It has been proven that the DEPFET matrix can be operated in 'blind' (gated) mode
- In this talk, parameter optimization for:

→ Minimum dead time, complete *noisy charge* removal and full *physics charge* preservation

How does gated mode work

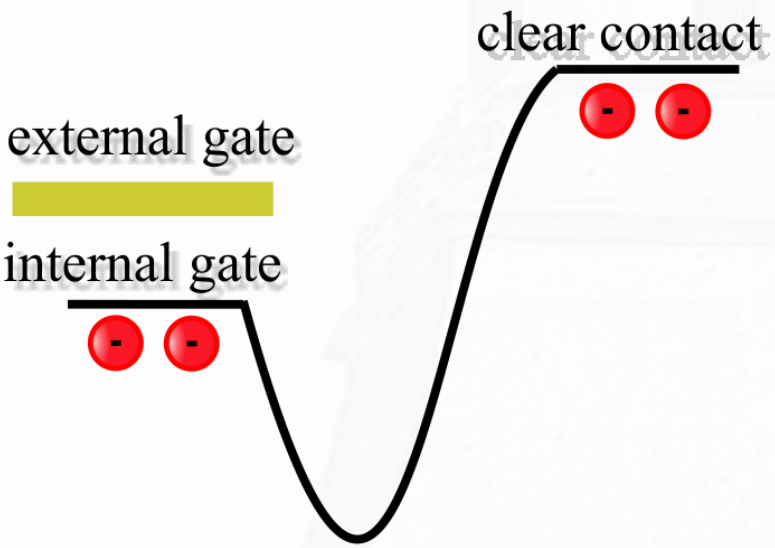
Real clear

Clear voltage high
Gate voltage low



Suppressed clear

Clear voltage high
Gate voltage high



Here: gated mode **with** read out is used!

Hybrid 5 Set Up

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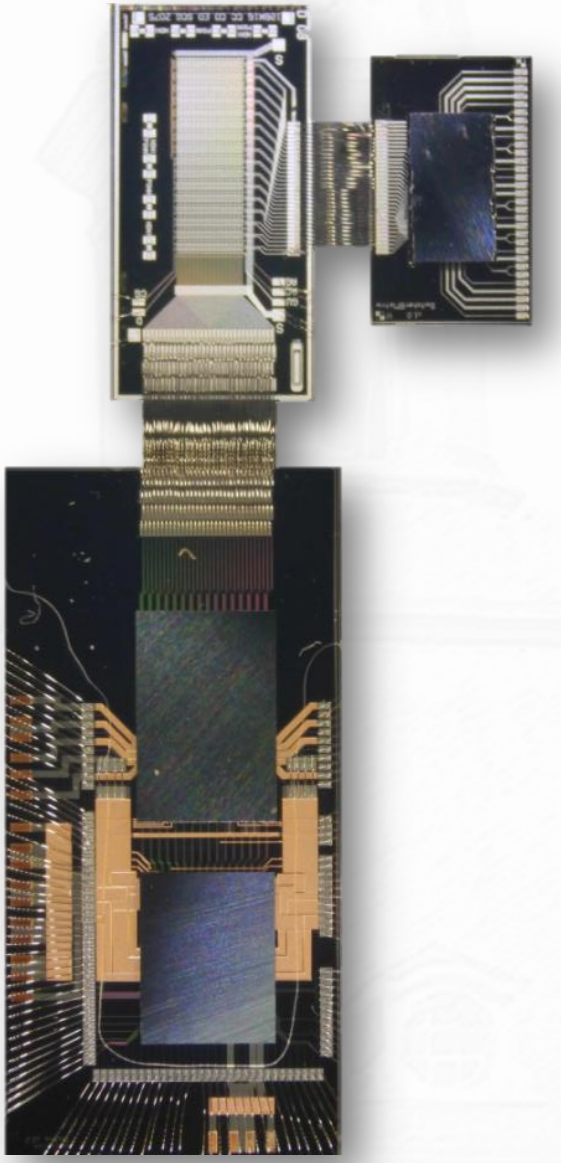
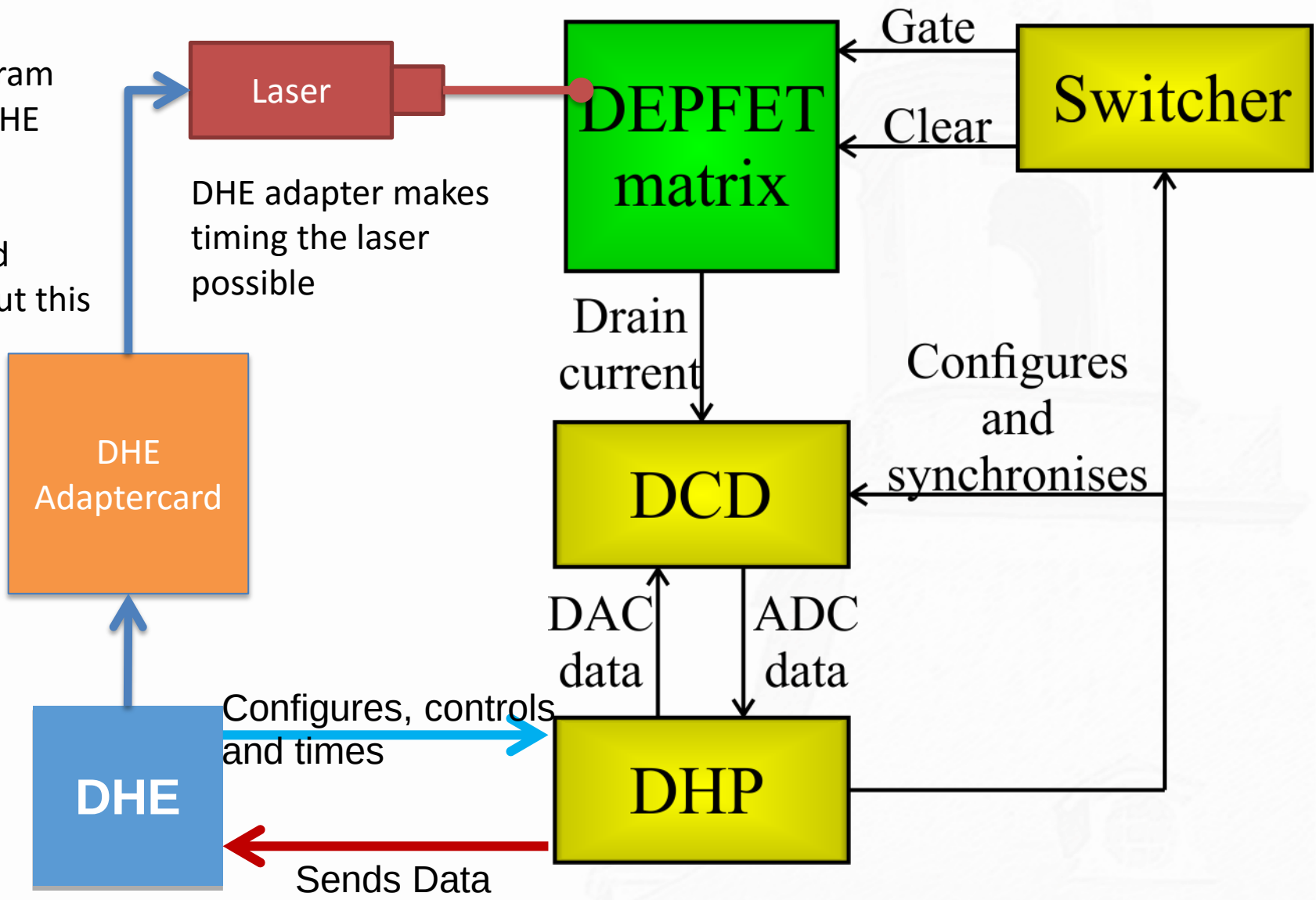
- PXD9 small Belle II type matrix
  - 32x64 pixels readout
- Final readout chain
  - SwitcherB1.8Gated
  - DCDBPipeline
  - DHPT1.0
  - DHE



DHP programing

Possible to program sequence into DHE memory!

DHE adaptercard allows to read out this sequence.

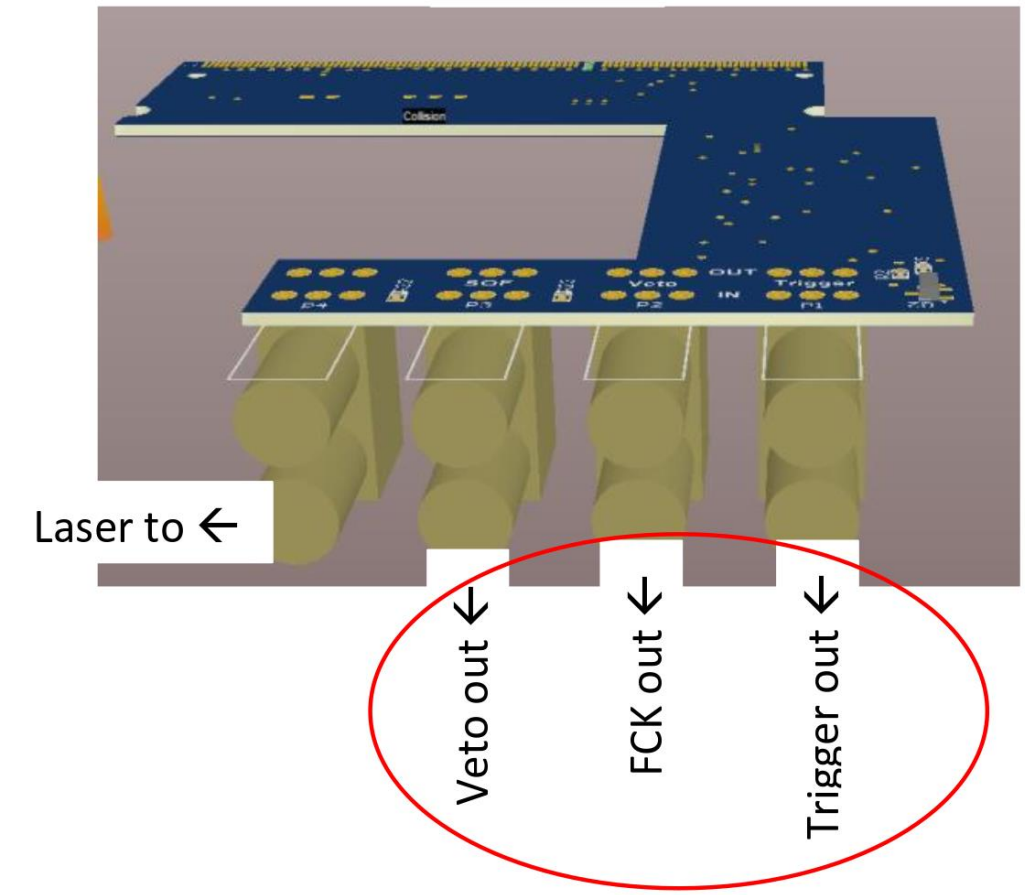


Adapter for DHE

Adapter card warrants the ability to display internal veto and trigger signals!

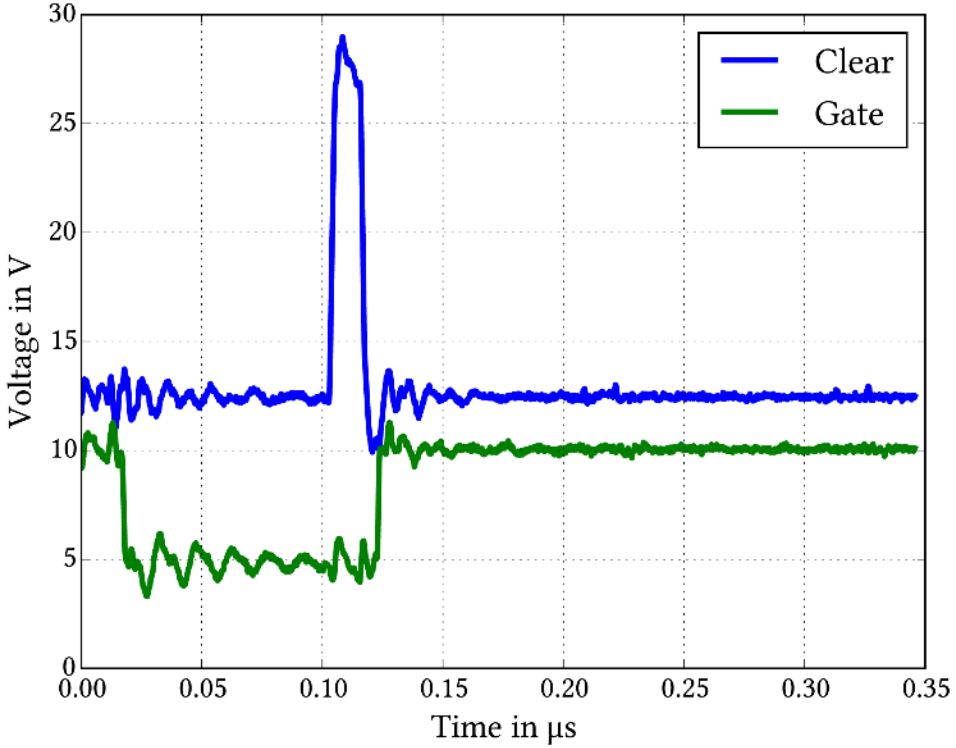
A trigger signal can be sent to the pulse generator connected to the laser.

Possibility to program a sequence to control precisely how long is triggered, when gated mode is active and when to shoot the laser.



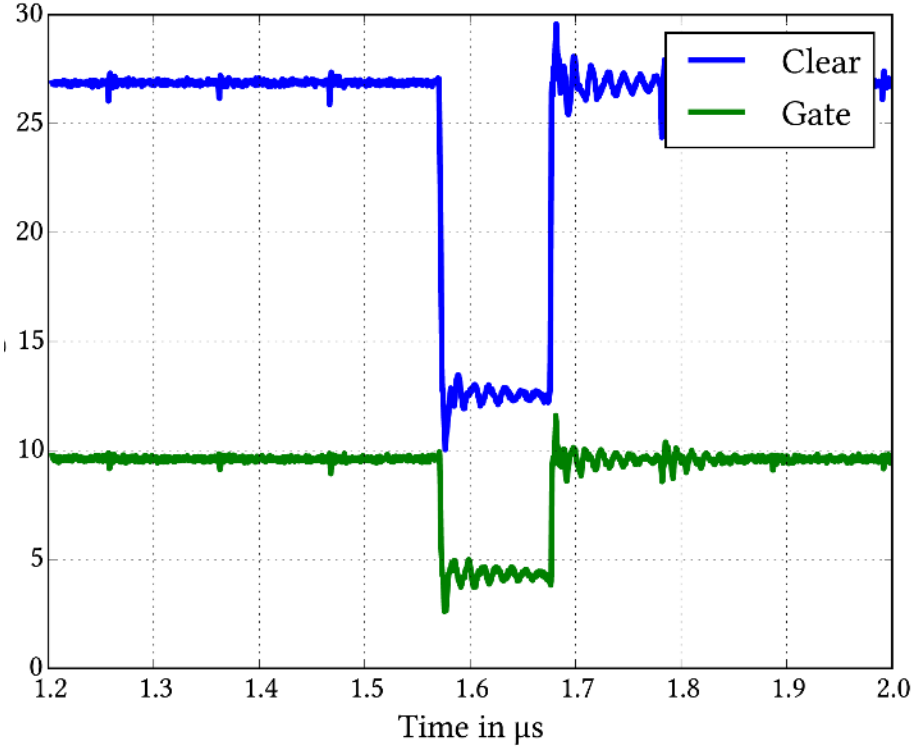
Normal operation vs gated mode

Normal operation



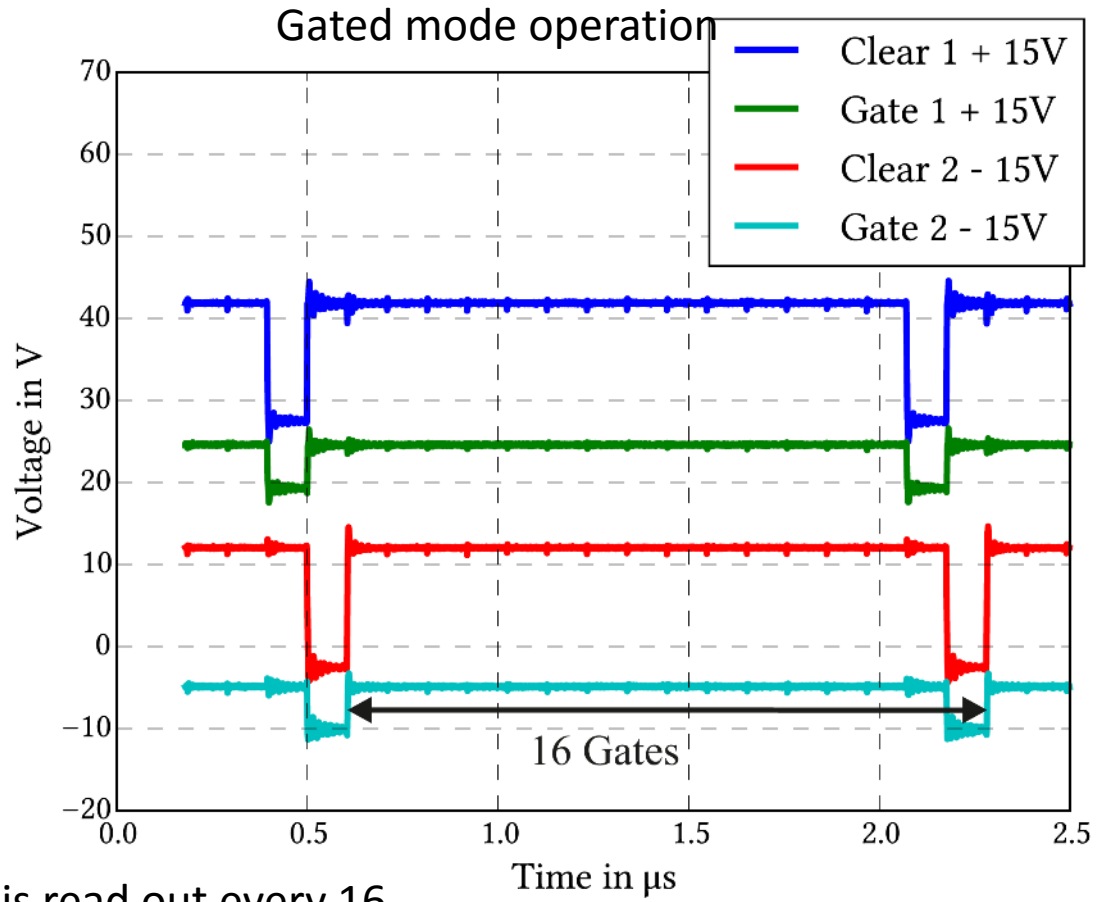
Short clear pulse is applied after sampling!

Gated mode operation



Clear is high except for when the corresponding gate is read out!
This gate is **not** shielded while we read that gate out.

Time length of one gate



The same pixel is read out every 16 gates.
Time distance can be used to calculate the length of one gate!

Belle II clock (76.33 MHz):

$$\Delta t_{1\,\mathrm{gate}} = (104.81 \pm 0.02)\ \mathrm{ns}$$

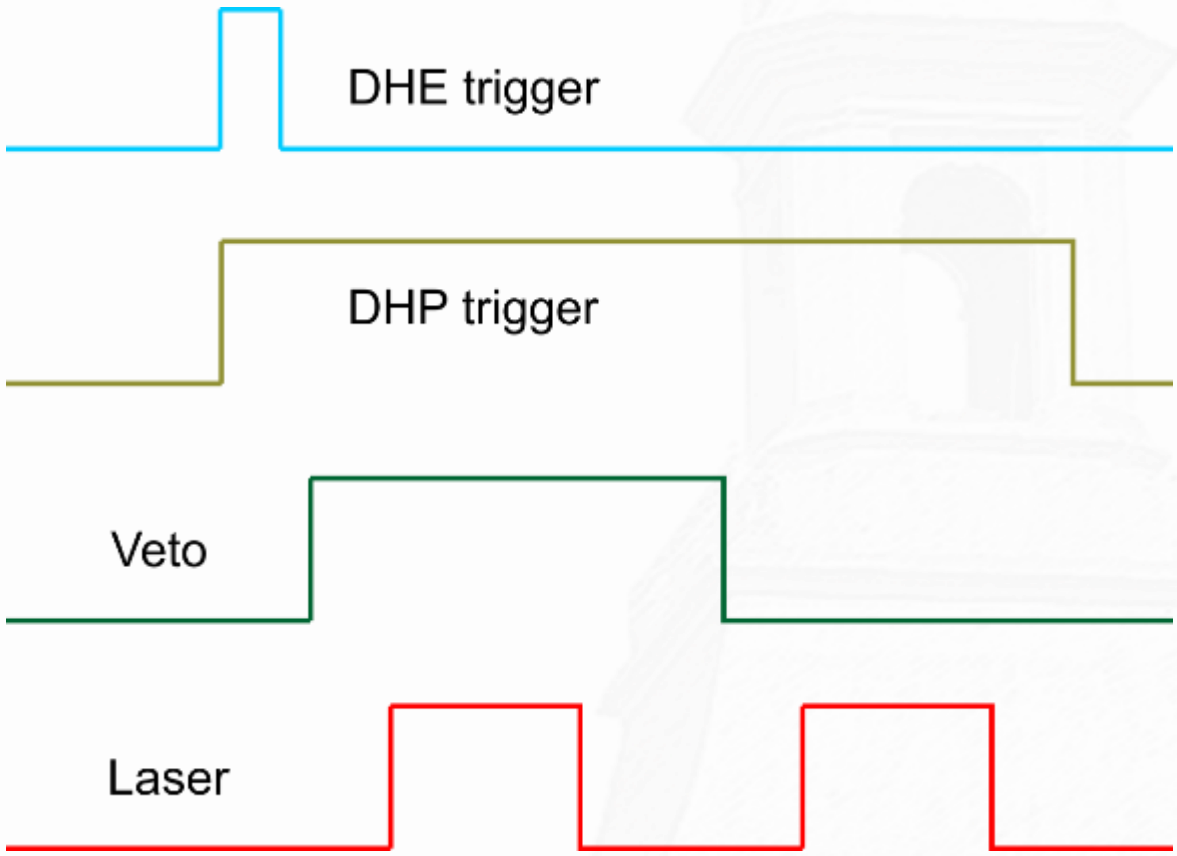
DHE memory sequence

At the start of the sequence the DHE receives the signal to expect data.

At the same time DHP trigger is switched on.

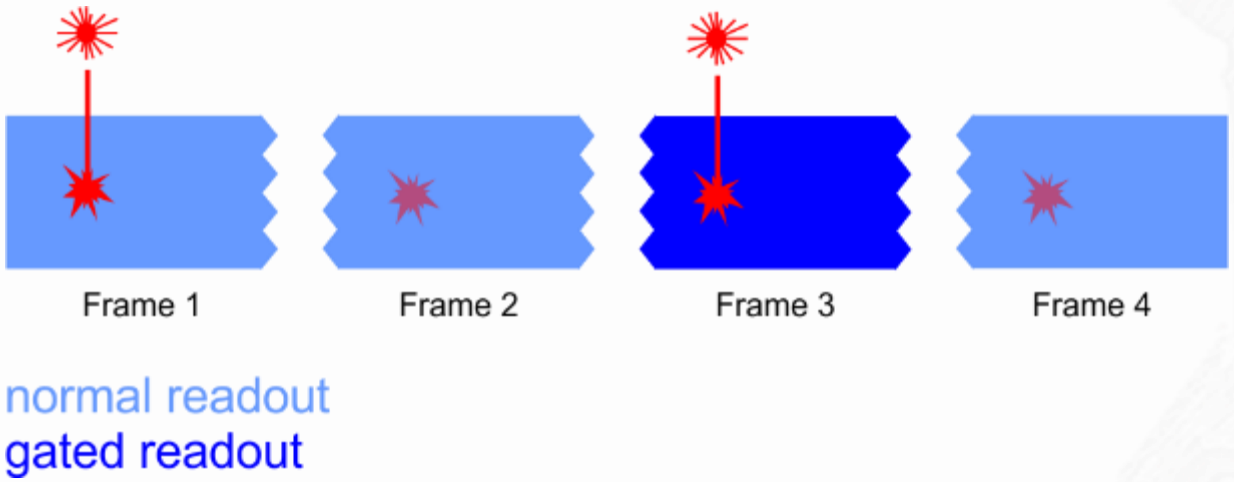
At some point gated mode is enabled by the veto signal.

Laser is shot twice once during gated mode and once during normal readout.



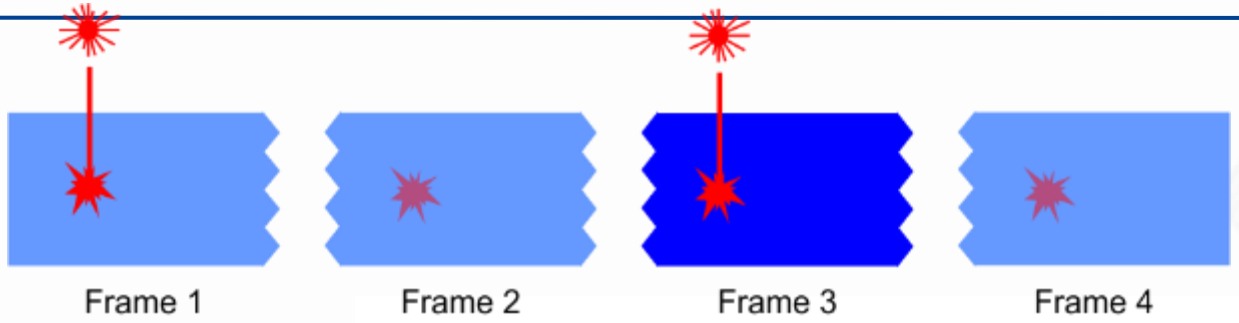
DHE sequence

DHE can be programed to follow a sequence, as soon as the gated mode is activated.



In Frame 1 the laser is fired.
In Frame 2 positions where the laser has been shot are checked for non cleared charge.
In Frame 3 the laser is fired again during gated mode.
In Frame 4 it is measured how much charge was injected, despite gated mode shielding.

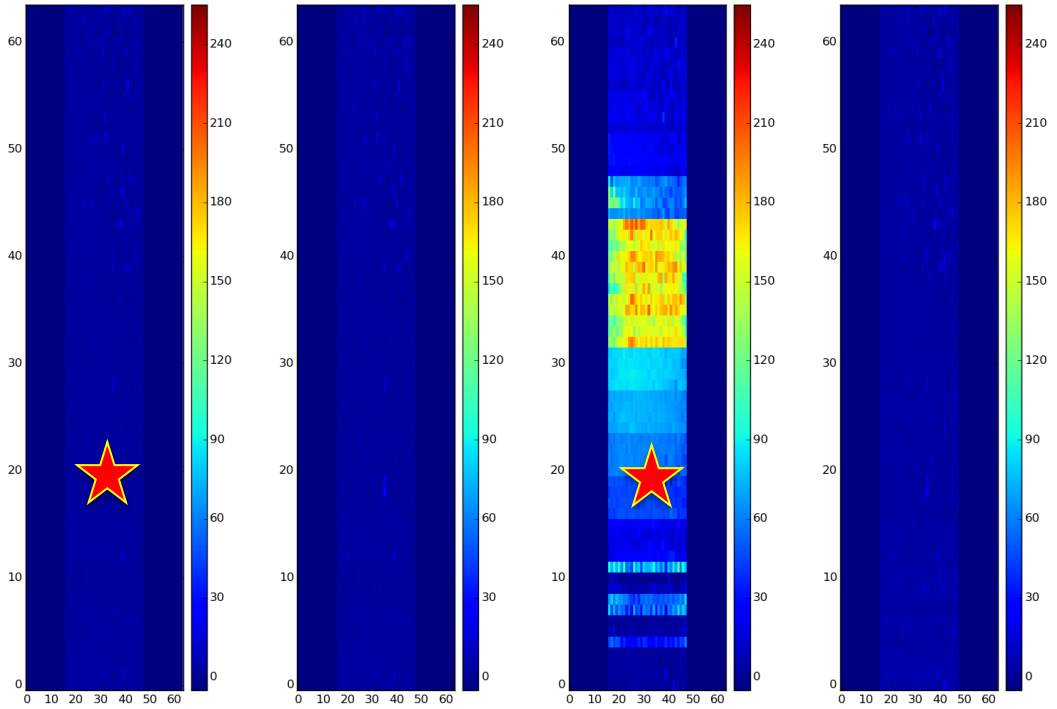
DHE sequence (2)



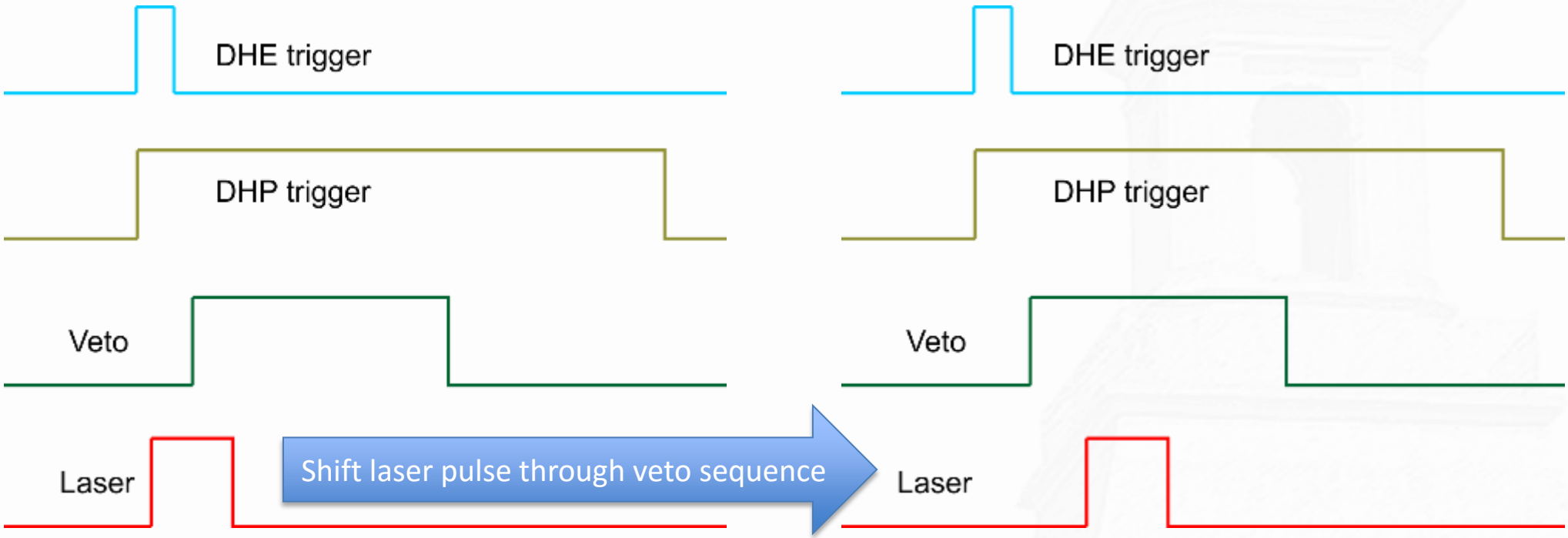
normal readout
gated readout

Laser is shot in Frame 1 and Frame 3.

Gated mode is activated in Frame 3 for 7 gates.



Laser delay measurement

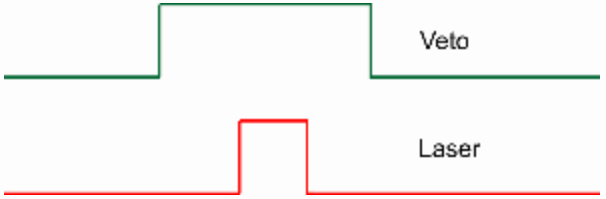


Start with laser pulses before the beginning of the gated mode sequence.
Then delay the laser until it hits in the gated mode sequence.

What do we expect?

1.) One shoots shortly **before** the gated mode sequence. The injected charge is measured twice. Once during gated mode and then again after gated mode.

2.) One shoots **during** gated mode. The injected charge is hindered from reaching the internal gate. Thus no signal is measured.

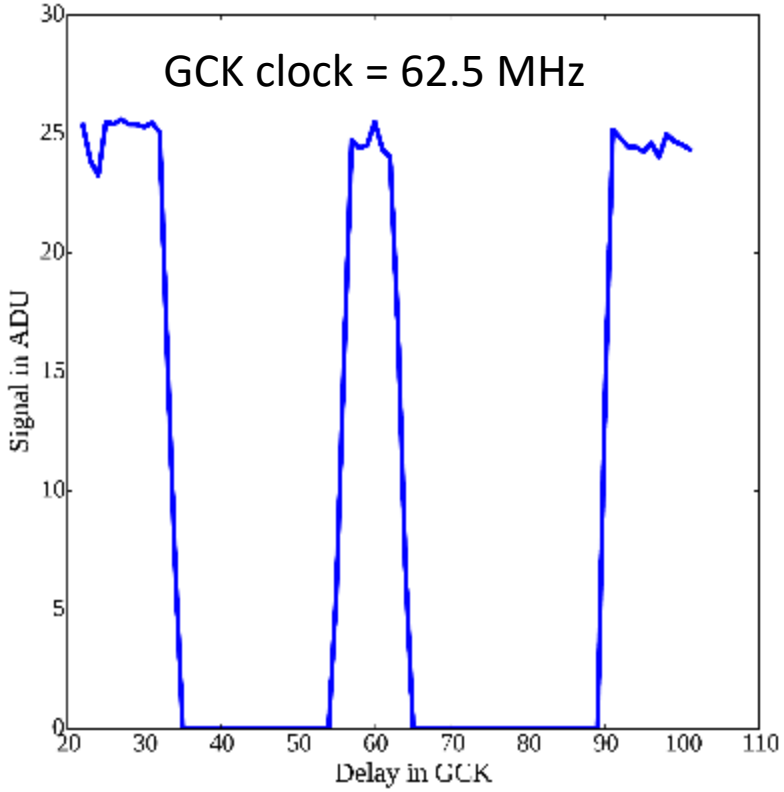


3.) One shoots **after** the gated mode sequence. The signal appears in the next frame.

The following measurements contain an offset of 3x8 = 24 GCK, obtained in separate measurements about laser delay!

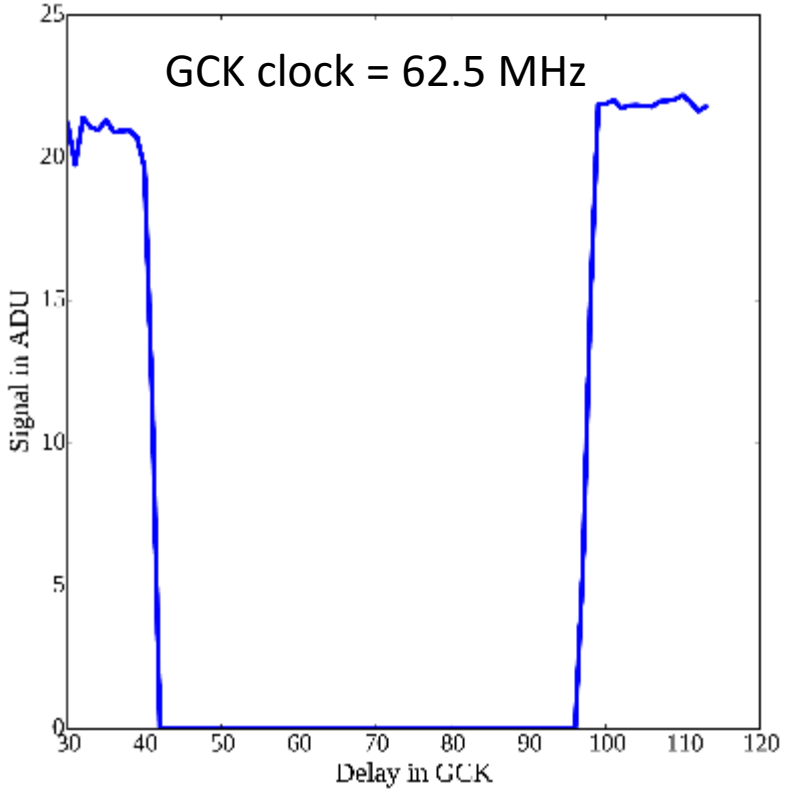
What do we see?

Pixel read out during gated mode operation



Plot only shows frame 4 for different laser delays!

Pixel outside of the read out region during gated mode operation



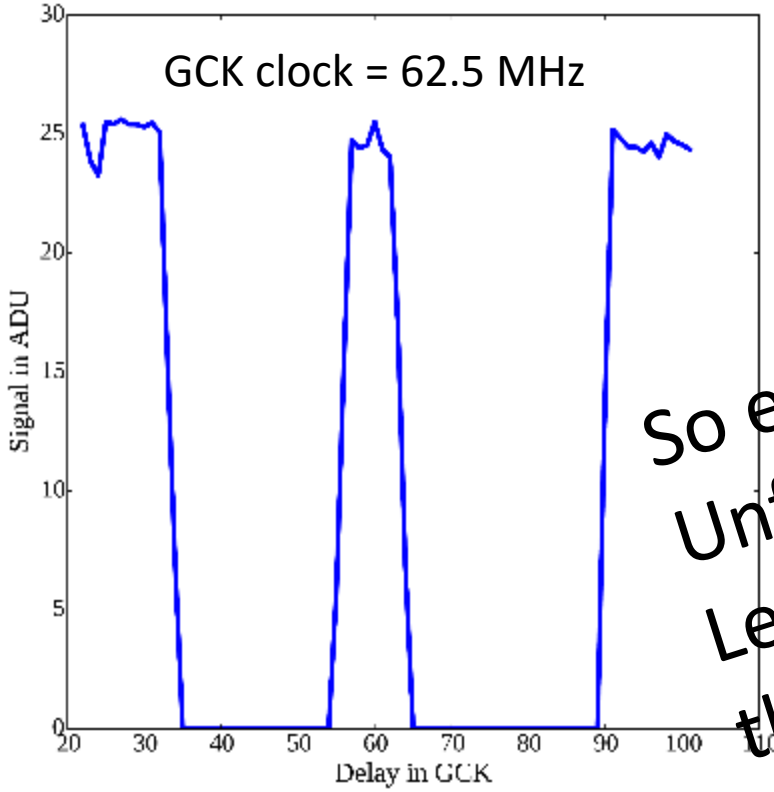
Time required to go into gated mode (starting when DHE signal is uploaded to the DHP): $\Delta t_{gate\_in} = (418 \pm 14)$ ns

Time required to go out of gated mode:

$\Delta t_{gate\_out} = (129 \pm 13)$ ns

What do we see?

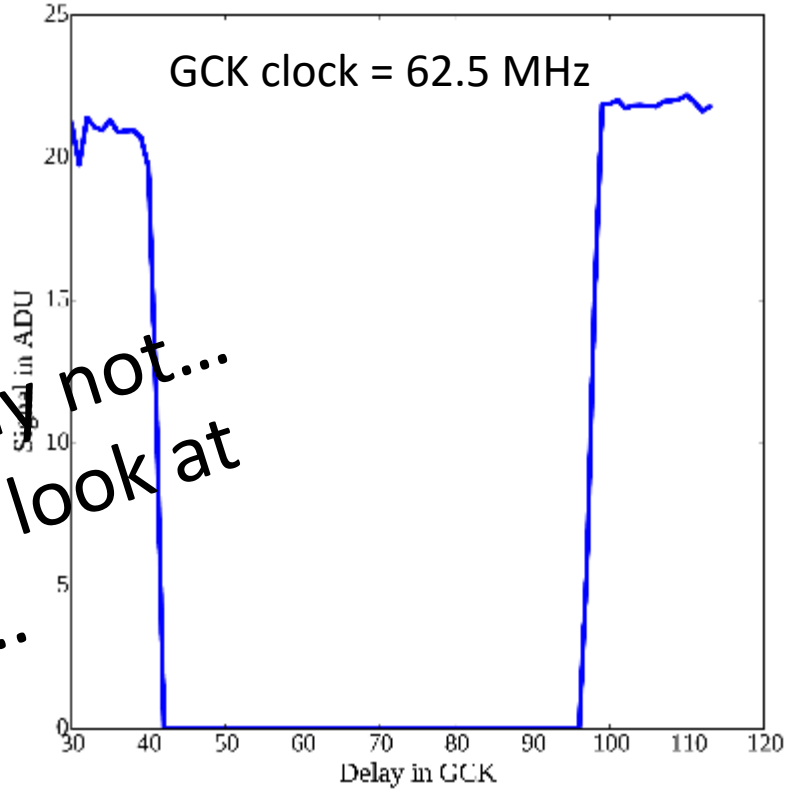
Pixel read out during gated mode operation



Plot only shows frame 4 for different laser delays!

So easy?
Unfortunately not…
Let's have a look at the details..

Pixel outside of the read out region during gated mode operation



Time required to go into gated mode (starting when DHE signal is uploaded to the DHP): $\Delta t_{gate\_in} = (418 \pm 14)$ ns

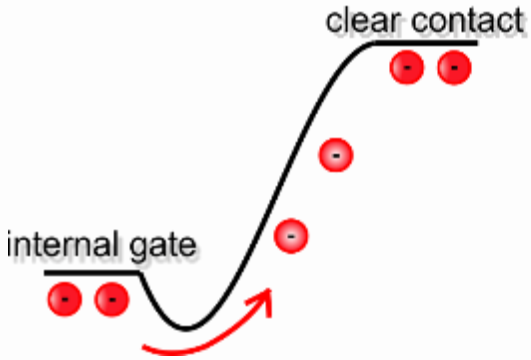
Time required to go out of gated mode:

$\Delta t_{gate\_out} = (129 \pm 13)$ ns

Clear high –gate off measurement (prerequisite)

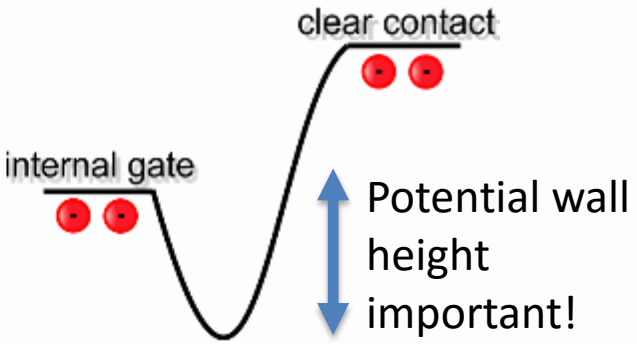
real clear

clear voltage high
gate voltage low



suppressed clear

clear voltage high
gate voltage high



Scan of clear low and clear high in search of optimal performance in both operation modes:

Gate Off: 2000 – 4500 mV
step size: 500 mV

Clear high: 15000 – 22000 mV
step size: 1000 mV

Complete set of standard voltages:

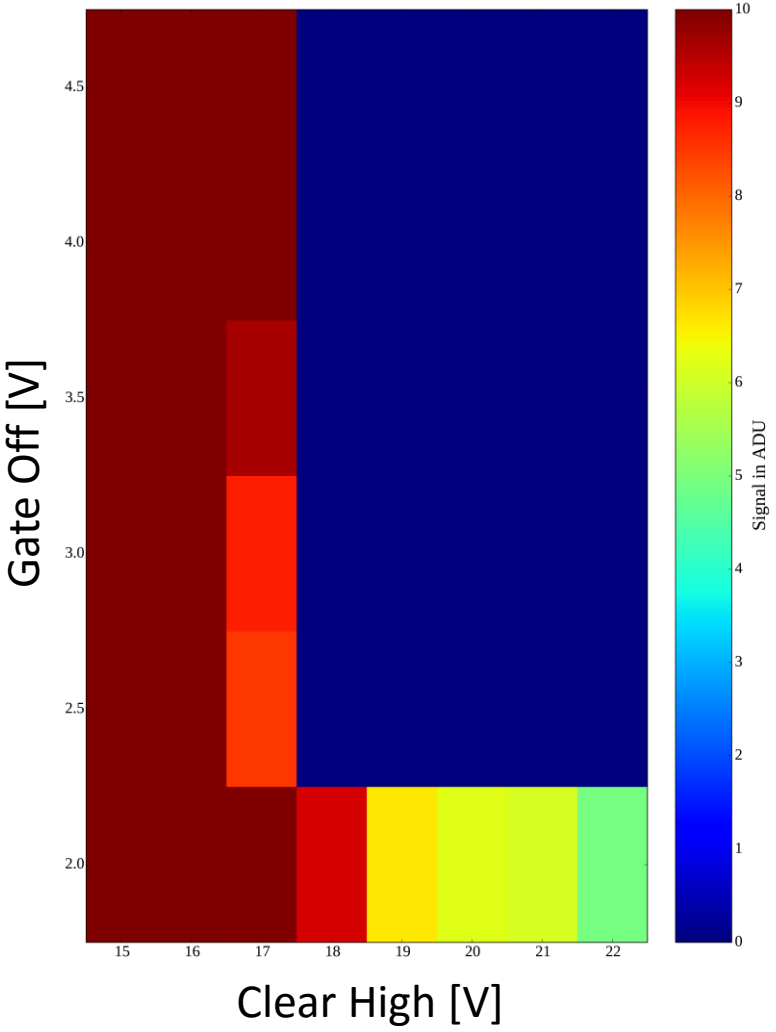
Source:	7000 mV
Gate off:	3000 mV
Gate on:	-2500 mV
Clear gate:	-1000 mV
Clear on:	19000 mV
Clear off:	6000 mV
High voltage:	-70000 mV
Drift:	-5000 mV

Clear high –gate off (outside pixel) shielding

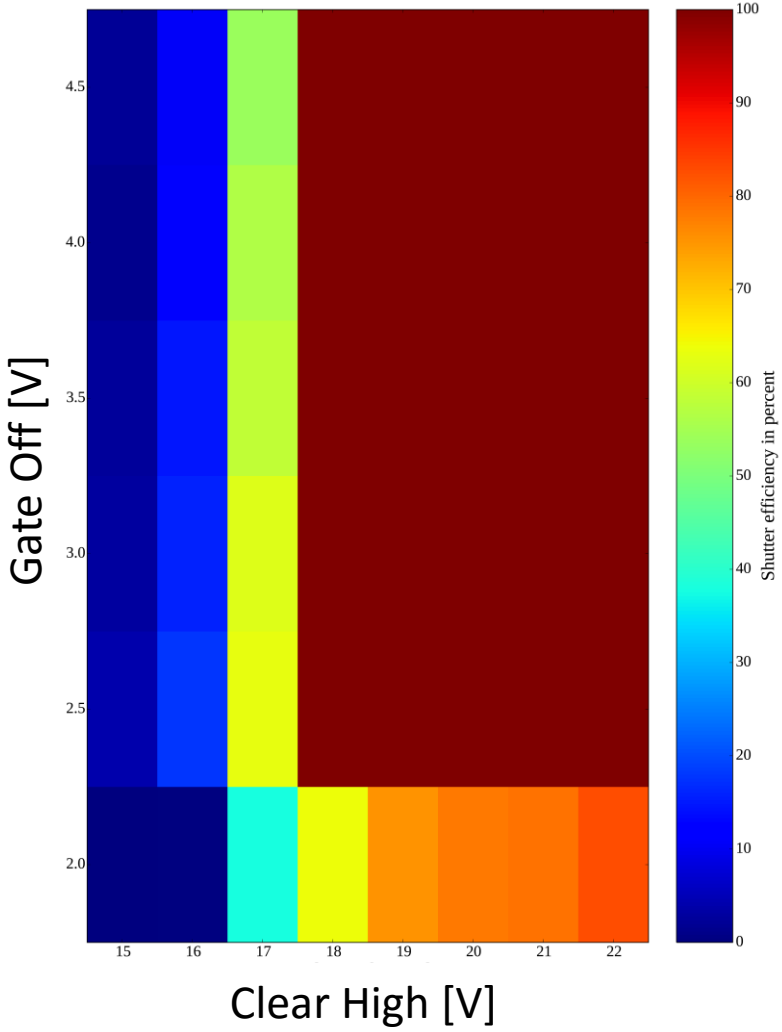
Laser shot during gated mode

With common mode correction without threshold

Measured signal [ADU]



Shutter efficiency [%]



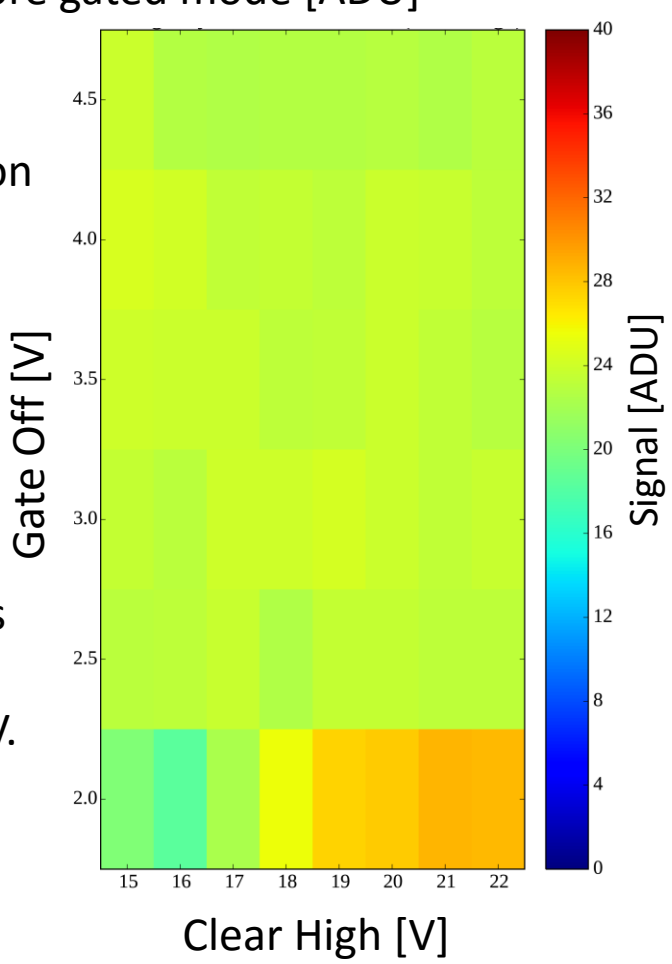
Clear high –gate off (outside pixel) charge preservation

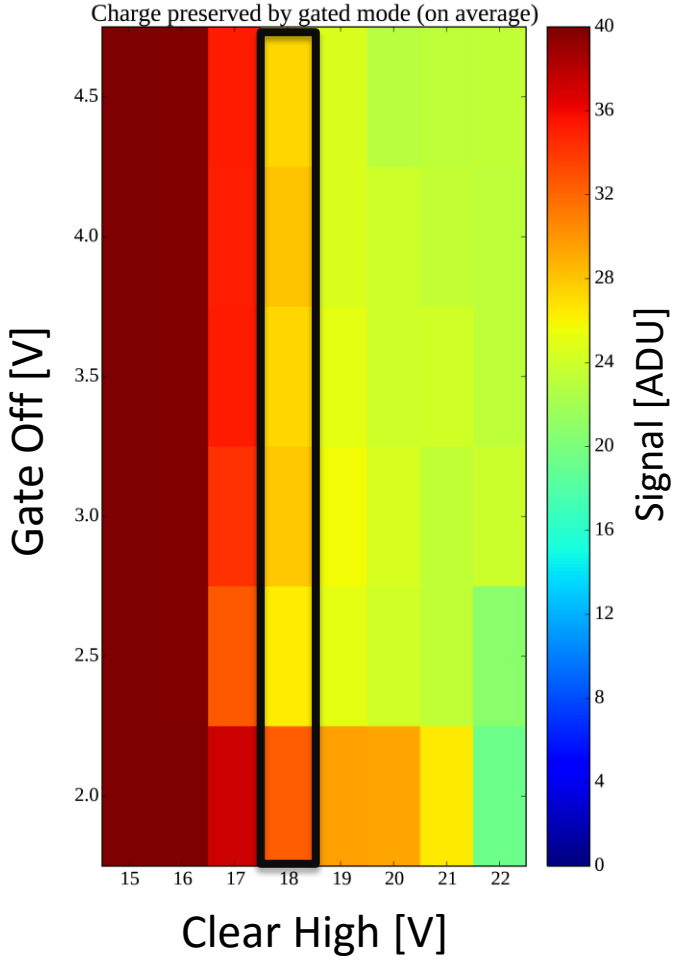
Measured signal with charged injected before gated mode [ADU]

Existing charge after gated mode [ADU]

With common mode correction and threshold of 4 ADU

Charge from previous frames remains in the internal gate, when ClearHigh is set to 18 V.

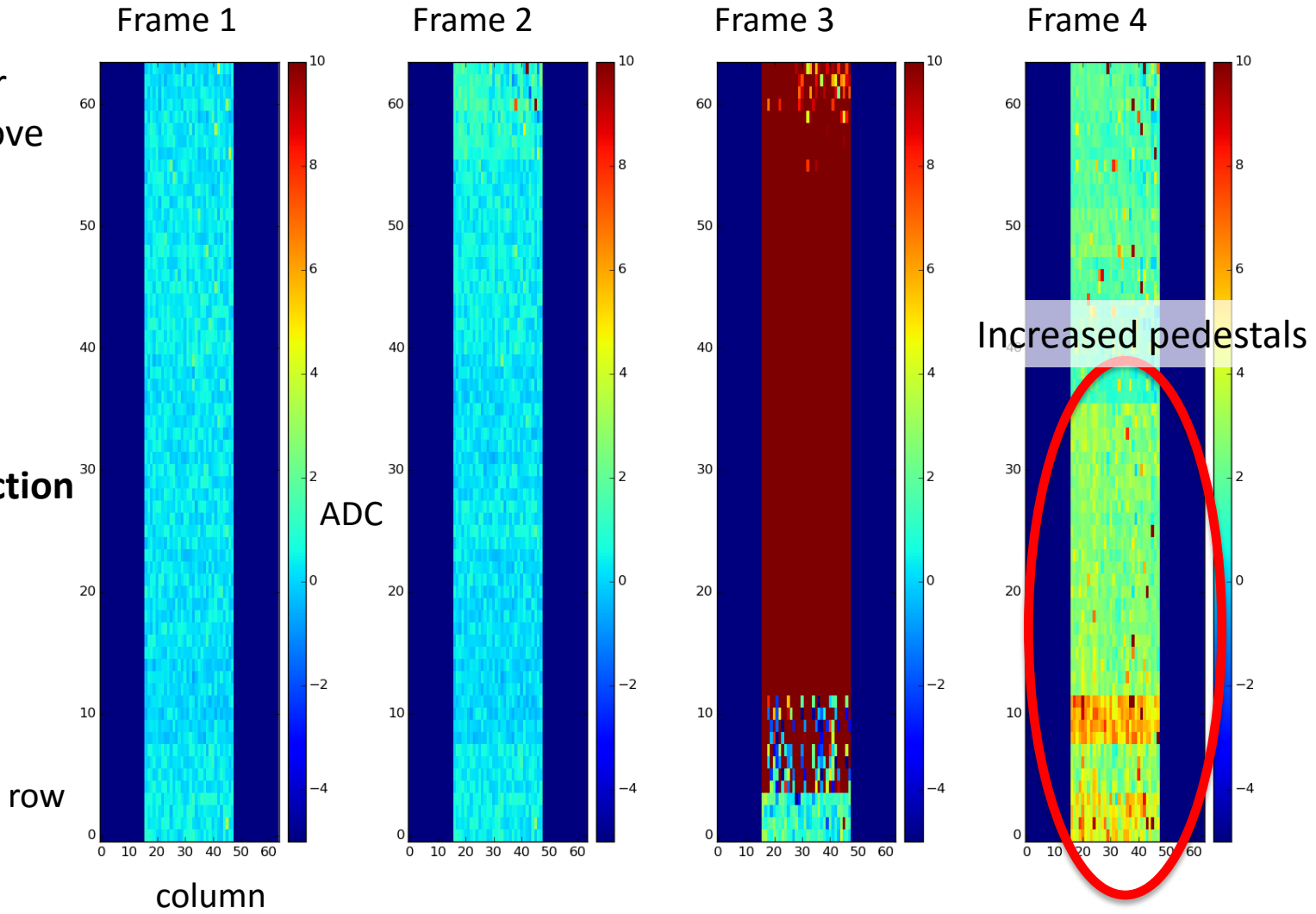




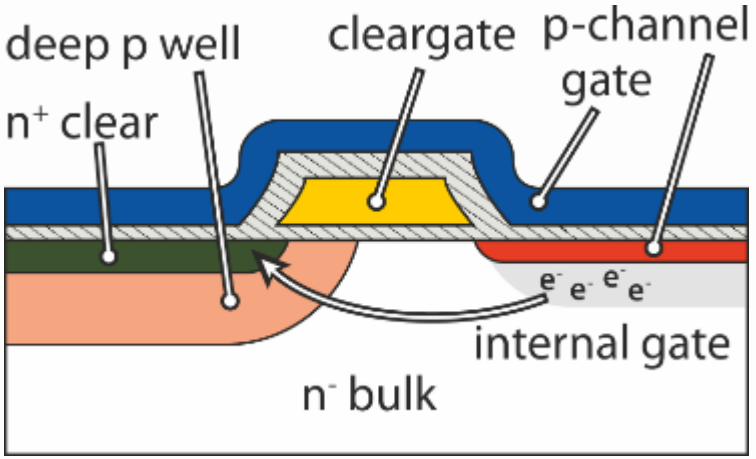
What challenges are there with gated mode?

Row number and time move upwards!

No common mode correction active!



Clear high –clear low measurement (prerequisite)



How to decrease the pedestal ringing?

Scan of clear low and clear high:

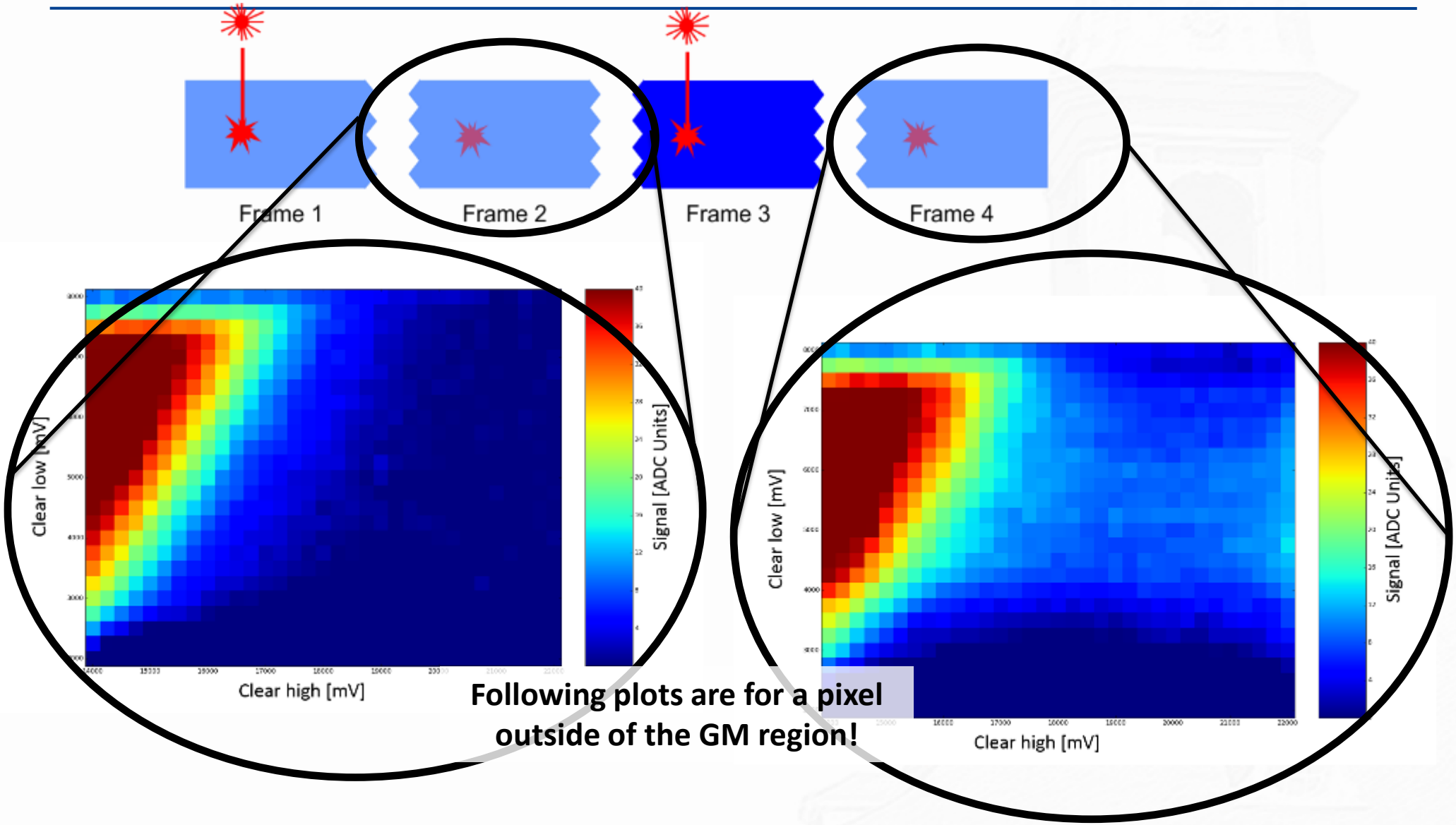
Clear low: 2000 – 6000 mV
step size: 250 mV

Clear high: 14000 – 22000 mV
step size: 250 mV

Complete set of standard voltages:

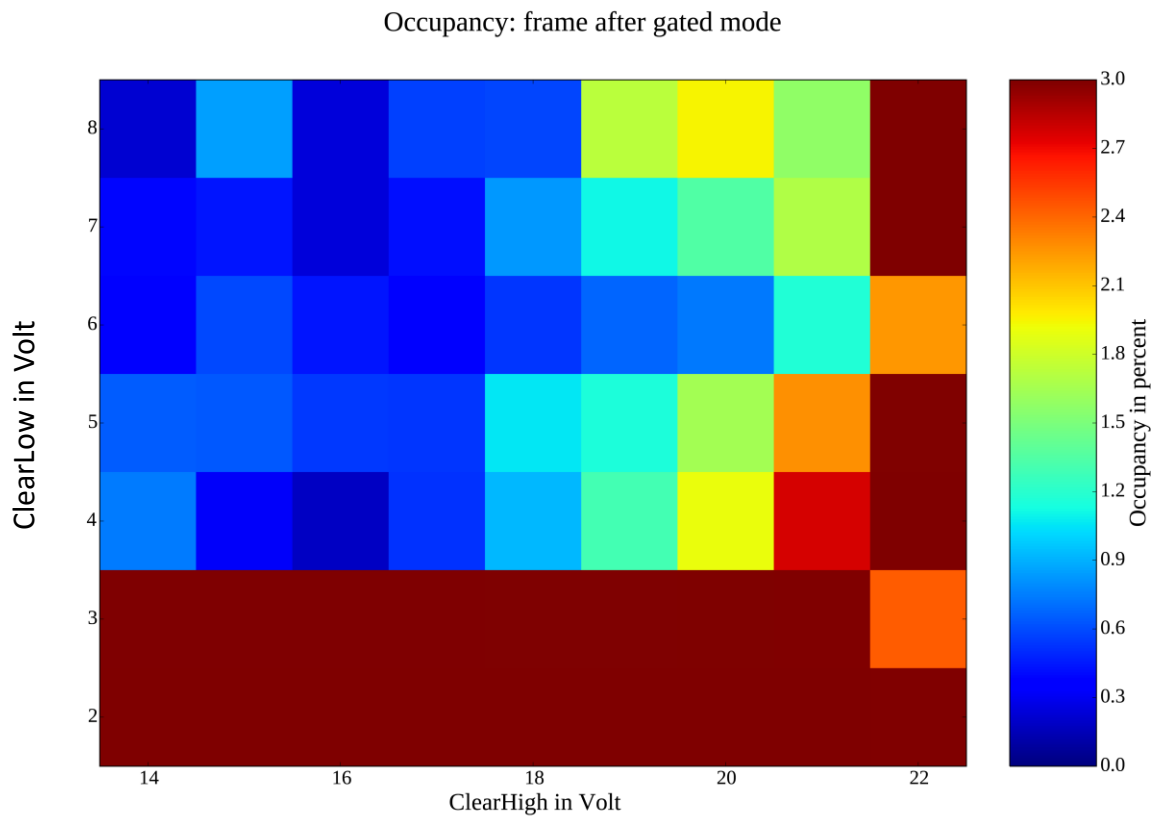
Source:	7000 mV
Gate off:	3000 mV
Gate on:	-2500 mV
Clear gate:	-1000 mV
Clear on:	19000 mV
Clear off:	6000 mV
High voltage:	-70000 mV
Drift:	-5000 mV

Clear high – clear low measurement

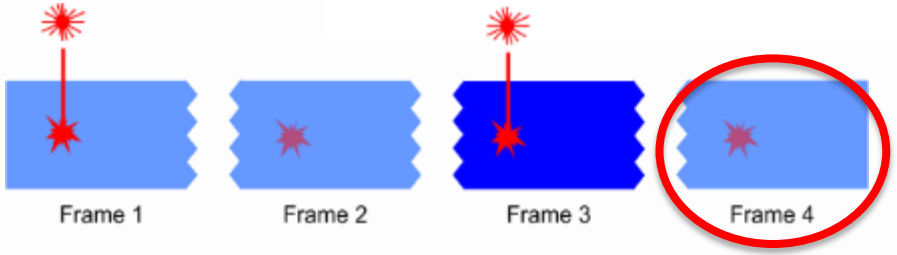


Following plots are for a pixel outside of the GM region!

Clear high – clear low measurement(2)

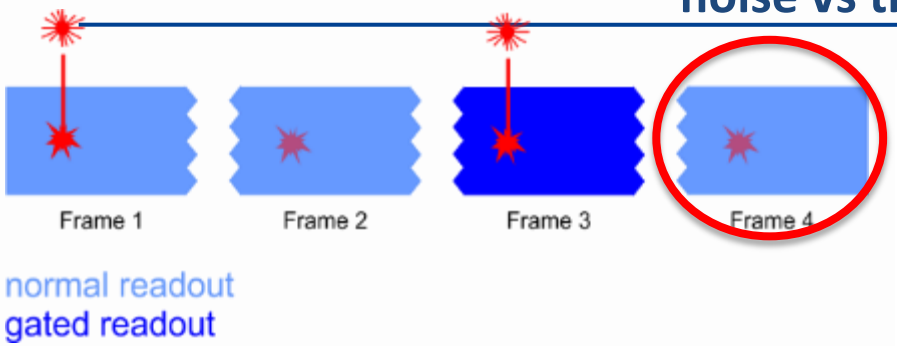


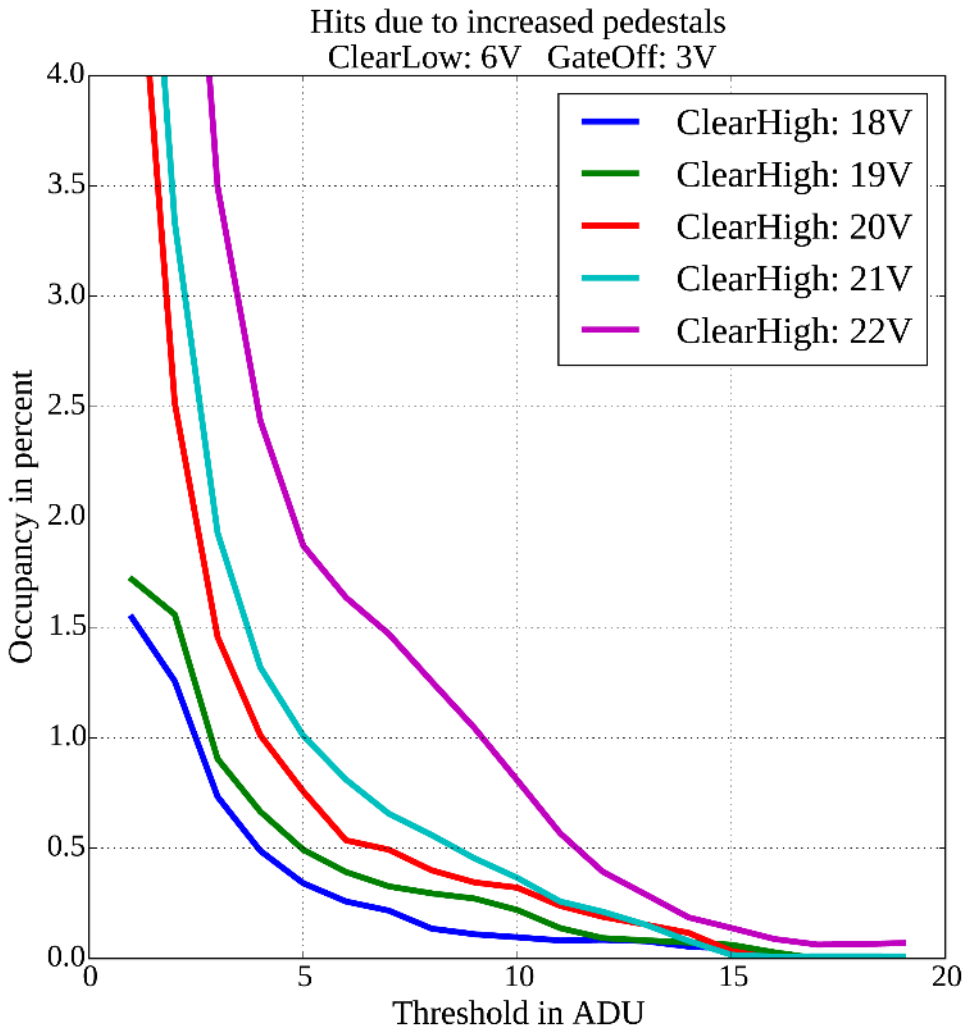
Common mode correction enabled and threshold is 4 ADU



Occupancy caused by **noise** (no laser shot) hits in Frame 4.

Clear high – clear low noise vs threshold

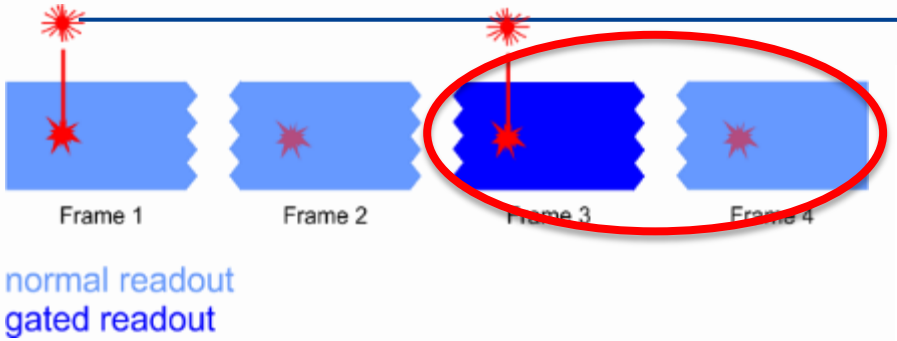




Occupancy caused by noise hits in Frame 4, i.e. frame after gated mode (the system had already some time to cool down).

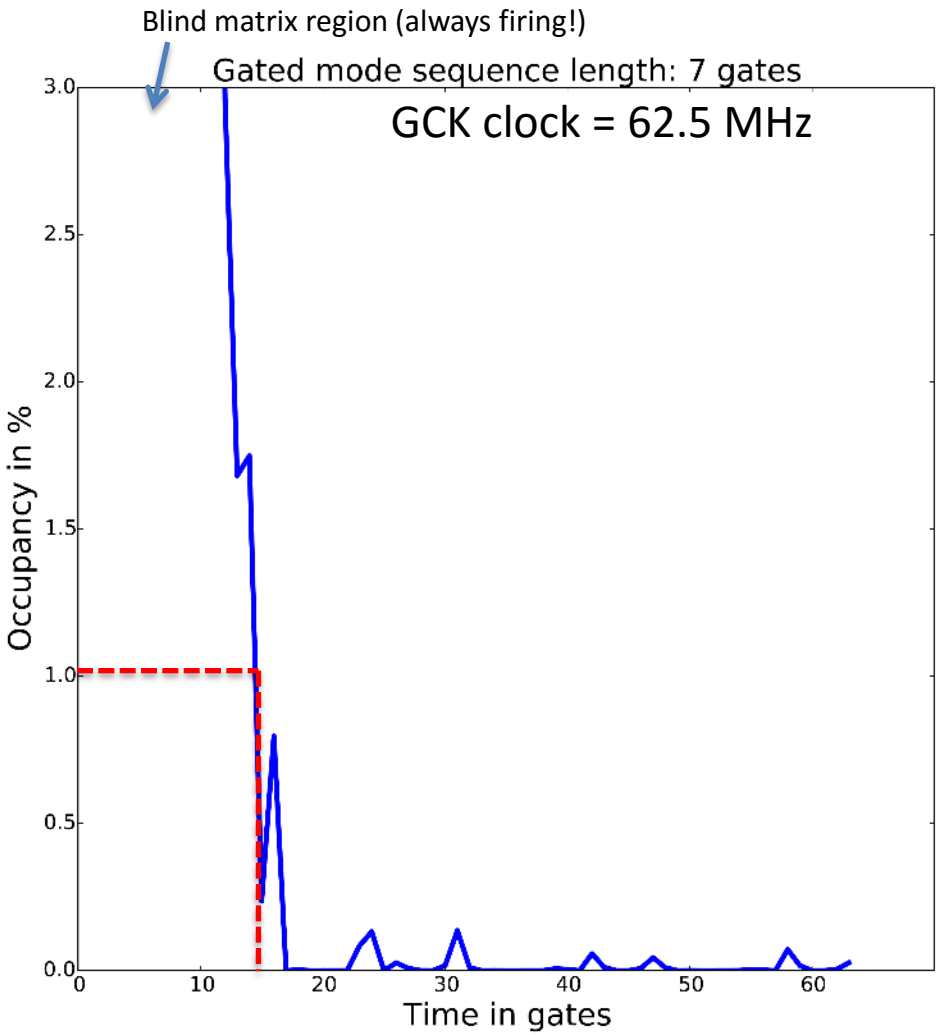
Starting from a ClearHigh voltage of 19 V the number of noise hits seems to saturate.

Cool down time

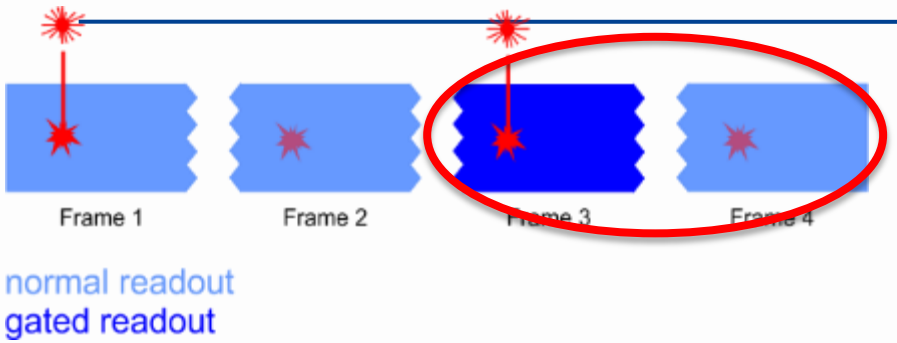


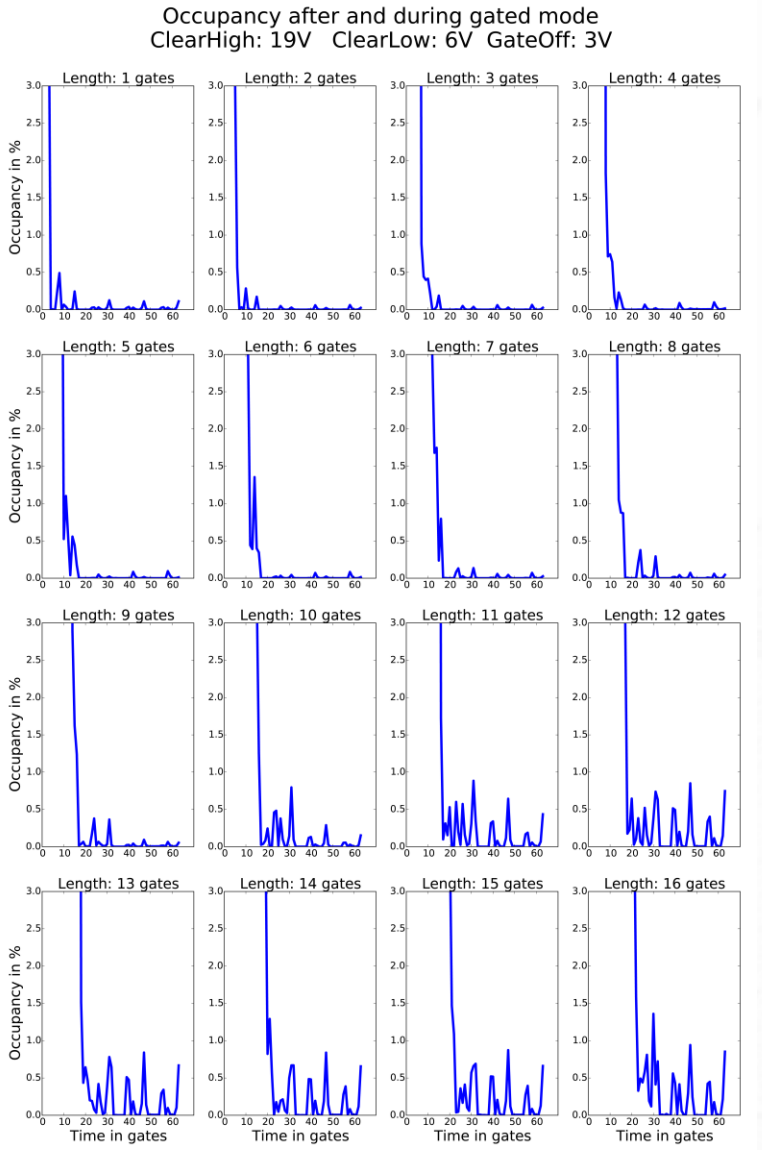
Occupancy caused by a gated mode sequence of length 7.

From the start of the gated mode sequence until occupancy is bellow 1% takes 15 gates. Subtracting the length of the sequence leaves 8 gates (~1 µs).
(Not counting time it takes to go in and out of gated mode.)



Cool down time: different gated mode sequence lengths





Time until cool down minus length of gated mode sequence gives on average:

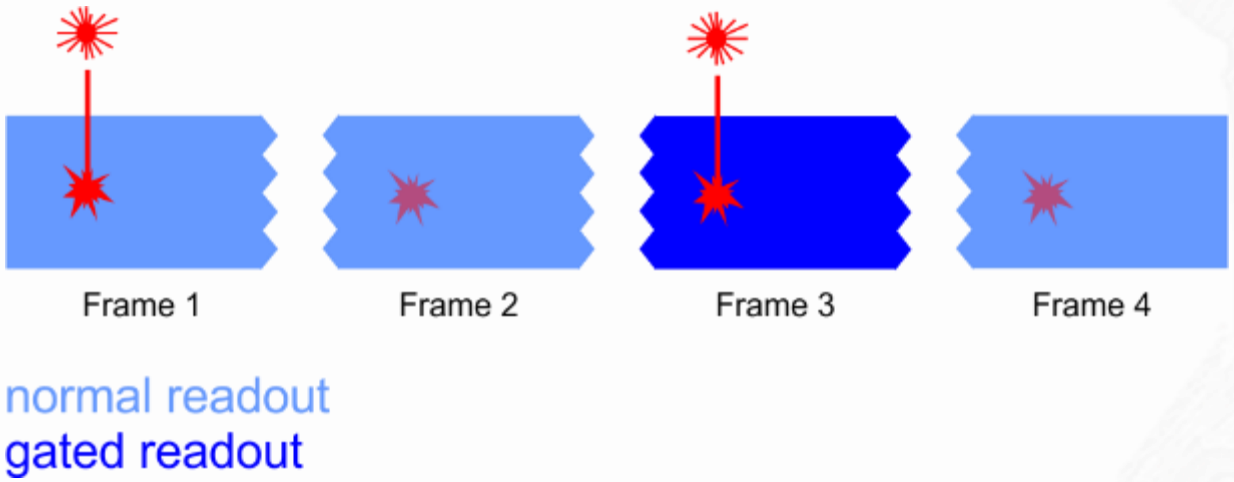
(6.5 ± 0.9) gates (~839 ns)

The length of the sequence is subtracted

Leaving out the sequence lengths from 1 to 4 gates in calculation.

DHE sequence

DHE can be programed to follow a sequence, as soon as the gated mode is activated.

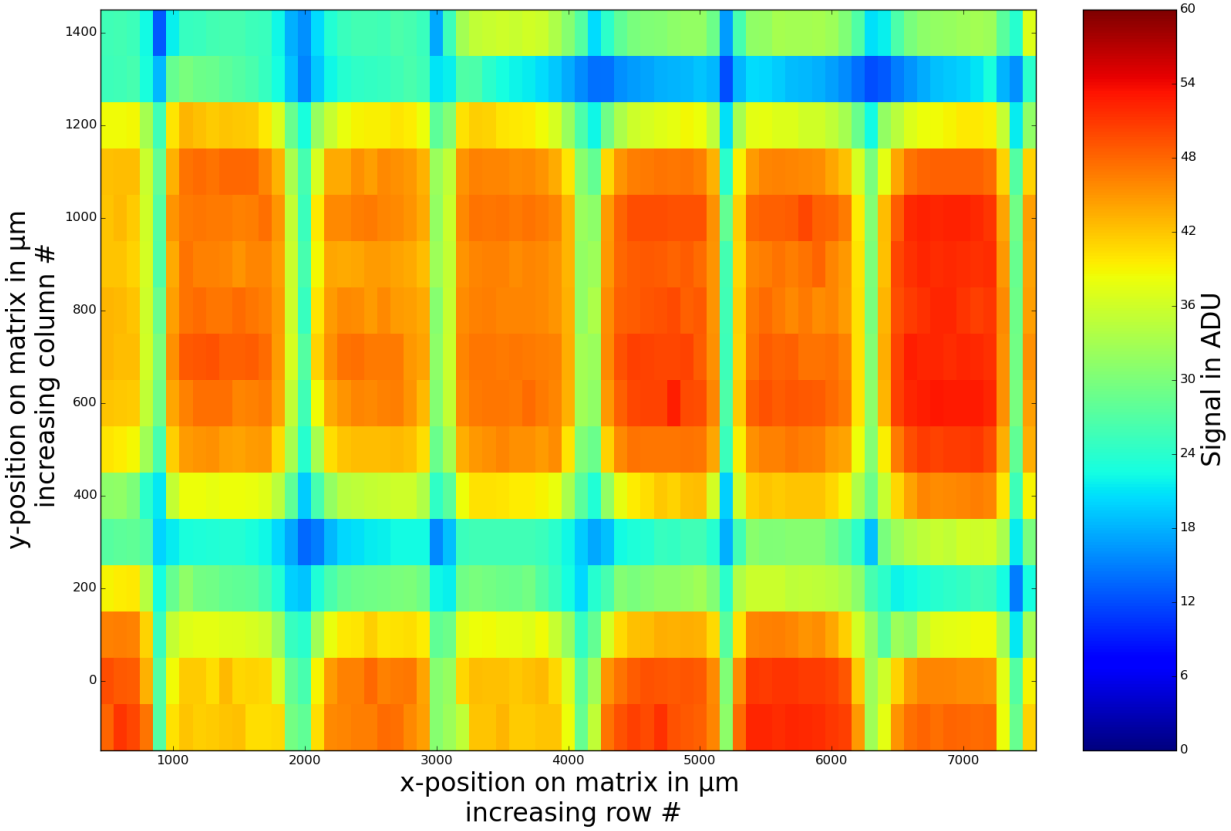


In Frame 1 the laser is fired.
In Frame 2 positions where the laser has been shot are checked for non cleared charge.
In Frame 3 the laser is fired again during gated mode.
In Frame 4 it is measured how much charge was injected, despite gated mode shielding.

Position dependent scans

How strongly does gated mode's performance depend on the location where charge is injected?

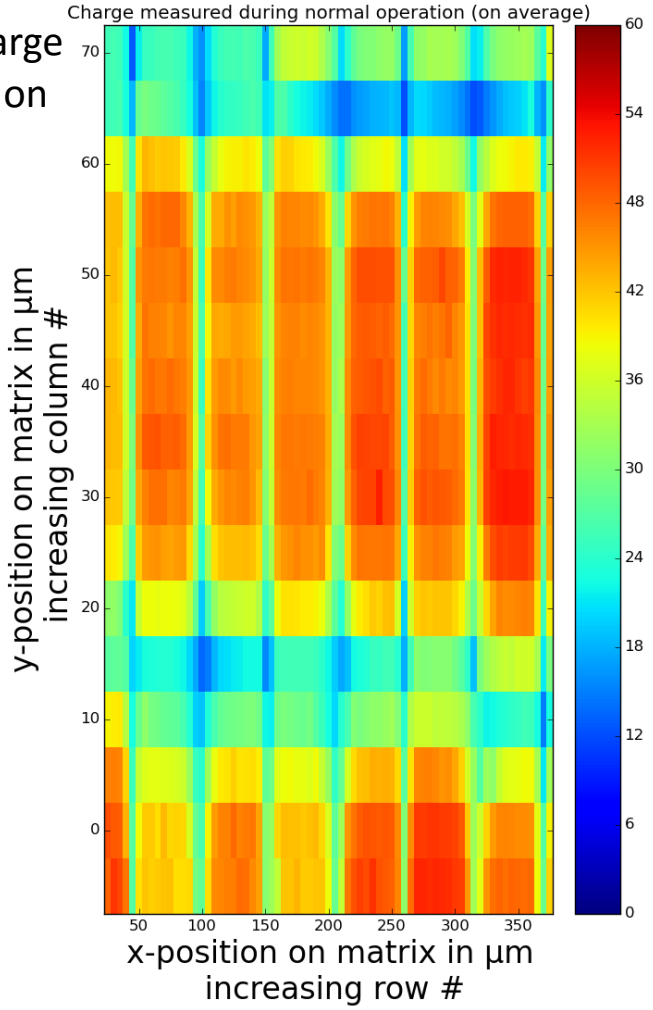
Pixel outside of gated region!

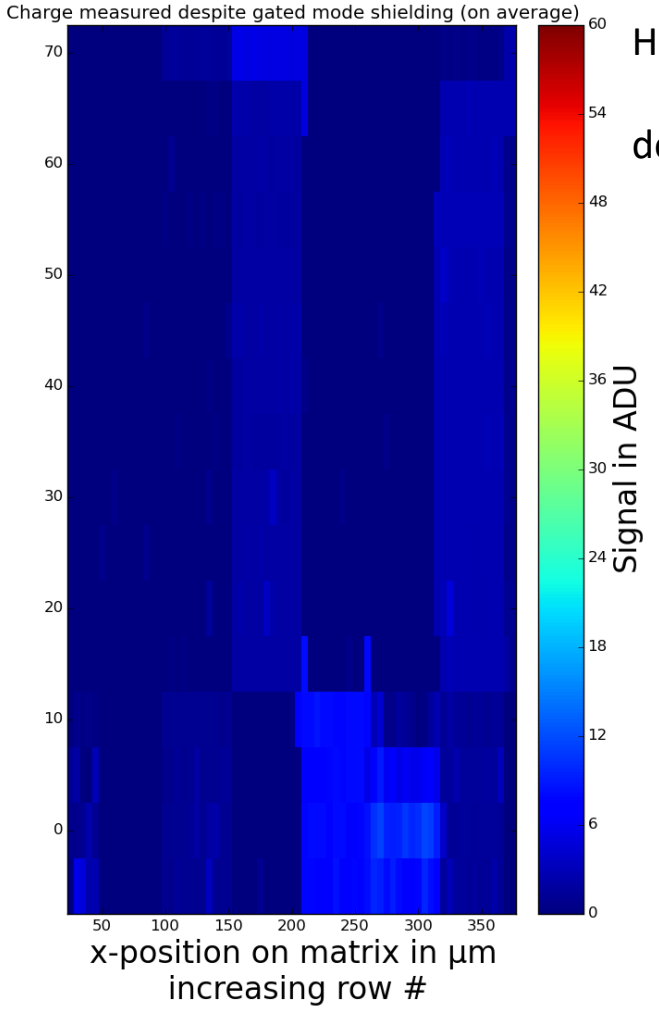


Seed signal (shielding) – laser shot for 4 GCK

Pixel **outside** of gated region!

Reference:
How much charge was injected, on average?



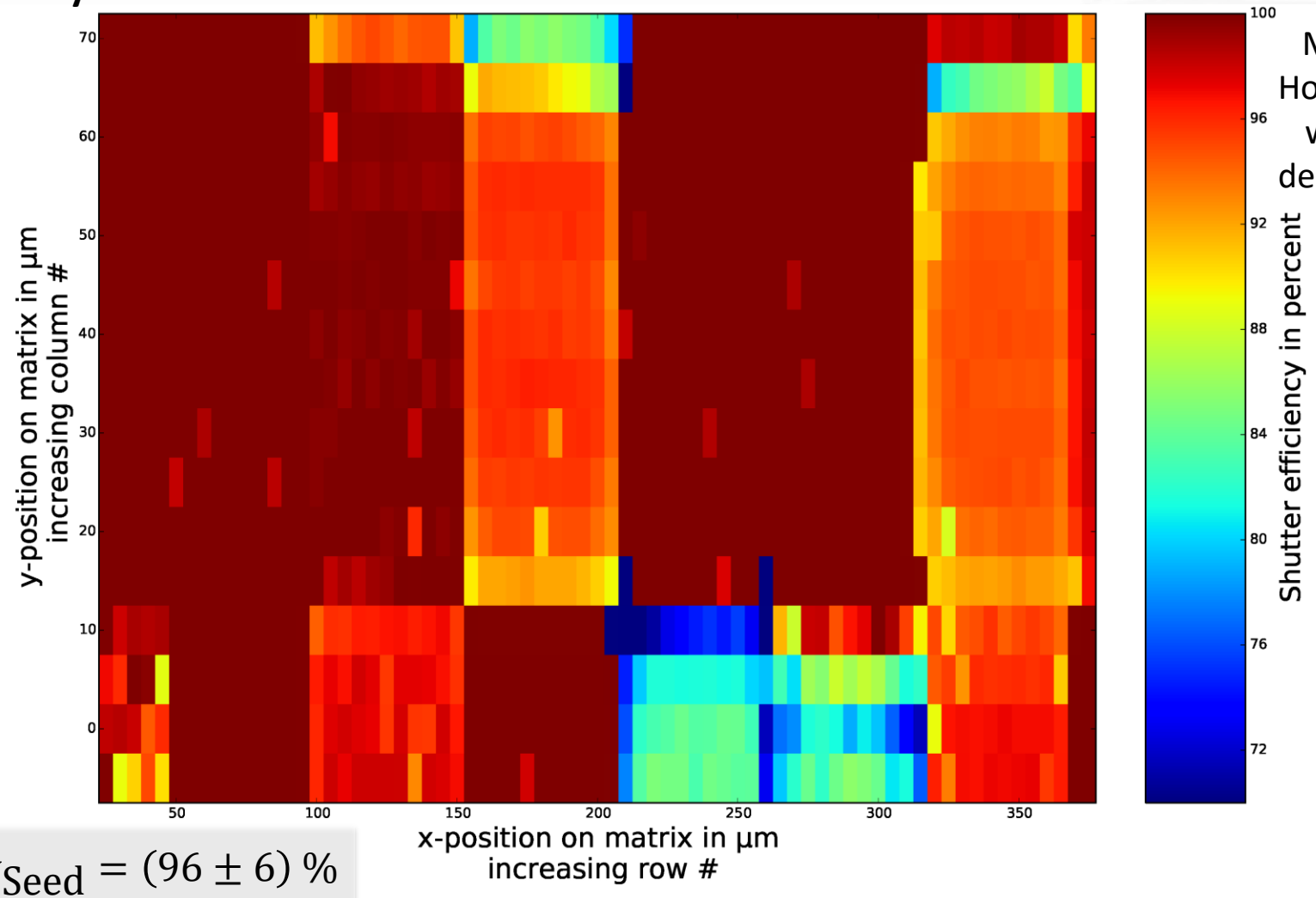


Measurement:
How much charge was measured despite shielding?

Seed signal (shielding) – laser shot for 4 GCK

GM efficiency

Pixel **outside** of gated region!



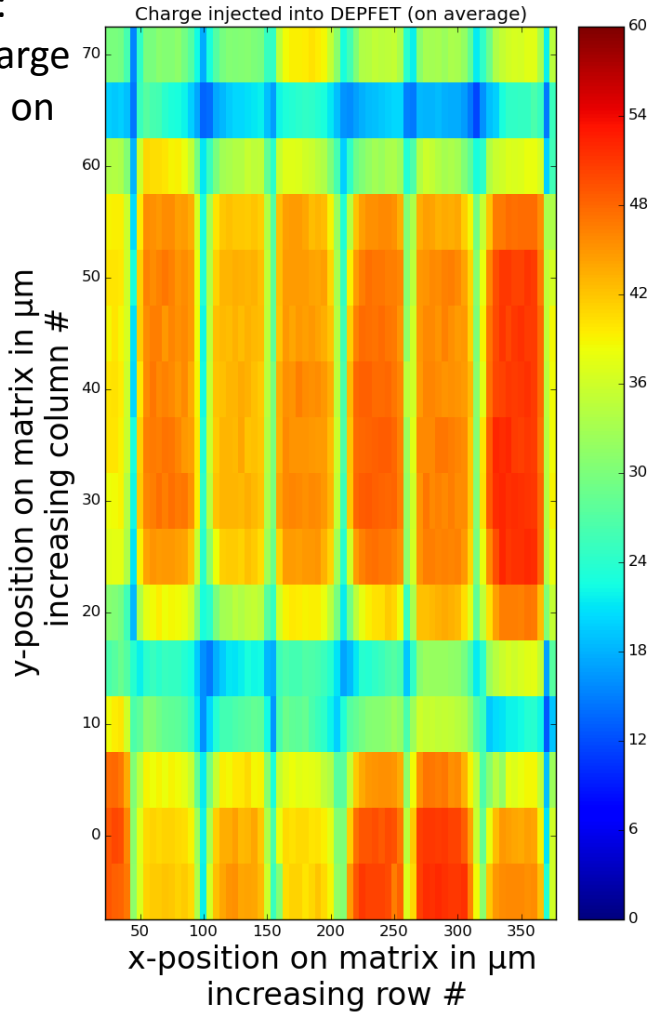
Measurement:
How much charge was measured despite shielding?

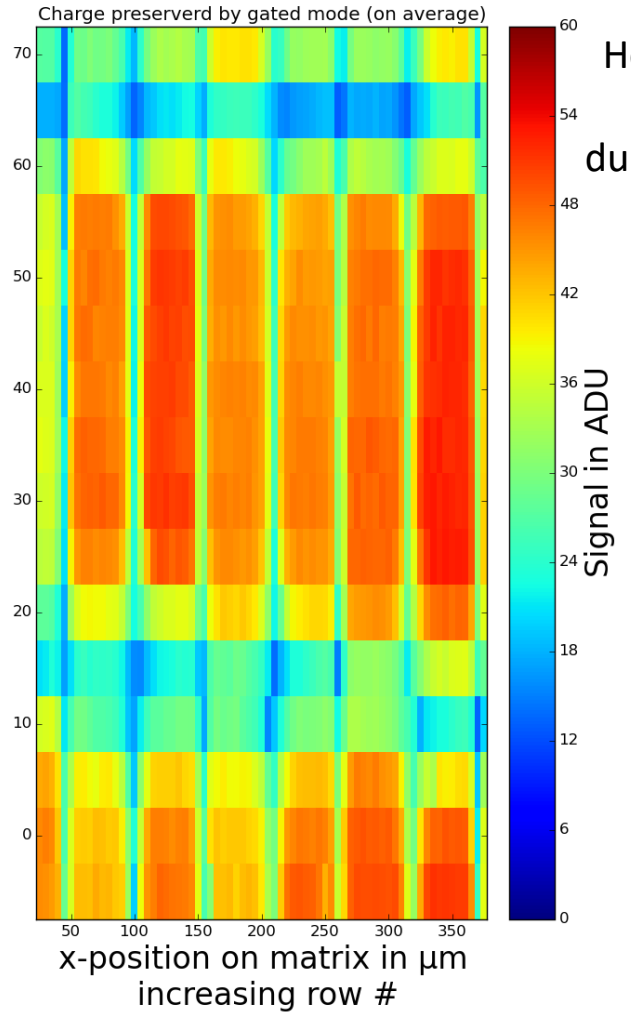
$$\text{Efficiency}_{\text{Seed}} = (96 \pm 6)\ \%$$

Seed signal (preservation) – laser shot for 4 GCK

Pixel **outside** of gated region!

Reference:
How much charge was injected, on average?



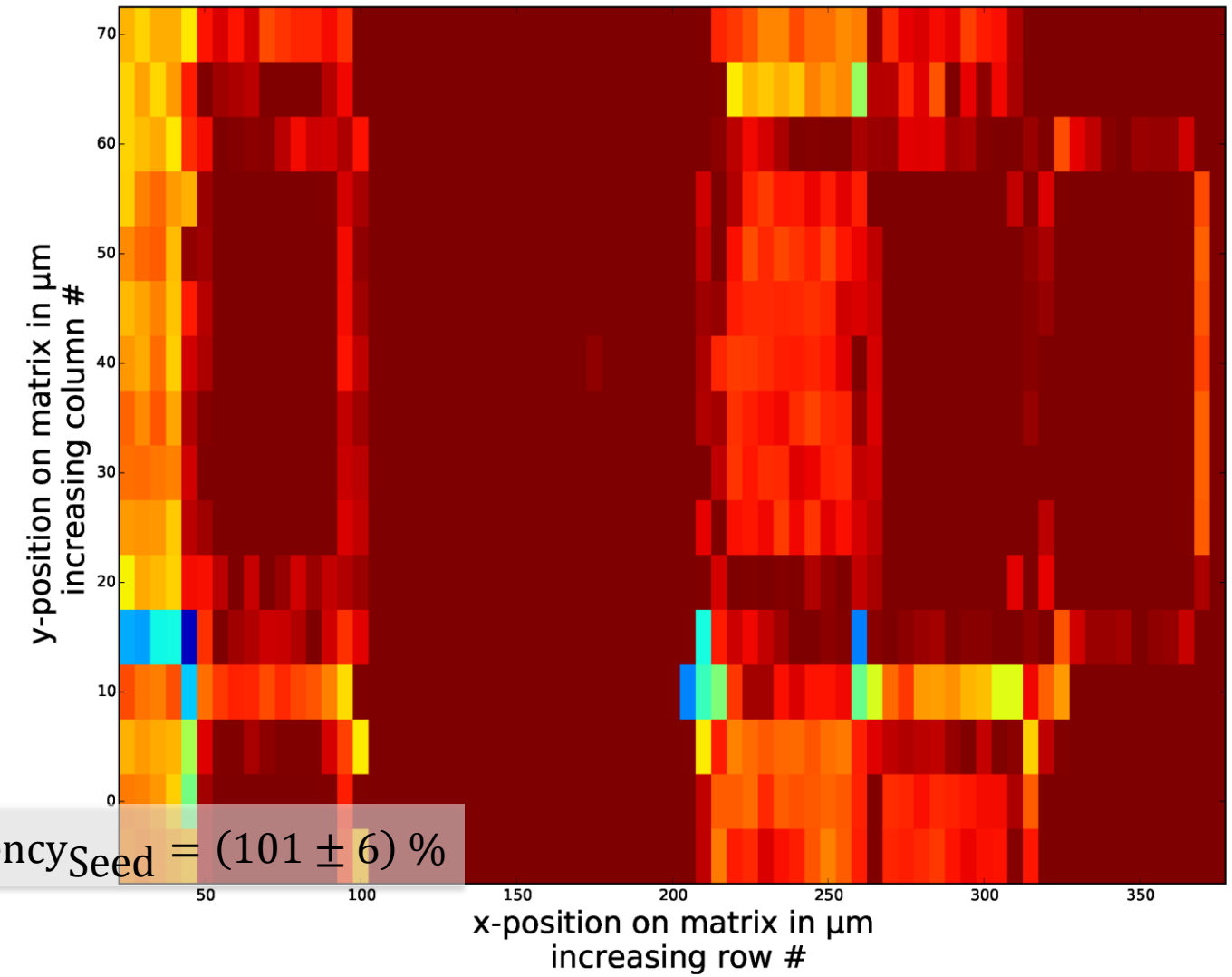


Measurement:
How much charge was preserved during gated mode?

Seed signal (preservation) – laser shot for 4 GCK

GM efficiency

Pixel **outside** of gated region!



Measurement: How much charge was measured despite shielding?

$\text{Efficiency}_{\text{Seed}} = (101 \pm 6)\ \%$

Outlook and conclusion

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Measurements:

How DEPFET behaves while going in and out of gated mode:

→ Pedestal increase due to quick switching of clear signal when going out of gated mode

How gate off voltage influences shielding efficiency.

→ Minimal gate off voltage required

How clear low and clear high influence gated mode performance:

→ Gated mode sets an upper limit for clear high

Position dependent performance measurements:

→ Differences between pixels, but location where charge is injected inside a pixel not important

Still needed are position dependent optimization of clear low, clear high and gate off voltage!

Next step

Cool down measurement with **large** matrix using the following set of optimized voltages

Source:	7000 mV
Gate off:	3000 mV
Gate on:	-2500 mV
Clear gate:	-1000 mV
Clear on:	19000 mV
Clear off:	6000 mV
High voltage:	-70000 mV
Drift:	-5000 mV

Minimal pedestal ringing, complete charge preservation and fully efficient shutter

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Thank you

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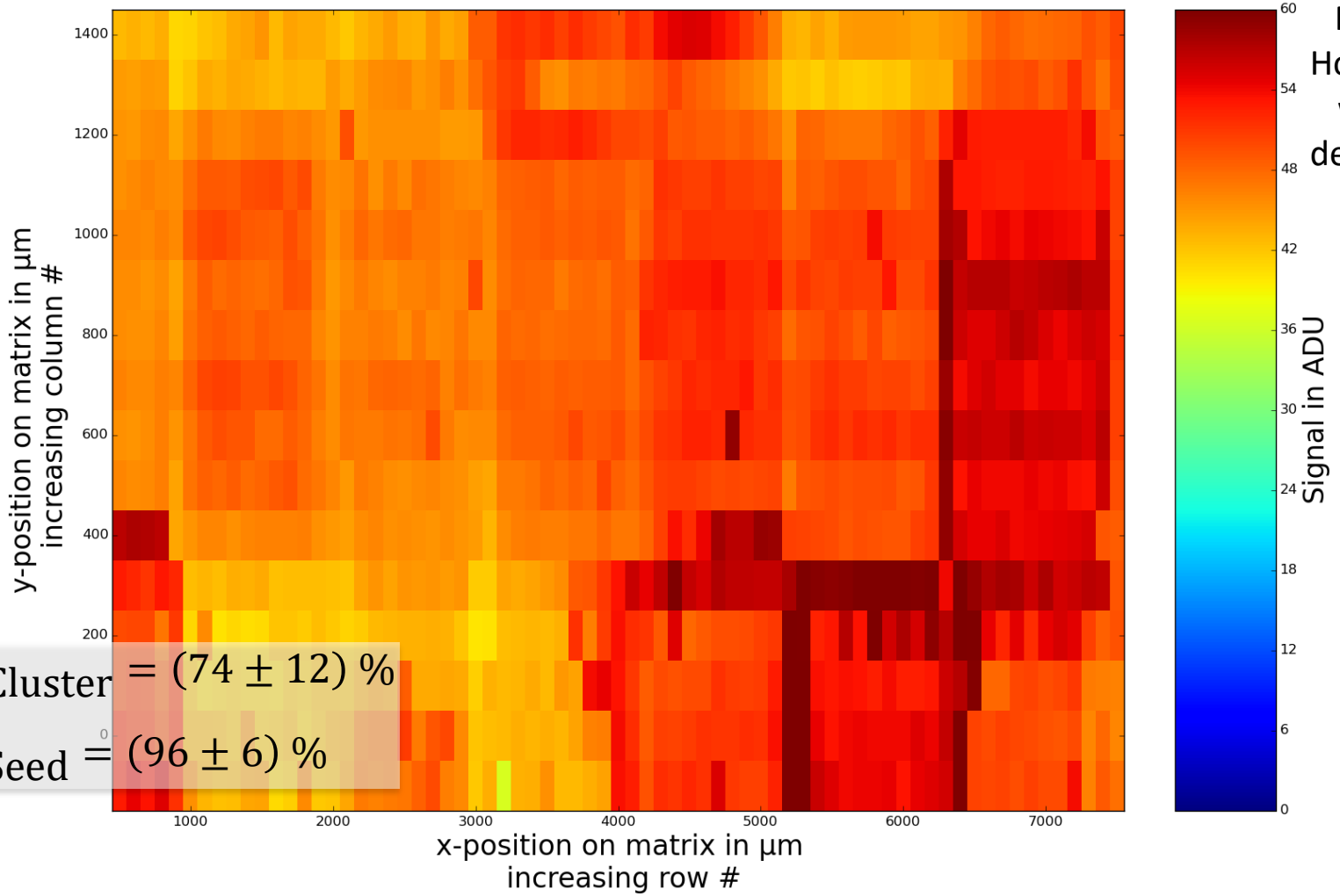
Backup

Cluster signal (shielding) – laser shot for 4 GCK

Pixel **outside** of gated region!

GM efficiency



Measurement: How much charge was measured despite shielding?

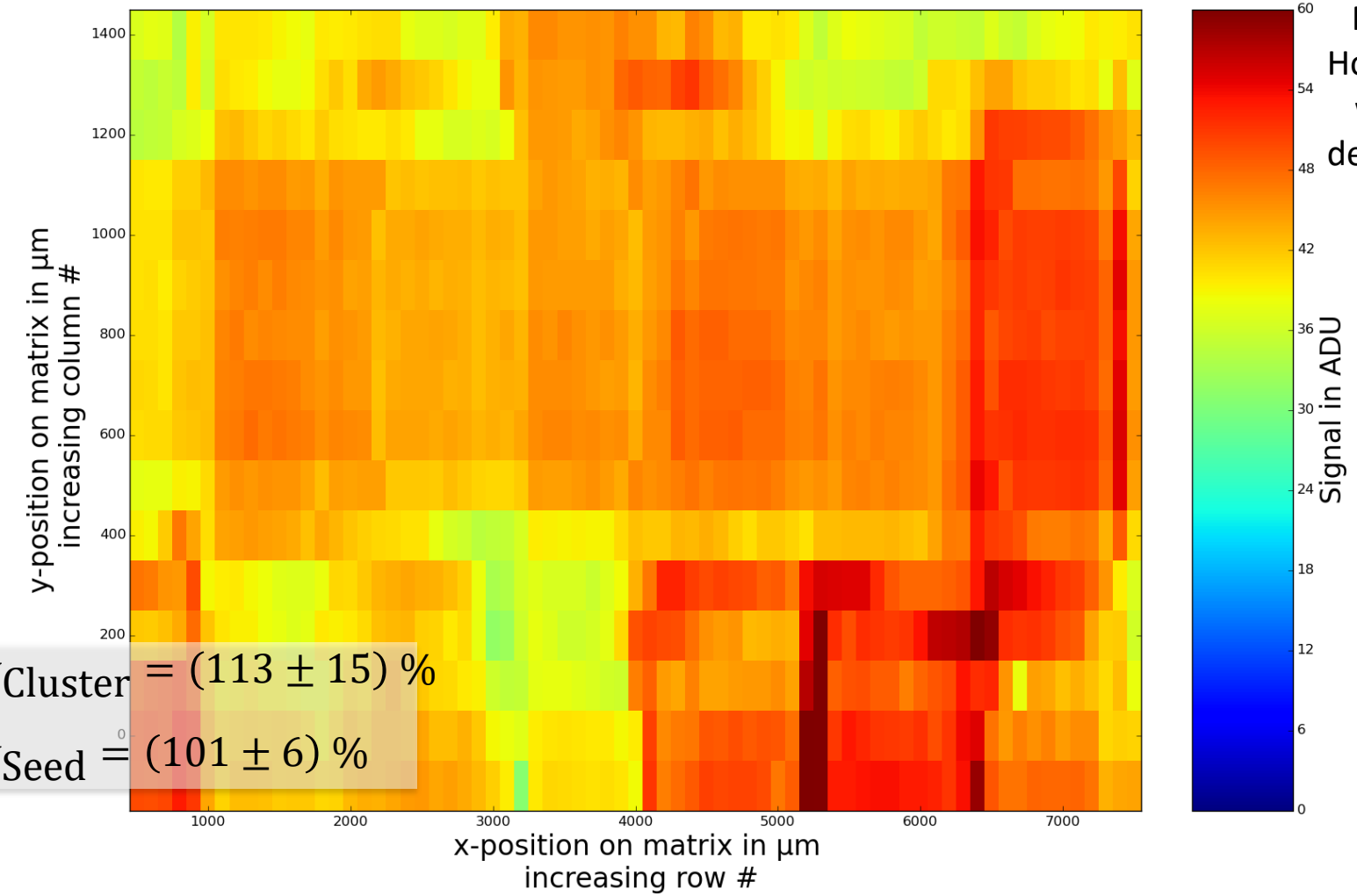
$$\text{Efficiency}_{\text{Cluster}} = (74 \pm 12)\ \%$$

$$\text{Efficiency}_{\text{Seed}} = (96 \pm 6)\ \%$$

Cluster signal (preservation) – laser shot for 4 GCK

Pixel **outside** of gated region!

GM efficiency



Measurement: How much charge was measured despite shielding?

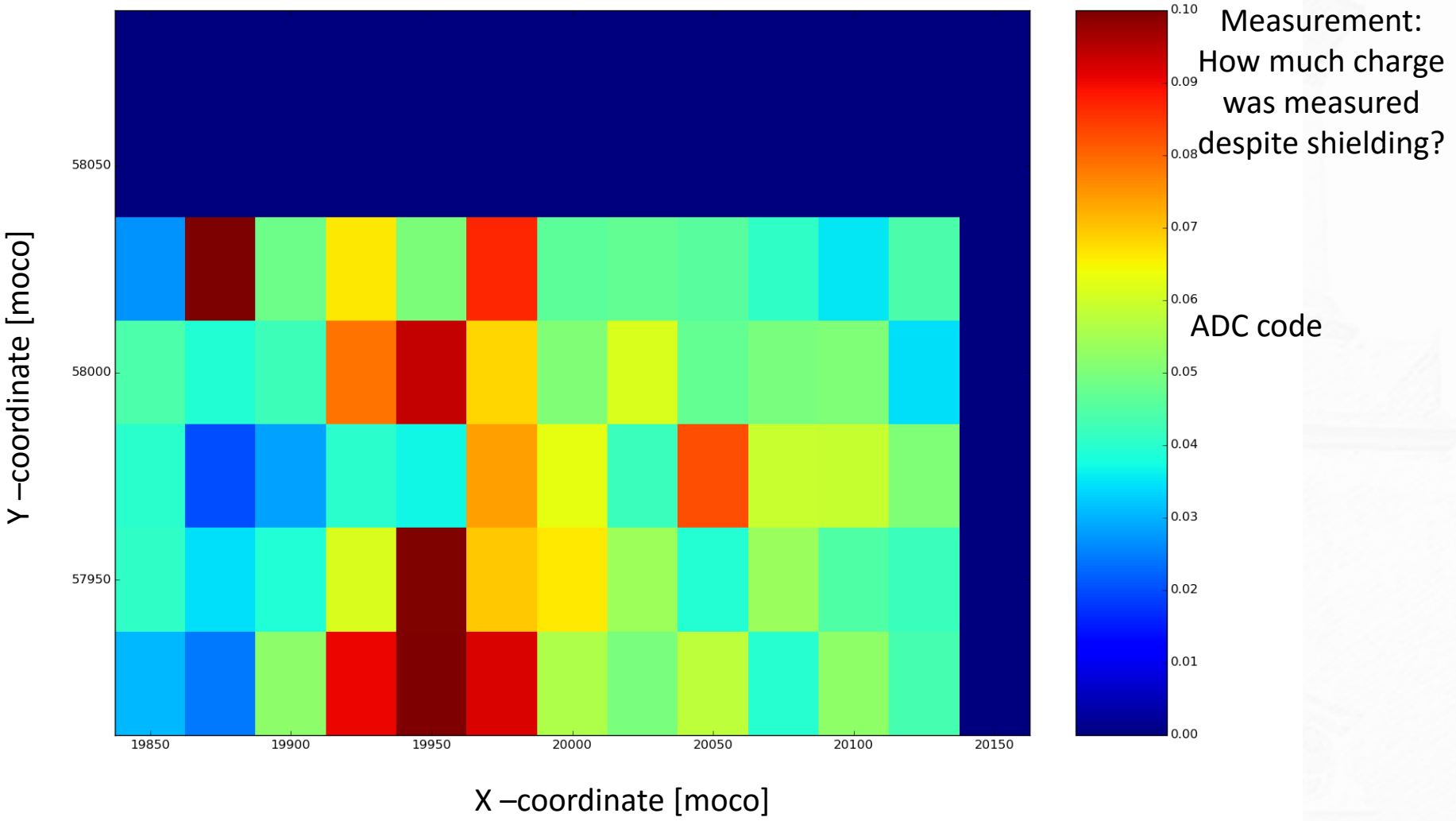
$$\text{Efficiency}_{\text{Cluster}} = (113 \pm 15)\ \%$$

$$\text{Efficiency}_{\text{Seed}} = (101 \pm 6)\ \%$$

Cluster signal (shielding) – laser shot for 2 GCK

GM efficiency

Pixel **inside** of gated region!

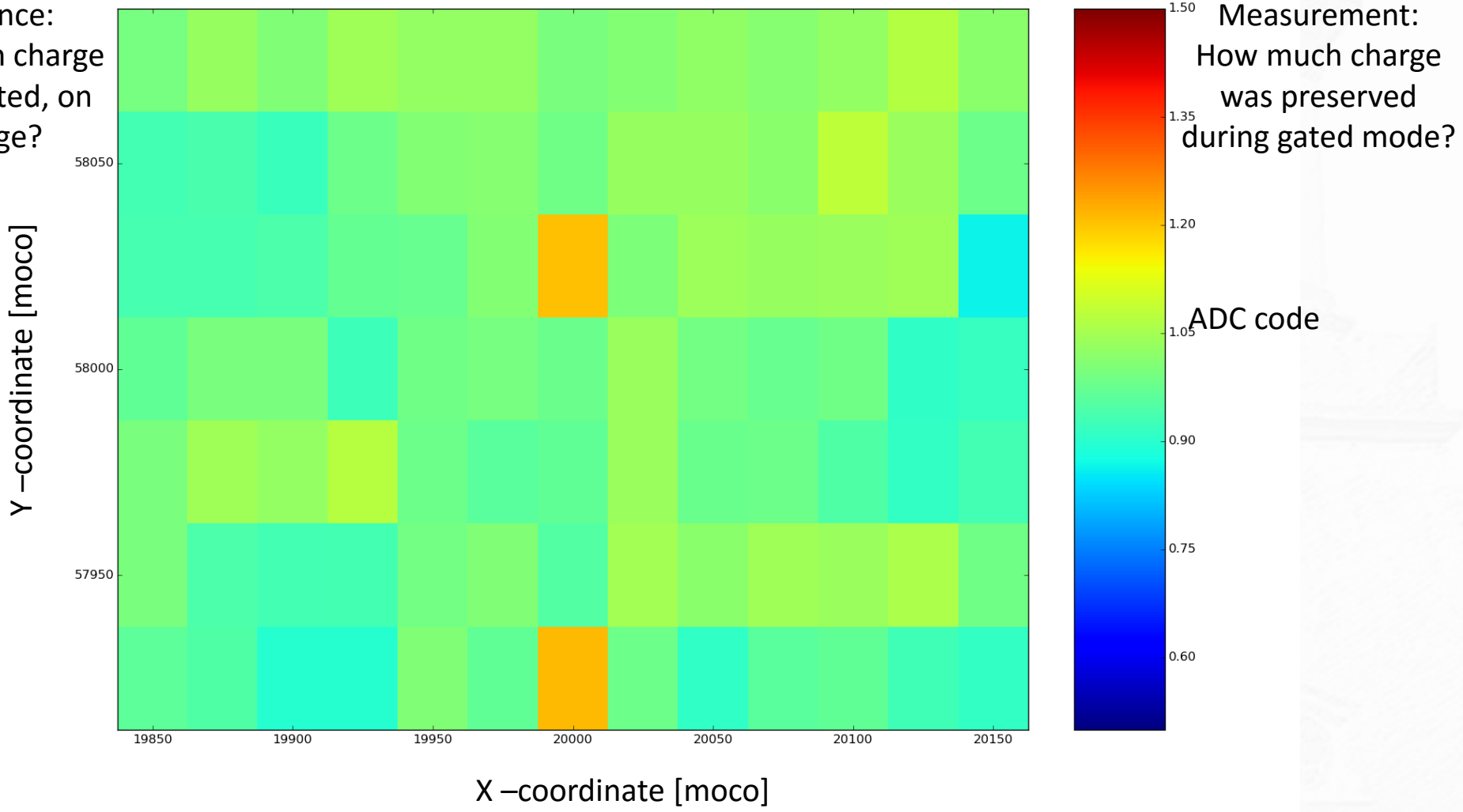


Measurement: How much charge was measured despite shielding?

Cluster signal (preservation) – laser shot for 2 GCK

Pixel **inside** of gated region!

Reference:
How much charge was injected, on average?



Measurement:
How much charge was preserved during gated mode?