Gated Mode
Timing Observations

The Gated Mode

SwitcherB allows to operate Gating in two different Modes:

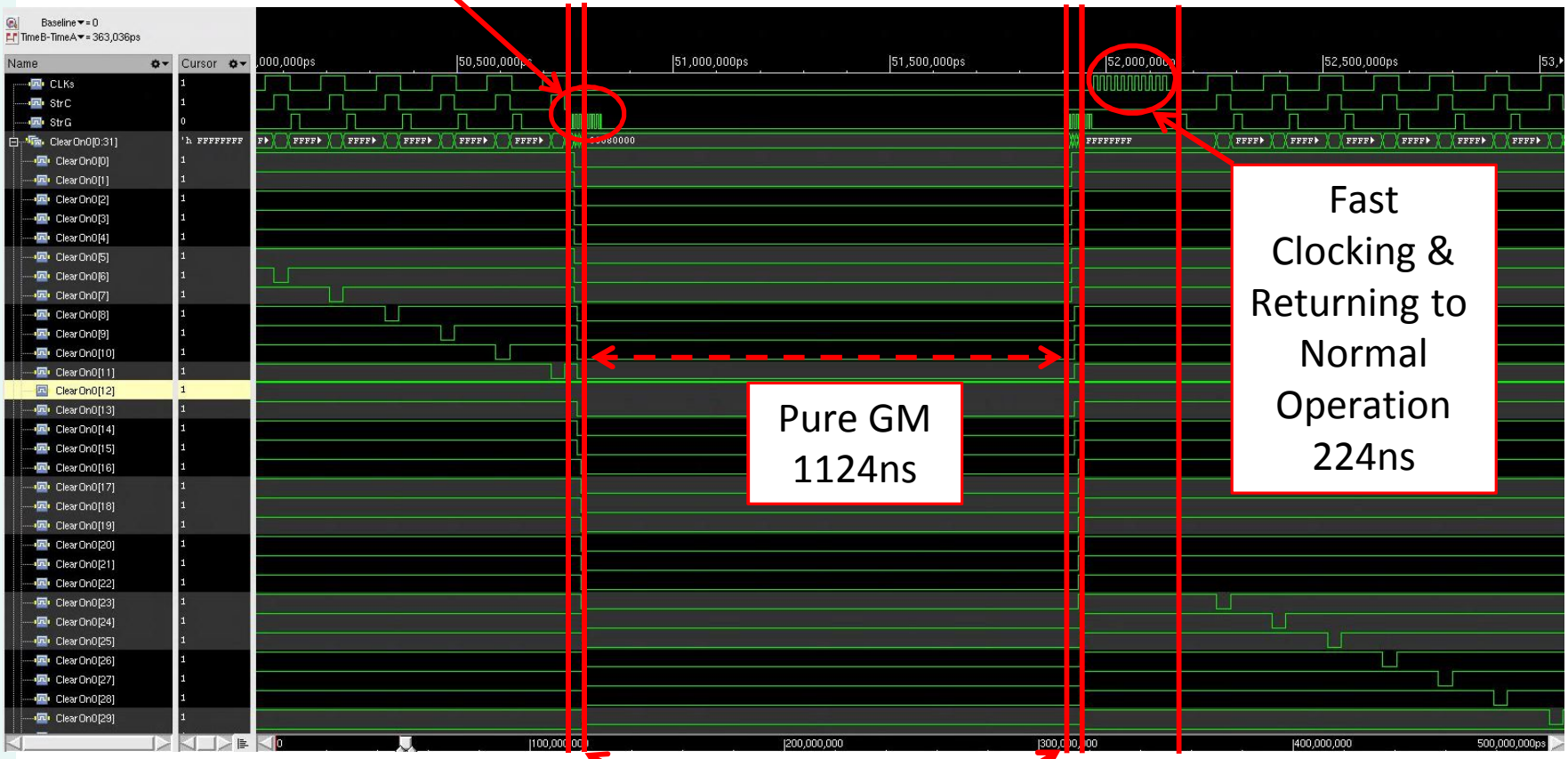
- **Gated Mode without Readout:** Clocking is disabled, Clear moves to high for all gates except current one
  - Needs fast clocking to synchronize with correct readout position
  - Problem with DHPT1.0: when gating starts at end of frame, SerIn signal is omitted because of missing clock and hence full frame will be lost. *Hopefully solved with new DHPT1.2 version.*

- **Gated Mode with Readout:** Clock continues to run, so frame readout will be synchronized with SerIn, Clear changes to high level immediately on non-active channels
  - Losing at least 600ns for turning in & out of Gated Mode
  - Hope for lower pedestal oscillations

Gated Mode Simulation 11 gates @250MHz = 1,408µs

At least 5 StrG for initiating GM

Disable GM:
switch StrC to low +
falling edge of StrG

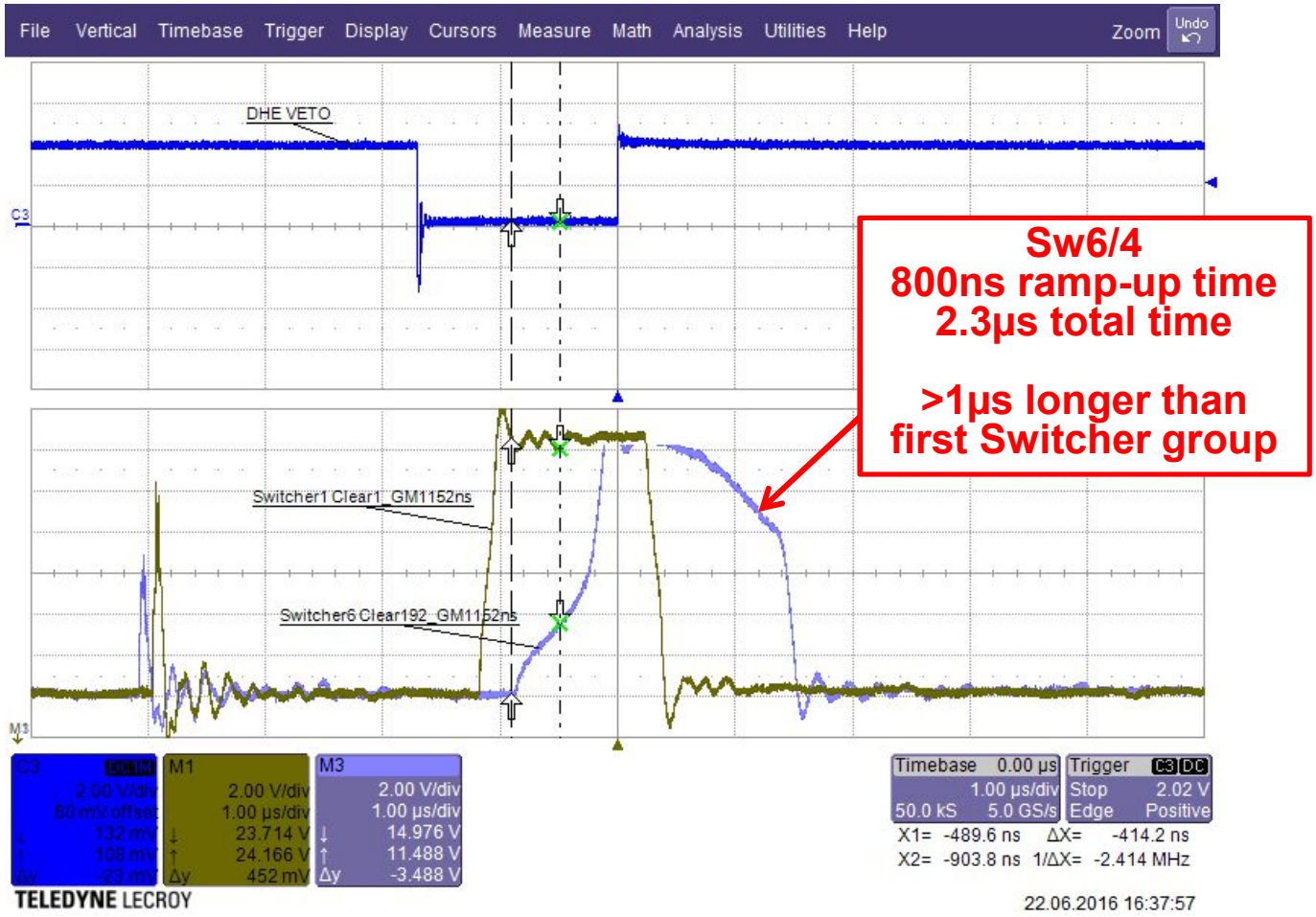


1 gate @250MHz = 128ns

36ns for Switching all Switcher Groups ON or OFF

Oscilloscope Sw1/1 vs Sw6/4 GM 11 gates

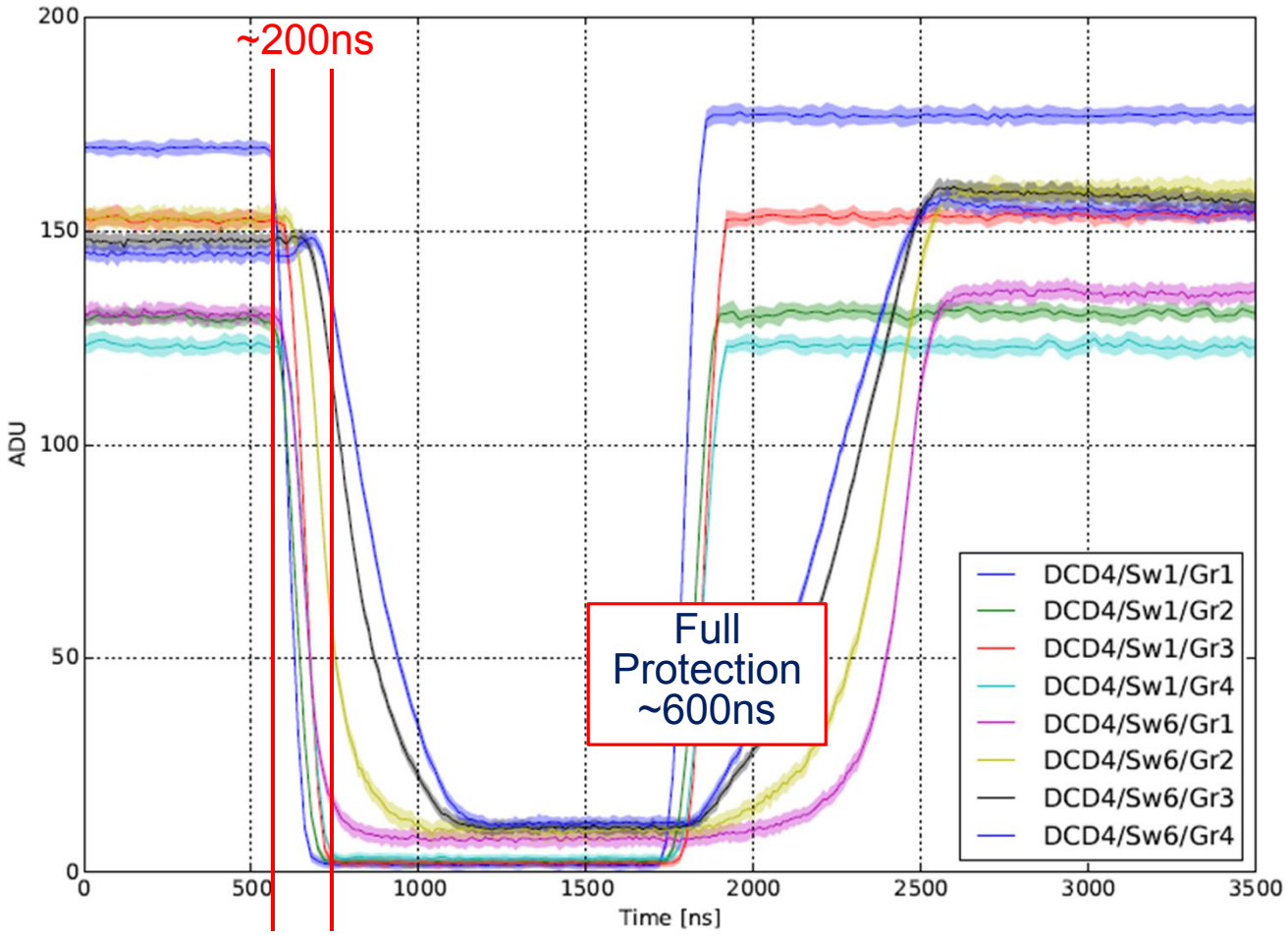
Only first and last Clear contact are accessible via oscilloscope

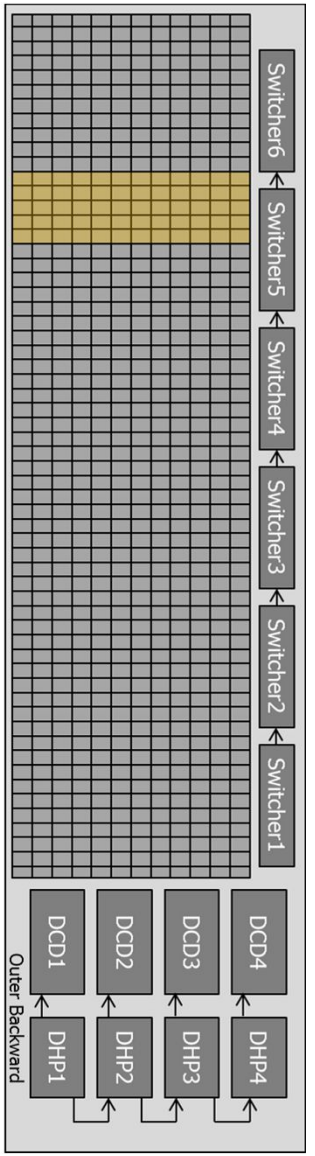


Rise time Sw1/1 ~ 200ns
Rise time Sw6/4 ~ 800ns

This compares to a substantial lower rise time in the SwitcherB manual but bear in mind that 6 SwitcherBs, separated into 4 groups@8Clear channels have to be switched on at once (4 times consecutively within 36 ns)

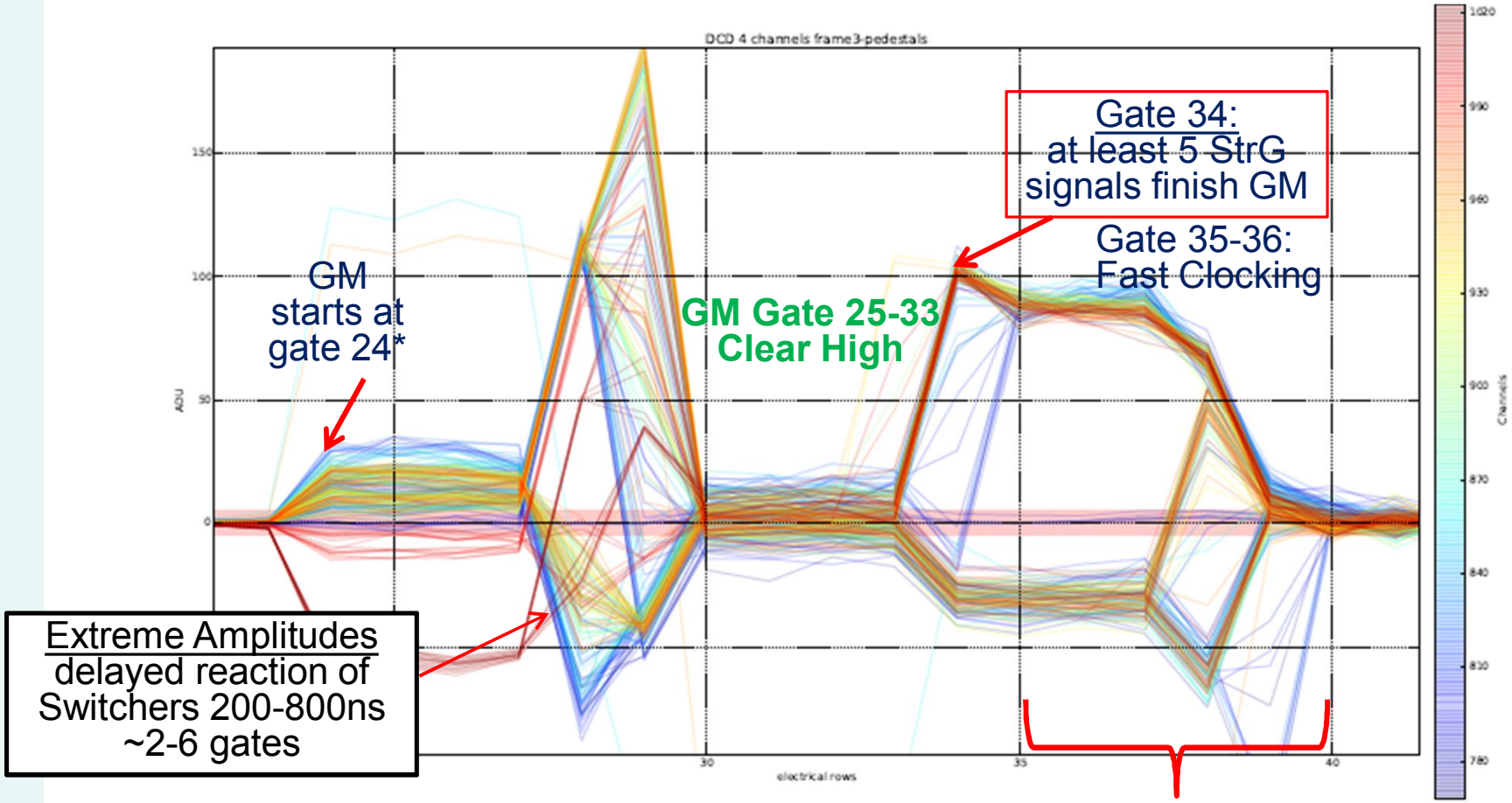
Laser Scans GM 11 gates sequence





Laser Activation Timing moved forward in 10ns steps

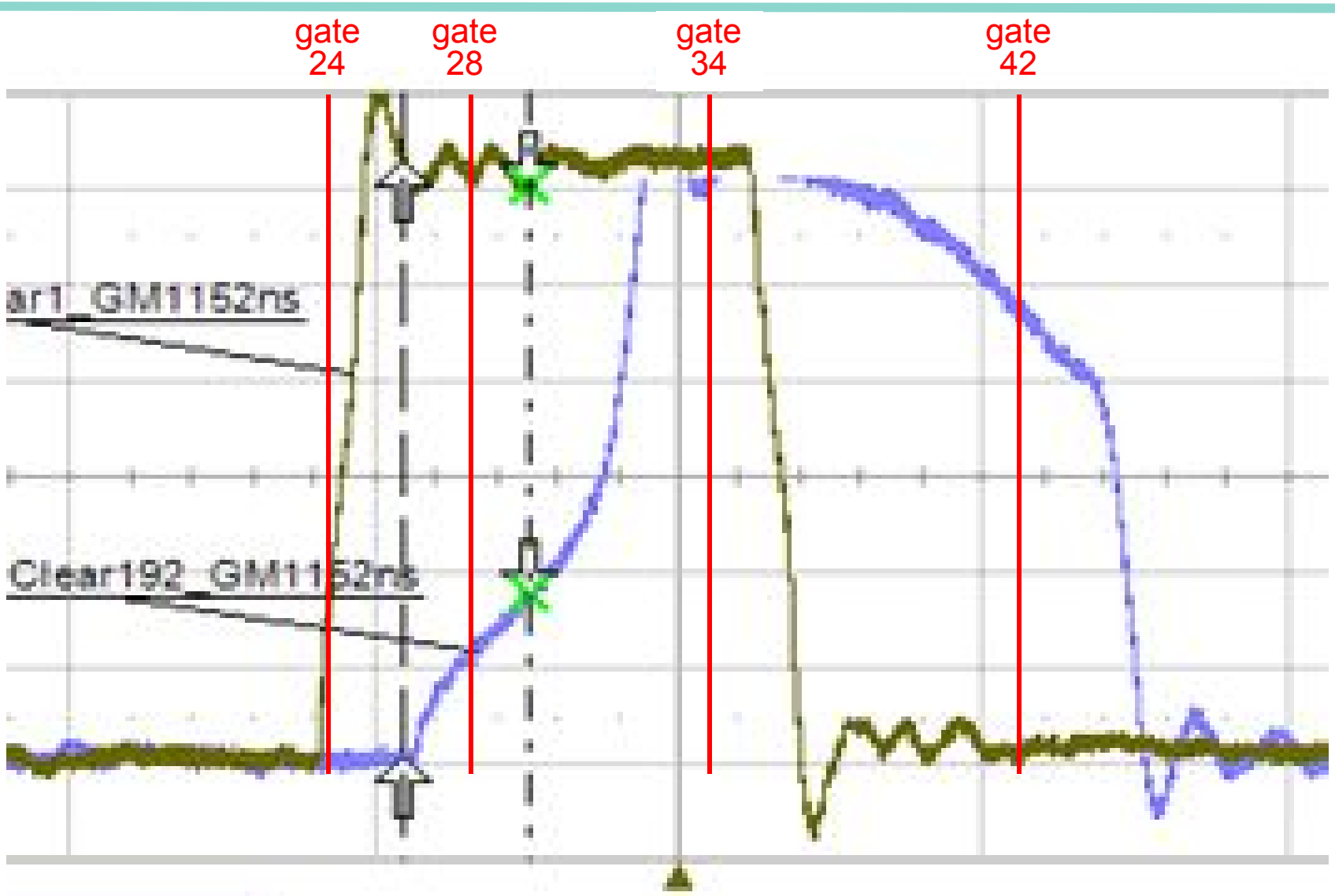
Pedestal Oscillations: 11 gates GM-sequence



Total GM period of 18 gates including pedestal variations

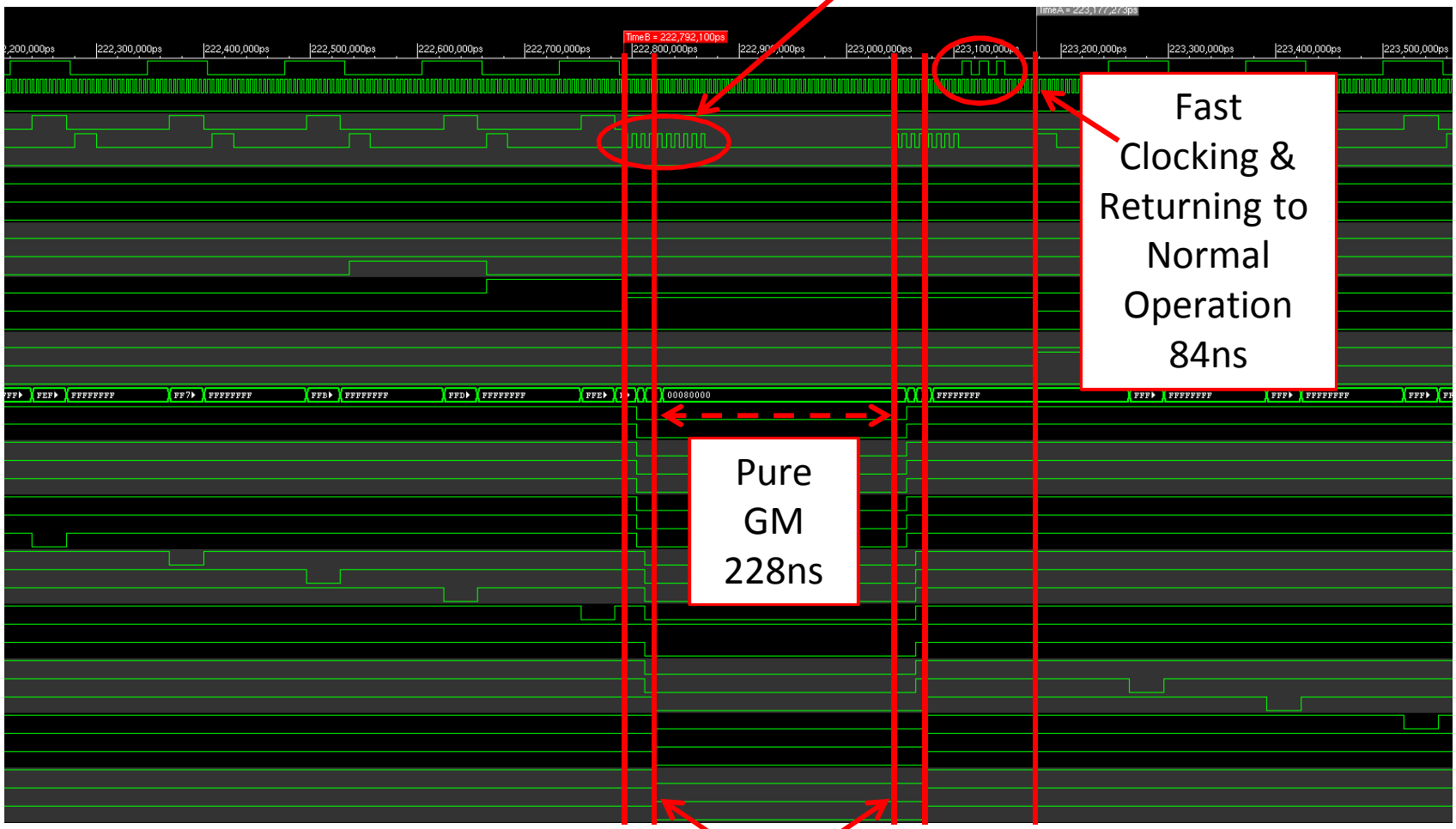
* DHPT1.0 Bug: GM is programmed for gate 22 but normal mode repeated twice

Oscilloscope Sw1/1 vs Sw6/4 GM 11 gates zoomed



Time base: 1µs/div

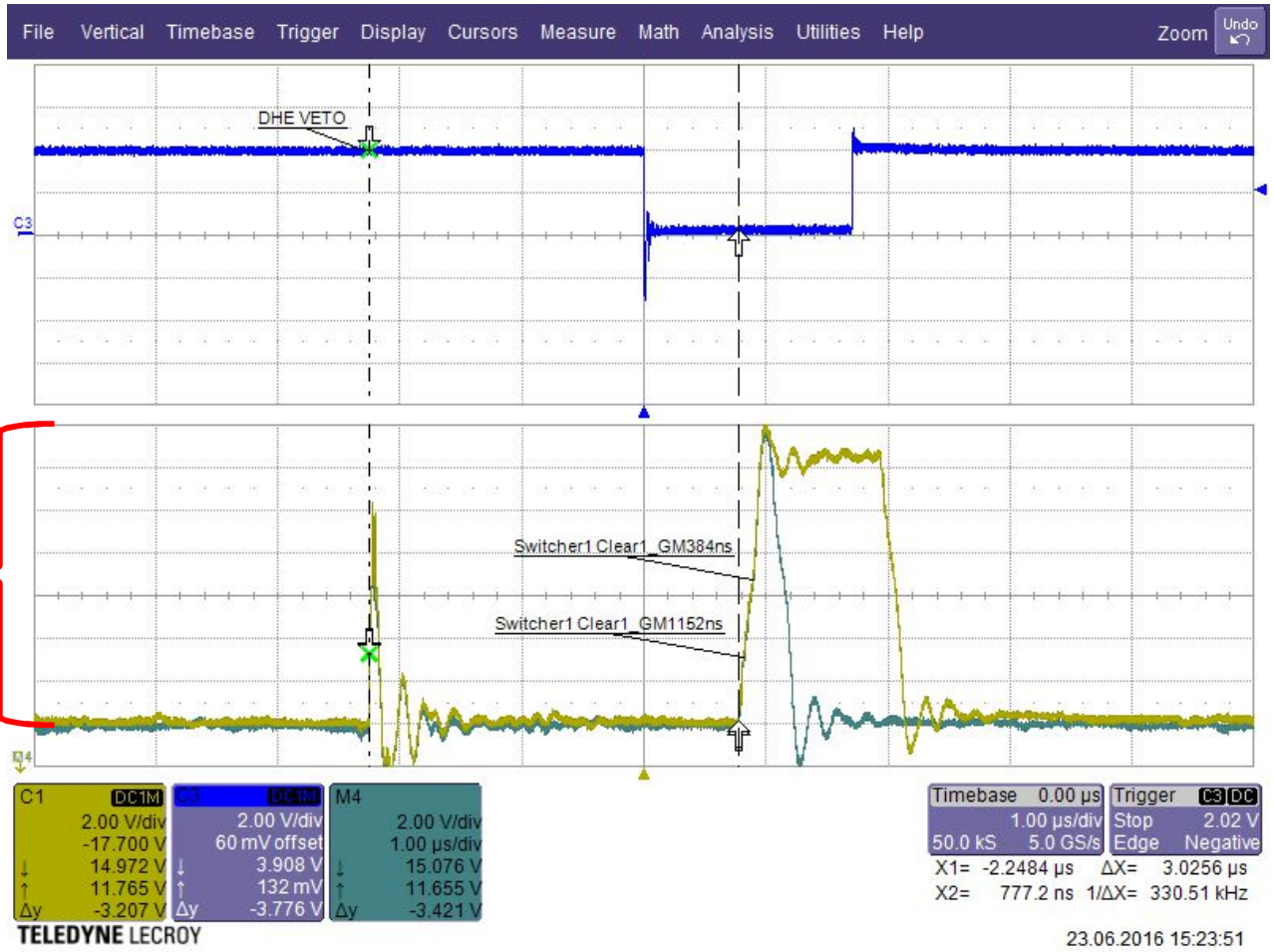
Gated Mode Simulation 3 gates @250MHz=384ns



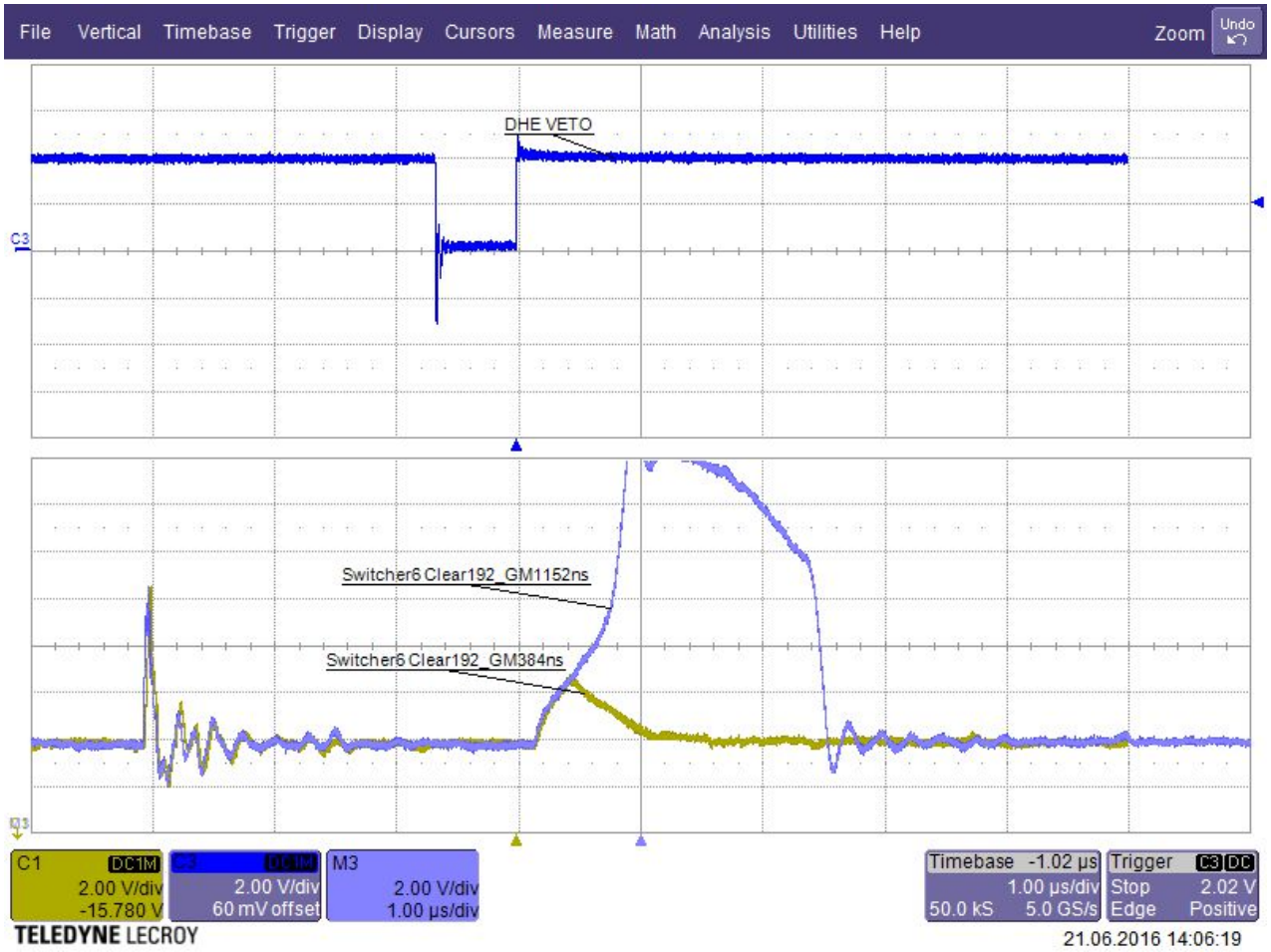
GM11gates vs GM3gates first Clear

Measured 14V
(C_{high}=20V, C_{low} =5V)

GM protection effective @ 9V above C_{low}

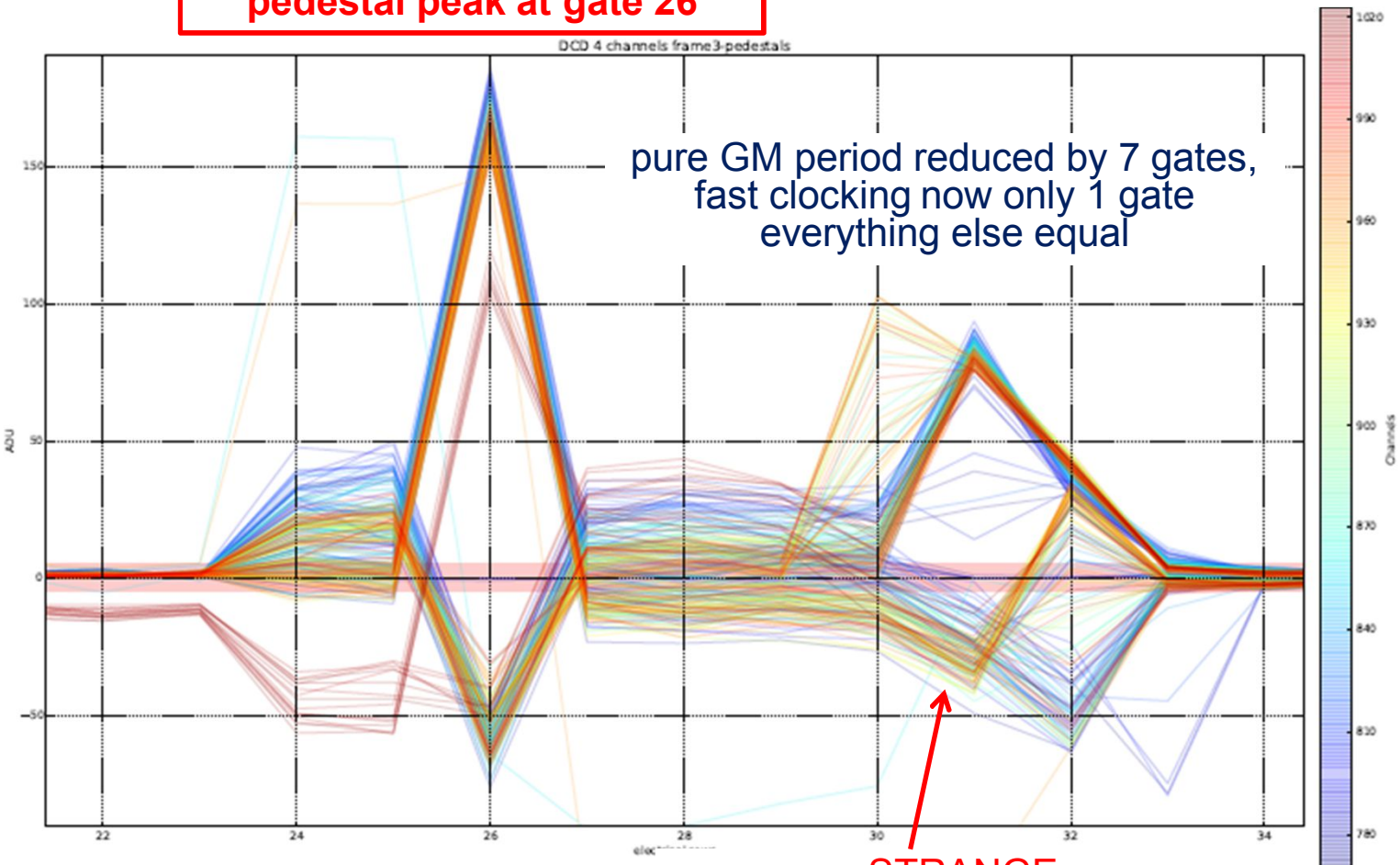


GM11gates vs GM3gates last Clear



GM short 384ns sequence

same starting sequence
pedestal peak at gate 26

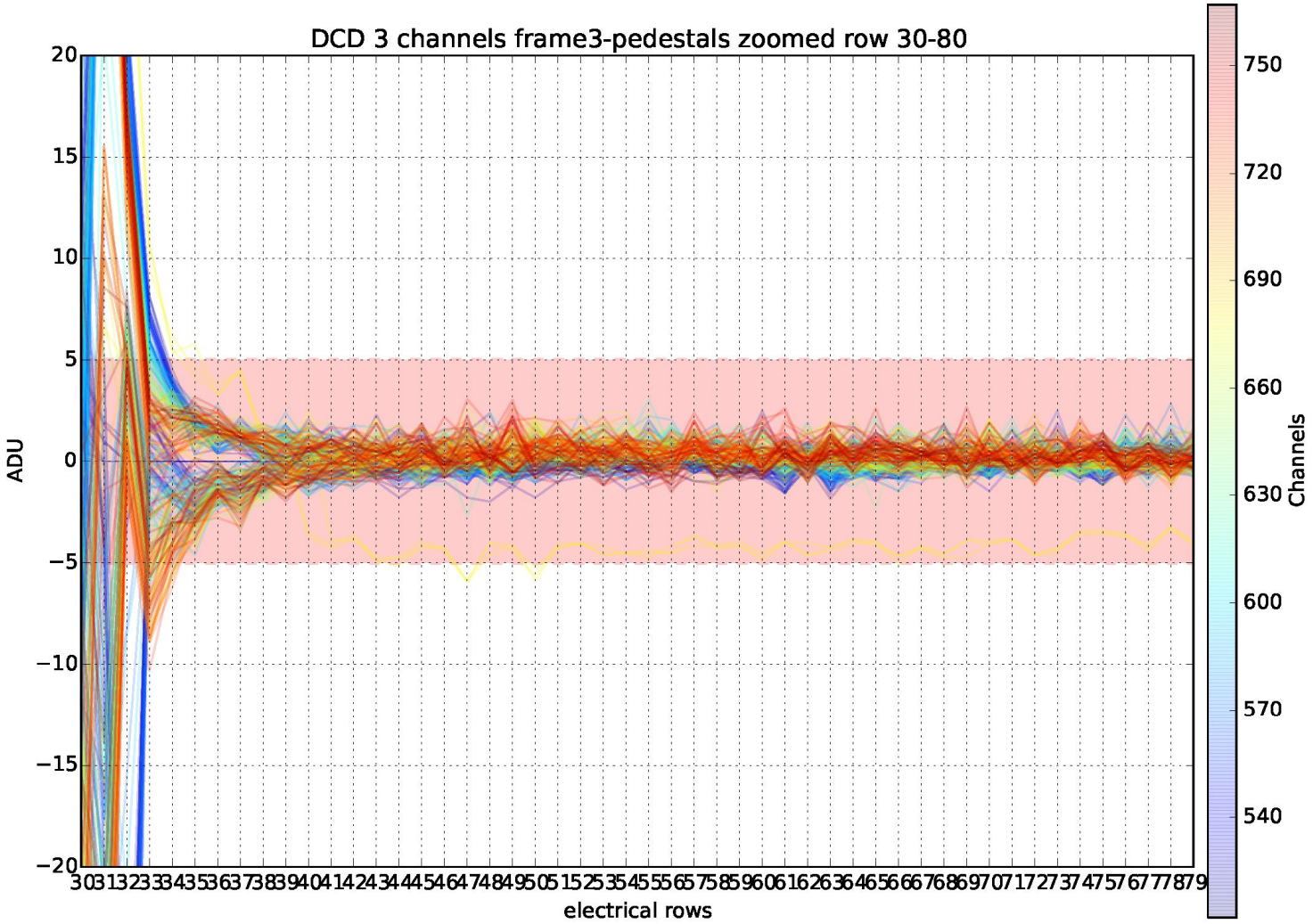


pure GM period reduced by 7 gates,
fast clocking now only 1 gate
everything else equal

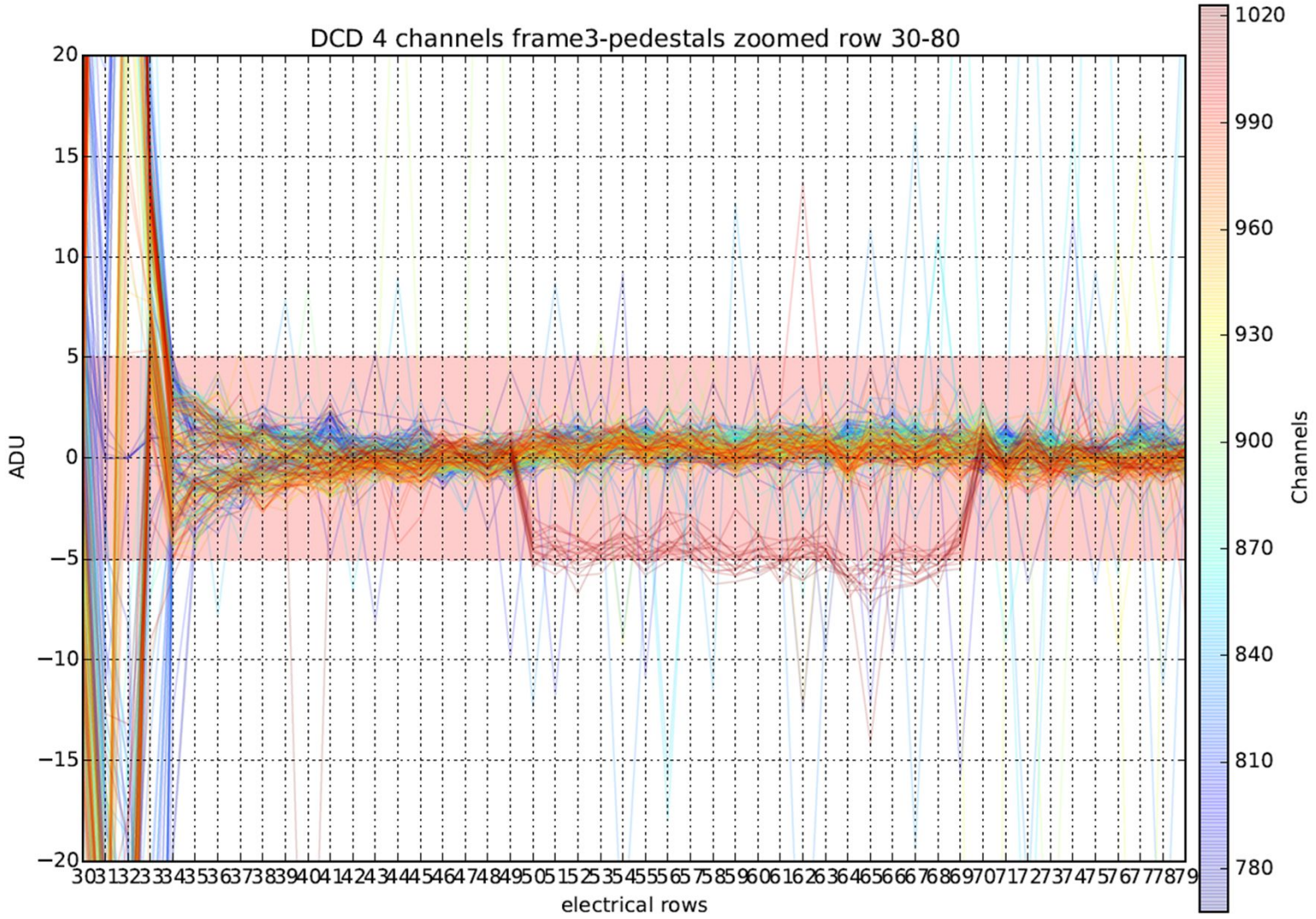
STRANGE:
Reason for higher pedestals 4
gates after stopping GM unclear

Total GM period reduced to 10 gates = 1,28µs including pedestal variations

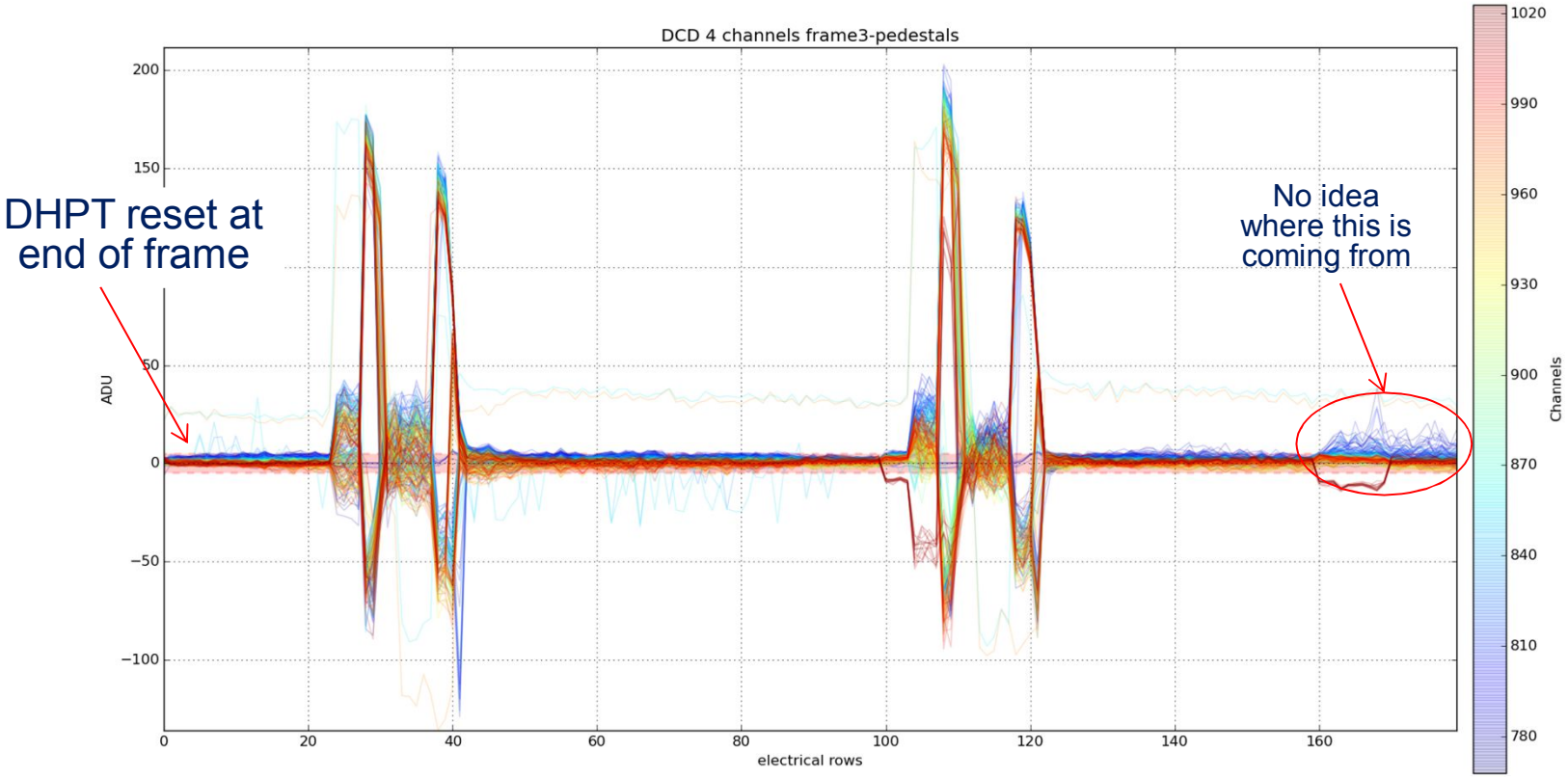
It’s not only a time constant… 250 MHz



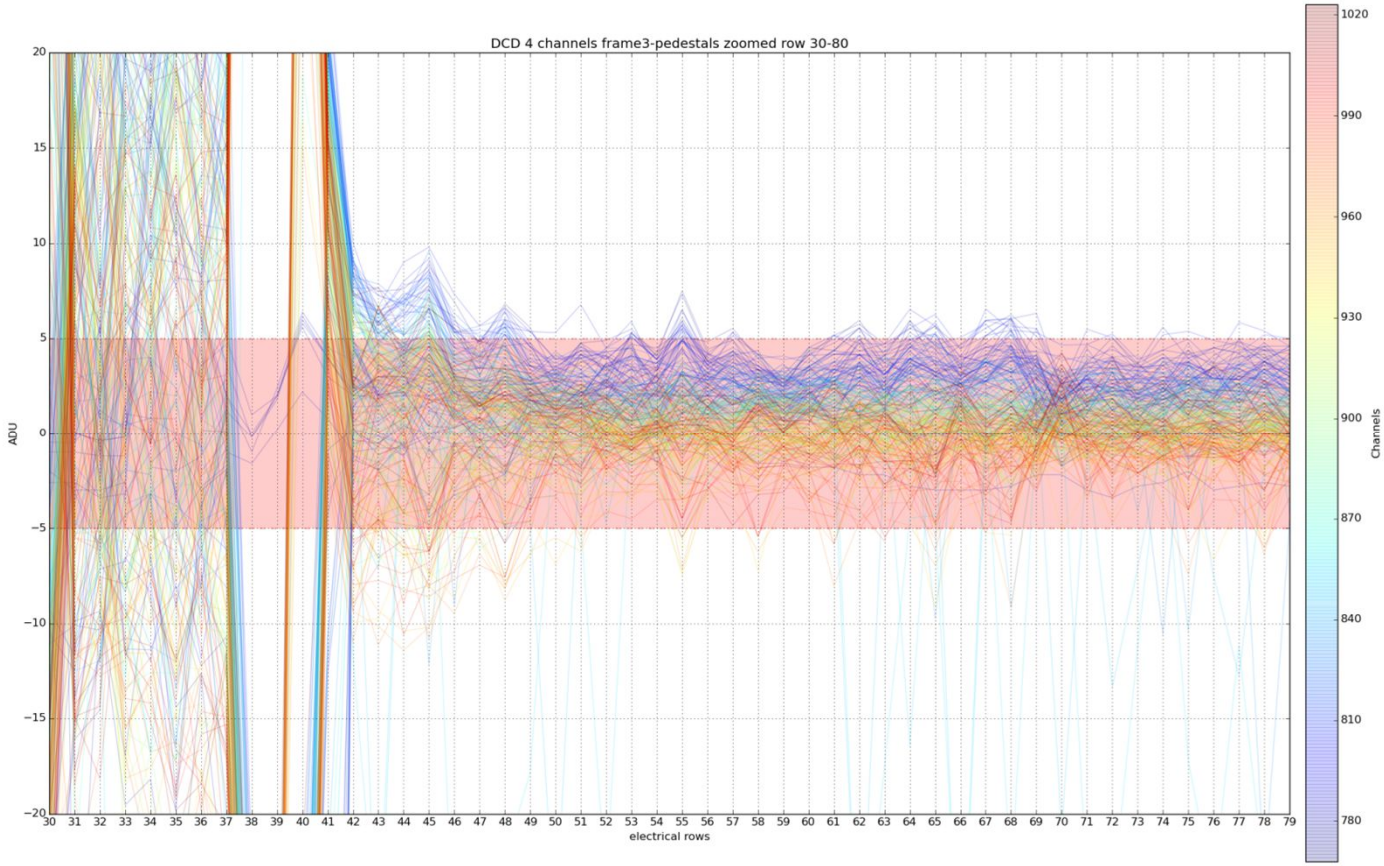
Pedestals back in range at gate 34 @285 MHz



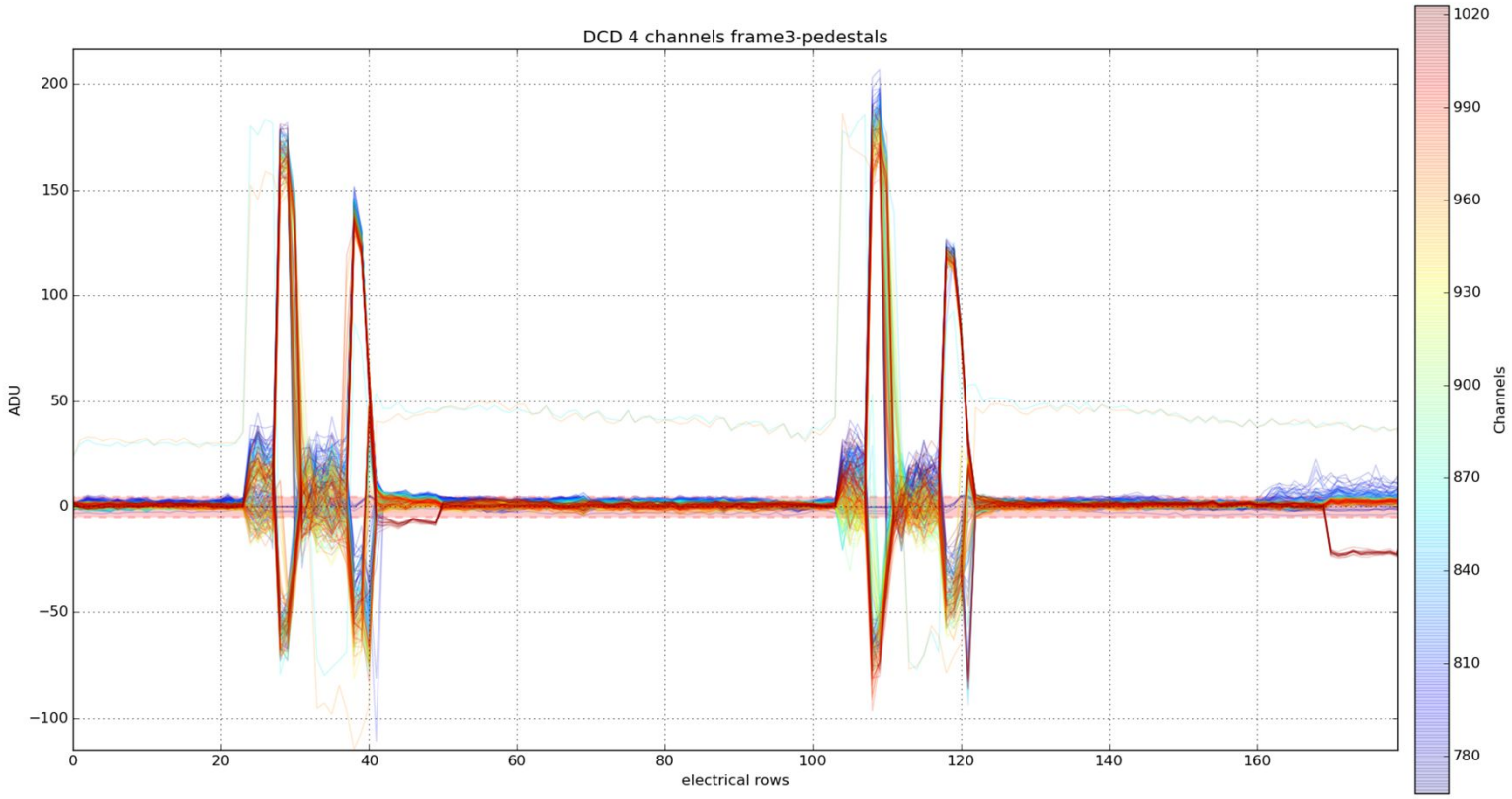
Short Cables – 11 Gates GM w/o RO overview



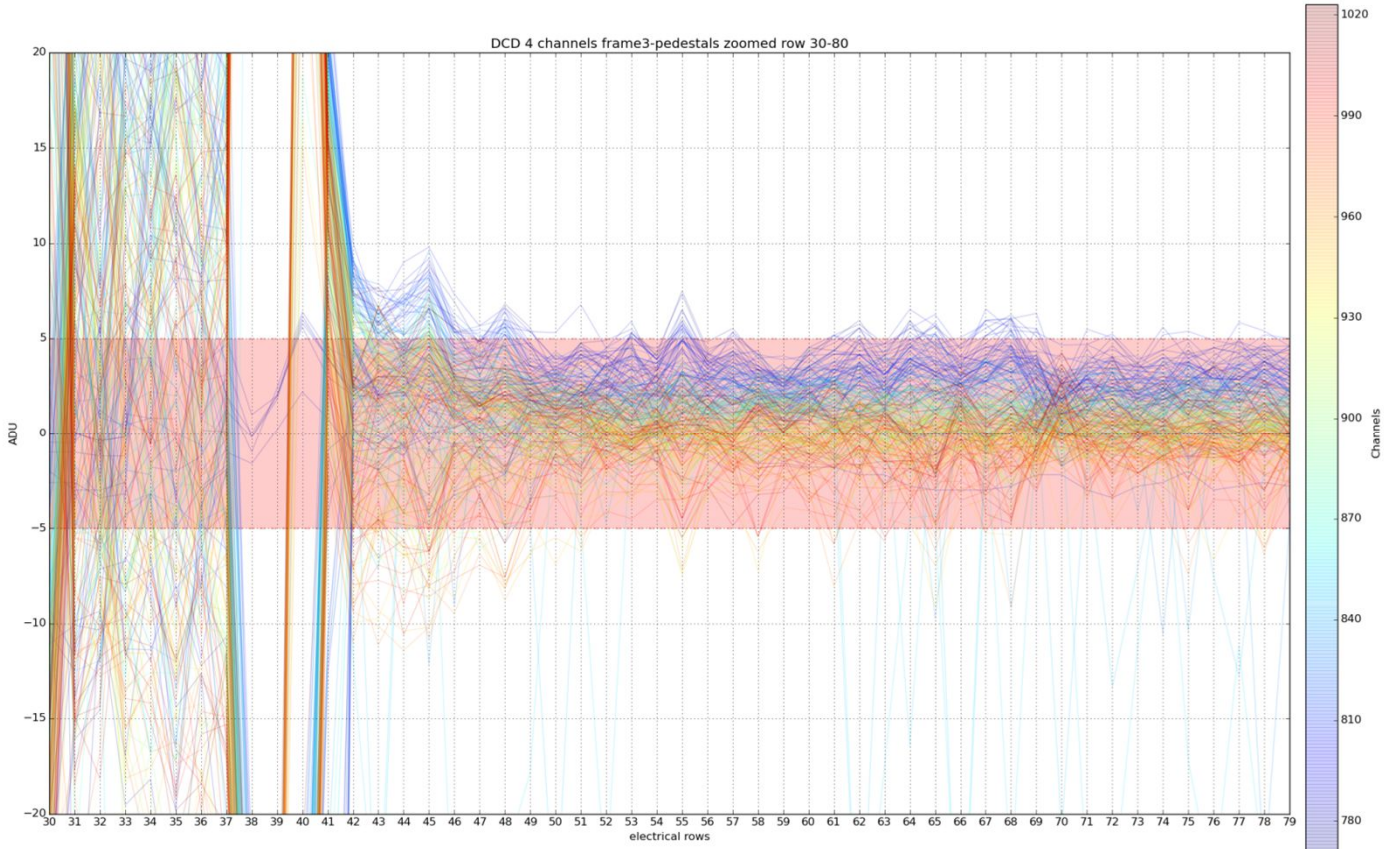
Short Cables – 11 Gates GM w/o RO zoomed



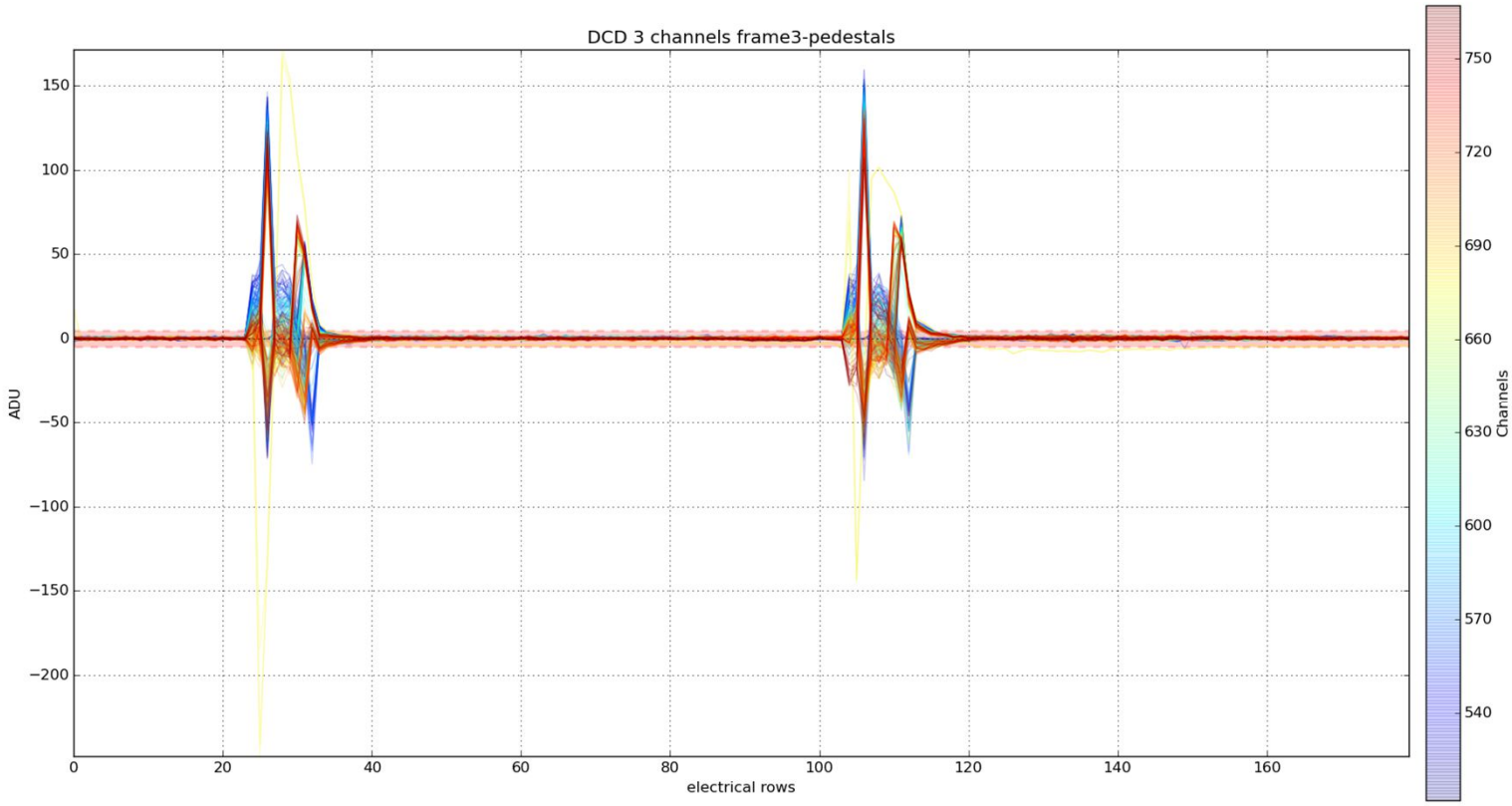
Long Cables – 11gates GM w/o RO overview



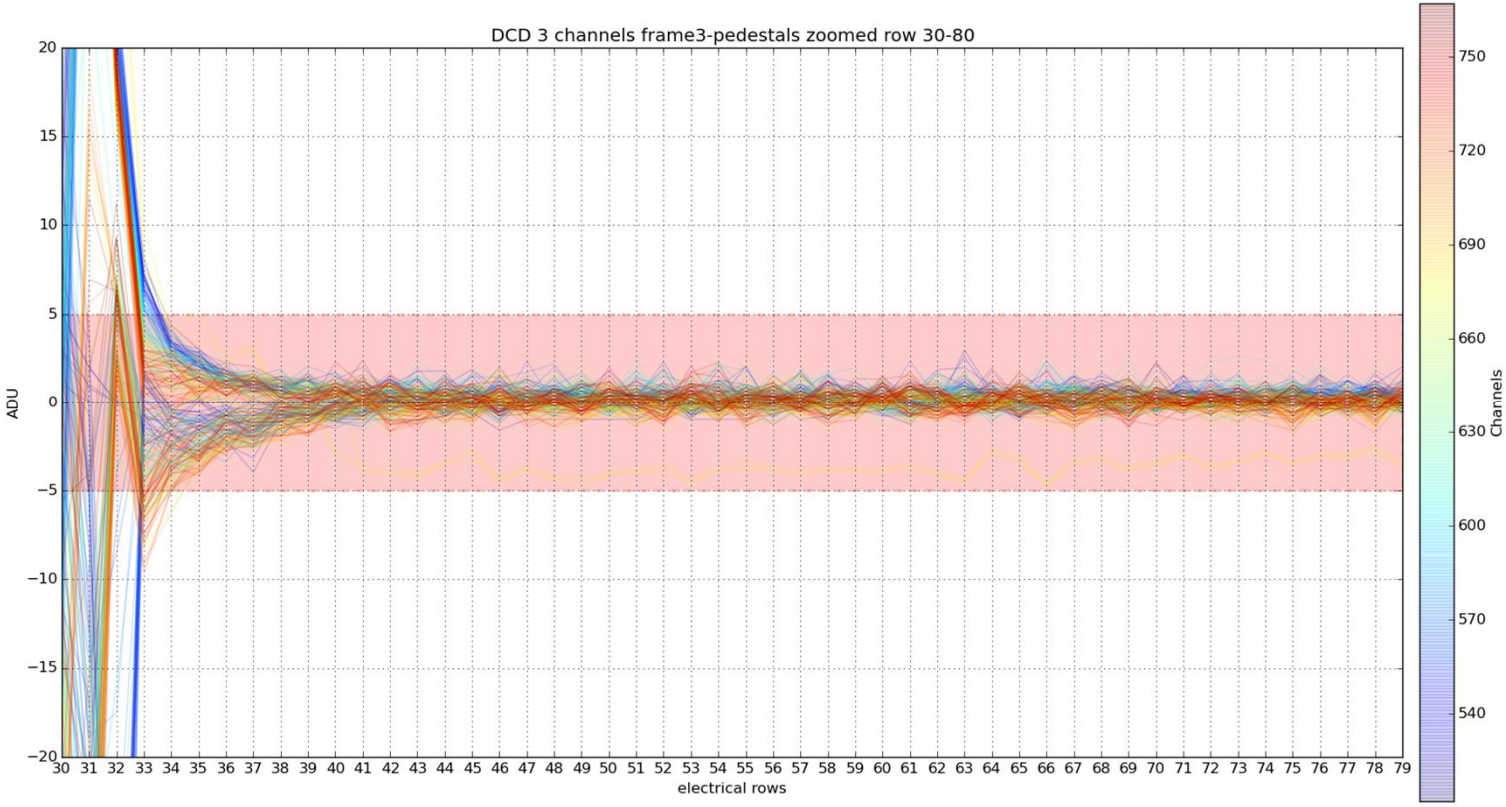
Long Cables – 11gates GM wo RO zoomed



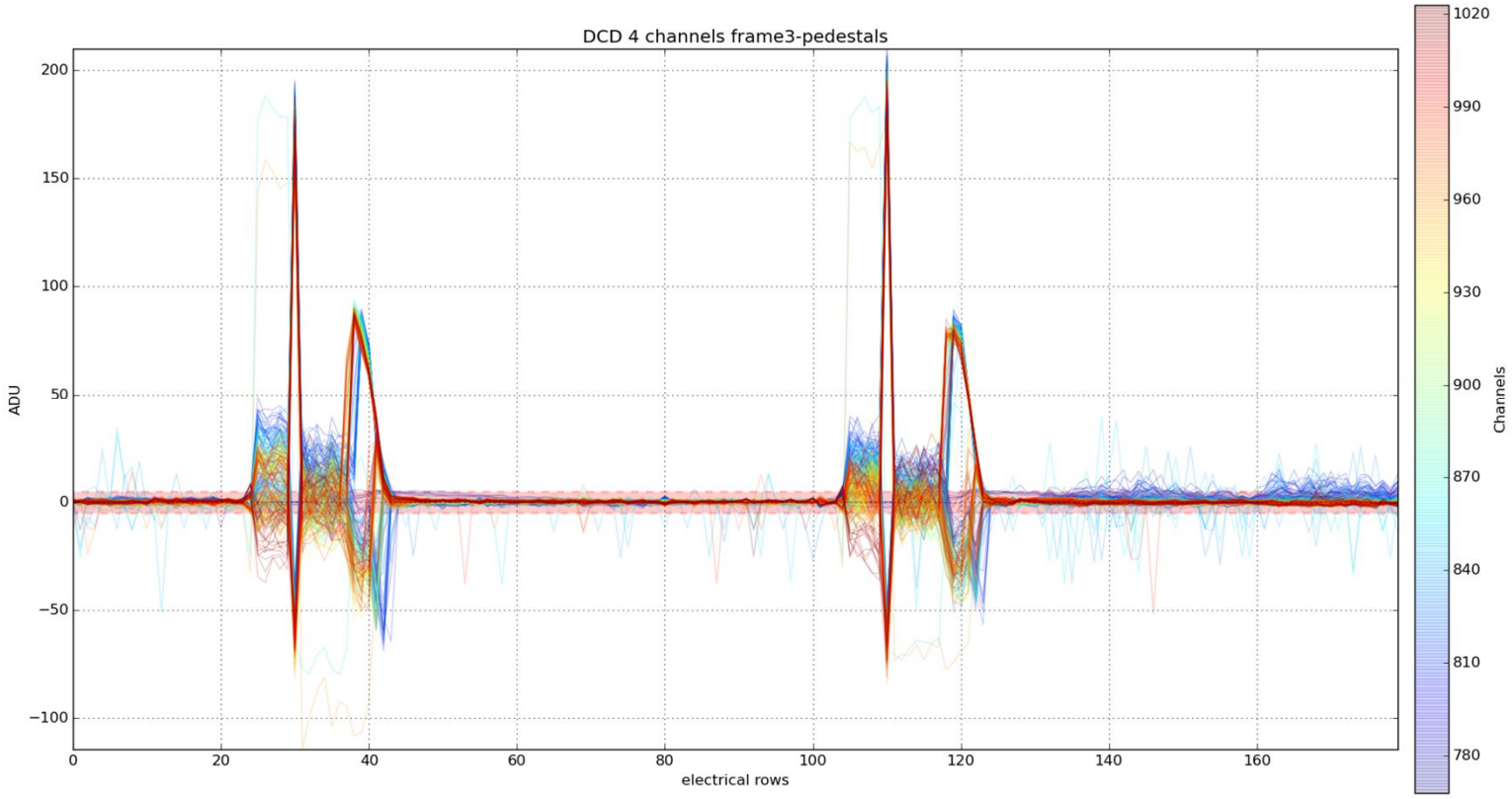
3gates GM w/o RO overview (DCD3 short cables)



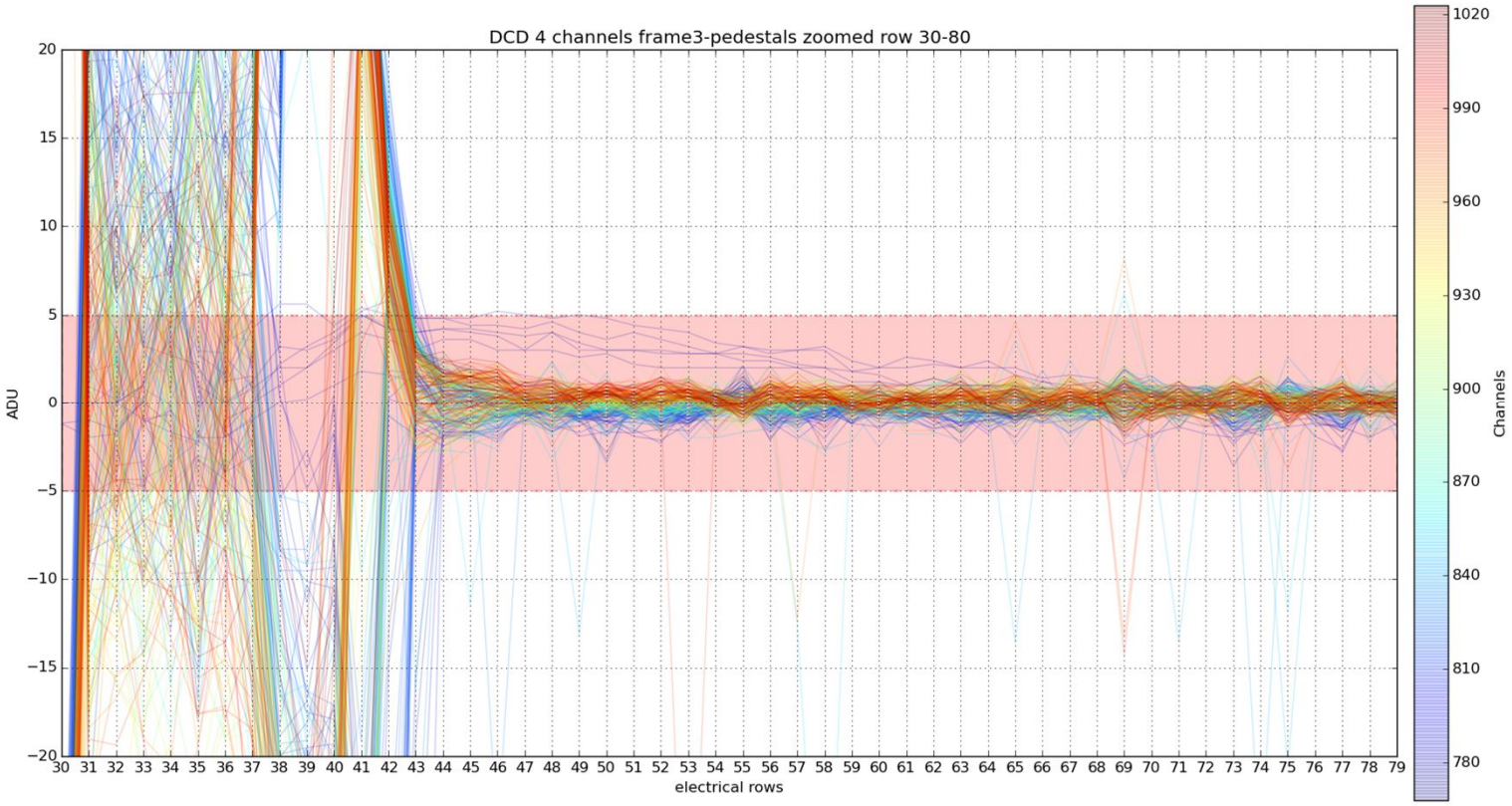
3gates GM w/o RO zoomed (short cables)



6gates GM with Read-Out overview

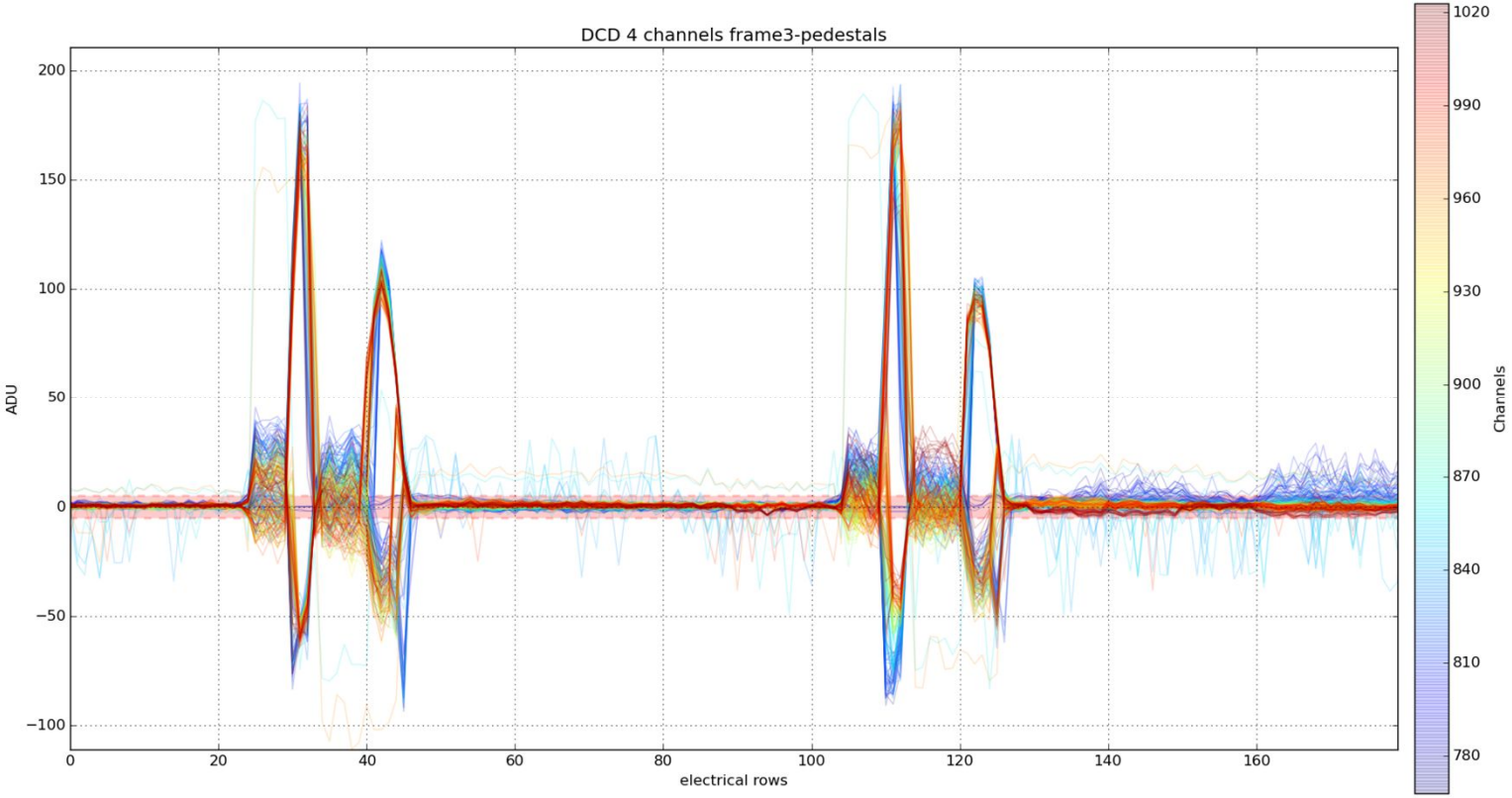


6gates GM with RO zoomed

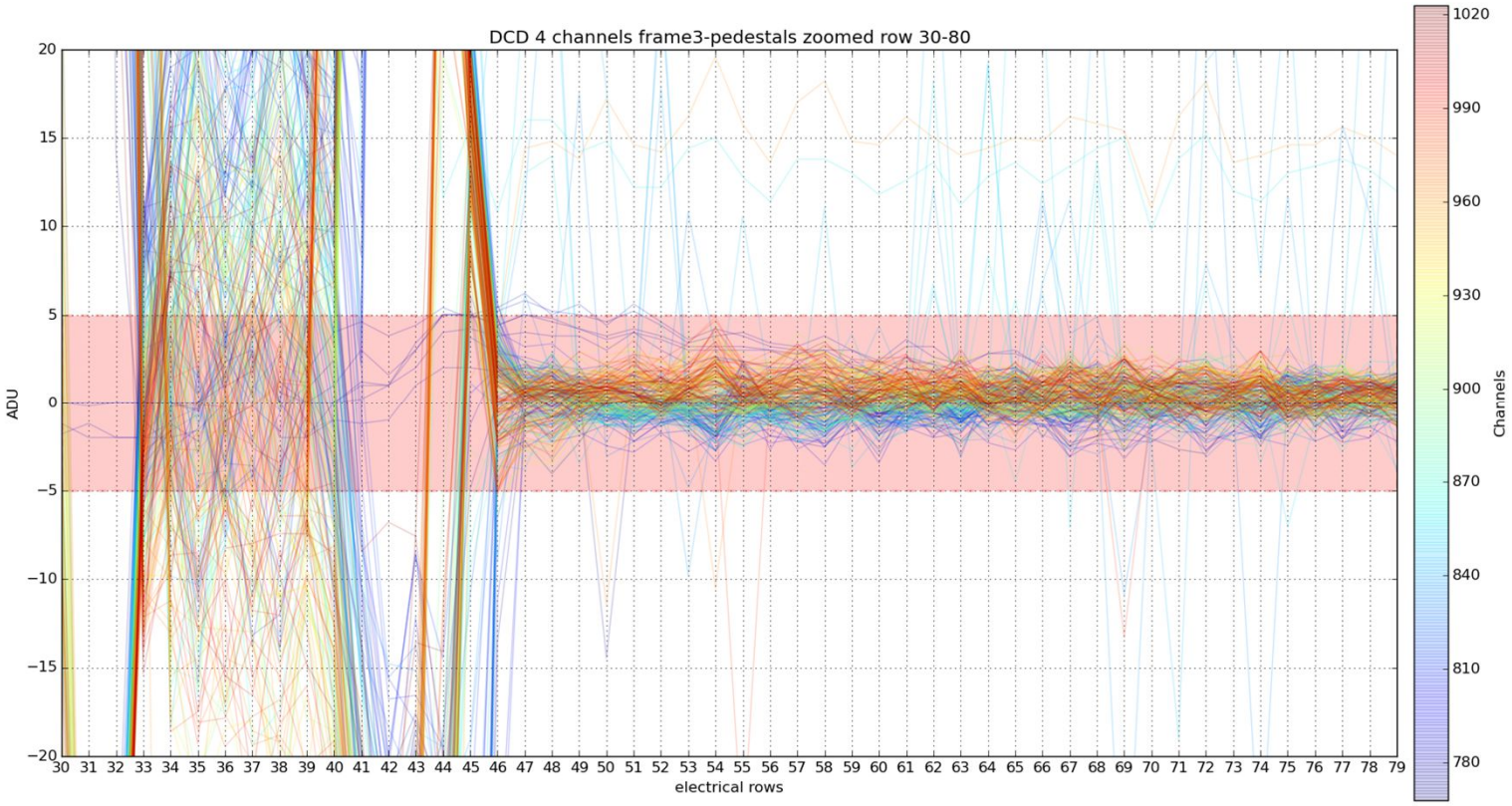


- although relatively short GM period pedestal oscillations persist longer than even 11gates w/o RO
- variation spread thereafter seems to be substantially lower!

10gates GM with RO overview

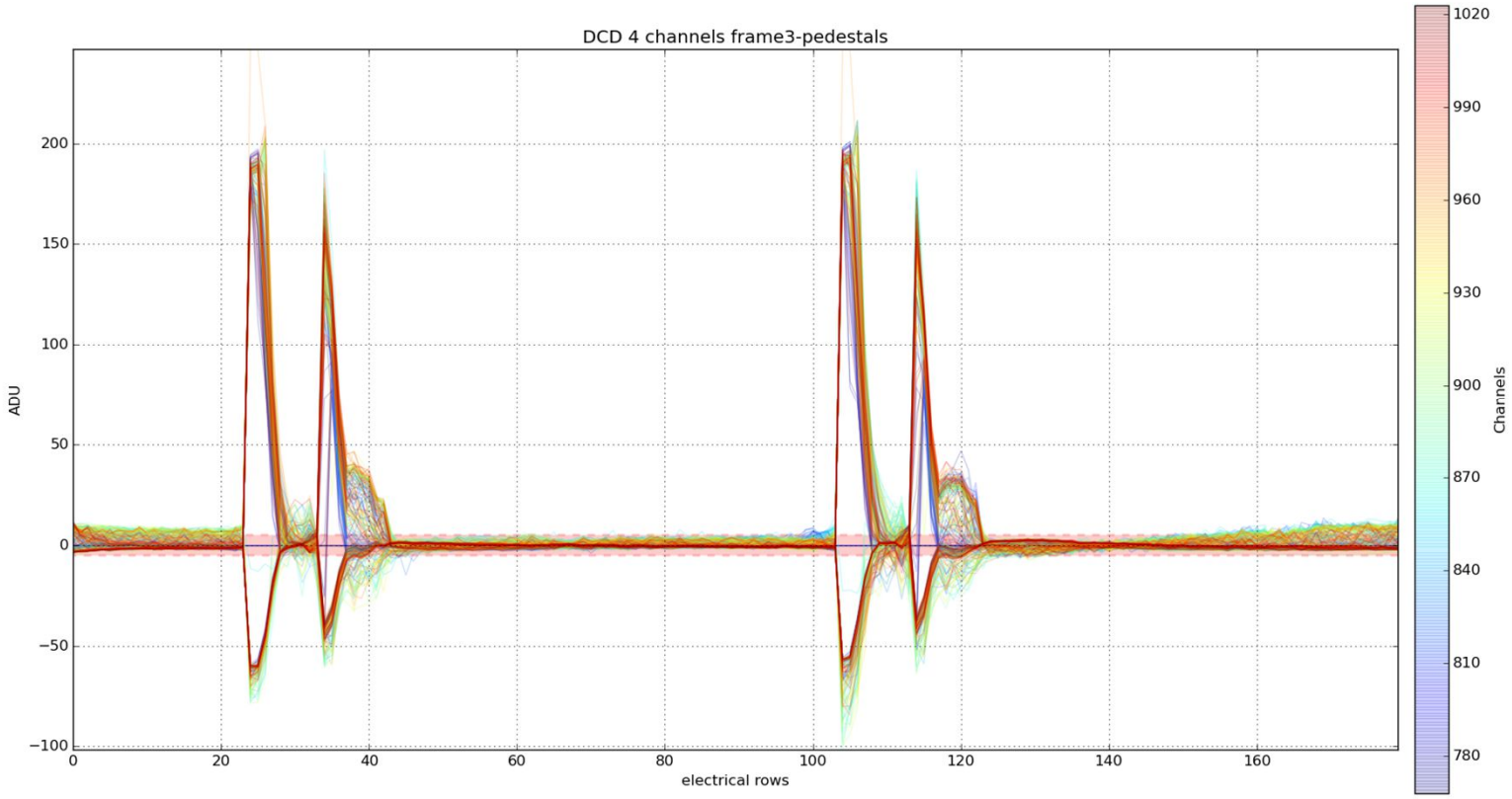


10gates GM with RO zoomed

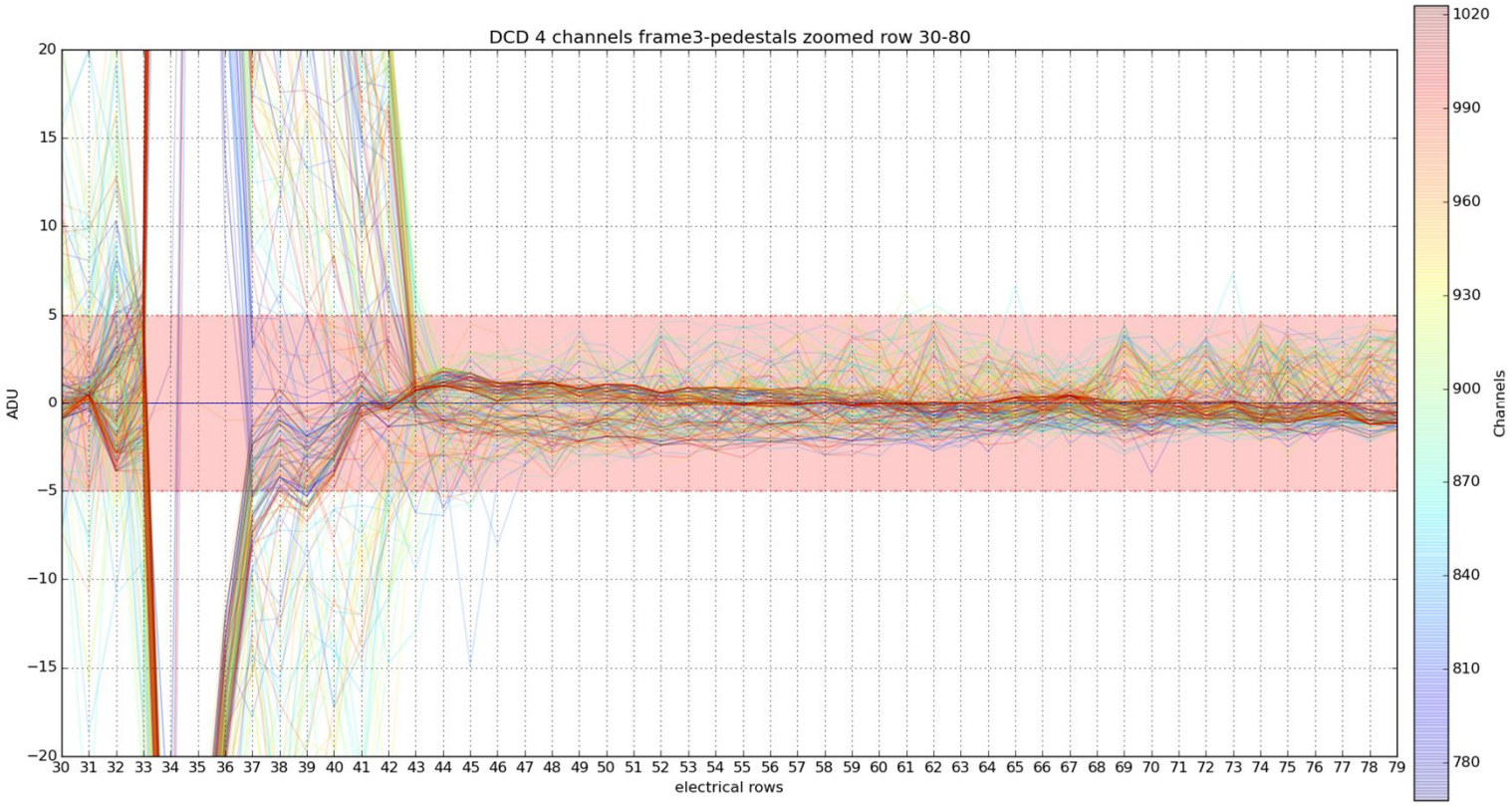


Pedestal oscillations are within arbitrarily chosen threshold limit of ±5 ADUs not before 23 gate periods = 2,94µs

GM11gates w/o RO analog CMC overview

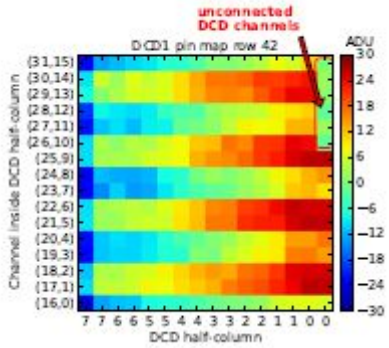


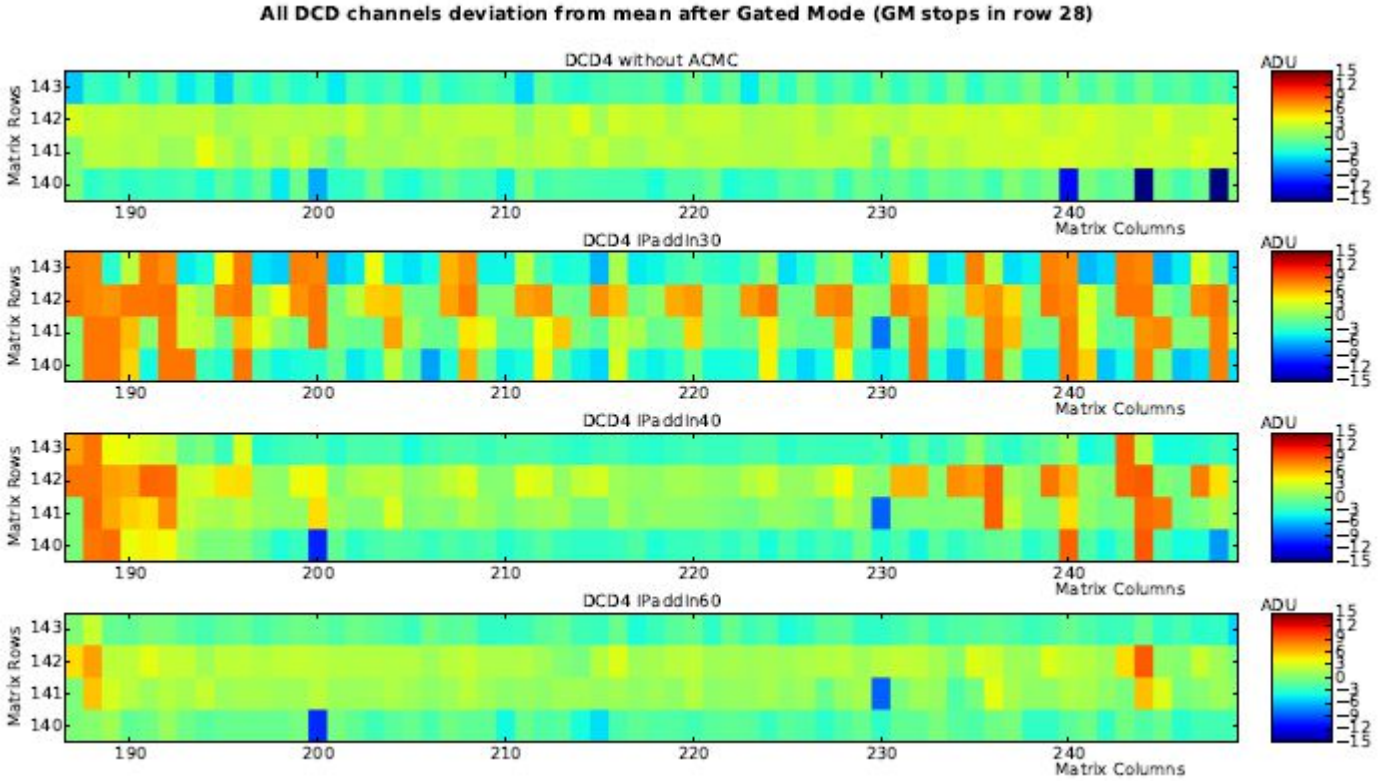
GM11gates w/o RO analog CMC zoomed



In general ACMC looks better but risk that leveling out absorbs signal charge information

ACMC, Single Row Pedestal Oscillations

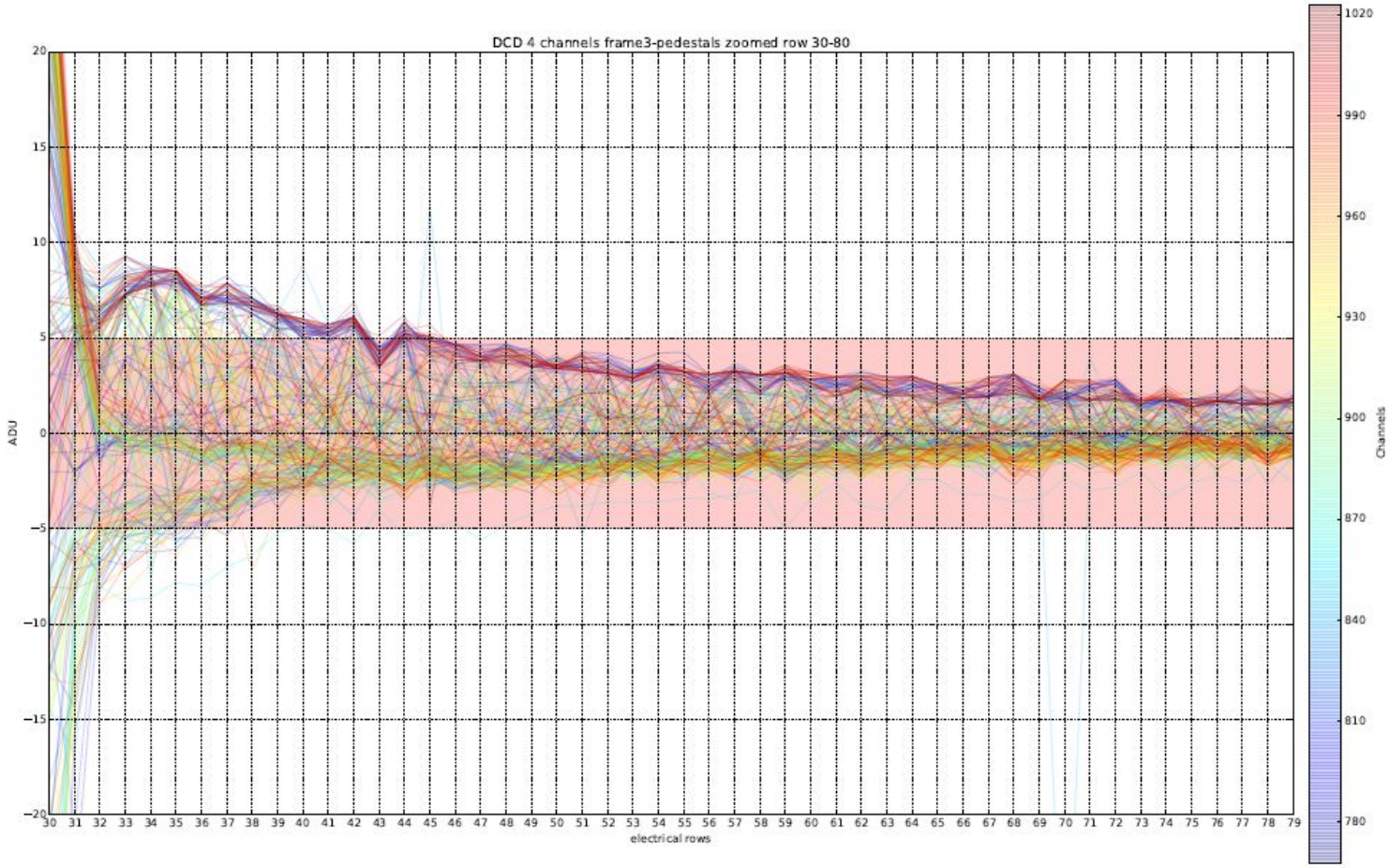




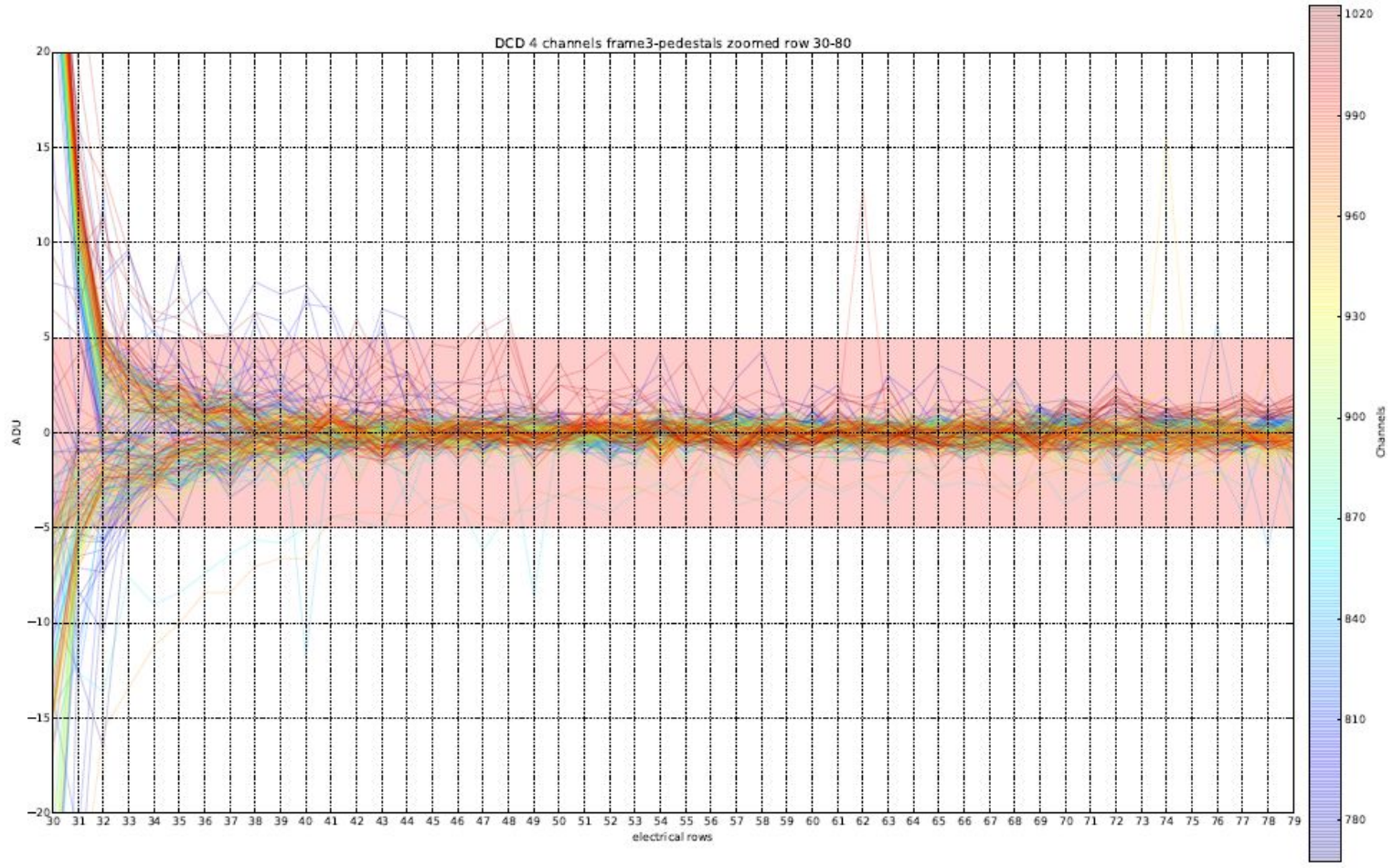
- Distinct DCD-Gradient disappeared after fixing cooling problem and attaching additional capacities on dock-box and break-out board
- Low IPaddIn seems to “swallow” low signal charge

BEWARE: ACMC seems to amplify higher signals

Analog CMC, IPAddIn = 30

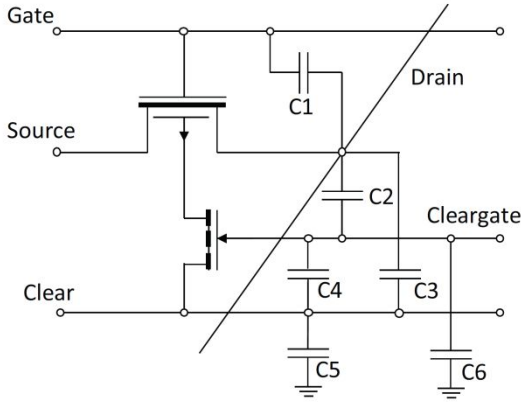


Analog CMC, IPAddIn = 60



Summary (1)

- Fast switching in & out of Gated Mode is key for the performance of the pixel detector
- Various parasitic capacitances extend
  rise and fall times of Clear voltage
  at gate level



- For various reasons (reducing deadtime, sync with CDC) the BELLE II collaboration wants to keep the total GM period (GM + pedestal oscillations) as short as 1µs
- Pedestal Oscillations after the Gated Mode can prevent the detector from recording reasonable data
- The presented analysis is based on meager Switcher Substrate connection at least for Switcher 5 + 6 (PXD9 Pilot Module), hence it is very difficult to draw accurate conclusions.

Summary (2)

- All we have are the following observations:
  - Pedestal Oscillations constitute a complex process, not everything can be traced back to a time constant
  - Pedestal Spikes after finishing GM look strange and have potentially something to do with the long fall time for the last switchers
  - It was shown that the shortest GM sequence (3gates w/o RO) reduces total GM time to 10 gates which would be equivalent to ~1µs @305MHz – CAUTION because of last switcher
  - GM with readout seems to elongate the total GM period although once falling under a certain threshold level pedestal variations appear much smoother
  - Mounting additional capacities on the dock-box and the patch panel as well as the analog CMC seem to reduce the Pedestal Oscillations
- **Looking forward to PXD9 series 7 incorporating heavily improved switcher voltage supply lines in order to find out more resilient results**

Thank you for your attention!

Analog CMC, IPAddIn = 60, ECG