FANGS

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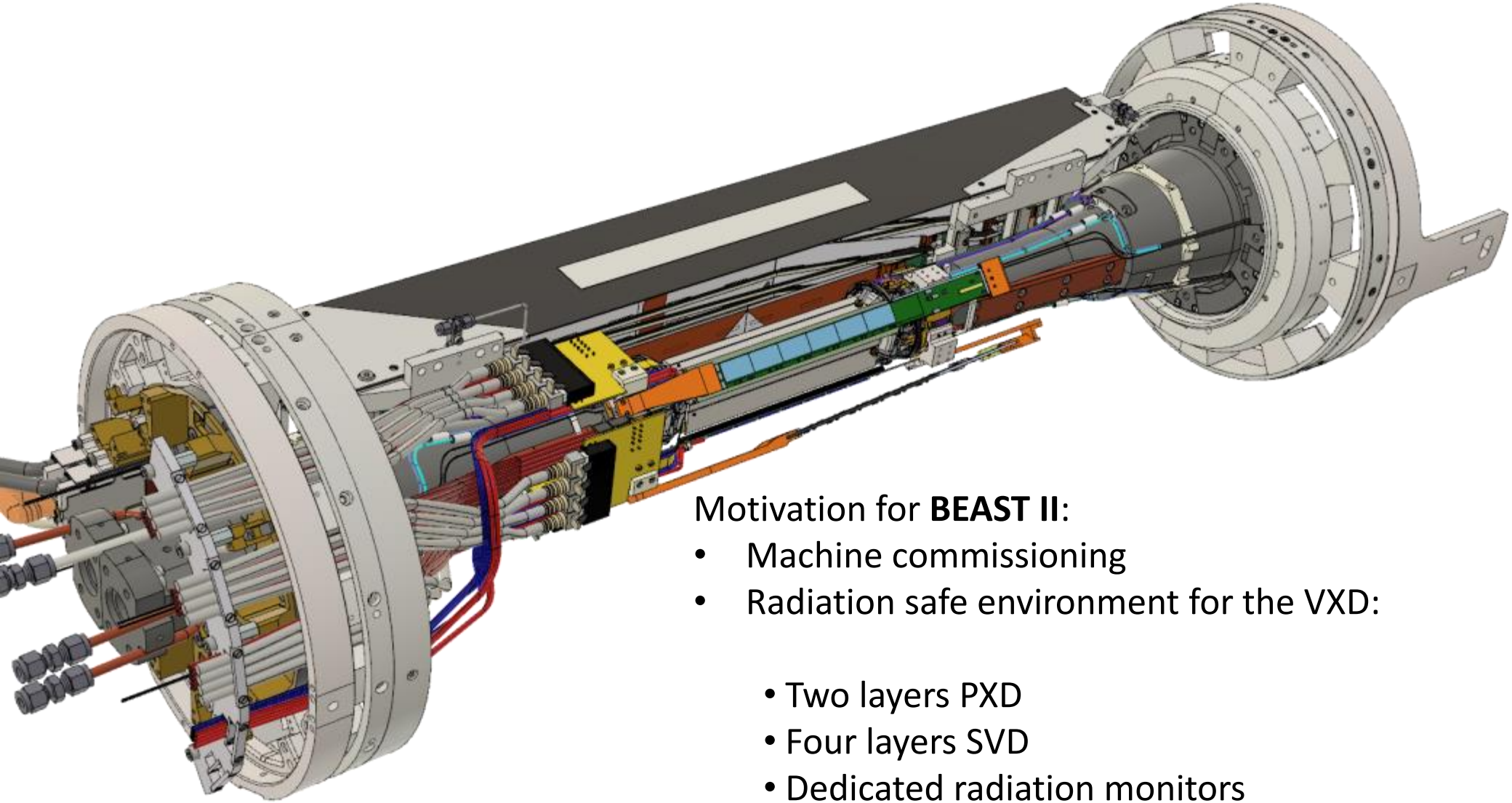
BEAST Commissioning Phase

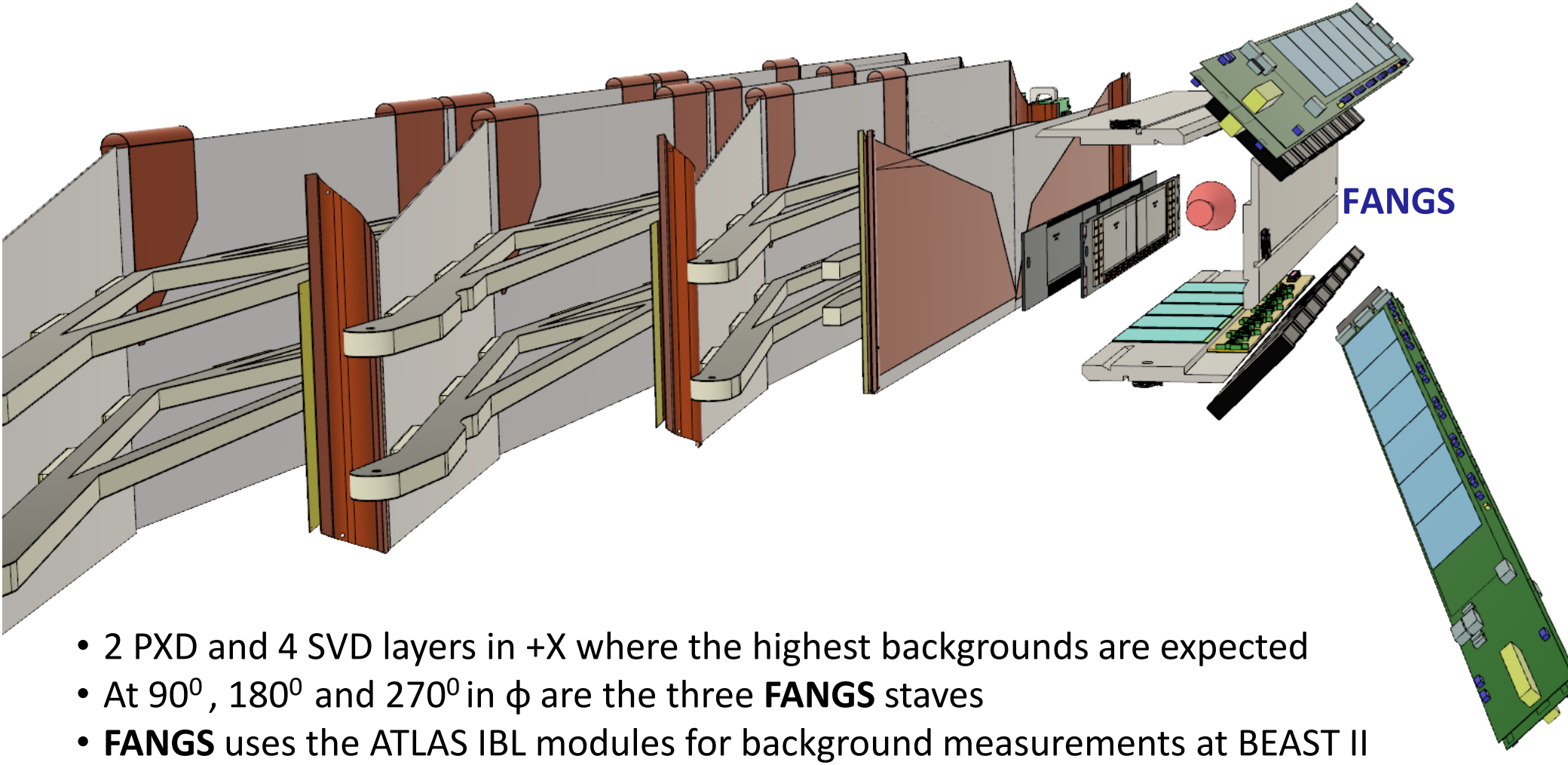


Motivation for **BEAST II**:

- Machine commissioning
- Radiation safe environment for the VXD:

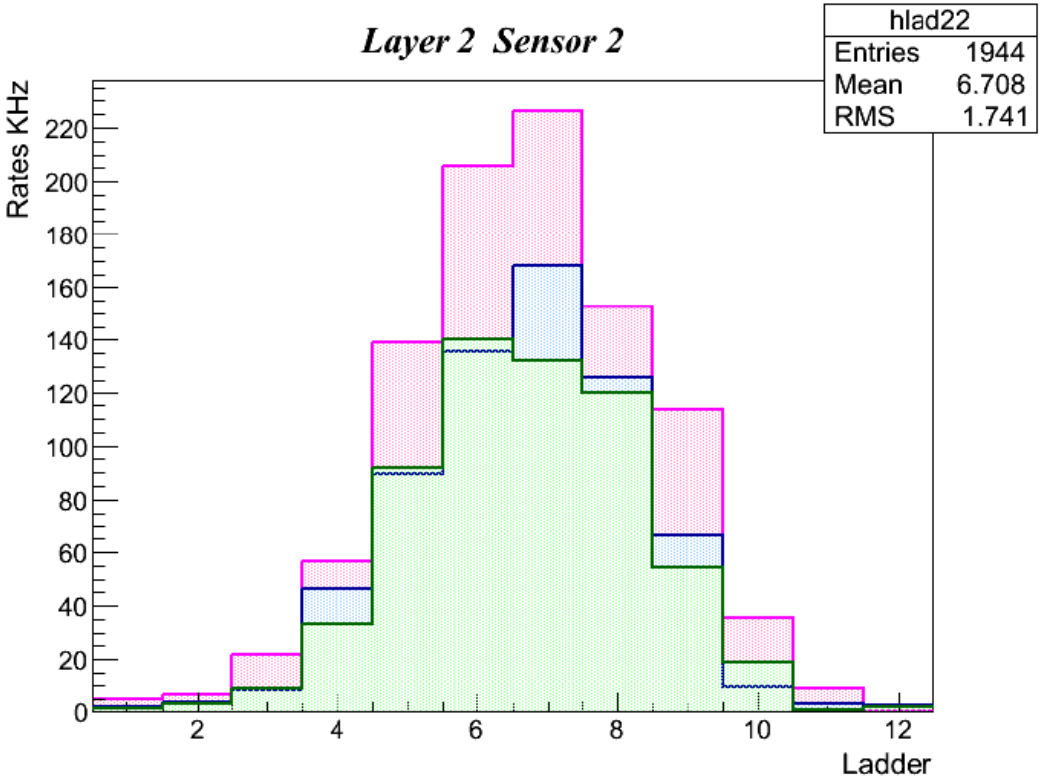
  - Two layers PXD
  - Four layers SVD
  - Dedicated radiation monitors
    FANGS, CLAWS, PLUME

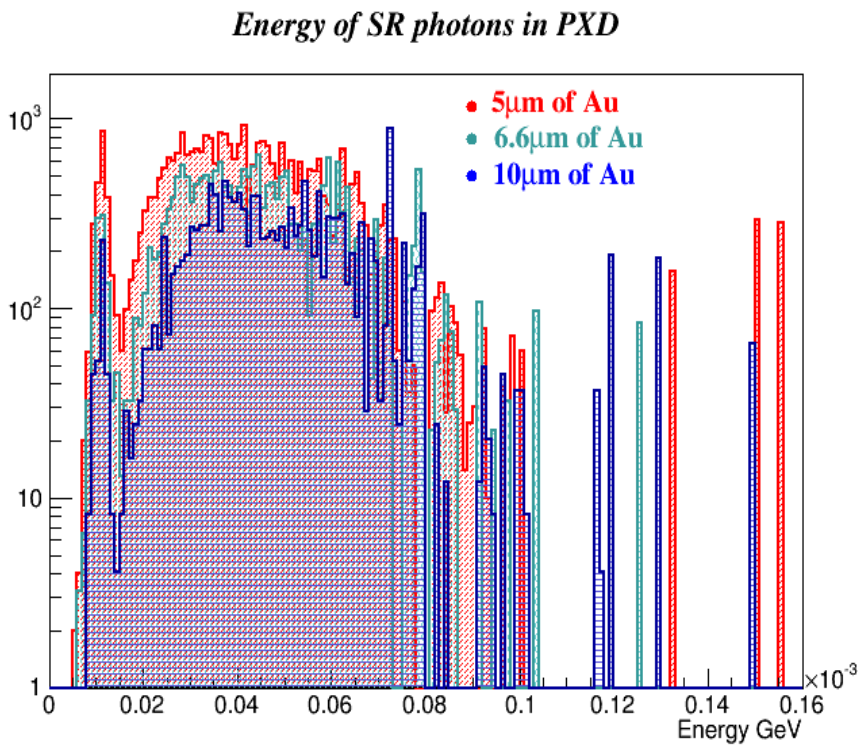
BEAST Commissioning Phase



- 2 PXD and 4 SVD layers in +X where the highest backgrounds are expected
- At 90^0, 180^0 and 270^0 in ϕ are the three **FANGS** staves
- **FANGS** uses the ATLAS IBL modules for background measurements at BEAST II

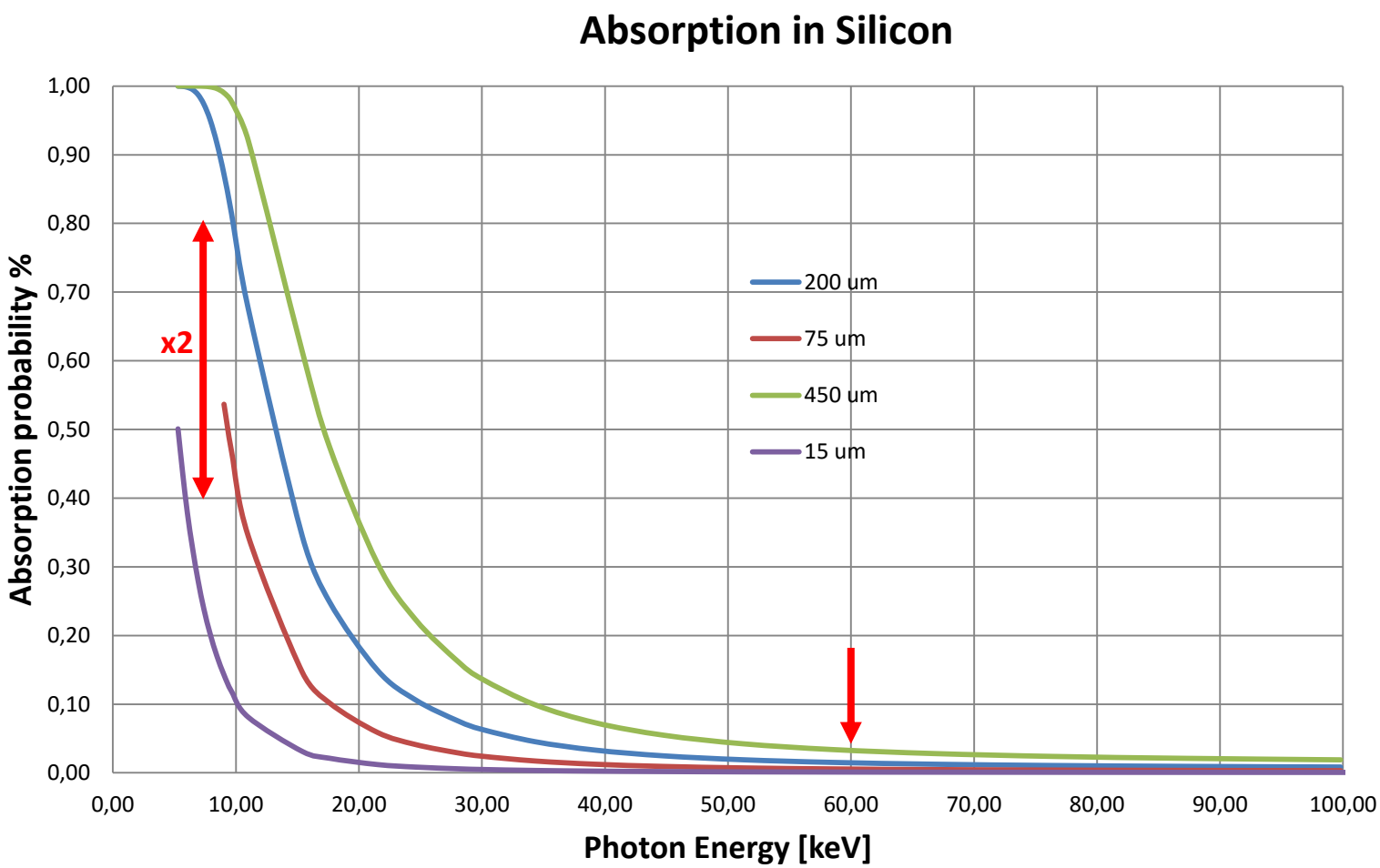
Detector Requirements



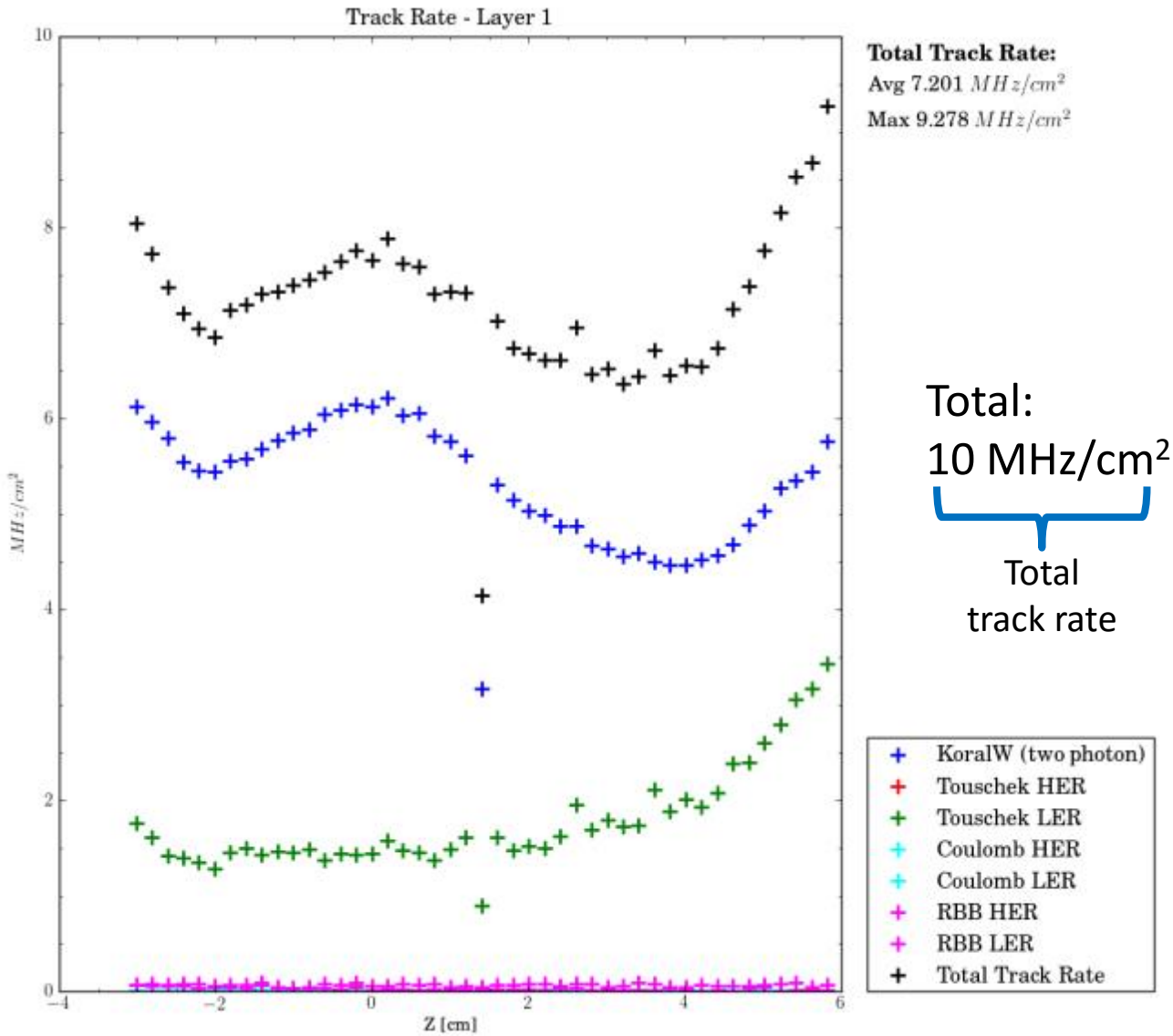


- During BEAST II: Final detector configuration (besides VXD chamber)
- 6.6 µm Au foil around beam pipe in BEAST II to enhance synchrotron radiation:
  - Maximum PXD hit rate of 28.64 KHz/cm^2 (~ factor 2 higher for FANGS)
  - Withstand a total dose of 4 Mrad
  - Largest contribution in the range of 10 - 90 keV

Absorption Probability



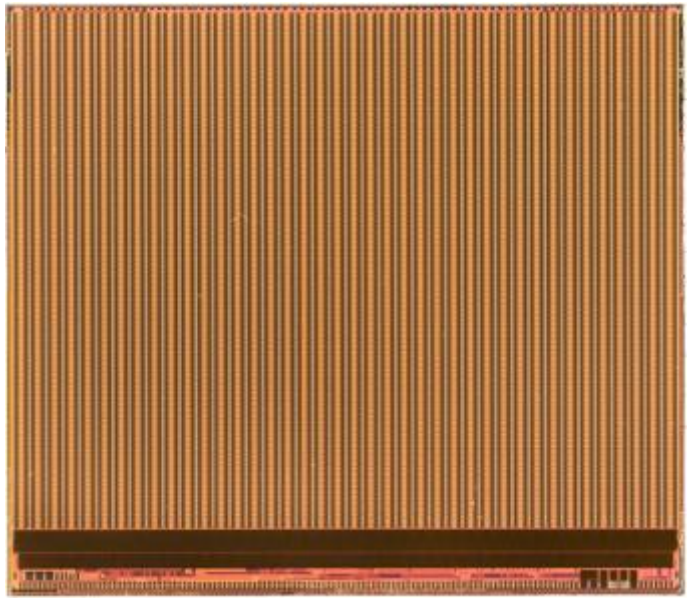
Total Particle Rates

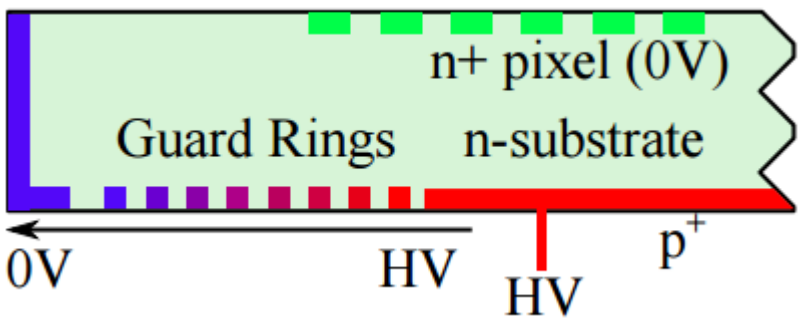


Total:

$$\underbrace{10\ \mathrm{MHz/cm^2}}_{\text{Total track rate}} + \underbrace{60\ \mathrm{kHz/cm^2}}_{\text{SR}}$$

FANGS: FE-I4 ATLAS Near Gamma Sensors



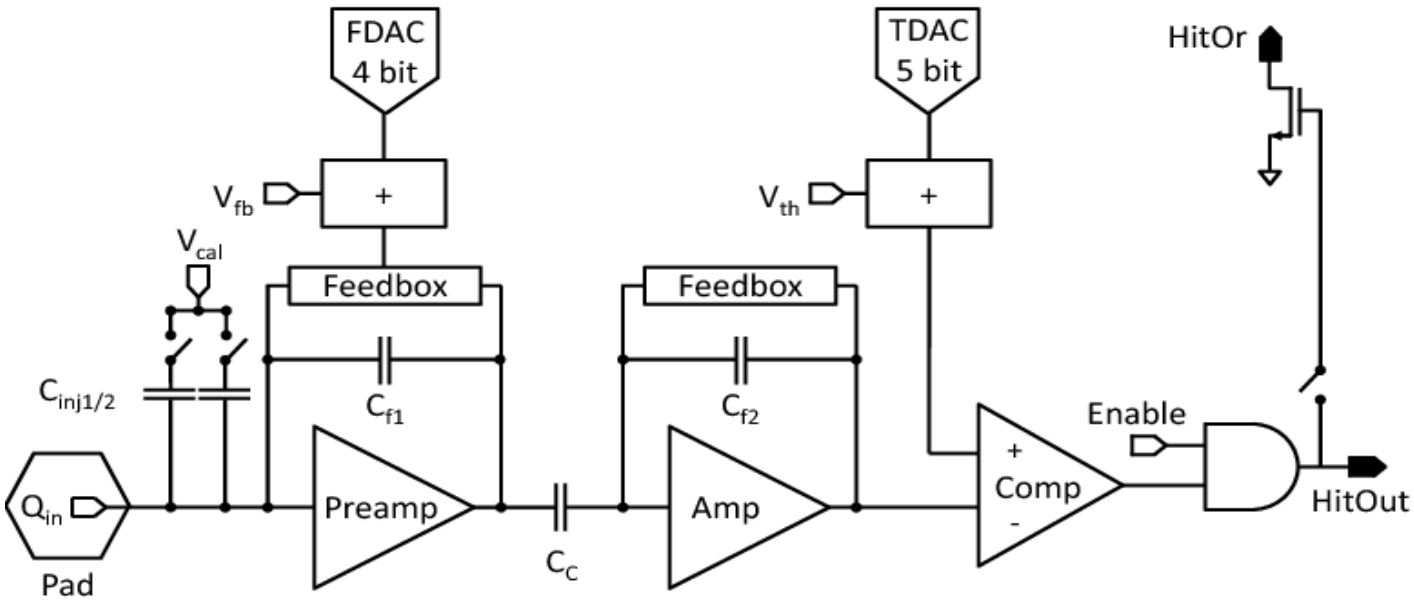


- FE-I4 read out chip
  High hit rates (400 MHz/cm²) and radiation hard (300 Mrad)
  IBM 130 nm CMOS process
  Read out for 80x336 pixels
  Thickness=150 µm
  Physical size=**21x19 mm²**

- Sensor:
  n-in-n planar
  Pitch=**50x250 µm²**
  Thickness=200 µm
  Physical size=19x20 mm²
  HV=60 V
  Power=1.2 W

- **Background radiation measurements in Phase 2:**
  - Sensitive to low keV X-rays
  - Ability to measure high particle rates

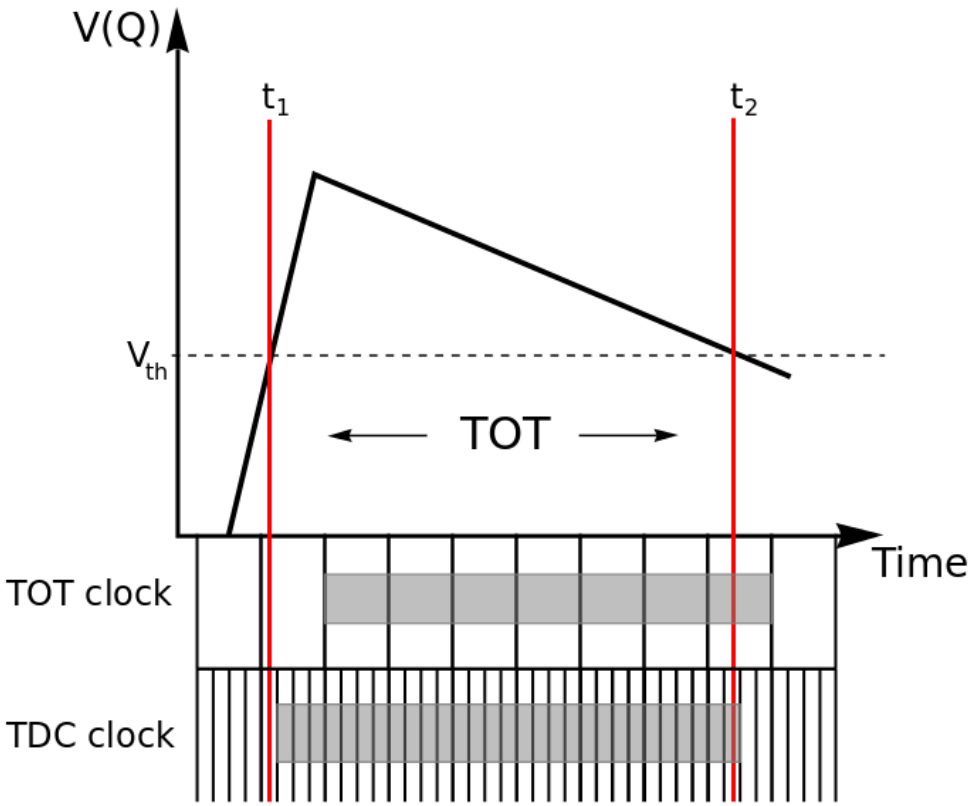
TDC Method



- Two stage amplifier → Discriminator with adjustable threshold.
- Time over threshold **(TOT)** with 40 MHz clock.
- Time to digital converter **(TDC)** uses 640 MHz FPGA clock.
- Output of each pixel is ORed (Trigger).
- Internal charge injection circuit for threshold tuning and calibration (PlsrDAC)

→ Both, high speed and adequate energy resolution achieved at the same time

TDC Method



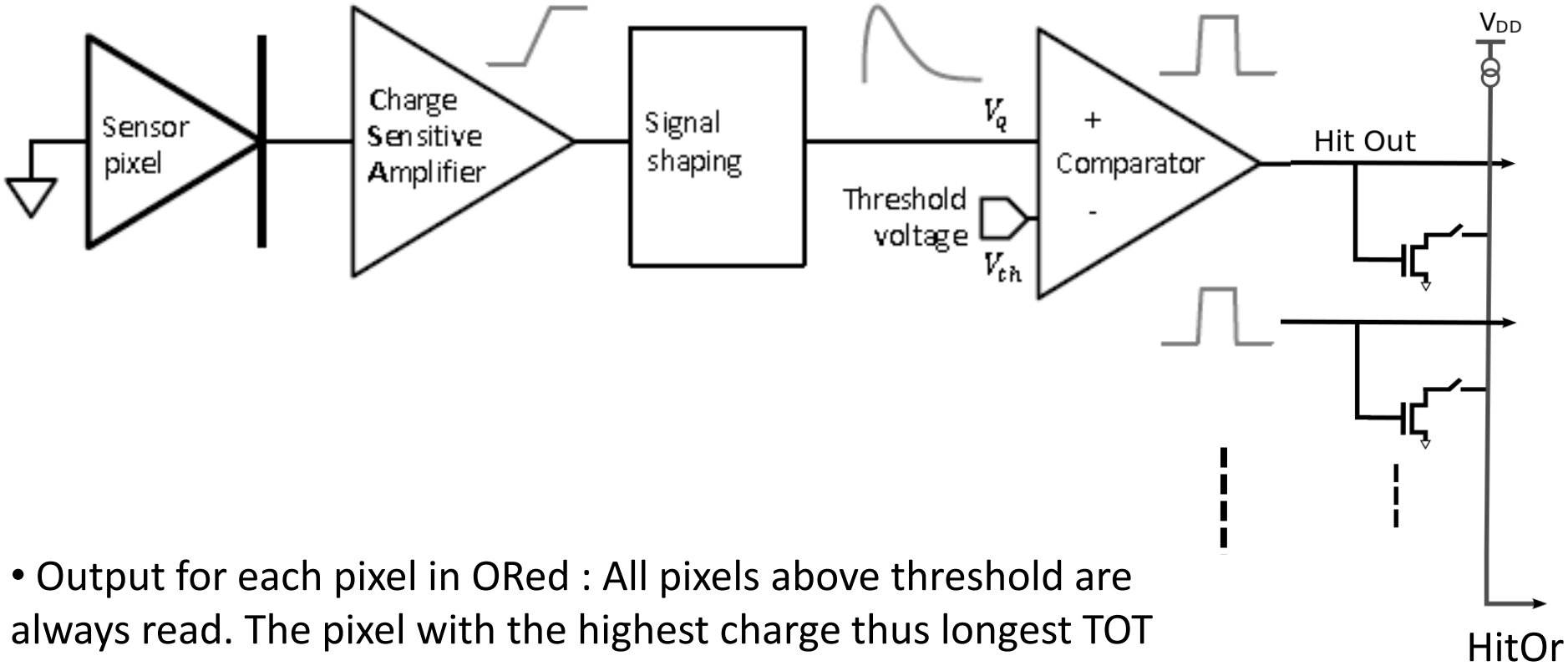
Two independent measurements simultaneously:

A. TOT 40 MHz clock: 4 bit resolution
- Contains pixel and timing information

B. TDC with external FPGA's 640 MHz clock: 12 bit resolution
- Voltage signal of comparator output with the highest charge
- Limited to **one** pixel per readout

➢ Improved resolution

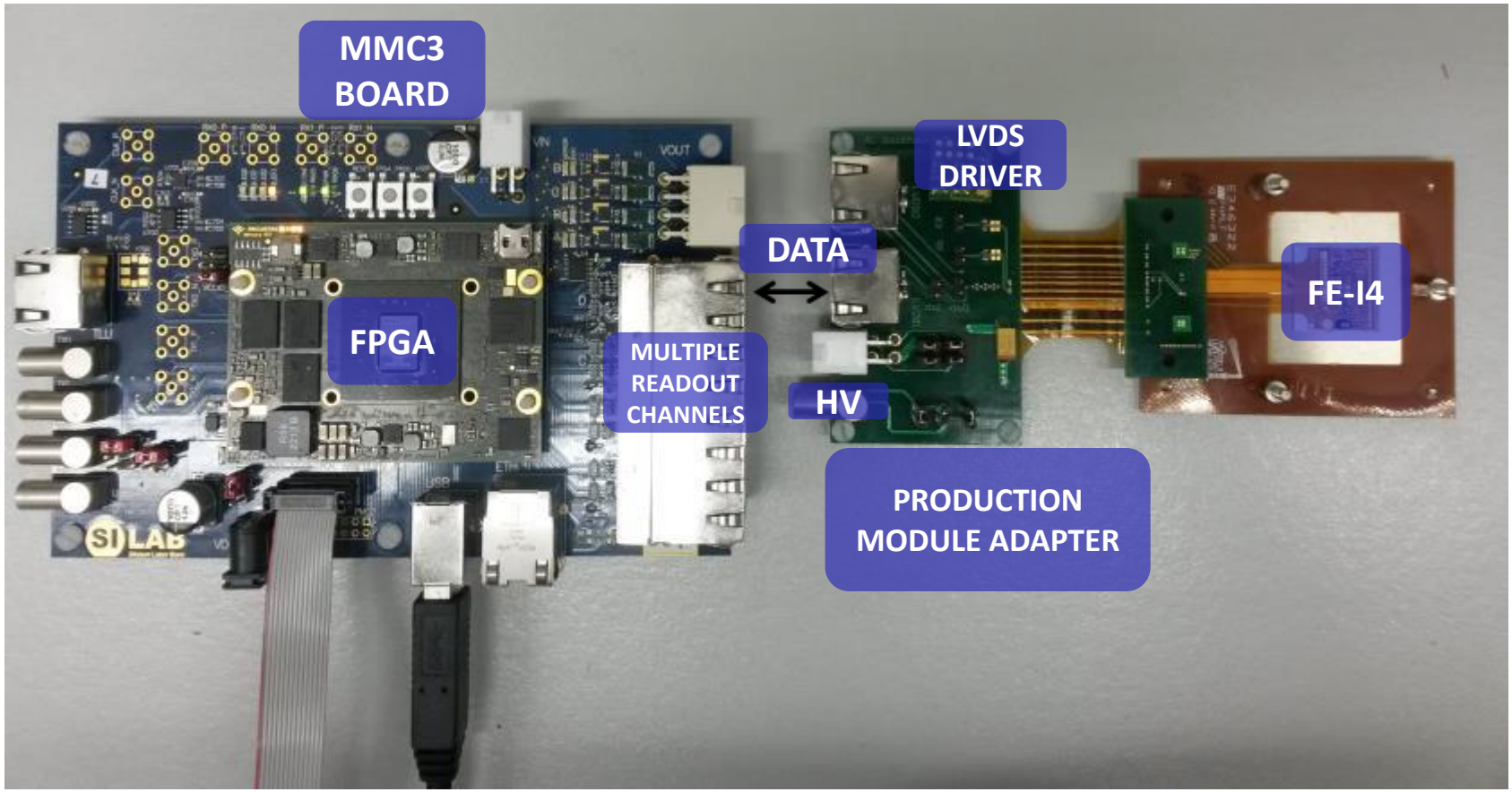
Pixel Schematic



- Output for each pixel in ORed : All pixels above threshold are always read. The pixel with the highest charge thus longest TOT can be additionally measured with the FPGA TDC to get the charge signal with higher precision.

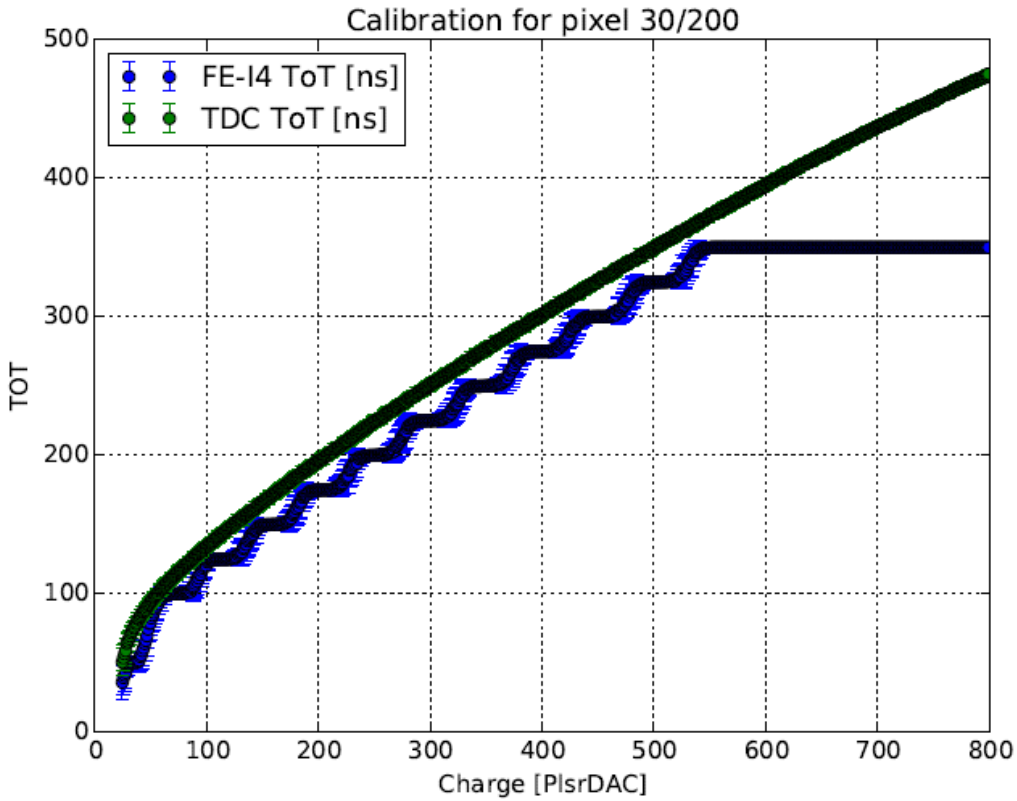
- Hit Bus also used as self trigger

Experimental Setup



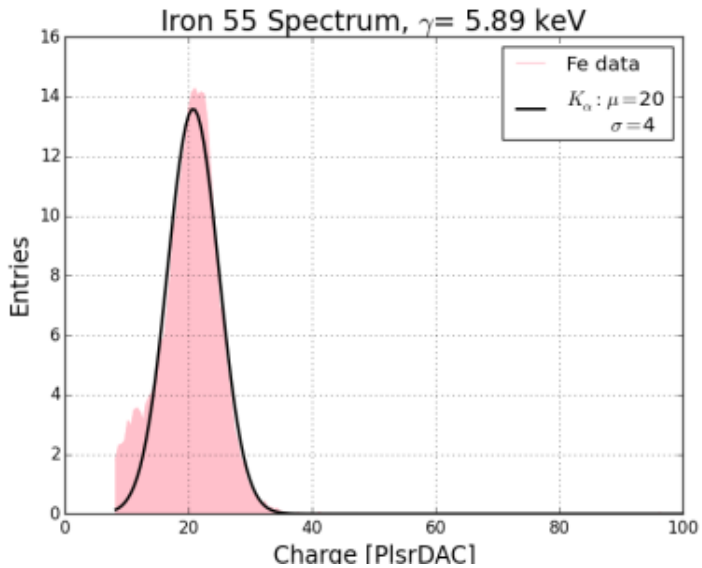
- MMC3: New data acquisition system for the BEAST experiment
  - Multiple FE read out in parallel
  - Faster FPGA; TDC Method may be improved
- Single ended HitOr signal converted to an LVDS signal.

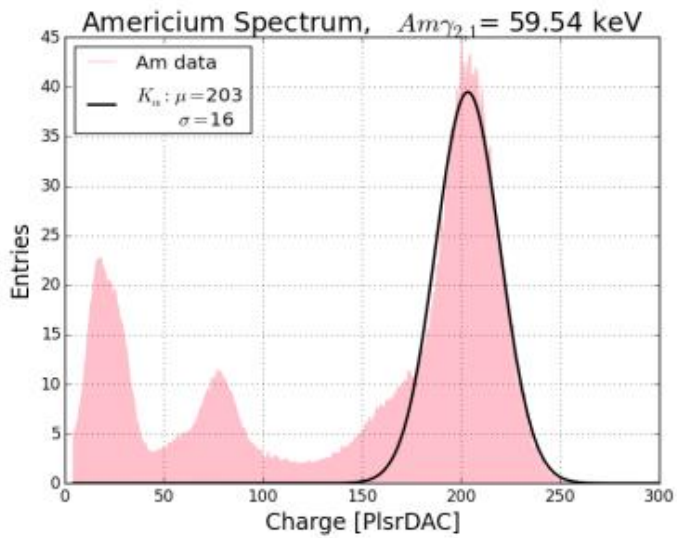
Pixel-per-pixel Calibration of Hit Or Signal

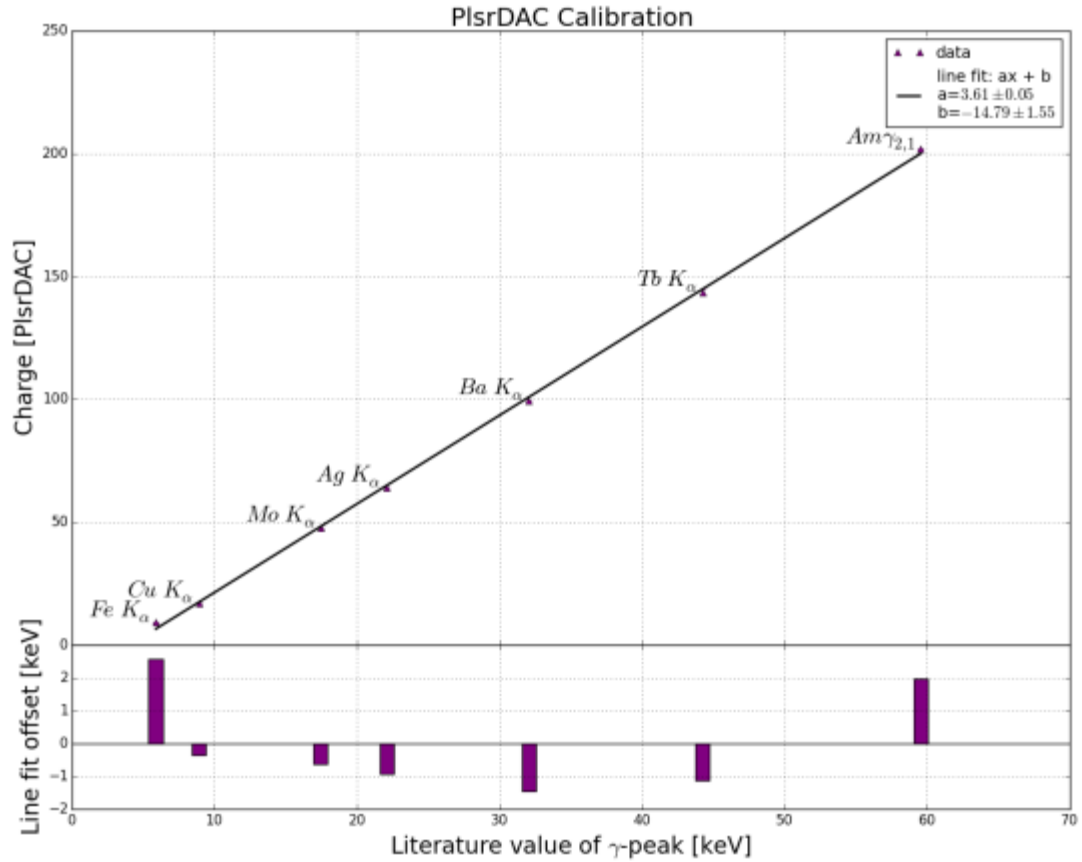


- Precise energy resolution requires pixel per pixel calibration
- Internal charge injection in units of PlsrDAC
- V_{th} and TDC as a function of charge different for each pixel.

Calibration and Dynamic Range

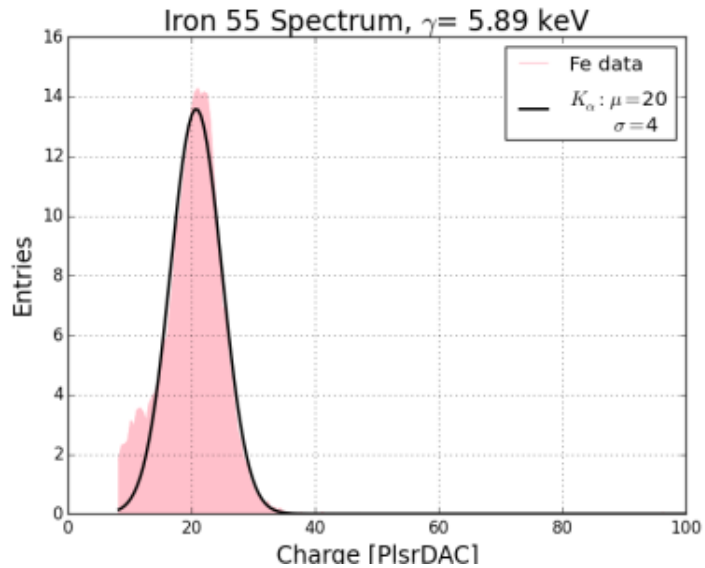


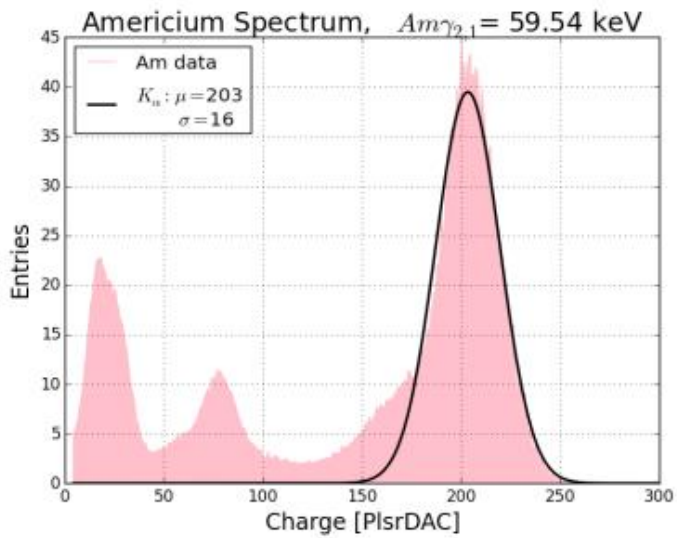


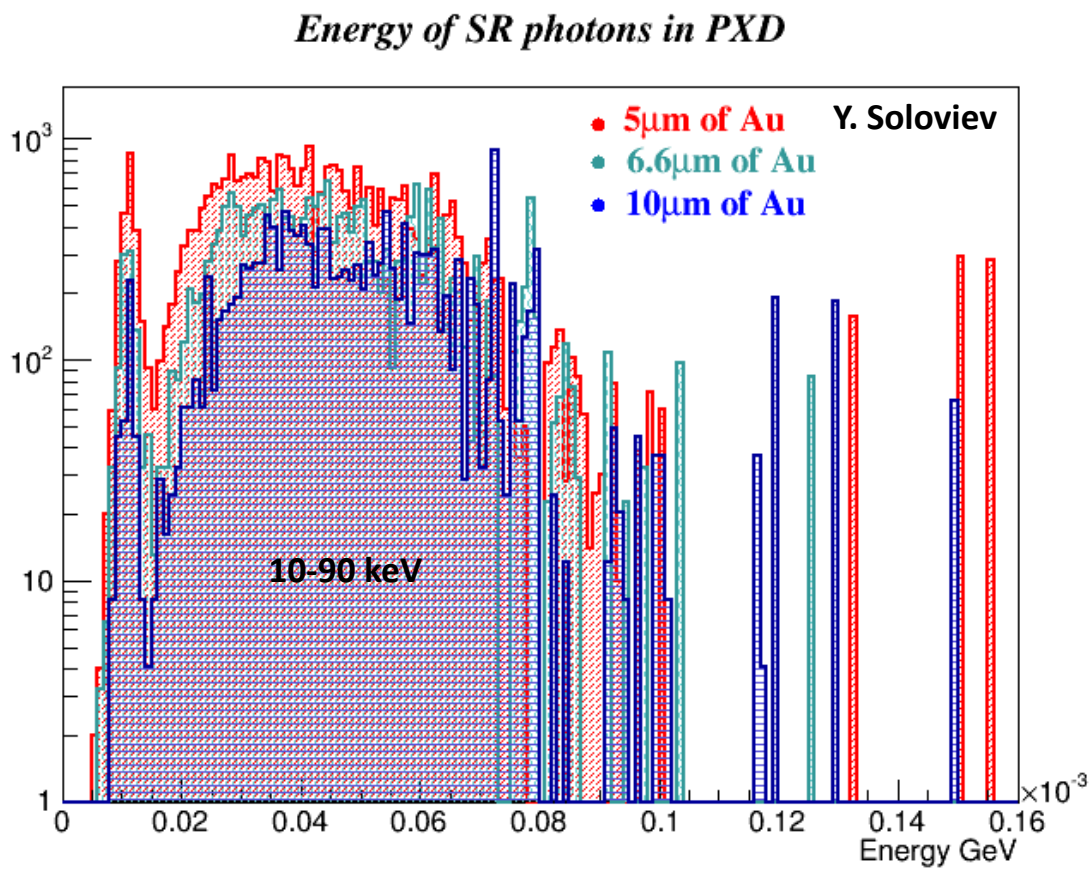


- Dynamic range 10-60 keV (wider also possible)
- Lowest measured plsrDAC value ~ 7
  - Threshold of ~1000 electrons feasible

Calibration and Dynamic Range







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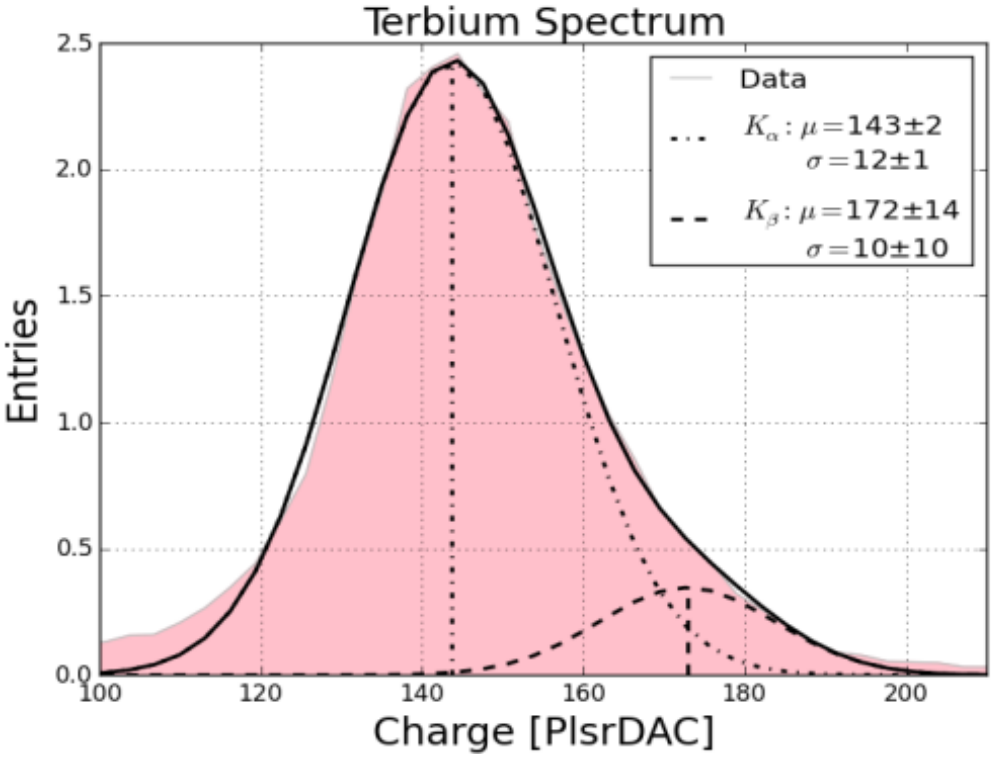
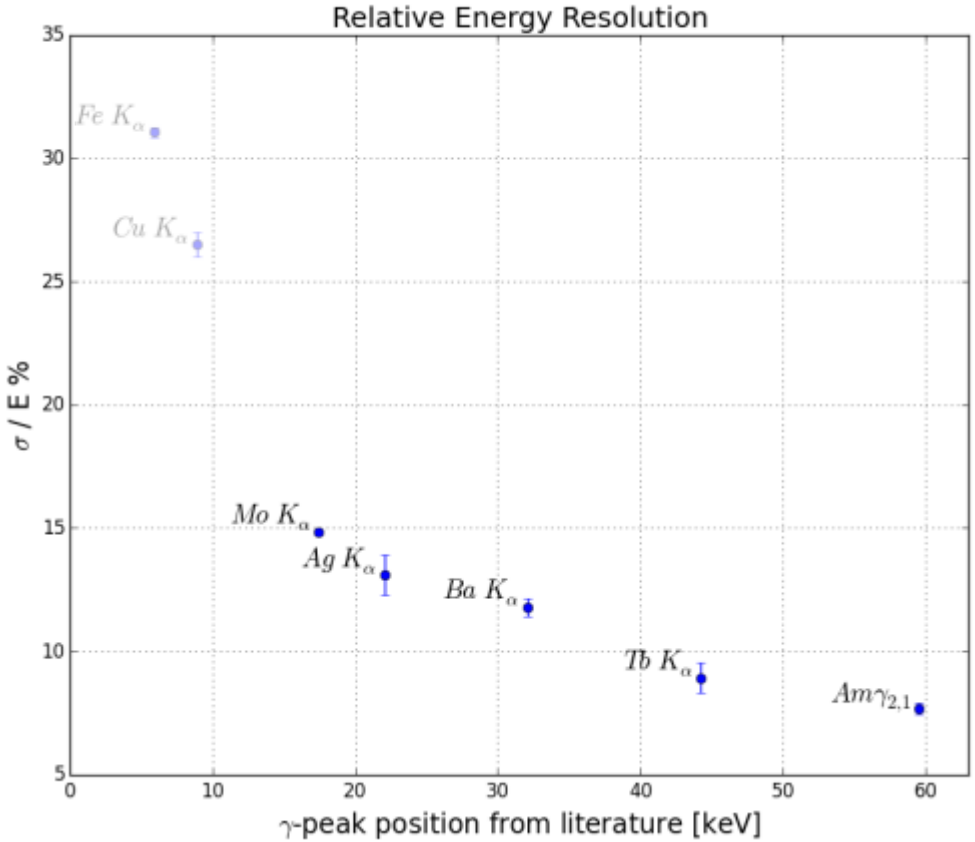
Energy Resolution



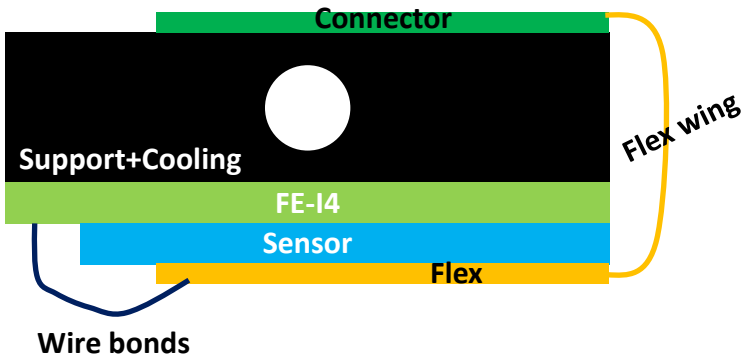


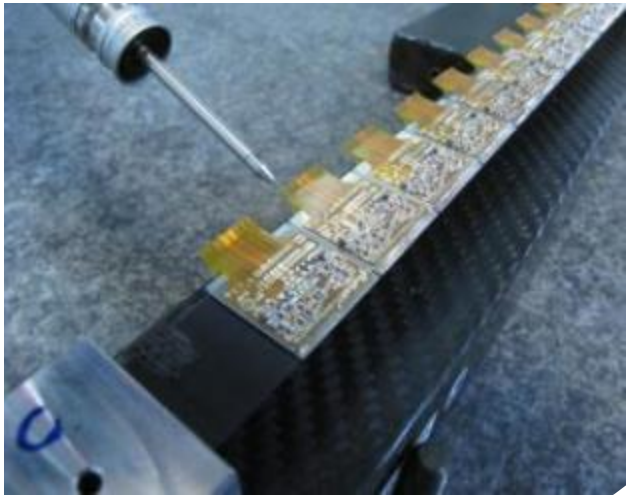
- Terbium K_α=44.2 keV, K_β =50.7 keV
- ΔE = 6.4 keV

- Adequate energy resolution
- Better than 15 % above 10 keV

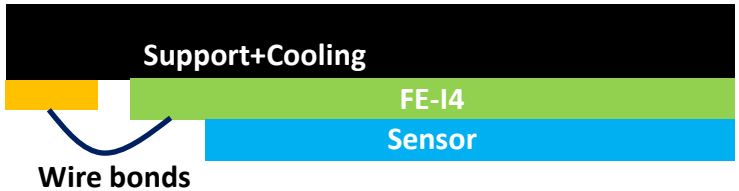
FANGS Stave Design Concept

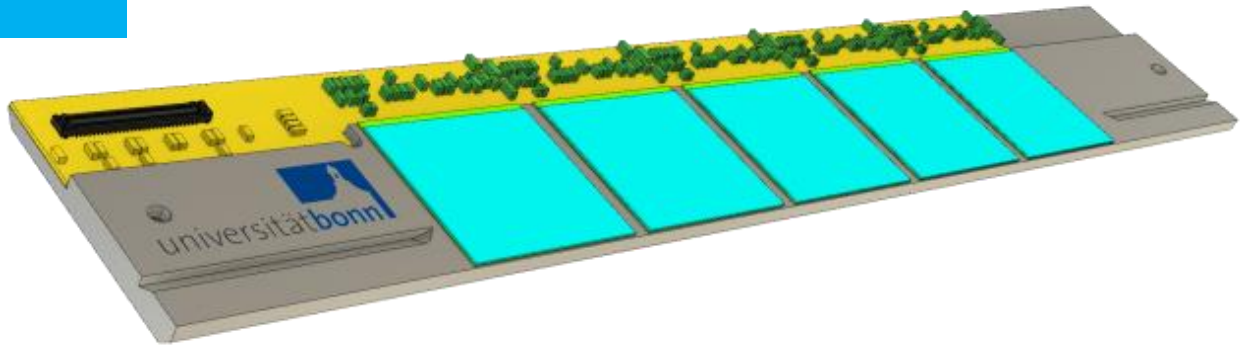
- Initial concept, following IBL stave design



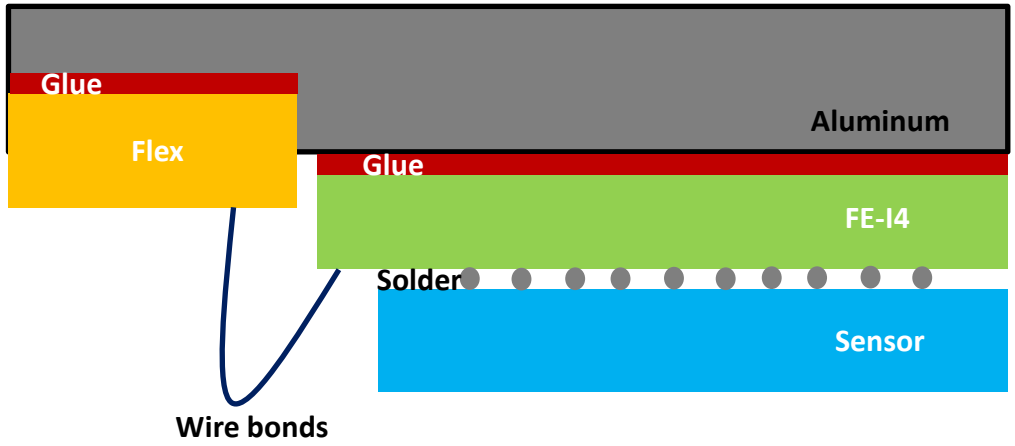


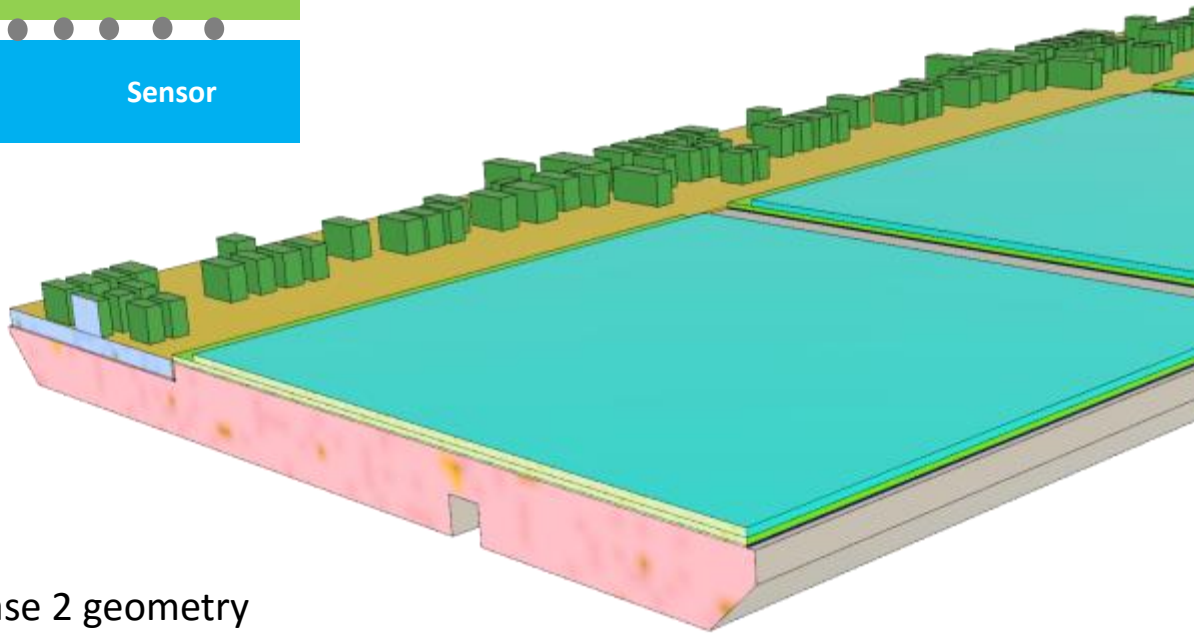
- Revised design, adapted to BEAST needs





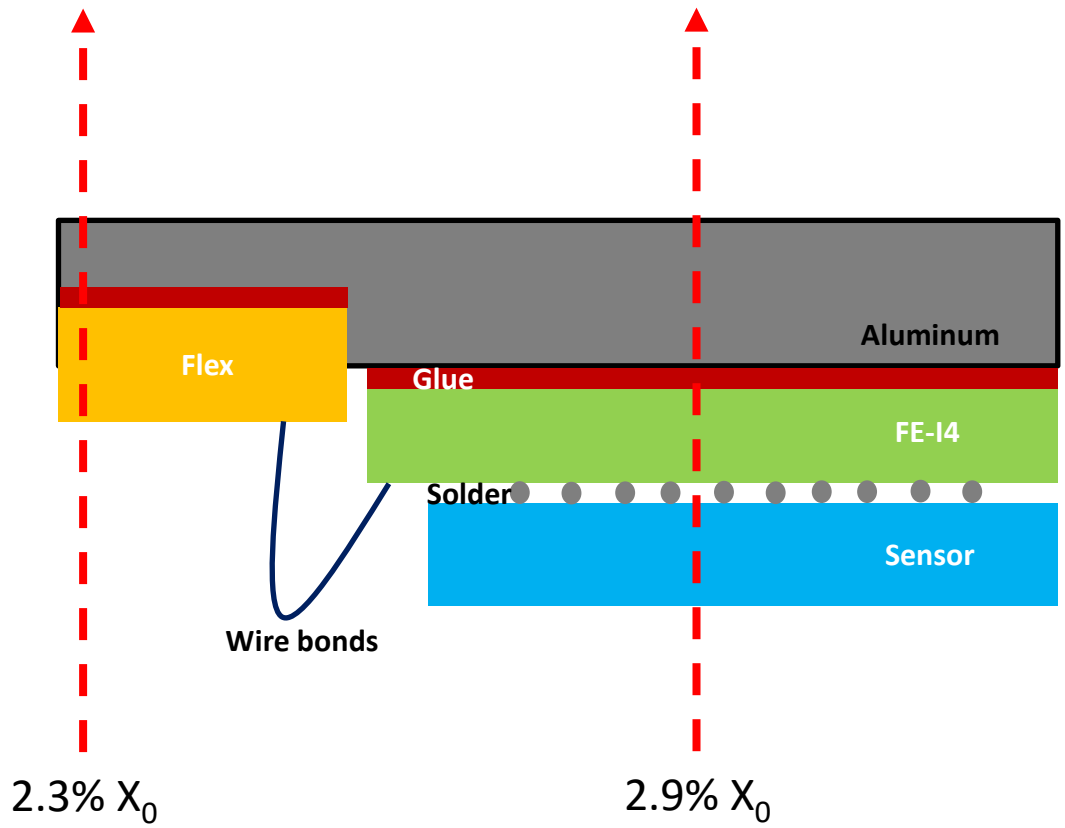
Stave Material Budget





Stave material description to be updated in Phase 2 geometry

Stave Material Budget



- Low and flat material budget distribution
- No impact in outer detectors

- Support:
2 mm thick Aluminum → 2.2%X_0

- Glue:
50 µm thick Epoxy → 0.014%X_0

- FE-I4
150 µm thick Silicon → 0.16%X_0

- Sensor:
200 µm thick Silicon → 0.21%X_0

- Solder balls
25 µm thick SnAg → 0.17%X_0 (3.3% of the area)

- Flex
66 µm thick polymide → 0.023%X_0
24 µm Cu (2 layers) → 0.17%X_0

$Total_{Max}$: **2.9% X_0**

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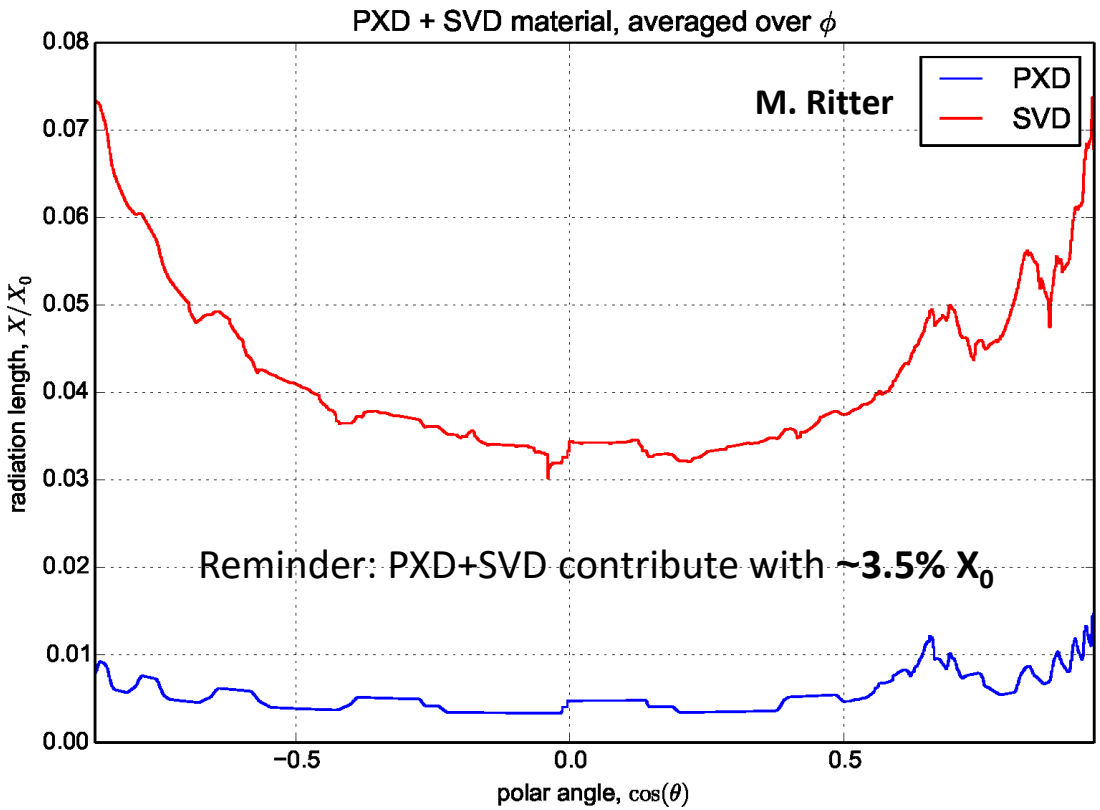

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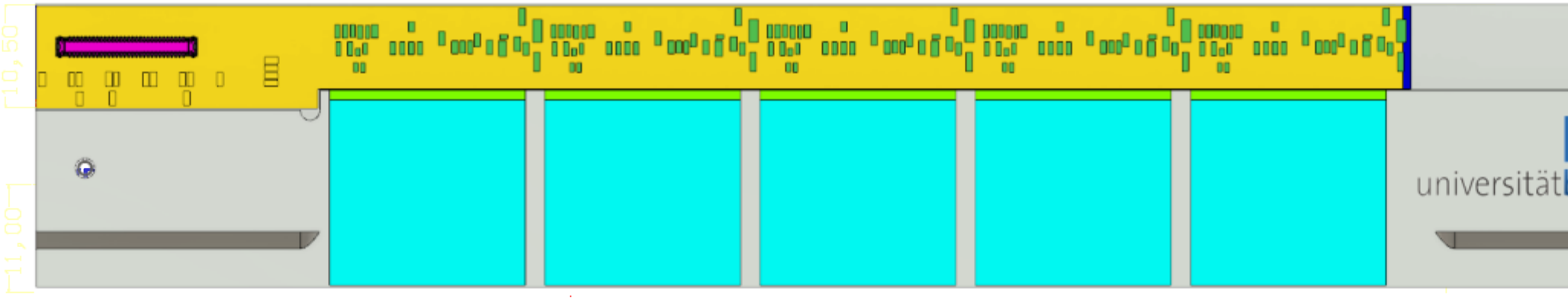
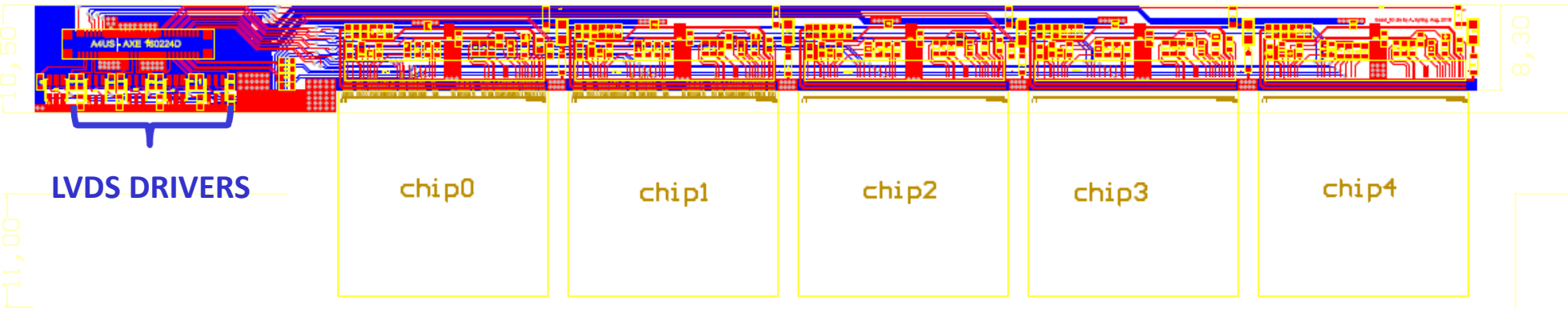
Kapton Design



- Flex design for a single stave of 5 FE-I4 chips
- LVDS drivers converting single ended HitOr signal to differential signal for propagation over long cables
- Drivers positioned in backward direction shielded from radiation behind the PXD cooling block
- Radiation hardness to be investigated

Kapton Design



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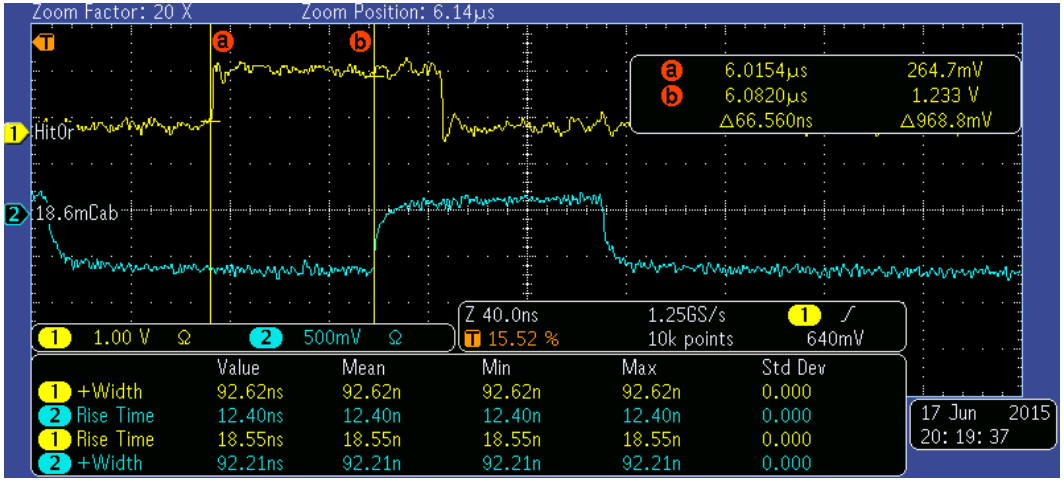
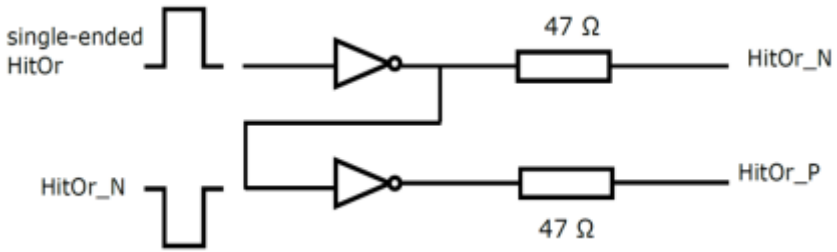
Hit Or Delay and Signal Quality Measurements

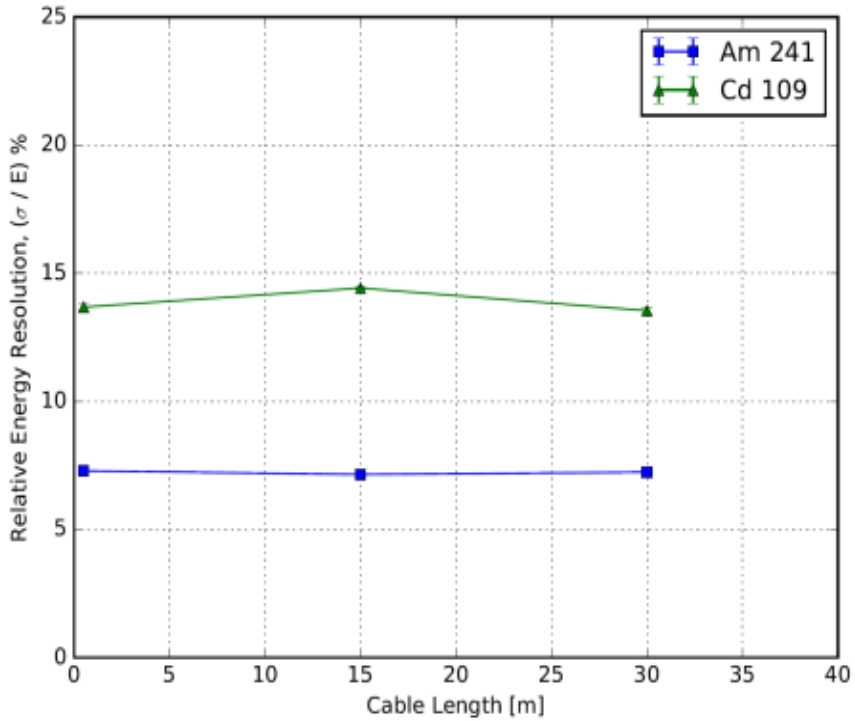


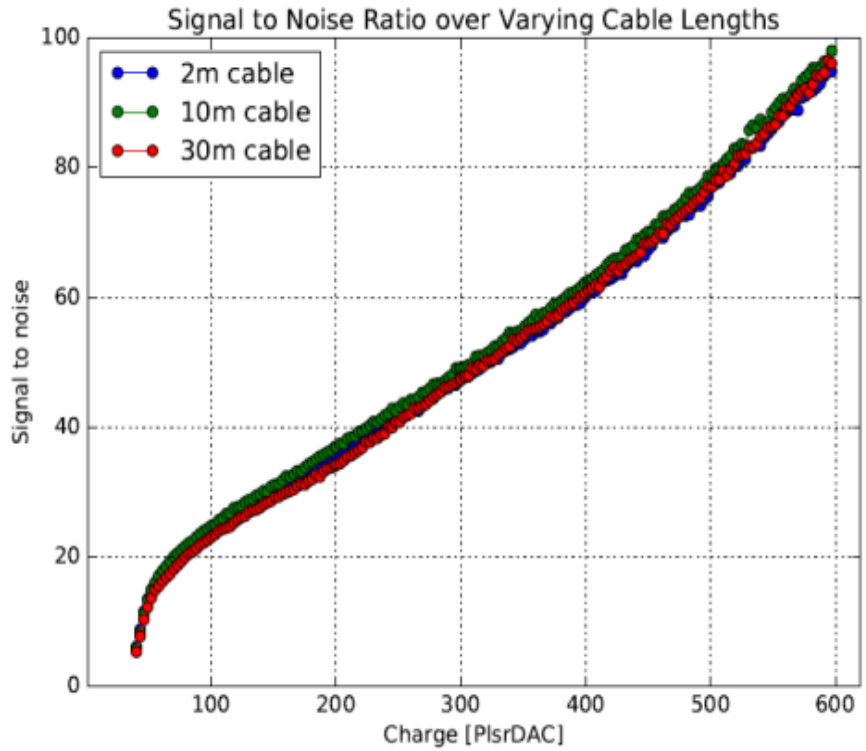


- Convert single ended HitOr to differential

- Propagation delay of HitOr over a 19 m CAT 7
- Signal integrity maintained with delay of ~60 ns
- Improvement pulse shape under investigation

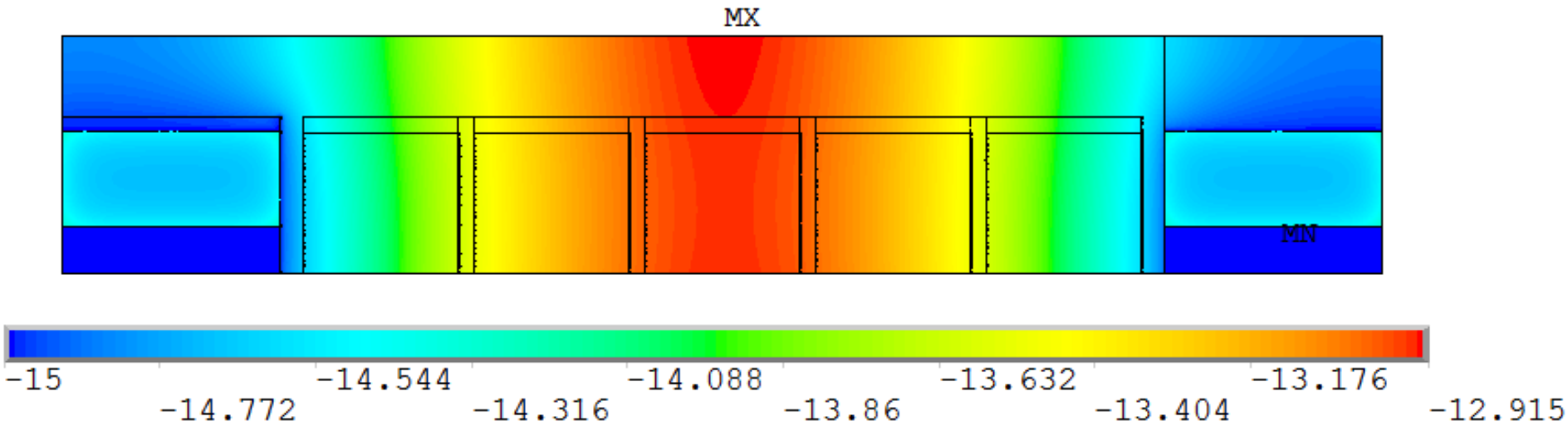
Signal Integrity





- Signal integrity maintained over 20 m cable
- Proper resolution over this range

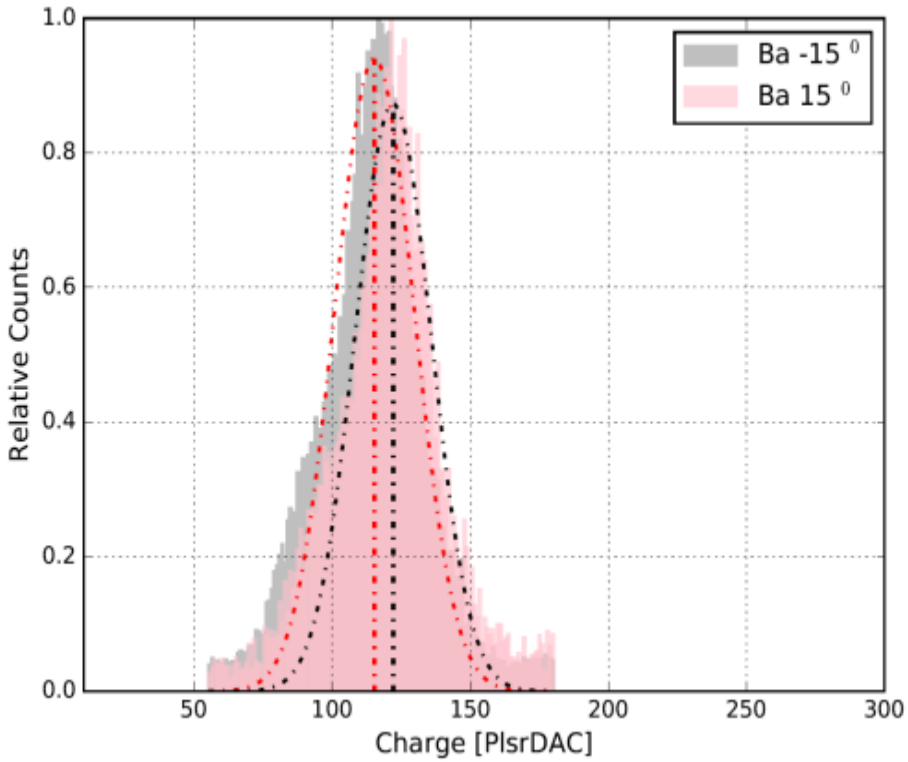
FEA of the FANGS Stave

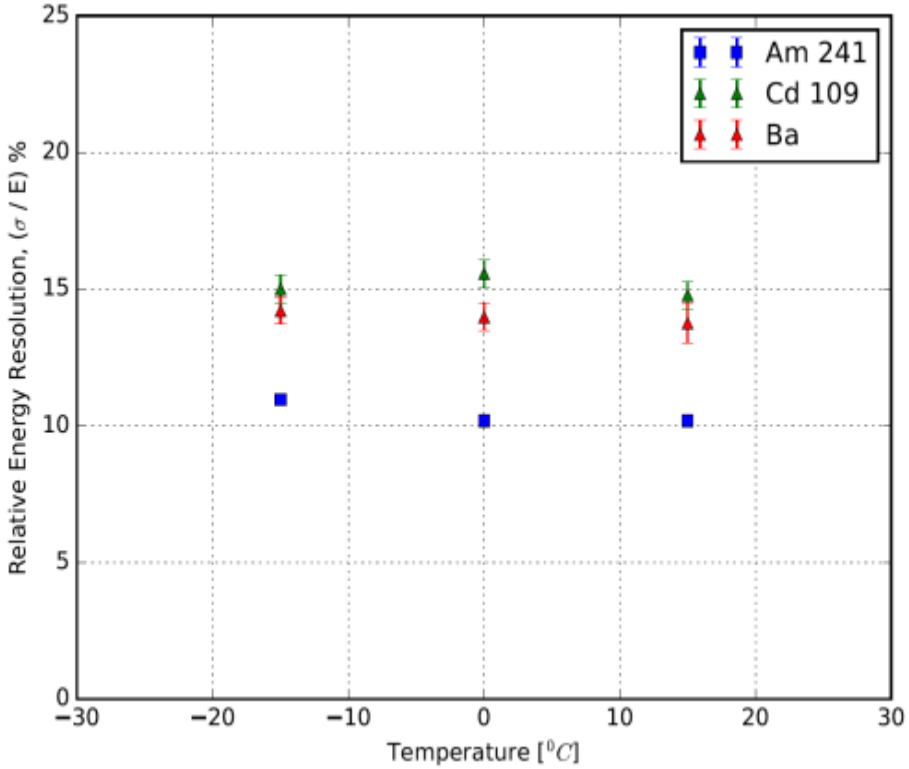


- Maximum temperature = -12 ºC
- Maximum ΔT within one sensor = 2 ºC
- Power = 1.2 W each FE
- Cooling block = -15 ºC
- Environment = 20 ºC at 2 m/s

- Proper heat handling
- Low and flat temperature profile
- FOS integrated on the Al profile for temperature measurements

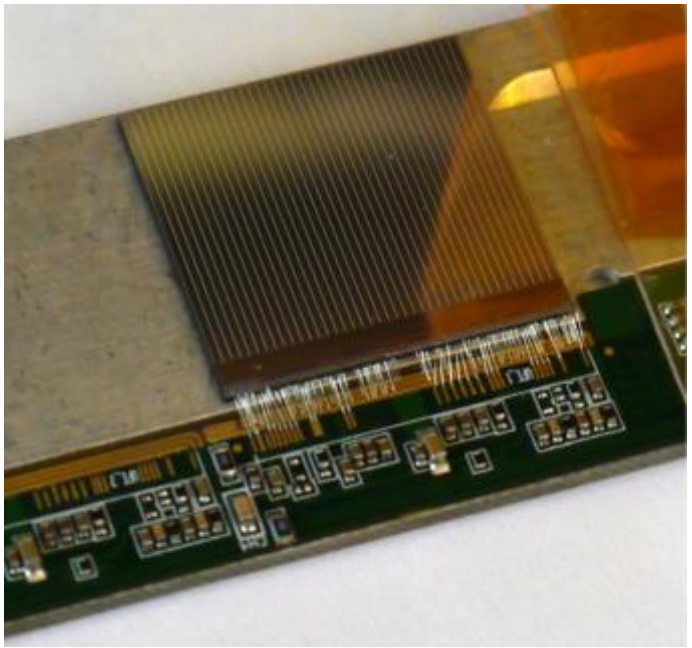
Energy Resolution with Temperature

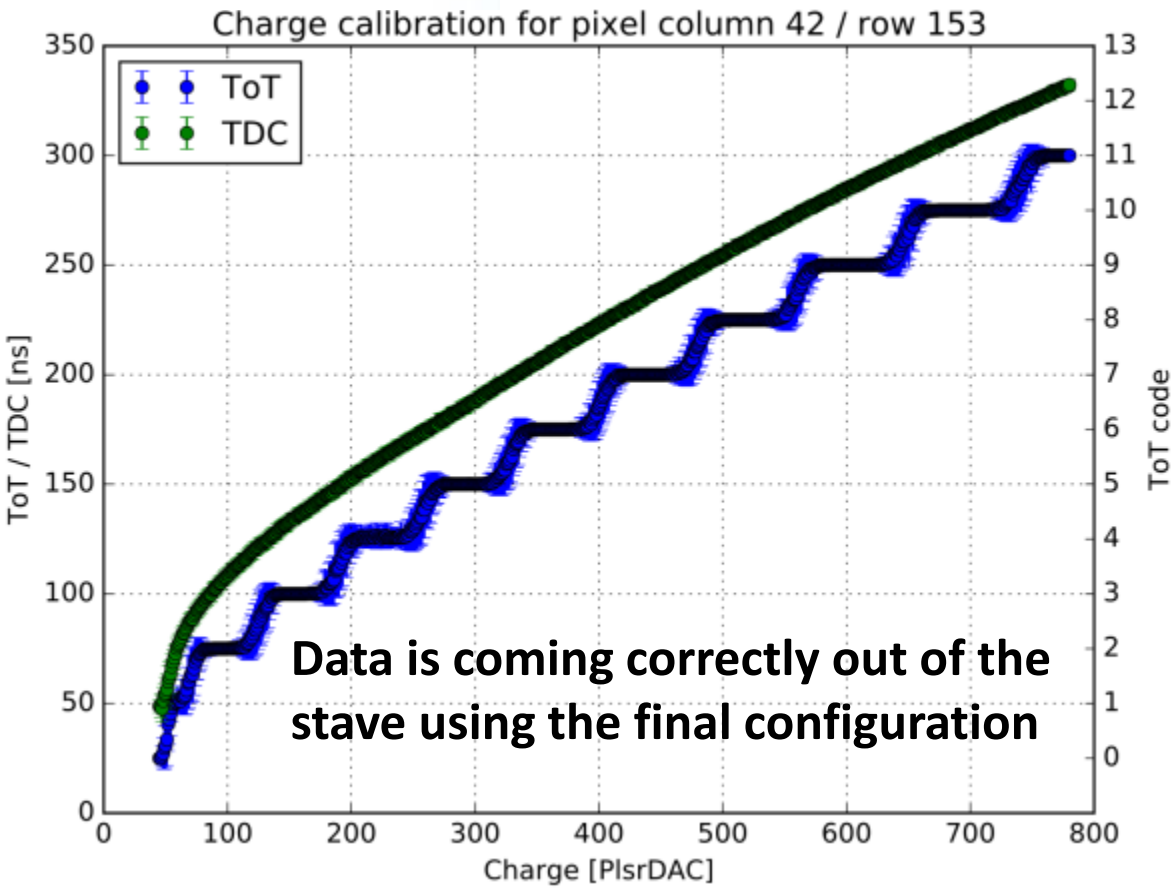




- No performance degradation is observed over the expected temperature range

HitOR Calibration





Data is coming correctly out of the stave using the final configuration

Test stand for **FANGS**:

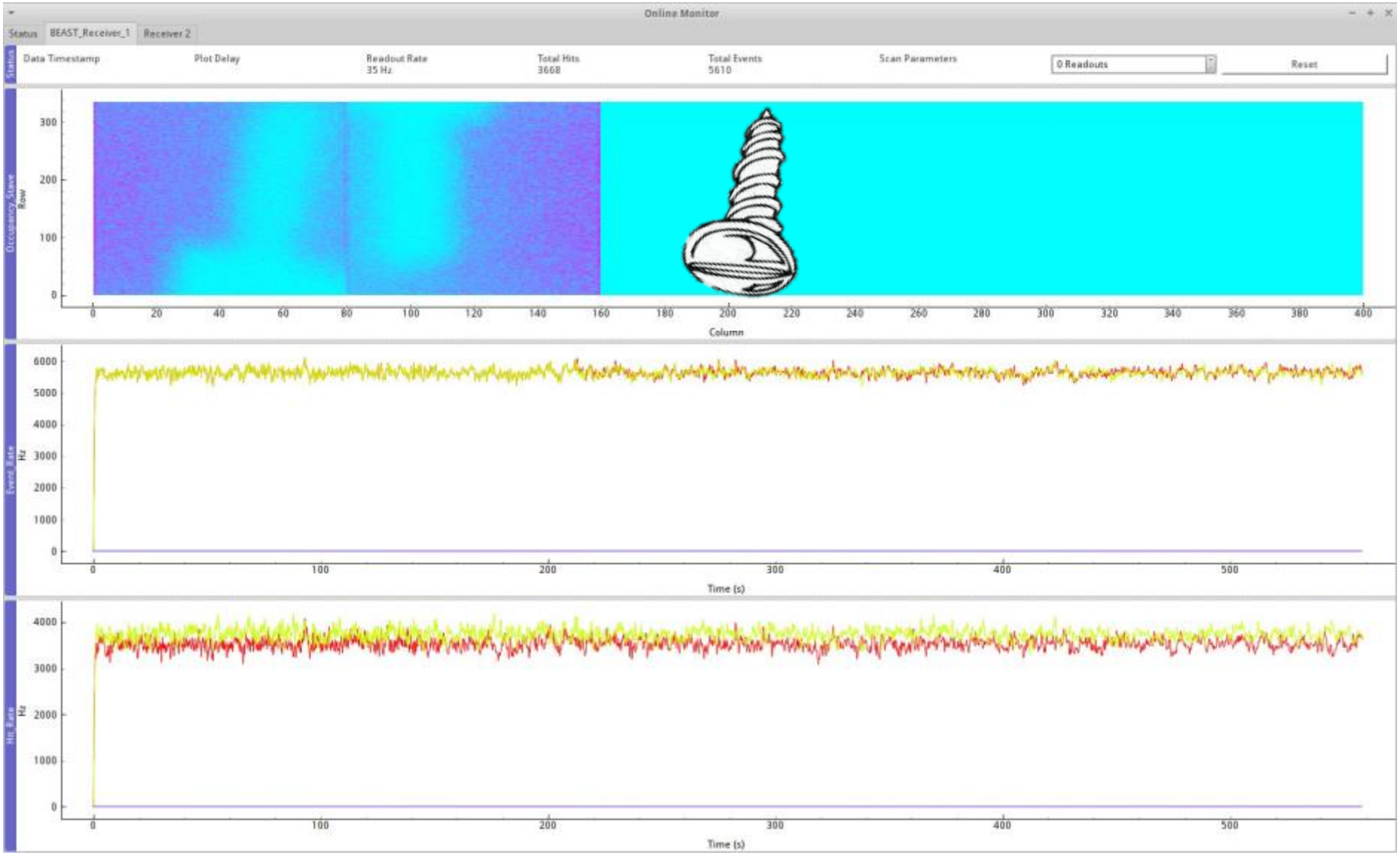
- Cooling block at 15^0C
- Gentle forced convection

First FANGS stave fully operational

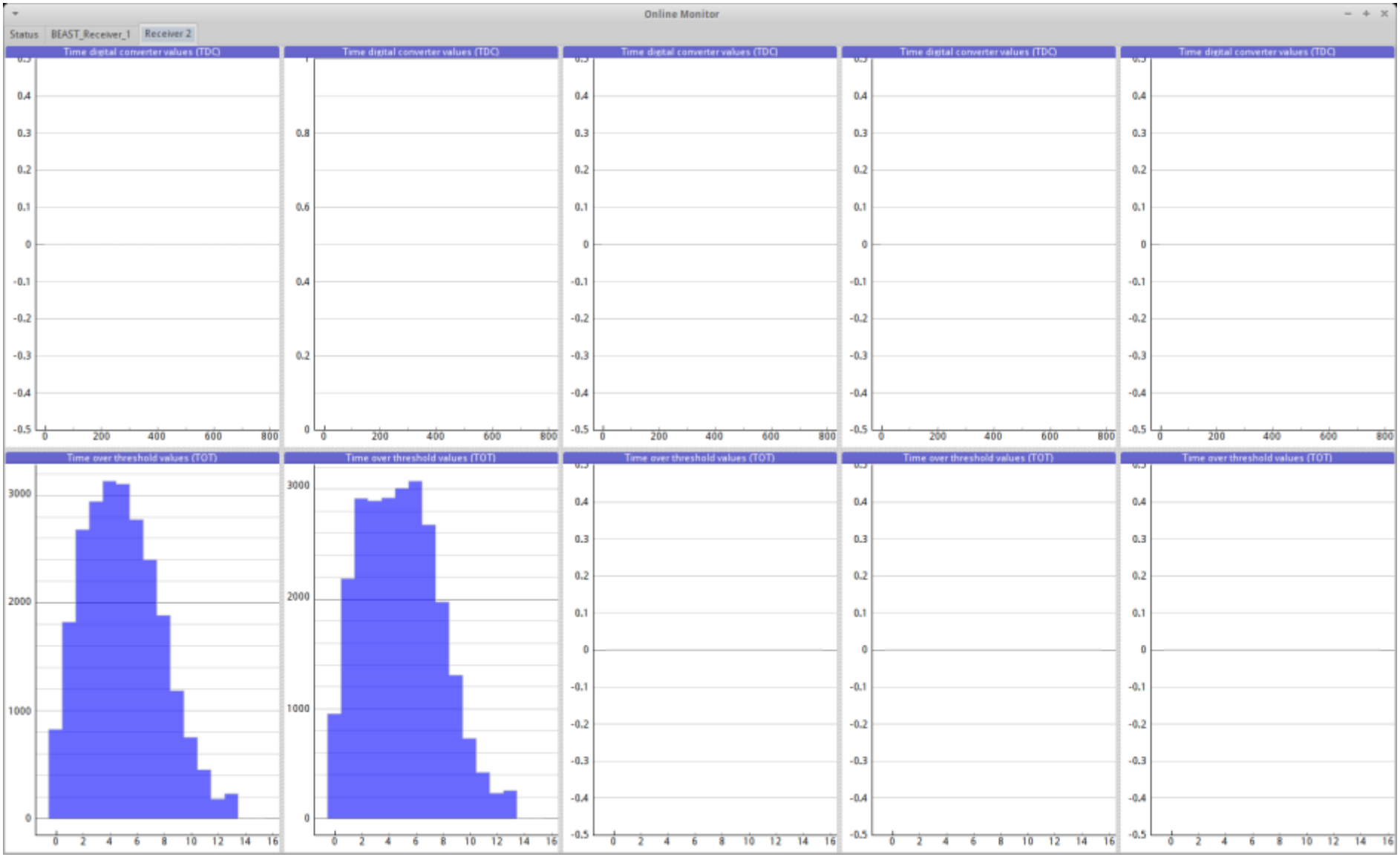
FANGS Production

- Final staves produced
- Testing ongoing

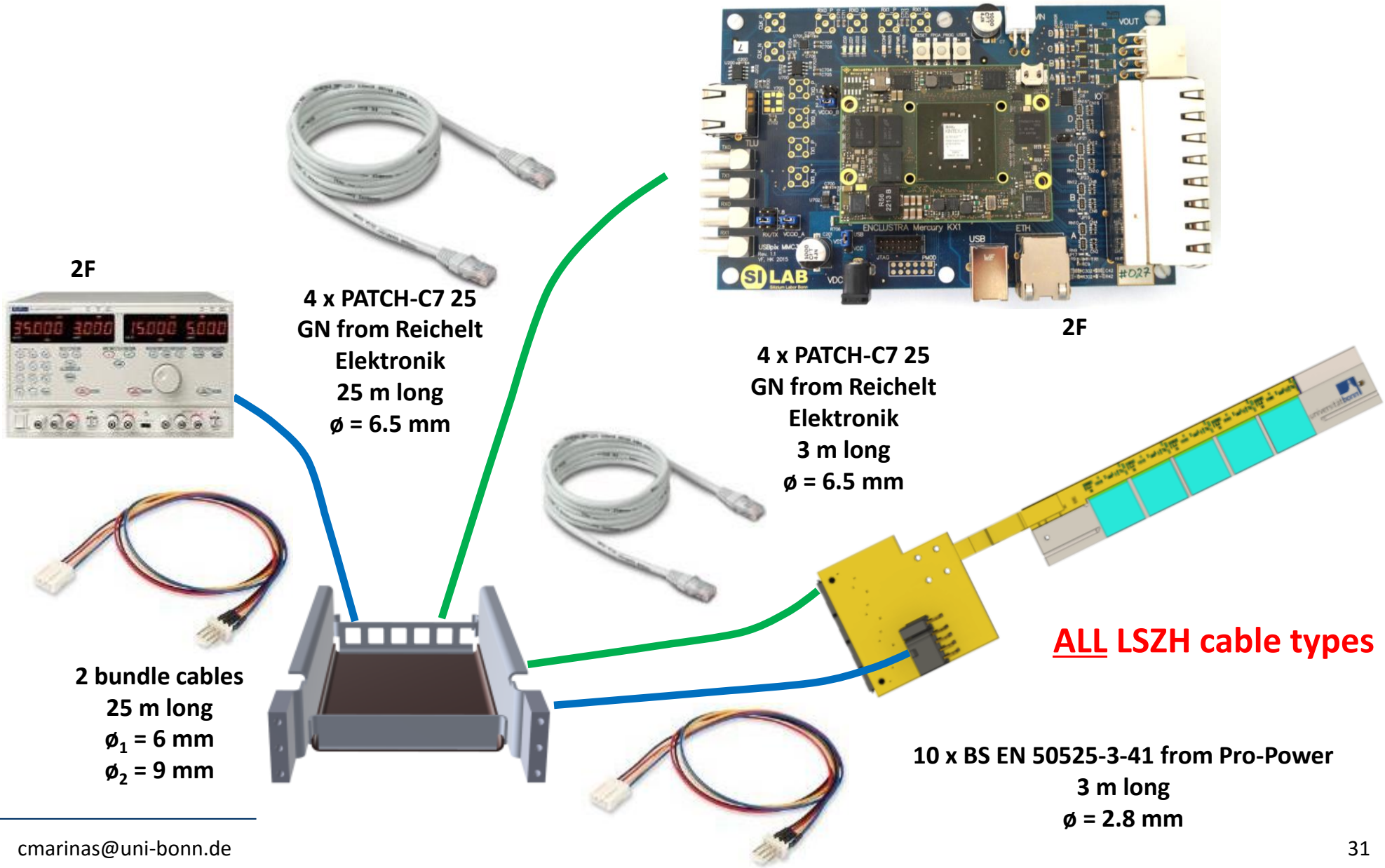
FANGS Stave Online Monitor



FANGS Stave Online Monitor



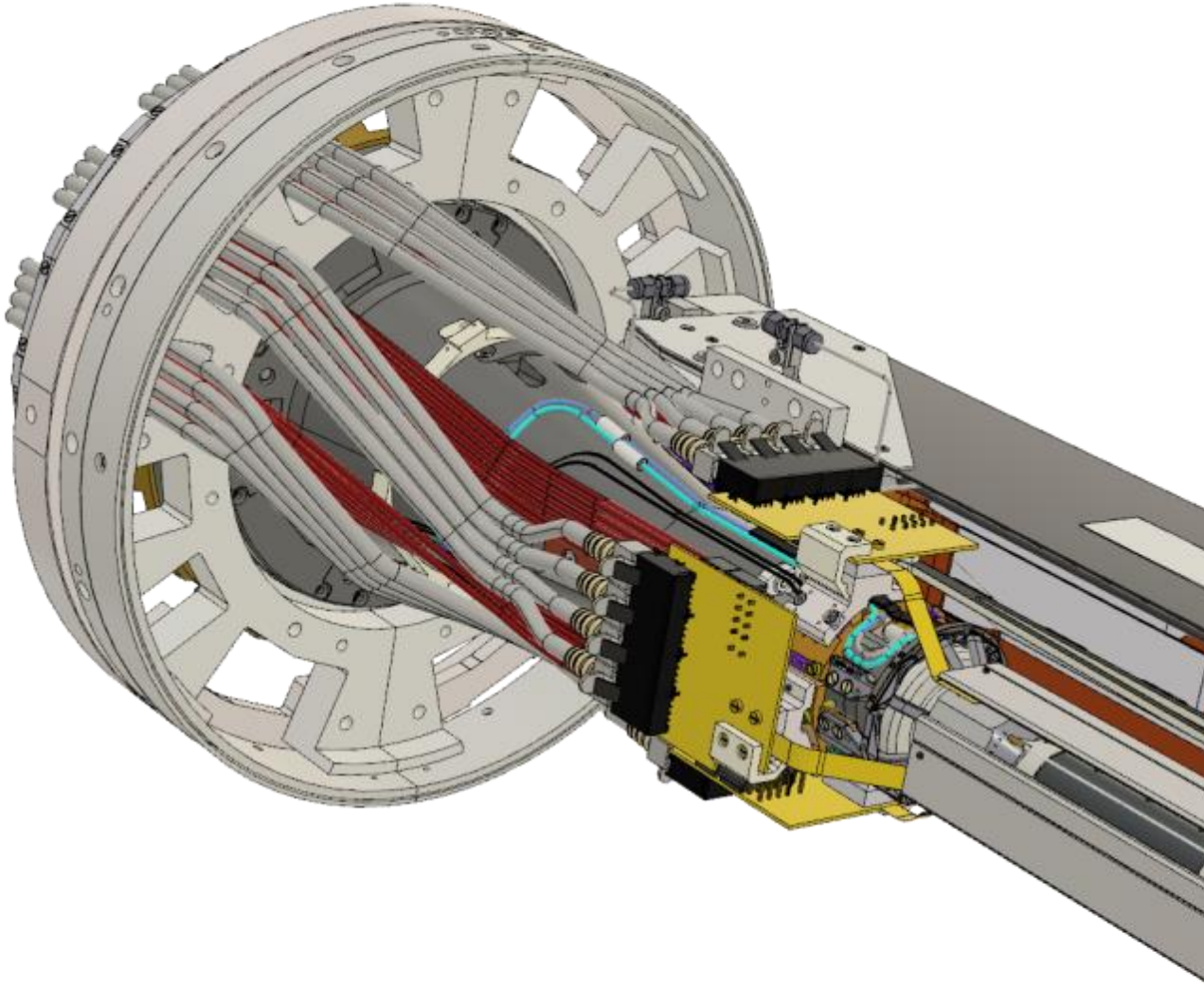
Cable Description Per Stave



Cable Routing

4 x PATCH-C7 25 GN from Reichelt Elektronik
ø = 6.5 mm
Minimum bending radius = 45.5 mm

10 x BS EN 50525-3-41 from Pro-Power
ø = 2.8 mm
Minimum bending radius = 11.2 mm



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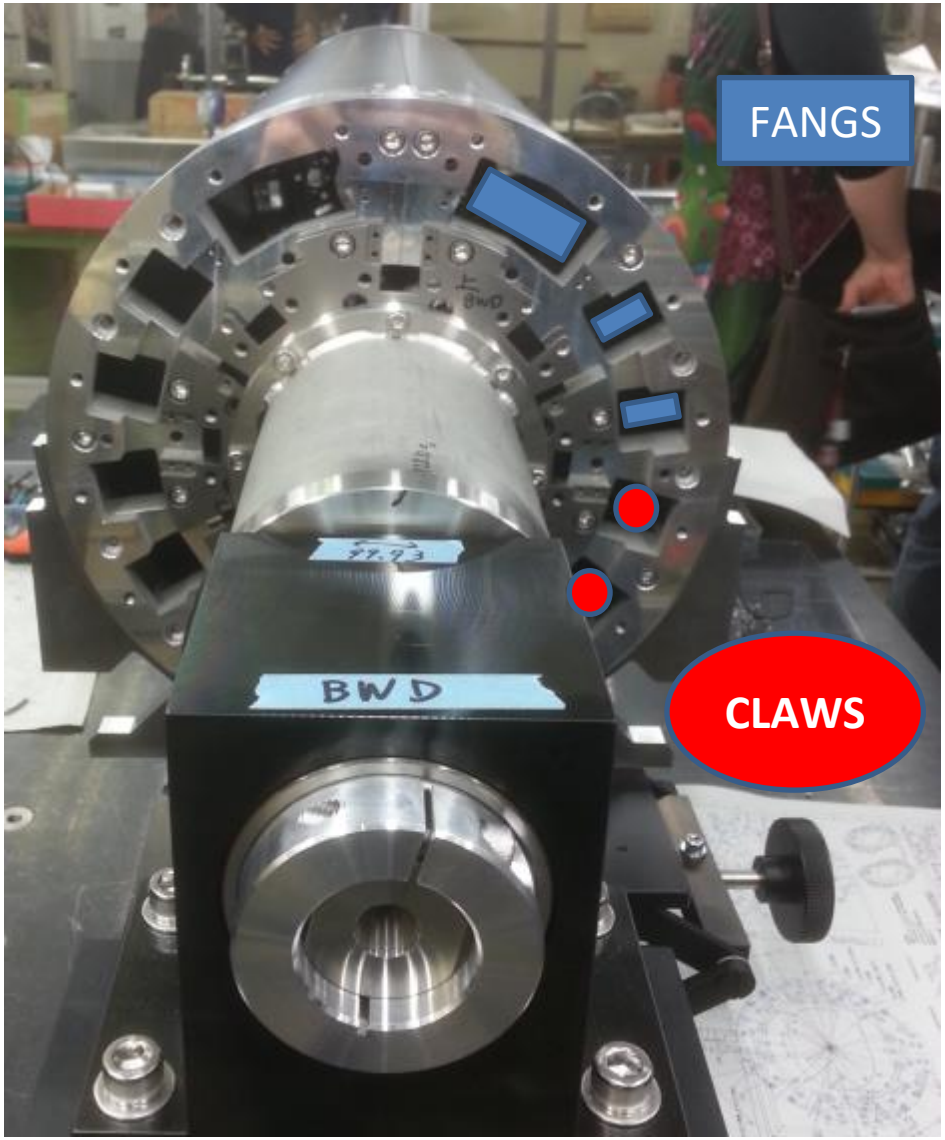
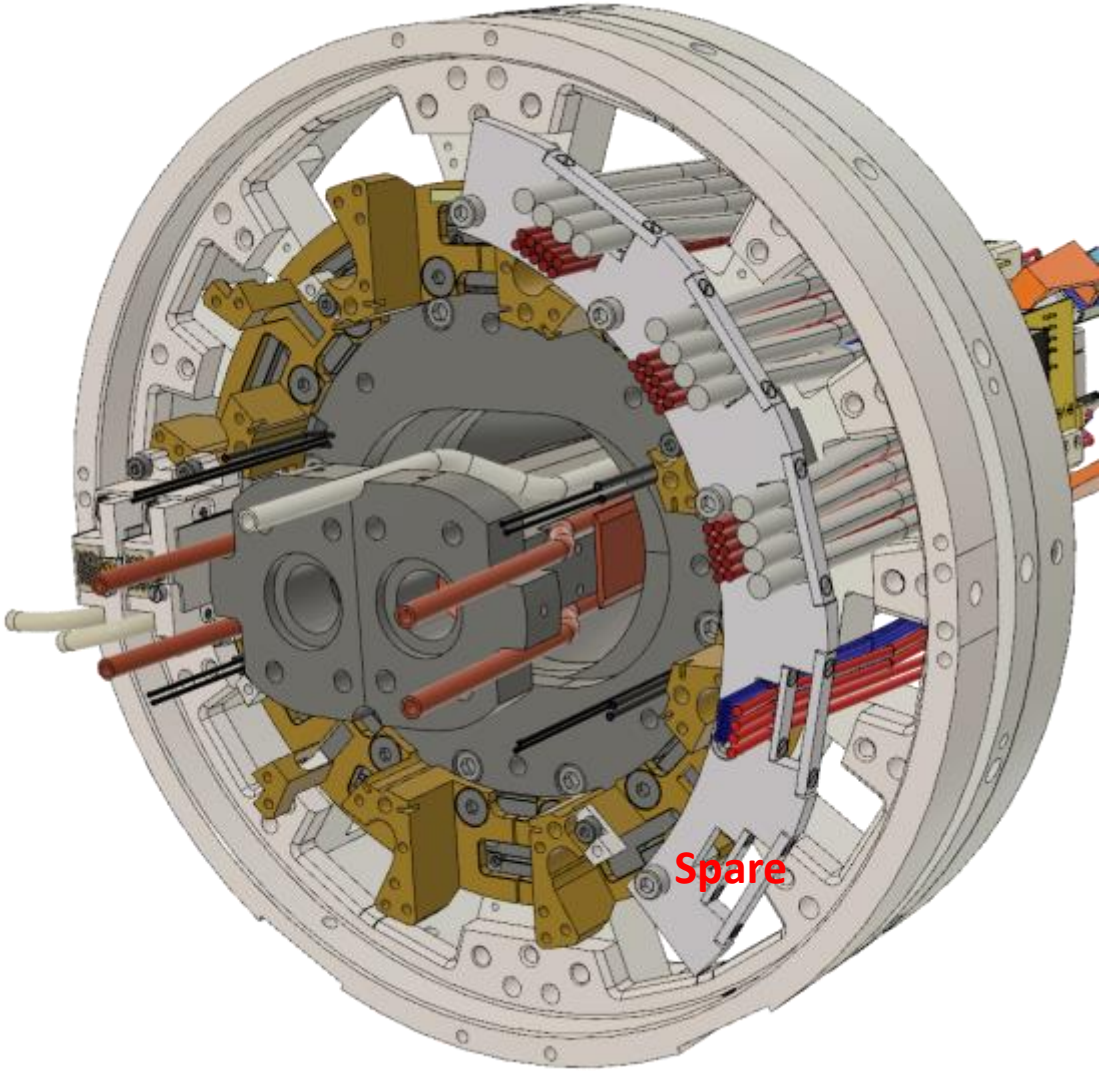
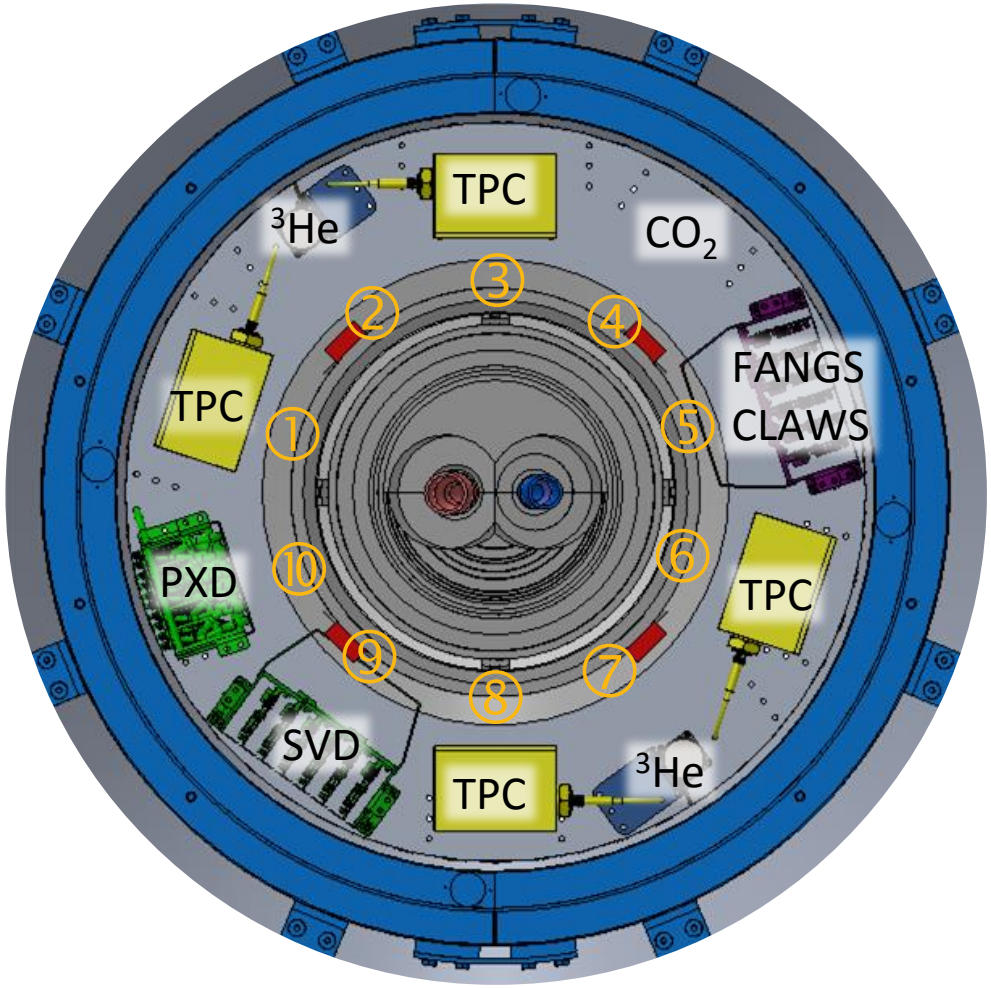


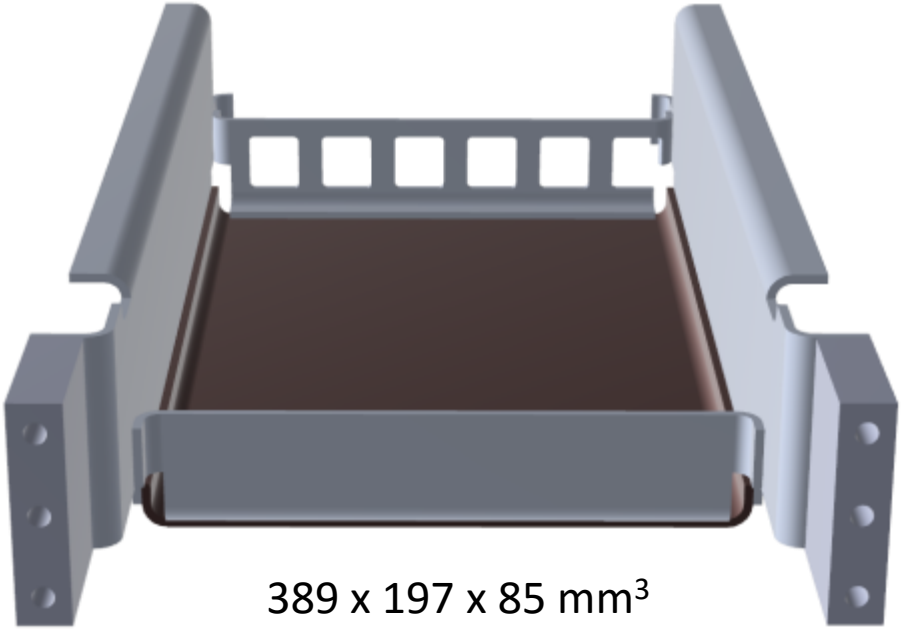


FANGS Dock

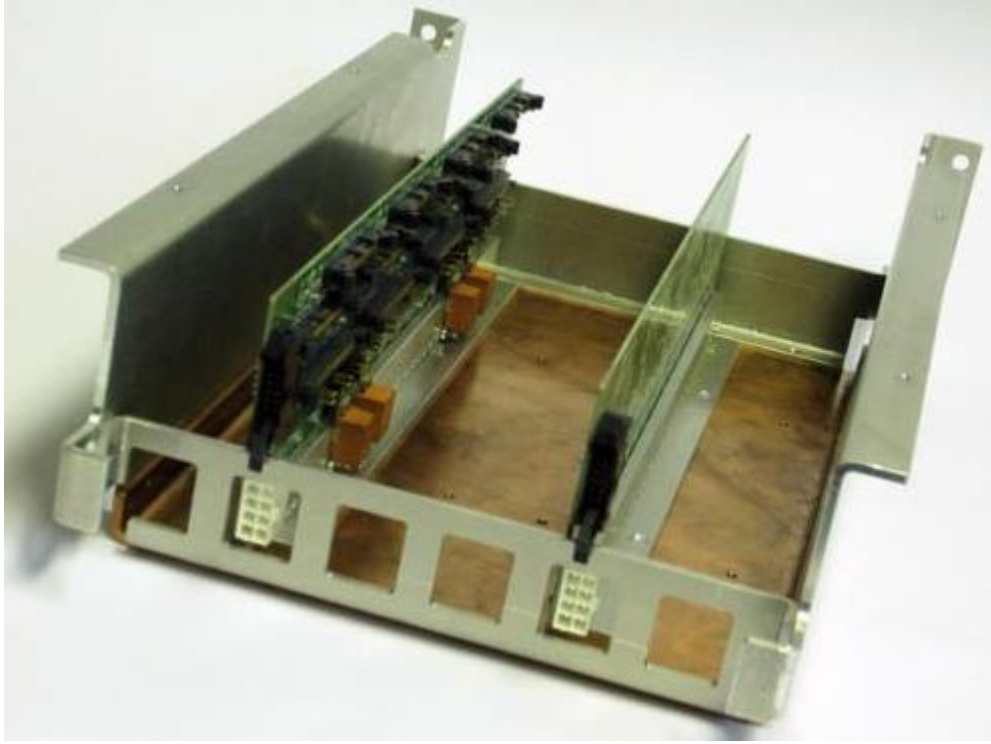
Backward

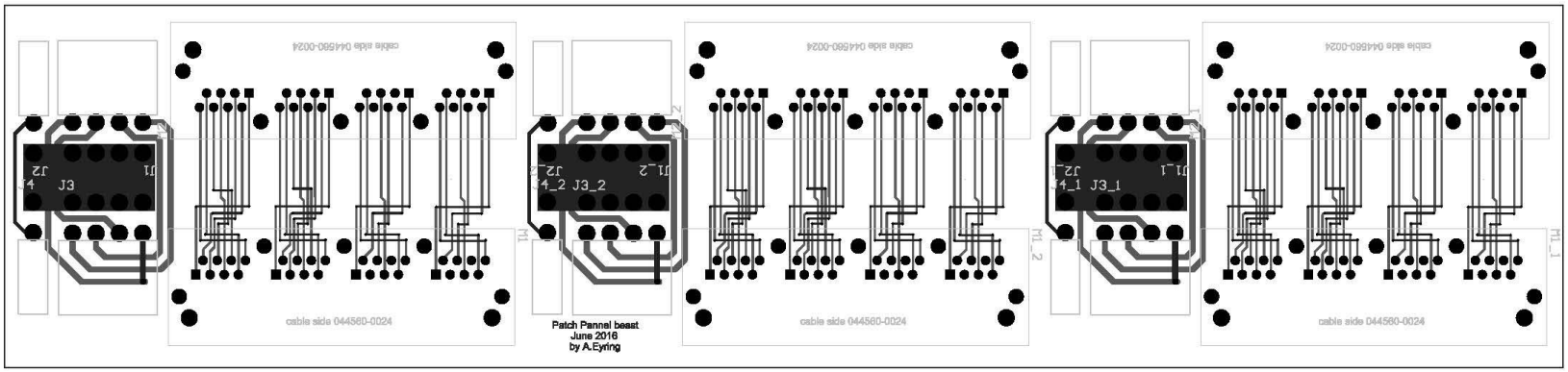


SVD Dock and FANGS Patch Panel



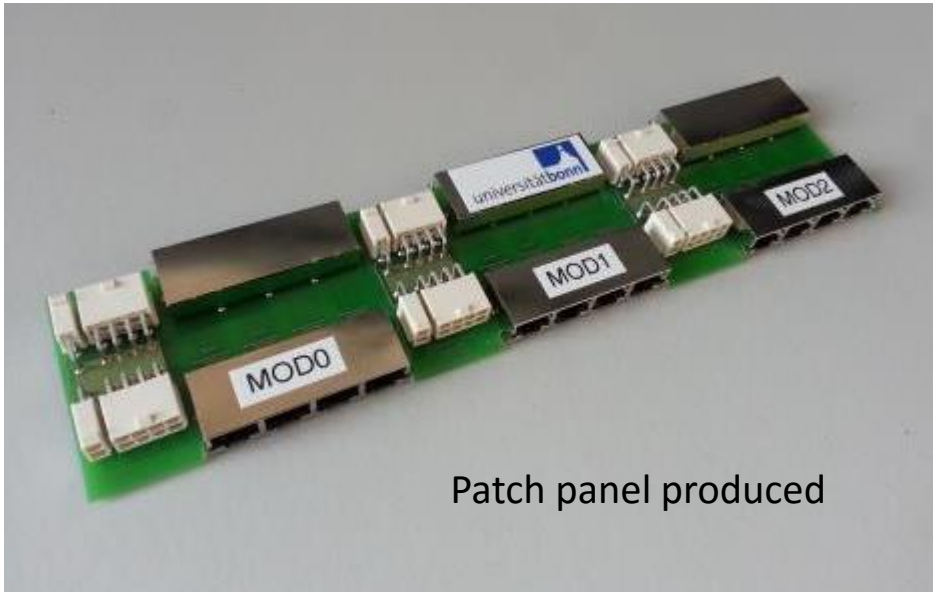
389 x 197 x 85 mm^3



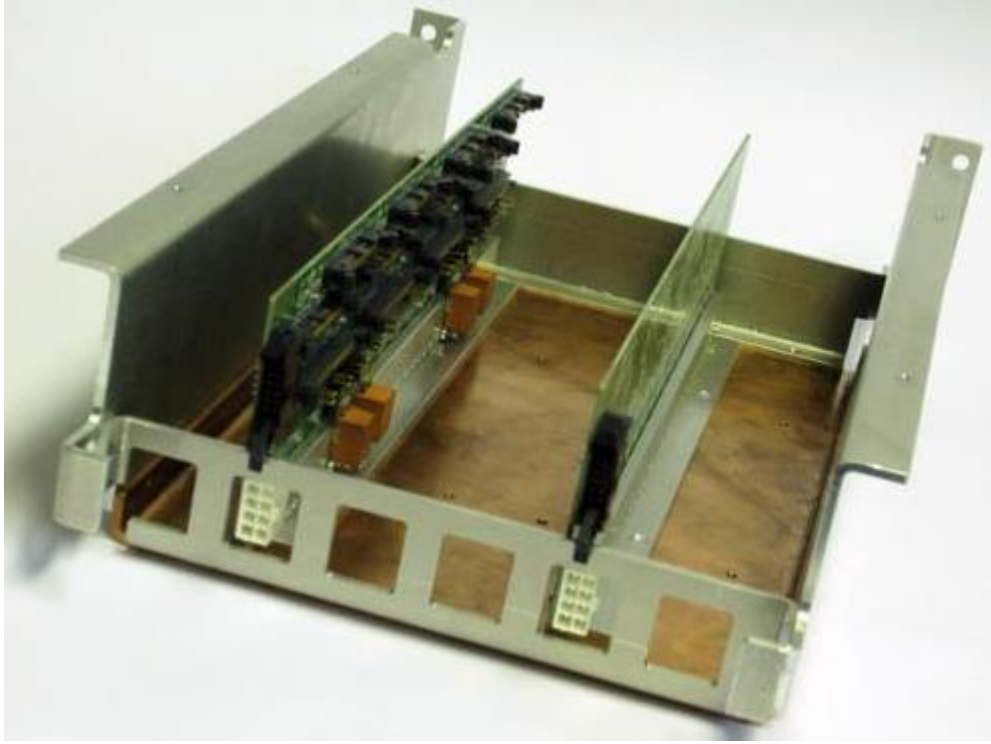


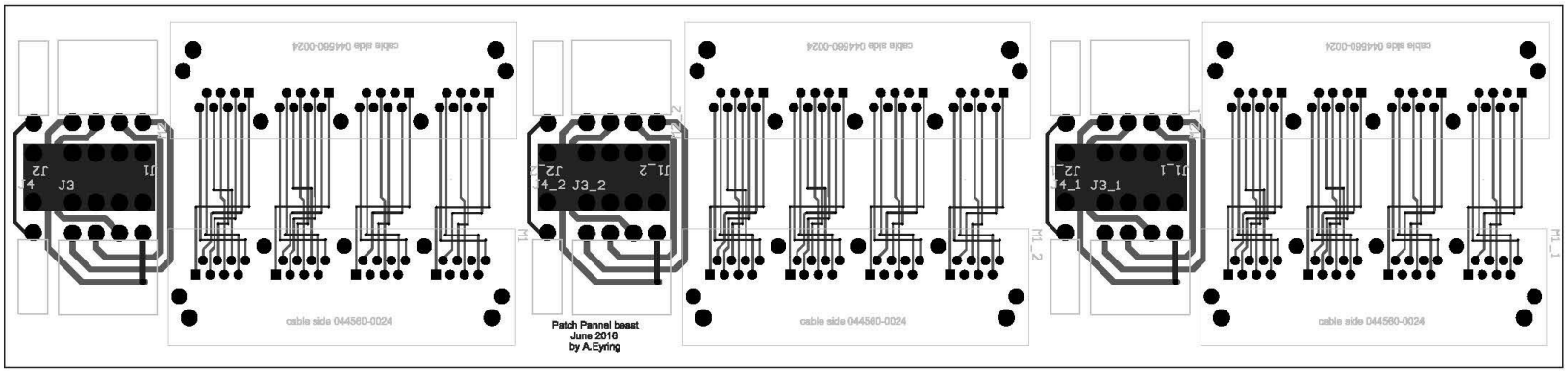
280 x 65 x 25 mm^3

SVD Dock and FANGS Patch Panel



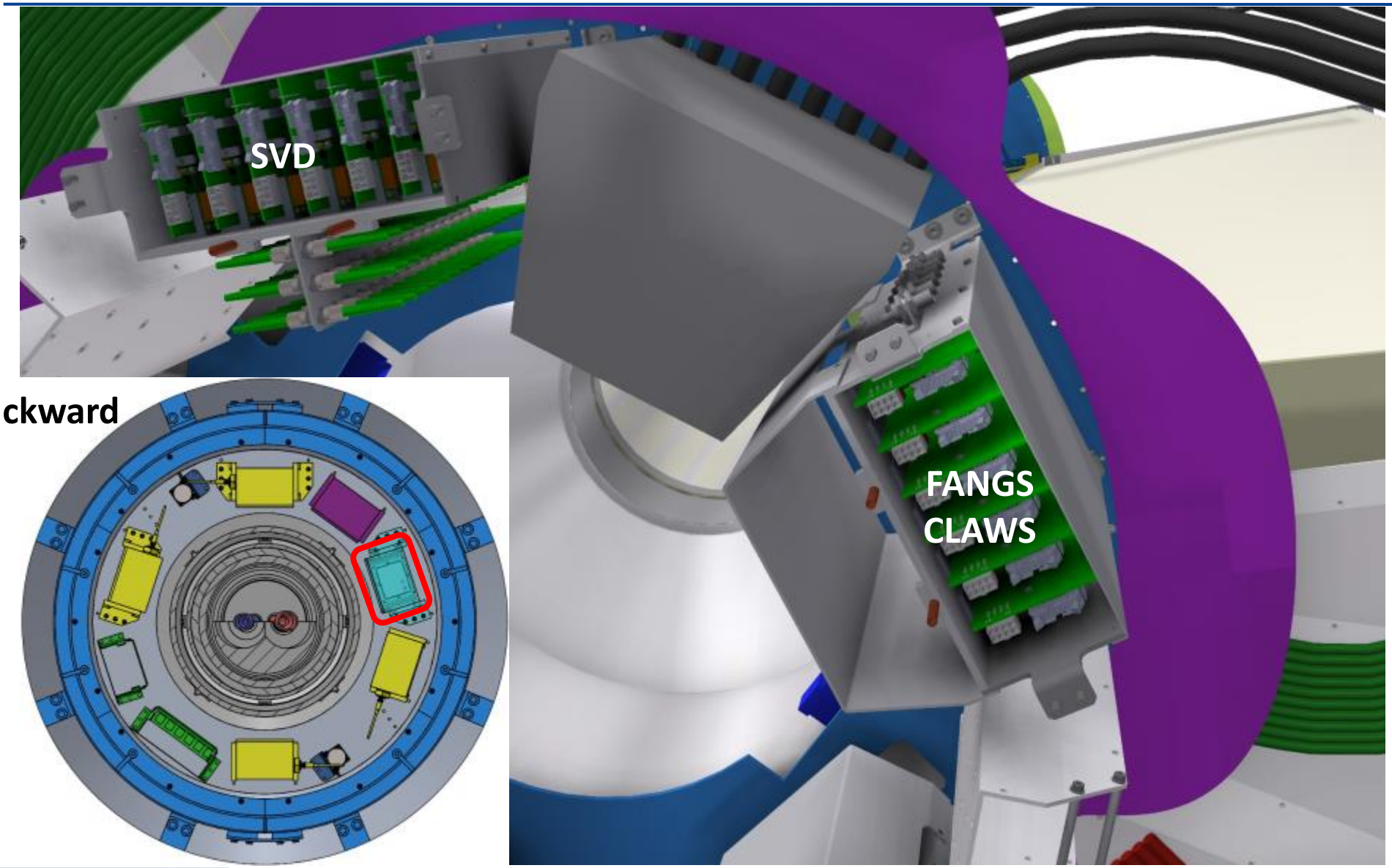
Patch panel produced



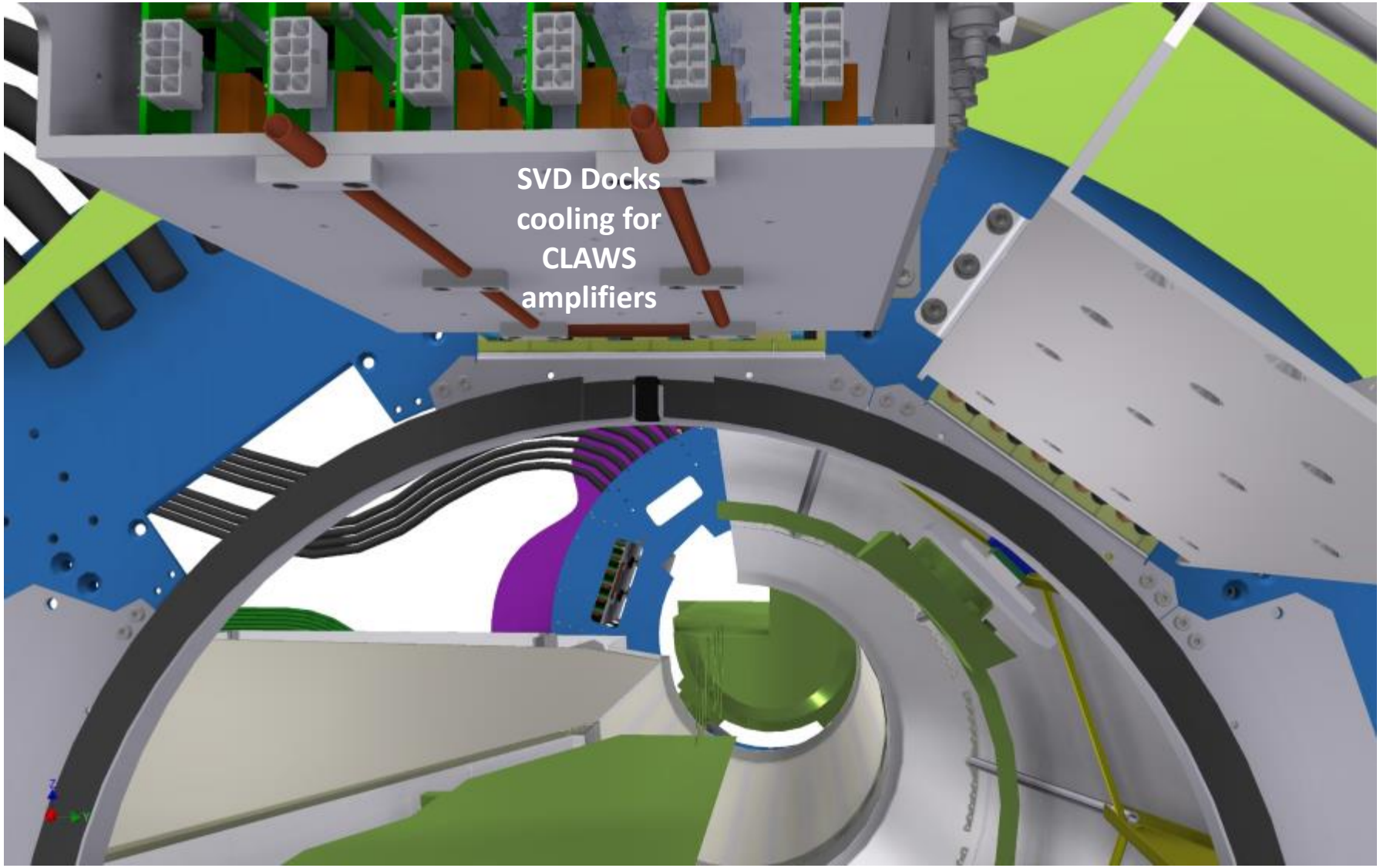


280 x 65 x 25 mm^3

FANGS-CLAWS Dock

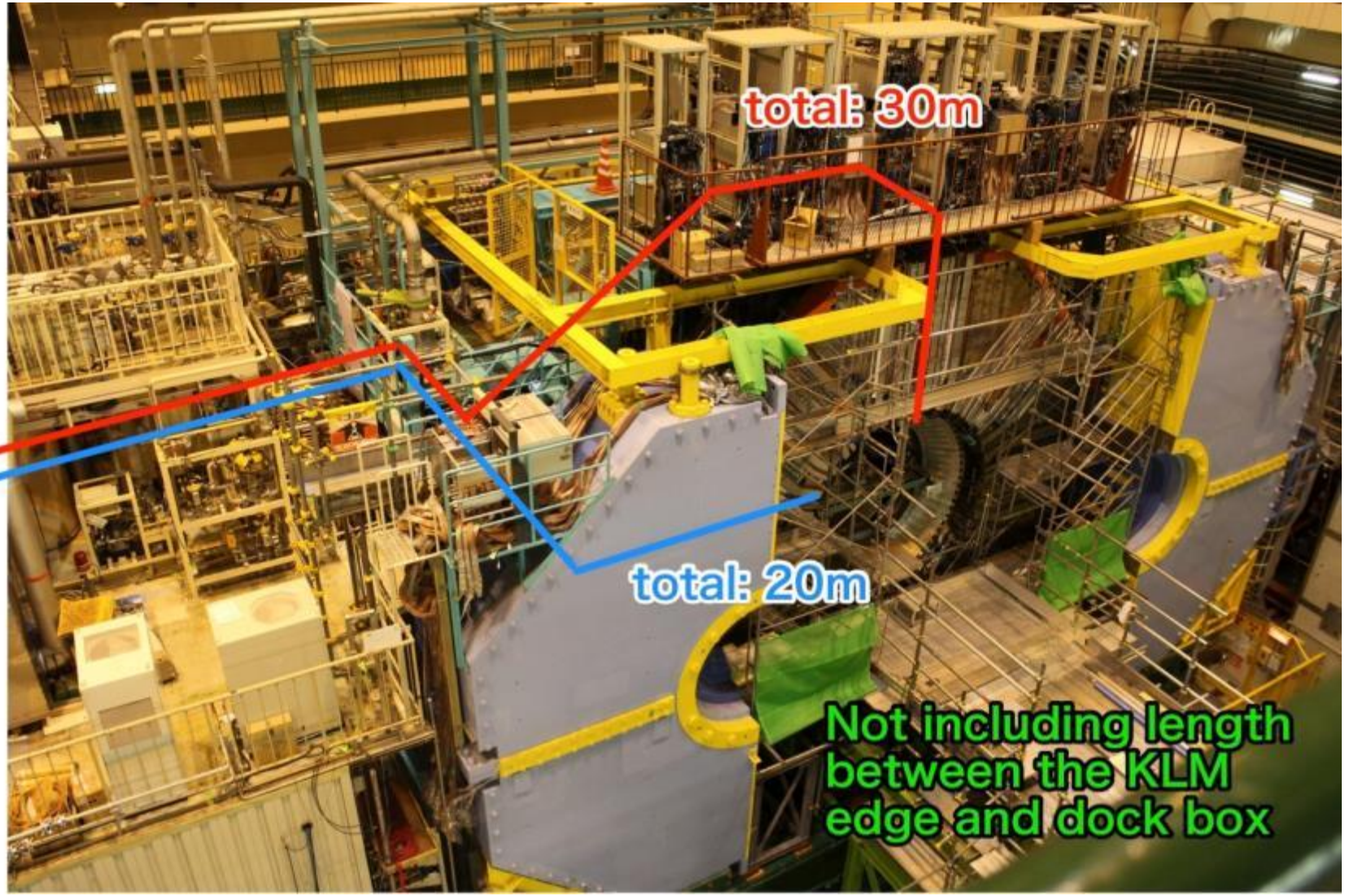


SVD Docks



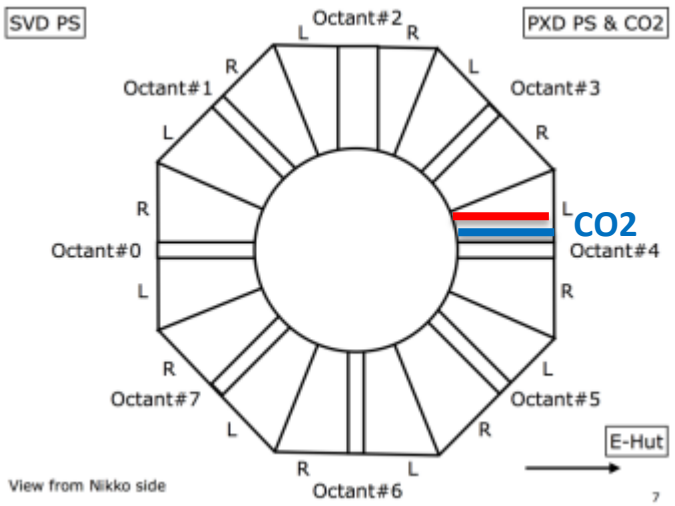
Cable Routing to 2F

Horizontal route in Backwards

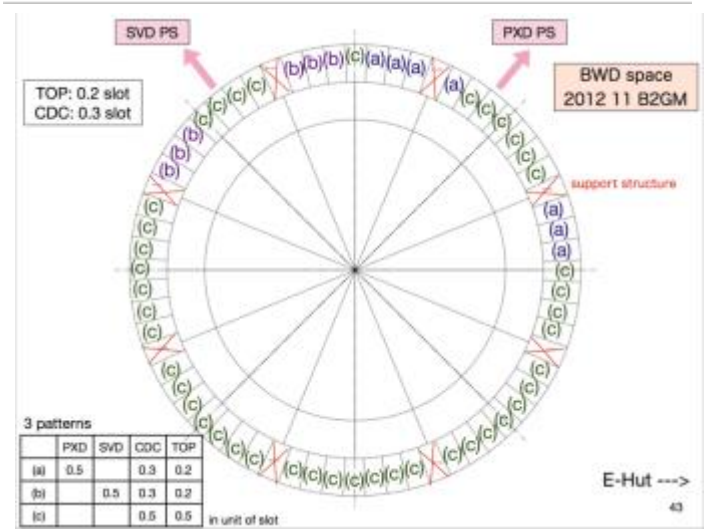


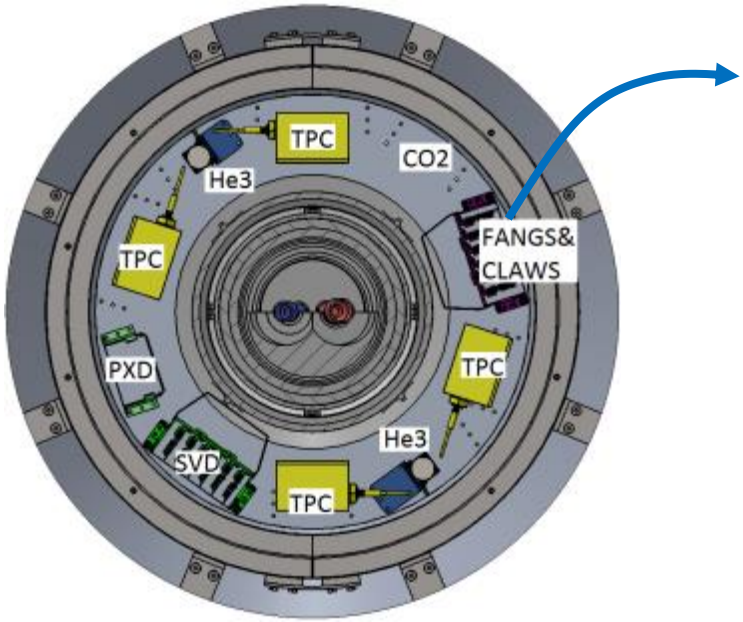
ECL and KLM Slots

KLM

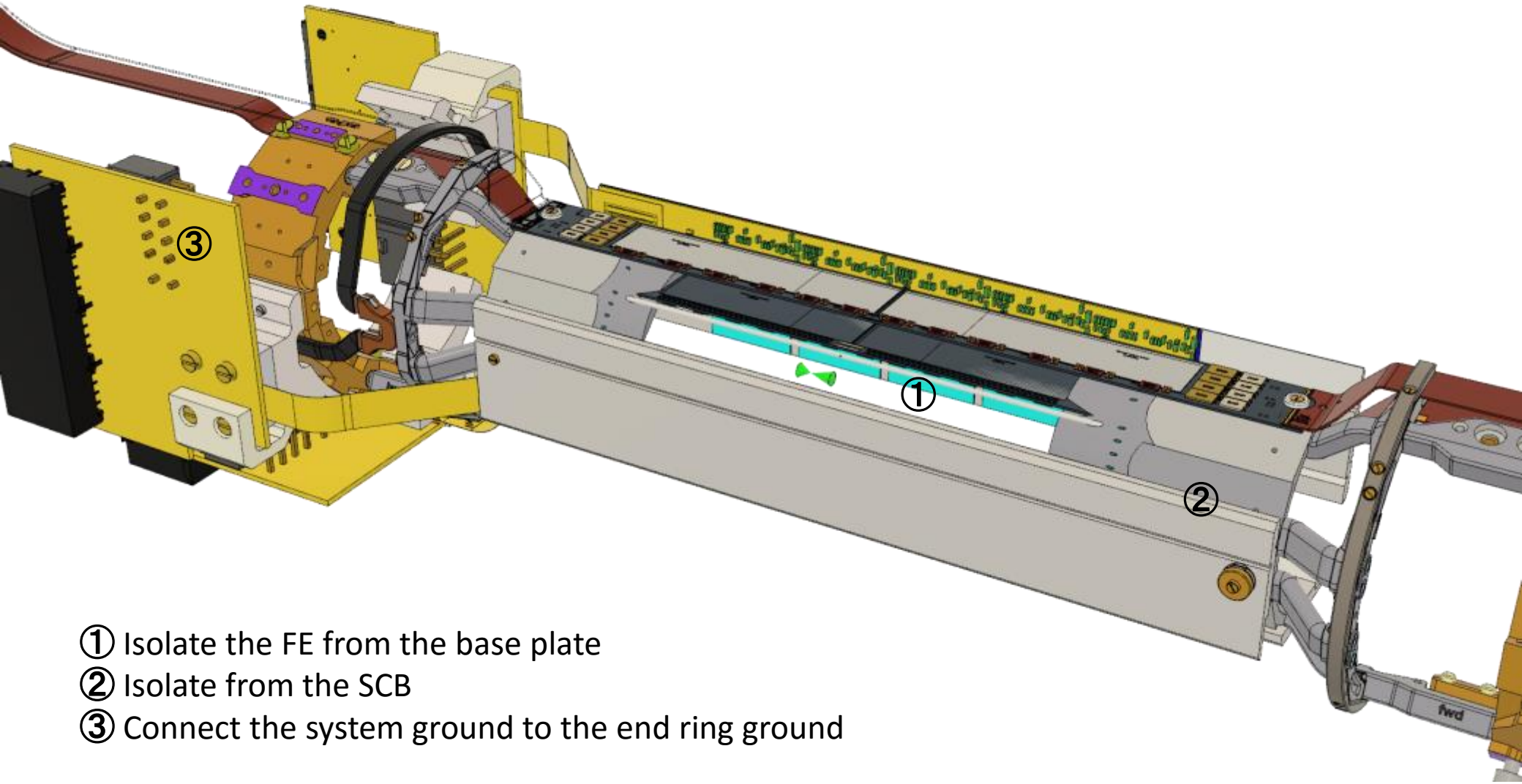


ECL



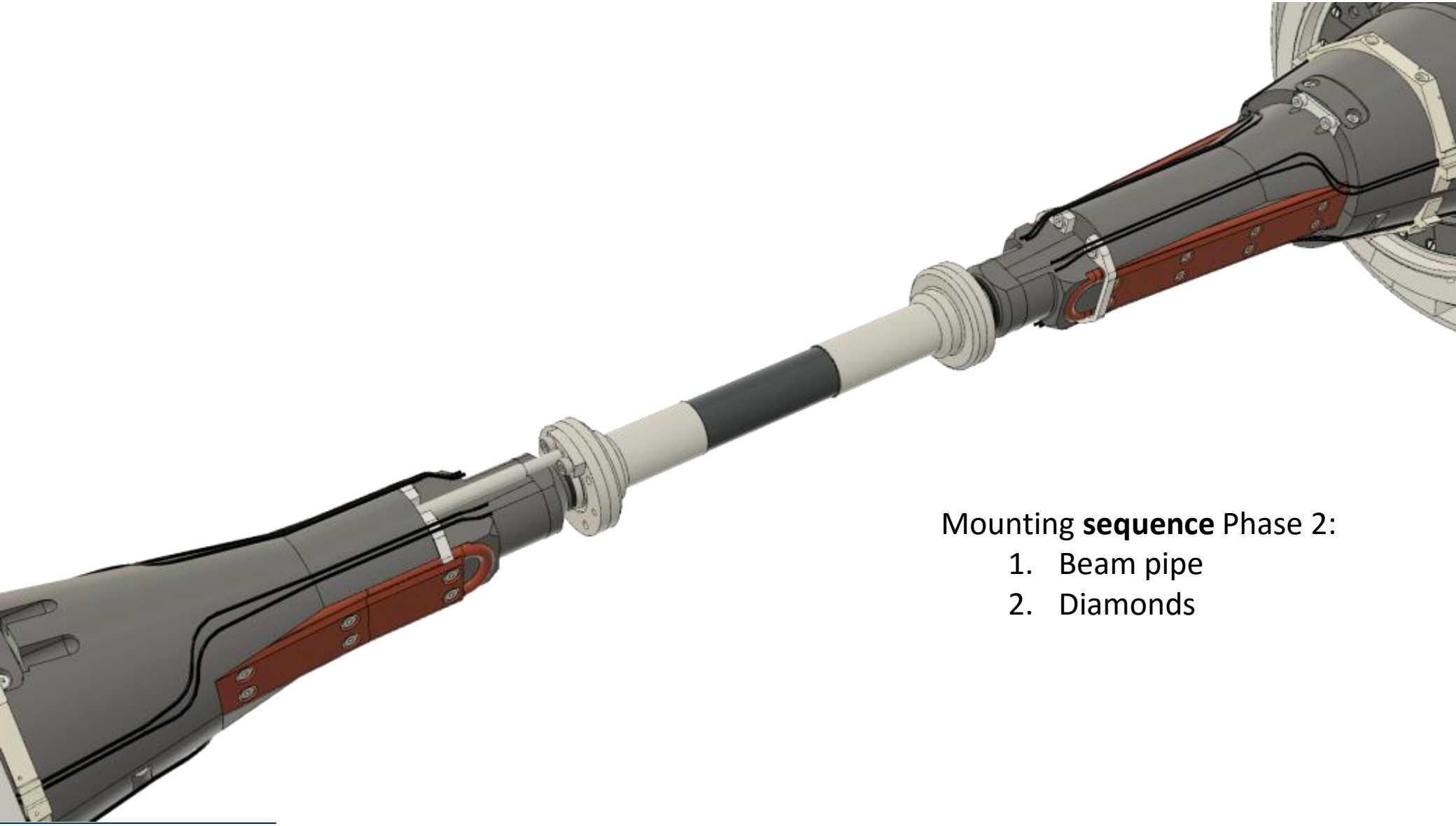


Grounding



① Isolate the FE from the base plate
② Isolate from the SCB
③ Connect the system ground to the end ring ground

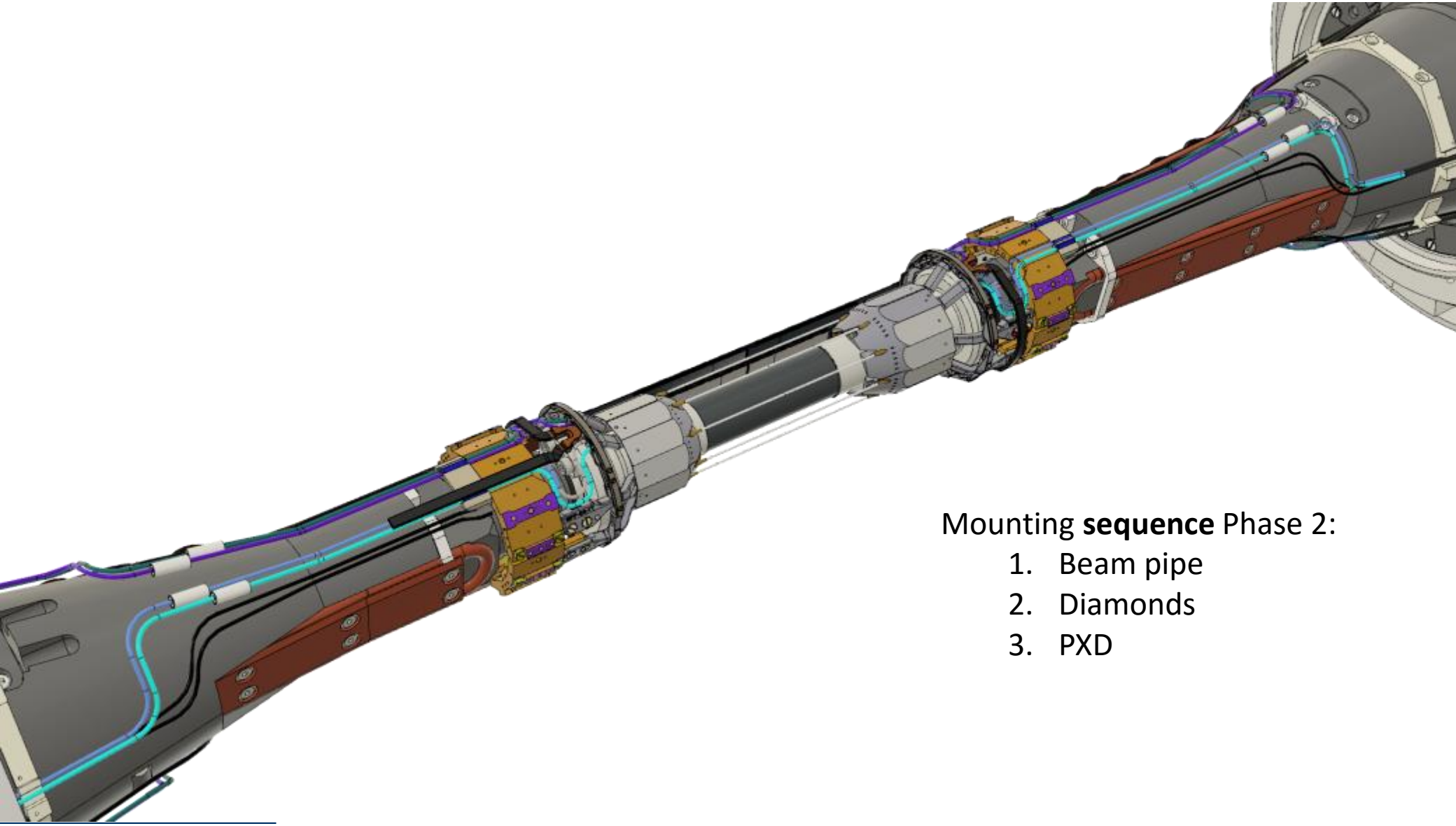
System Integration



Mounting **sequence** Phase 2:

1. Beam pipe
2. Diamonds

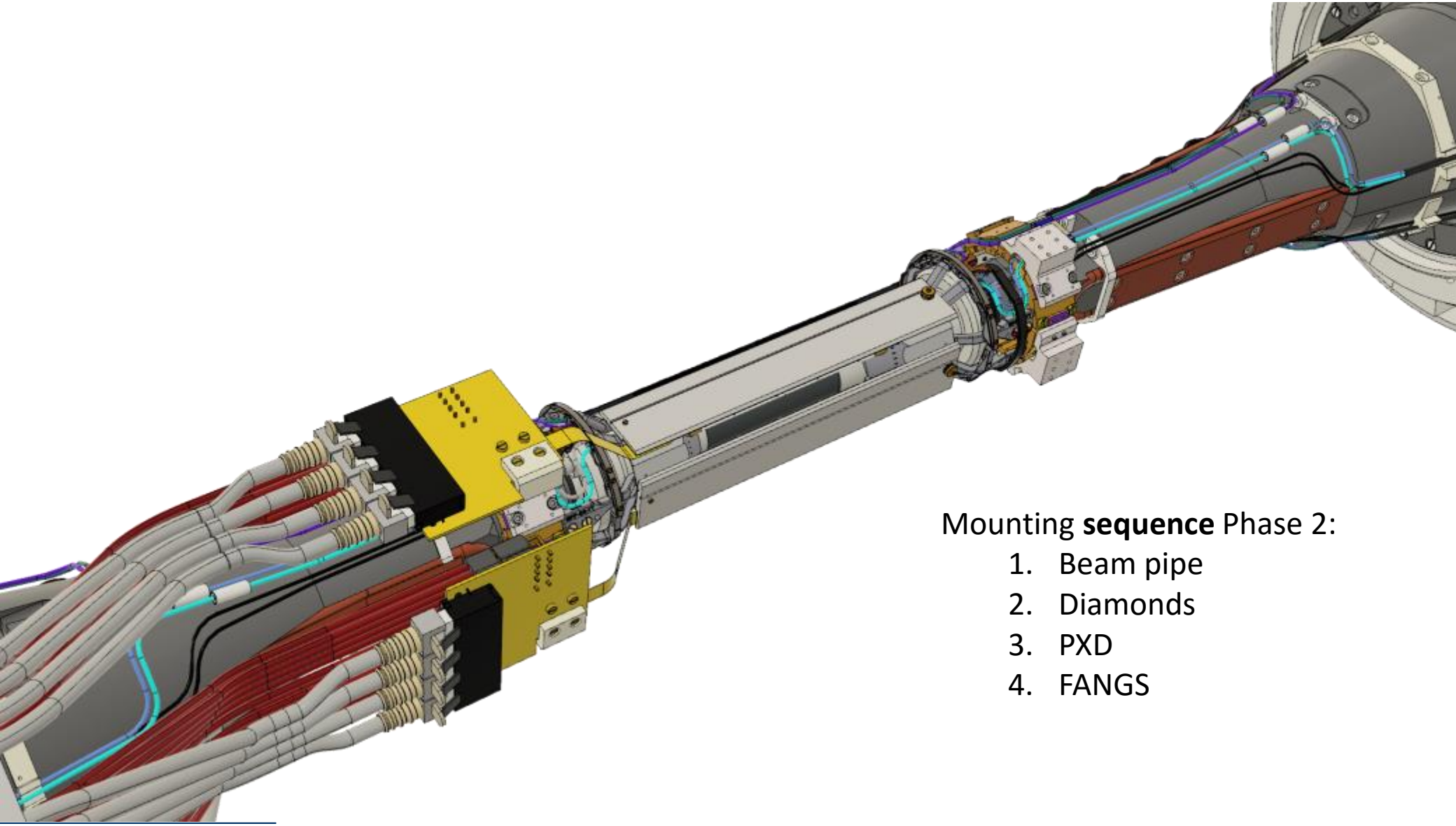
System Integration



Mounting **sequence** Phase 2:

1. Beam pipe
2. Diamonds
3. PXD

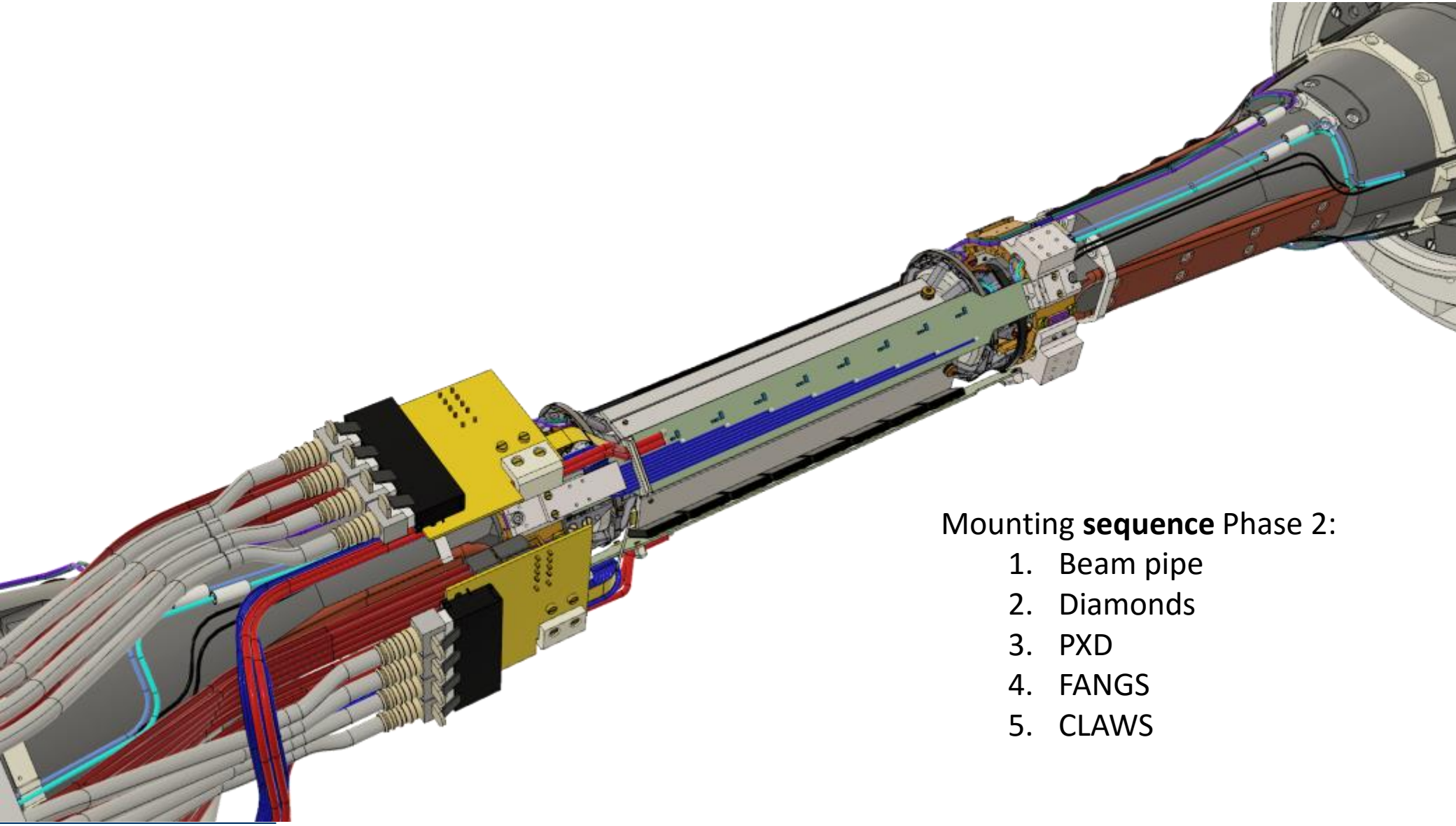
System Integration



Mounting **sequence** Phase 2:

1. Beam pipe
2. Diamonds
3. PXD
4. FANGS

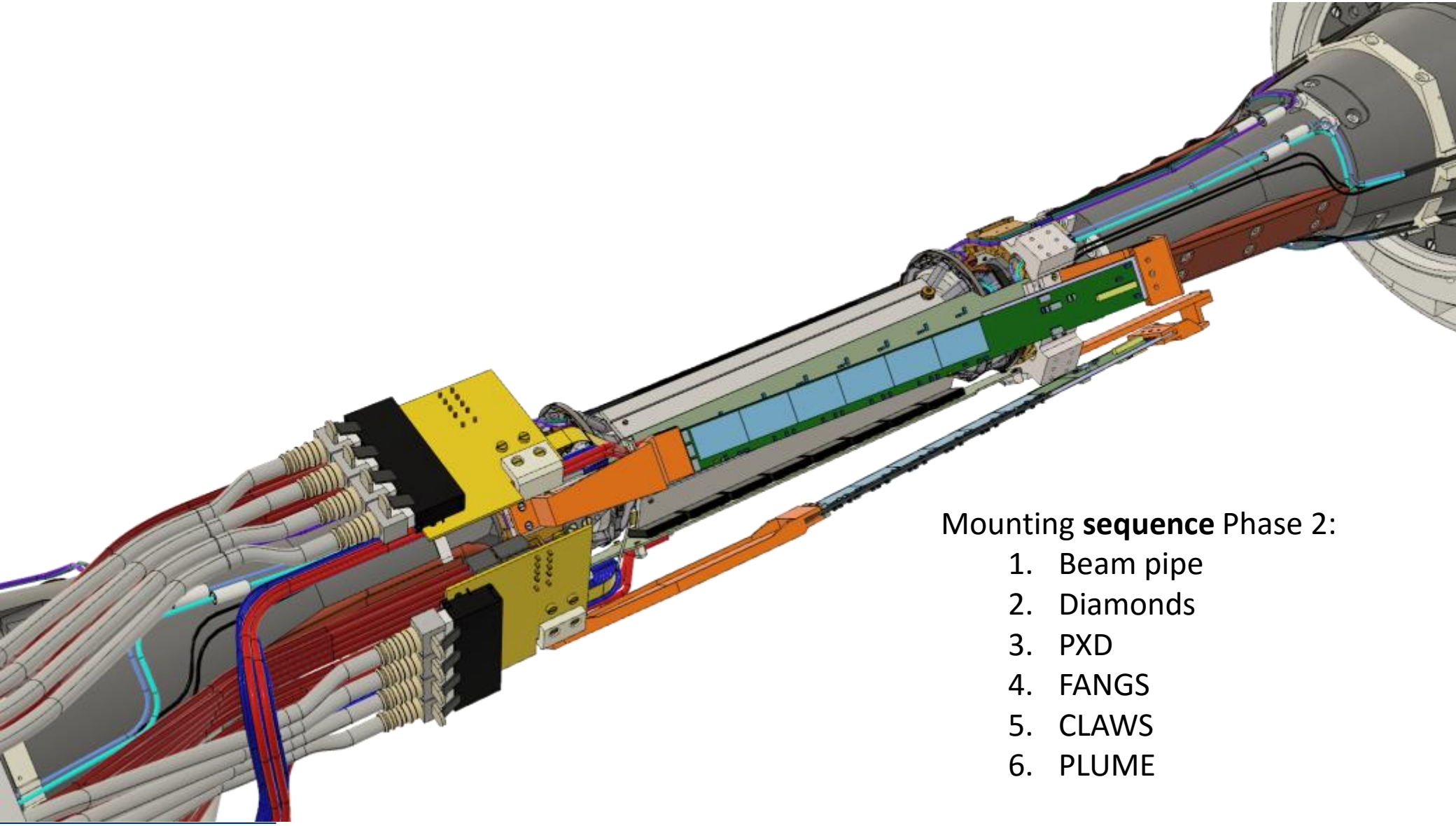
System Integration



Mounting **sequence** Phase 2:

1. Beam pipe
2. Diamonds
3. PXD
4. FANGS
5. CLAWS

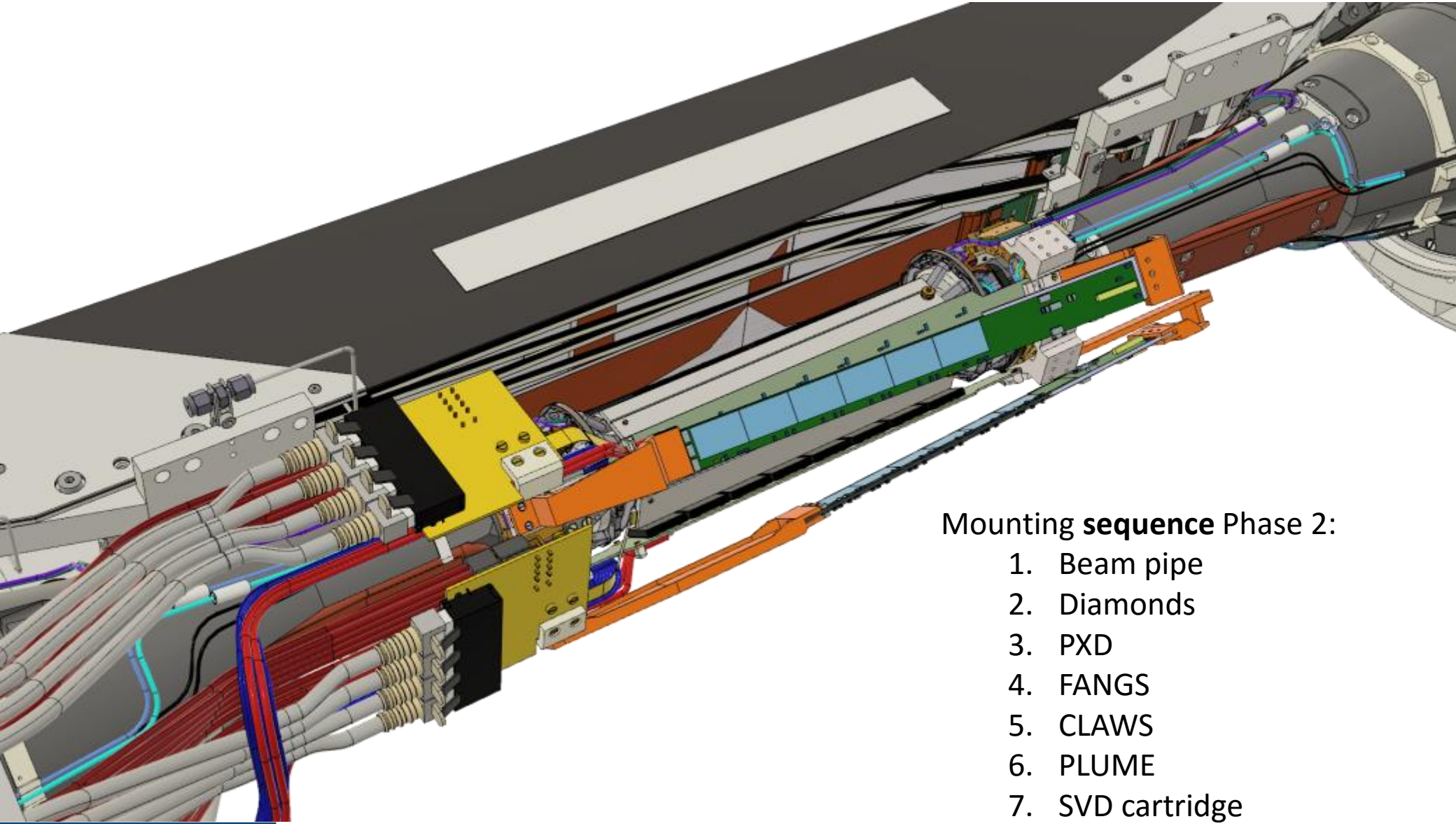
System Integration



Mounting **sequence** Phase 2:

1. Beam pipe
2. Diamonds
3. PXD
4. FANGS
5. CLAWS
6. PLUME

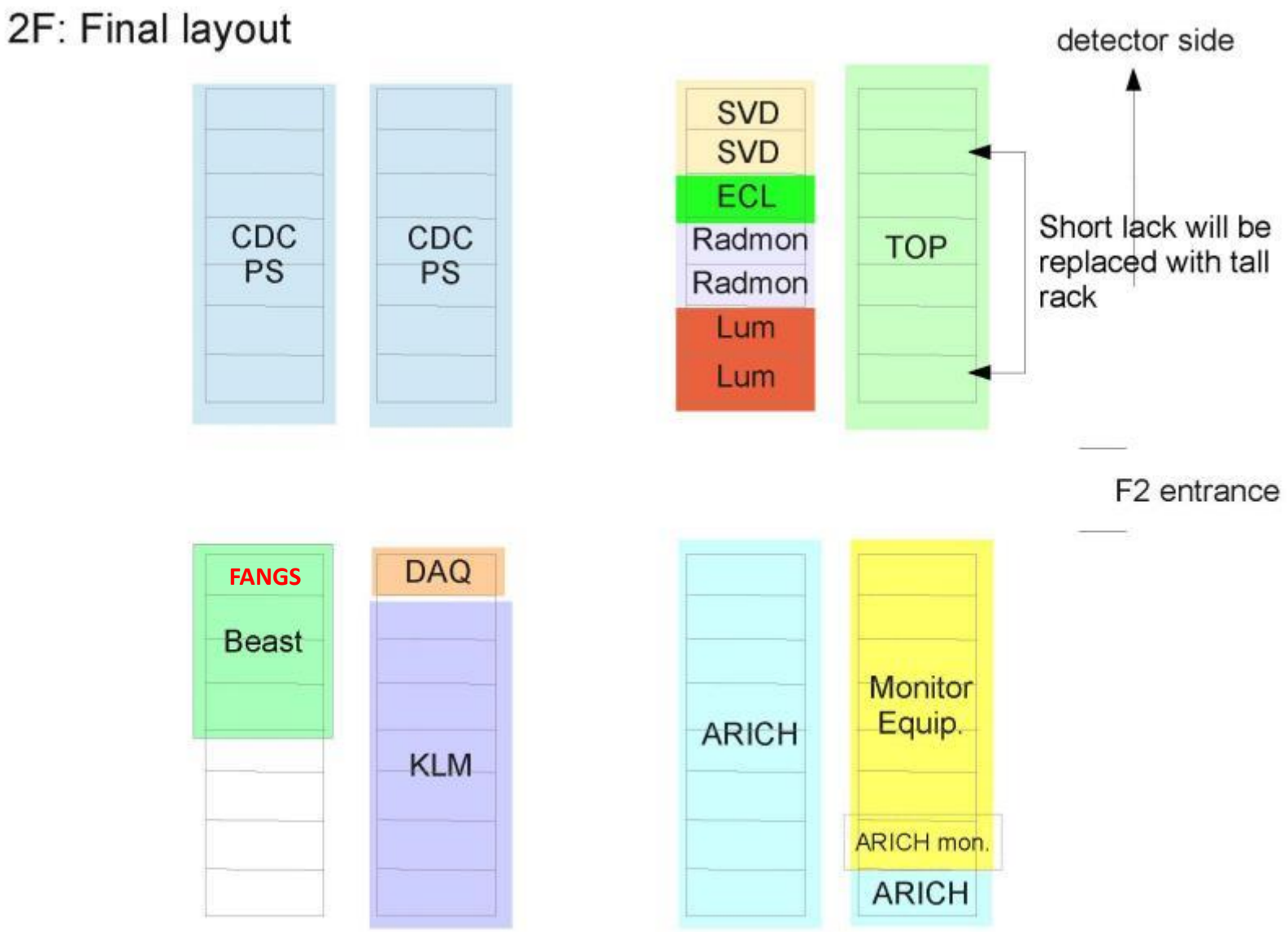
System Integration



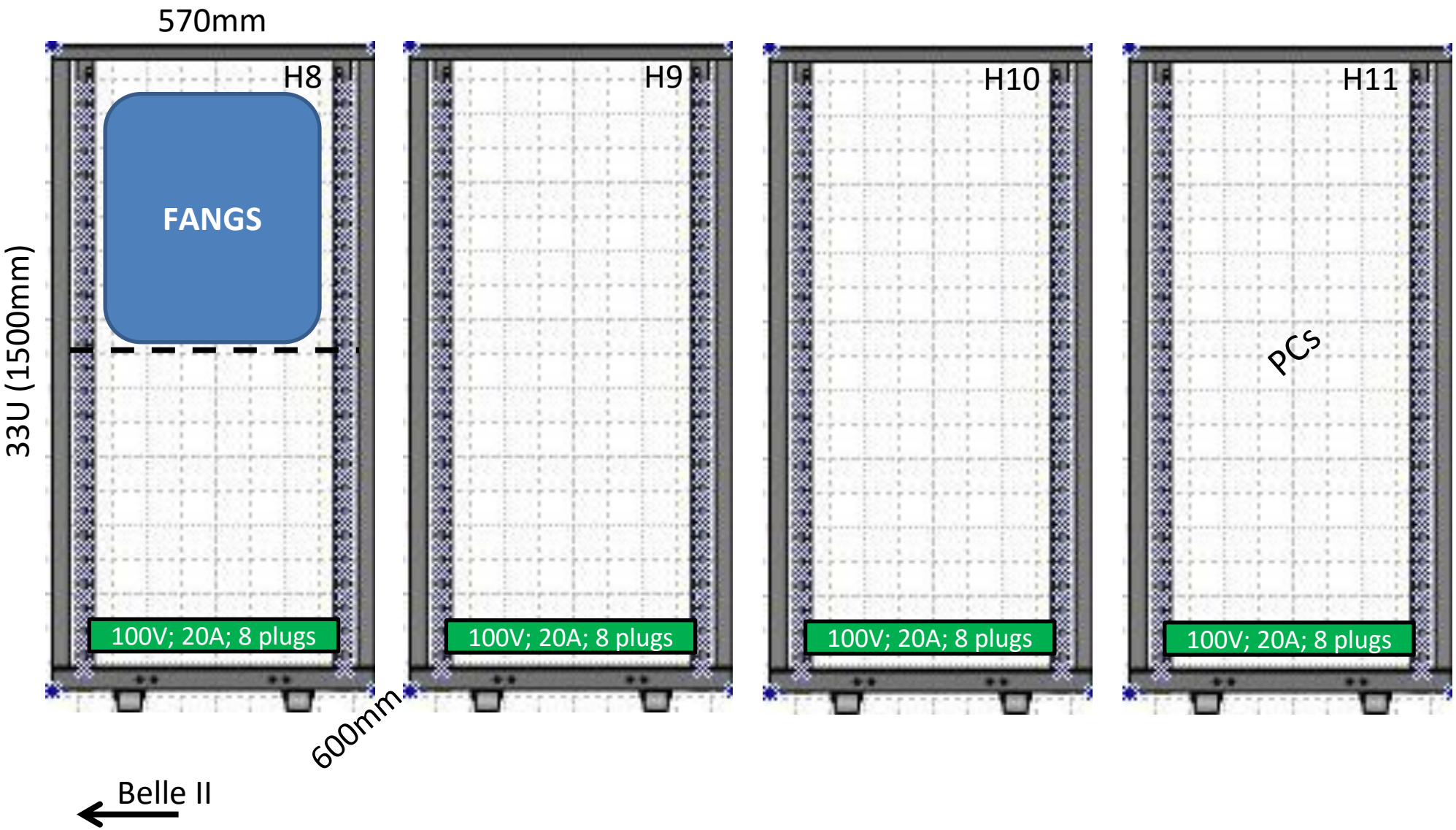
Mounting **sequence** Phase 2:

1. Beam pipe
2. Diamonds
3. PXD
4. FANGS
5. CLAWS
6. PLUME
7. SVD cartridge

Rack Space


2F: Final layout
detector side
CDC PS
CDC PS
SVD
SVD
ECL
Radmon
Radmon
Lum
Lum
TOP
Short lack will be replaced with tall rack
F2 entrance
FANGS
Beast
DAQ
KLM
ARICH
Monitor Equip.
ARICH mon.
ARICH

Rack Space

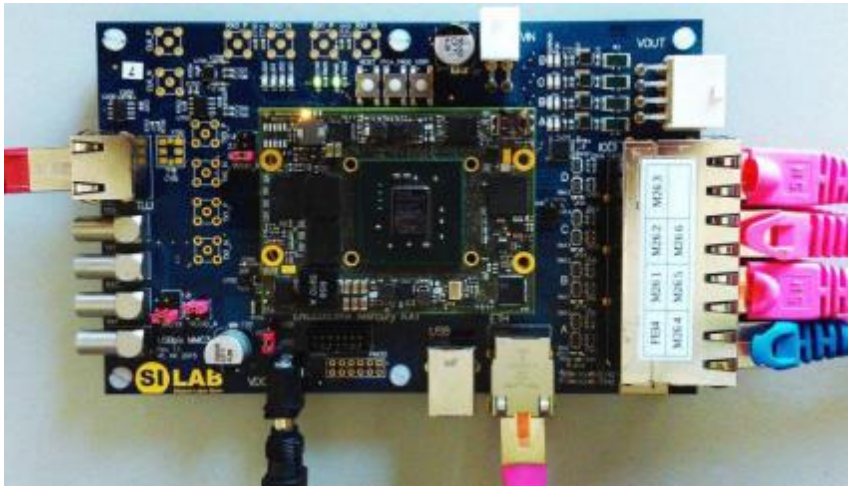

570mm
H8
FANGS
H9
H10
H11
PCs
33U (1500mm)
100V; 20A; 8 plugs
100V; 20A; 8 plugs
100V; 20A; 8 plugs
100V; 20A; 8 plugs
600mm
Belle II

Rack Space

230 x 110 x 420 mm^3
220 V, 50/60 Hz
1 unit

280 x 180 x 300 mm^3
220 V, 50/60 Hz
3 units

XX x XX x XX mm^3
220 V



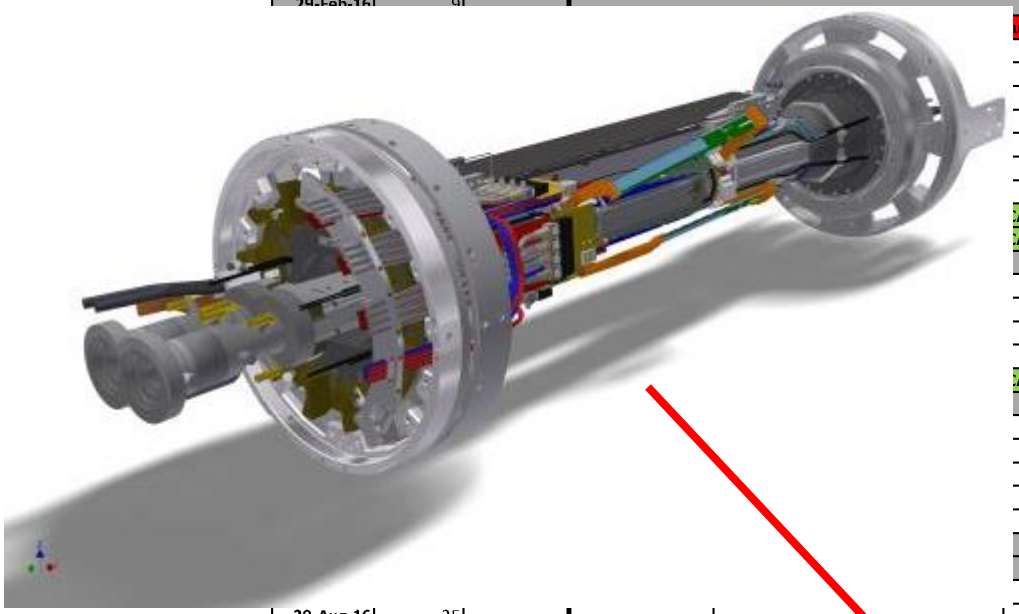
100 x 170 x 40 mm^3
5 V
3 units

Schedule 2016

DESY Testbeam Schedule 2016 - Version 8 - 27/04/2016

Rolf Diener, Norbert Meyners, Marcel Stanitzki - DESY Test Beam Coordinators

	Week		TB21		TB22		TB24/1		TB24	
			DATURA	none	DURANTA	none	Telescope in PCMAG	PCMAG	none	
4-Jan-16	1		Shutdown							
11-Jan-16	2									
18-Jan-16	3									
25-Jan-16	4									
1-Feb-16	5									
8-Feb-16	6									
15-Feb-16	7									
22-Feb-16	8									
29-Feb-16	9									
					up		Startup		Startup	
							Belle-II			
					ALICE-AHCAL				SiPM	
					ALICE-AHCAL				SiPM	
									CMS-Pixel-Phase1	
					ALICE-AHCAL					
29-Aug-16	35								CBM-TRD	
5-Sep-16	36								CBM-TRD	
12-Sep-16	37									
19-Sep-16	38									
26-Sep-16	39									
3-Oct-16	40									
10-Oct-16	41								PANDA-DIRC	
17-Oct-16	42		CMS-Phase2-EPI						PANDA-DIRC	
24-Oct-16	43		CMS-Phase2-EPI		HEP for Teachers				PANDA-DIRC	
31-Oct-16	44									
7-Nov-16	45				Mu3e					
14-Nov-16	46									
21-Nov-16	47									
28-Nov-16	48									
5-Dec-16	49									
12-Dec-16	50						Belle-II			
19-Dec-16	51	Beam till 23/12 0800								
26-Dec-16	52		Shutdown							



Phase 2 Dry Integration

Announced

Conclusion

- FANGS prove of principle demonstrated and design frozen at February B2GM
- 4 staves already available. First one fully tested and operational.
- 1 readout board available. Additional 3 are currently being tested.
- 2 sets of data and power cables available.
- Online monitor available. Hit maps, hit rates, trigger rates, energy distribution
- Steady progress. Ready by November for integration

NEXT:

- Radiation hardness flex electrical components (end of September)
- More realistic environment

universitätbonn

Thank you

cmarinas@uni-bonn.de