DCD4.1/DCD4.2 Review Analog Performance

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DCD4.x Design Improvements

DCD4.x

- JTAG sampling CLK edge compatible with industry standard
- option to increase DCD digital LVDS driver current from 1.3mA to 1.8mA (**LVDS boost**) → *see talk by Harrison Schreeck*
- option to increase DCD digital driver reference voltage by 30mV
- changed **TIA gain settings**
- IPDAC current reduced by factor of 2 to improve offset correction granularity
- added **IPSourceMiddle** DAC to cope with upper/lower channels asymmetry

DCD4.1

- added two antenna diodes and dummy structures to improve **transistor matching** in the ADCs

DCD4.2

- added diodes, dummy structures and increased transistor sizes to improve **transistor matching**
- more **complex digital test pattern** for improved delay optimization
- changed ID code

DCD4.x Testing Procedure

- test DCD4.1 and DCD4.2 functionality on Hybrid5 level
- confirm that stable operation is possible with both DCD designs
  - check correct implementation of gains
  - check that ADCs operation can be optimized within specifications
    - INLpp < 8 ADU within +-100 ADC
    - noise < 1.0 ADU
    - no long codes above 6 ADU
    - no bit errors visible in ADC curves
    - gains should be homogeneous among all DCD channels
      - adjust with new IPSourceMiddle DAC

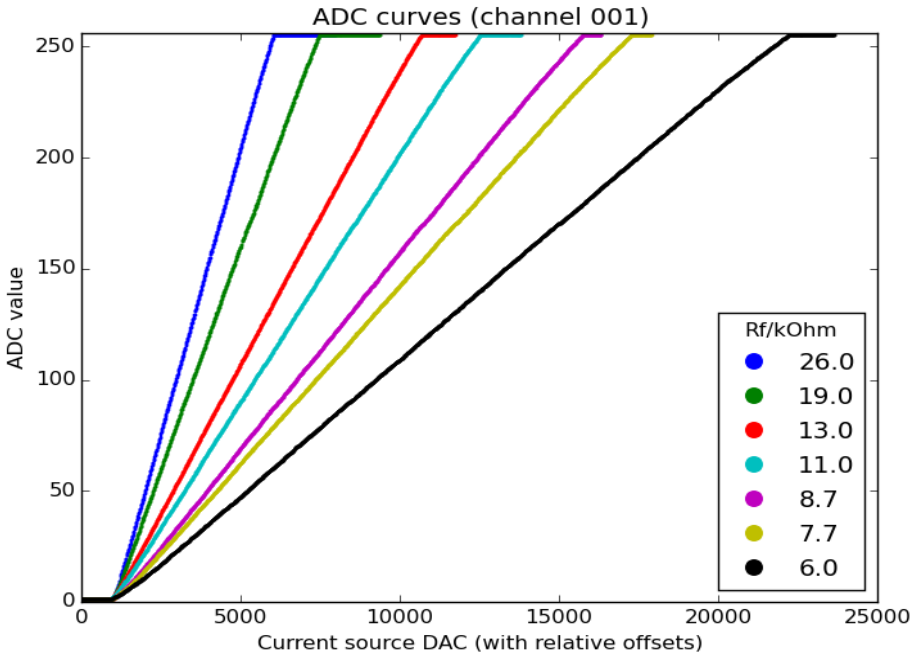
Hybrid5 Testing Boards with DCD4.x

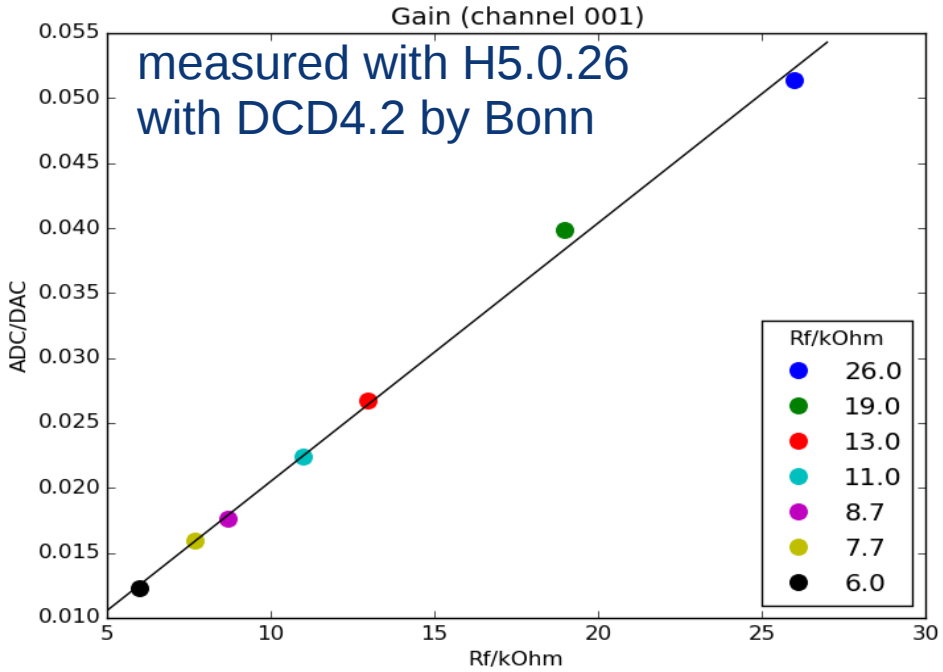
- DCD4.1
  - H5.0.24: measured in Goe and Bonn
    - equipped with switcher and matrix
  - H5.0.13: measured in Goe and Bonn
  - H5.0.12: not measured yet, located in Bonn
- DCD4.2
  - H5.0.15: measured in Goe
    - strange gain behaviour, large current offsets
  - H5.0.14: measured in Goe
    - equipped with switcher and matrix
  - H5.0.26: measured in Bonn

all measured at
GCK = 76 MHz
LVDS boost on
LVDS ref shift on

DCD4.x Gain Implementation

- TIA gain adjustable by combination of feedback resistors of 26k (En30), 13k (En60) and 19k (En90)



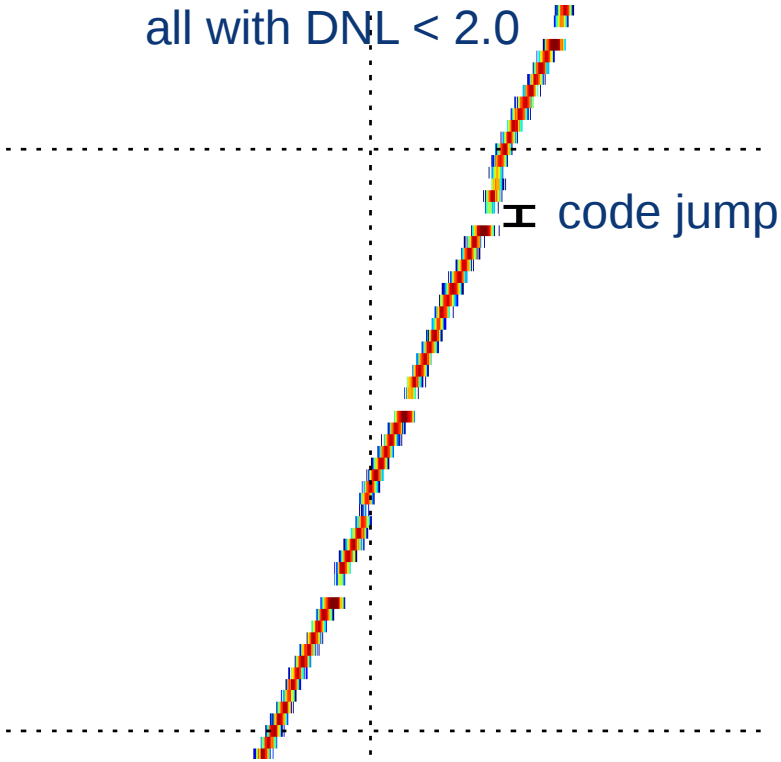


Rf [kOhm]	gain [nA/ADC]	range [uA]	range (+-100 ADC) [uA]
26 (En30)	75	19	15
19 (En90)	96	25	19
13 (En60)	144	36	29
8.7 (En30+En60)	171	44	34
7.7 (En60+En90)	217	61	48
6.0 (all)	313	80	63

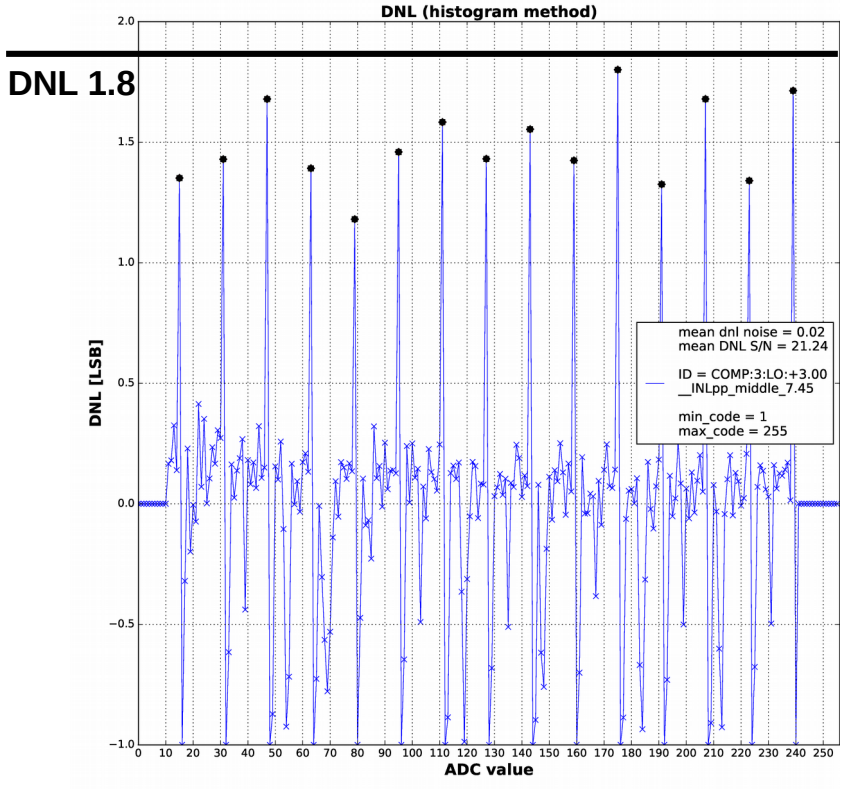
ADC Optimization Criteria

- check ADC curve for noise, INLpp, **long codes**, code range and bit errors

< 5% of channels per DCD, all with DNL < 2.0

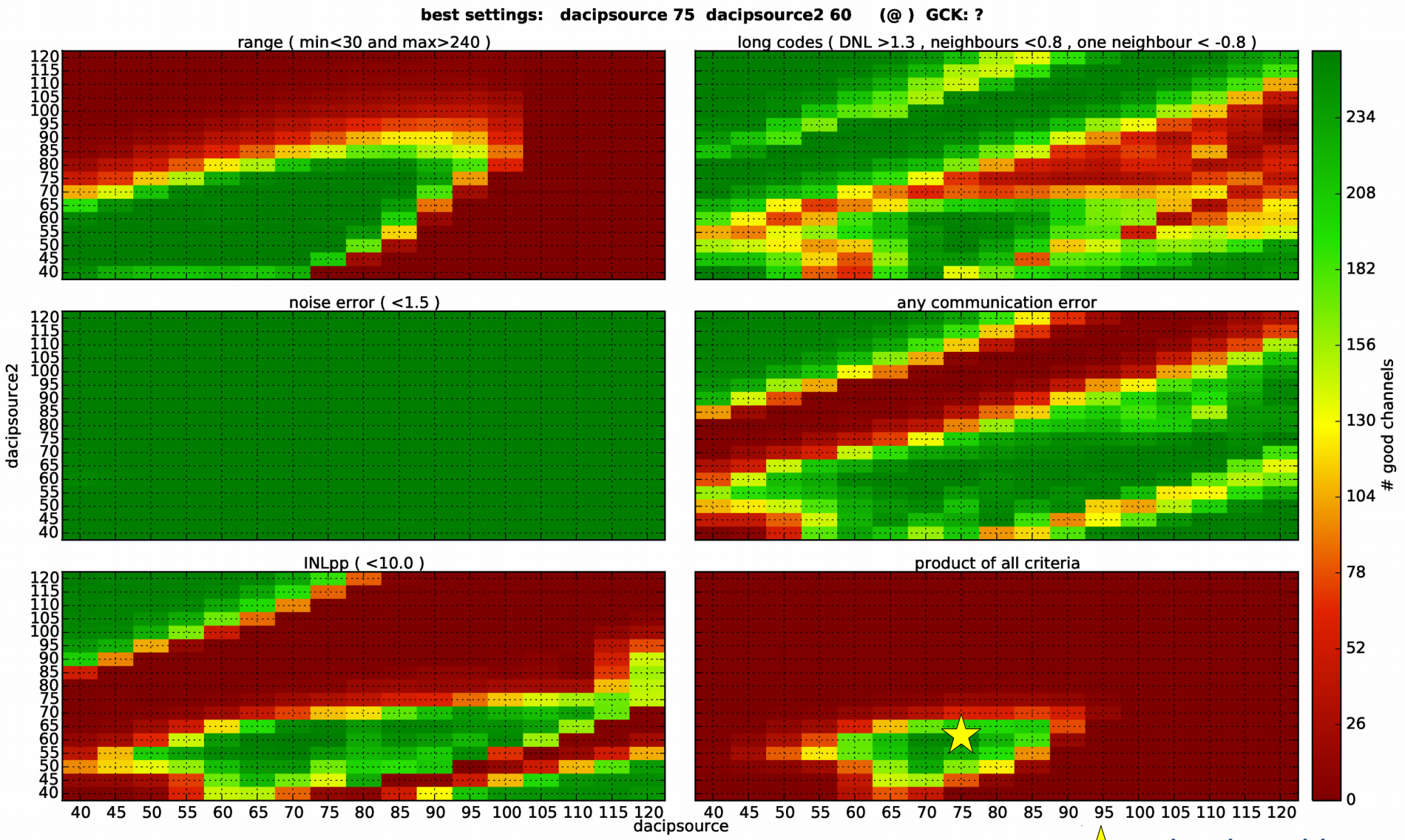


DNL



- long codes originate from transistor mismatches in the ADC comparators
- still see very few long codes in DCD4.x, but all with DNL < 6, not harmful according to DCD4.x design manual

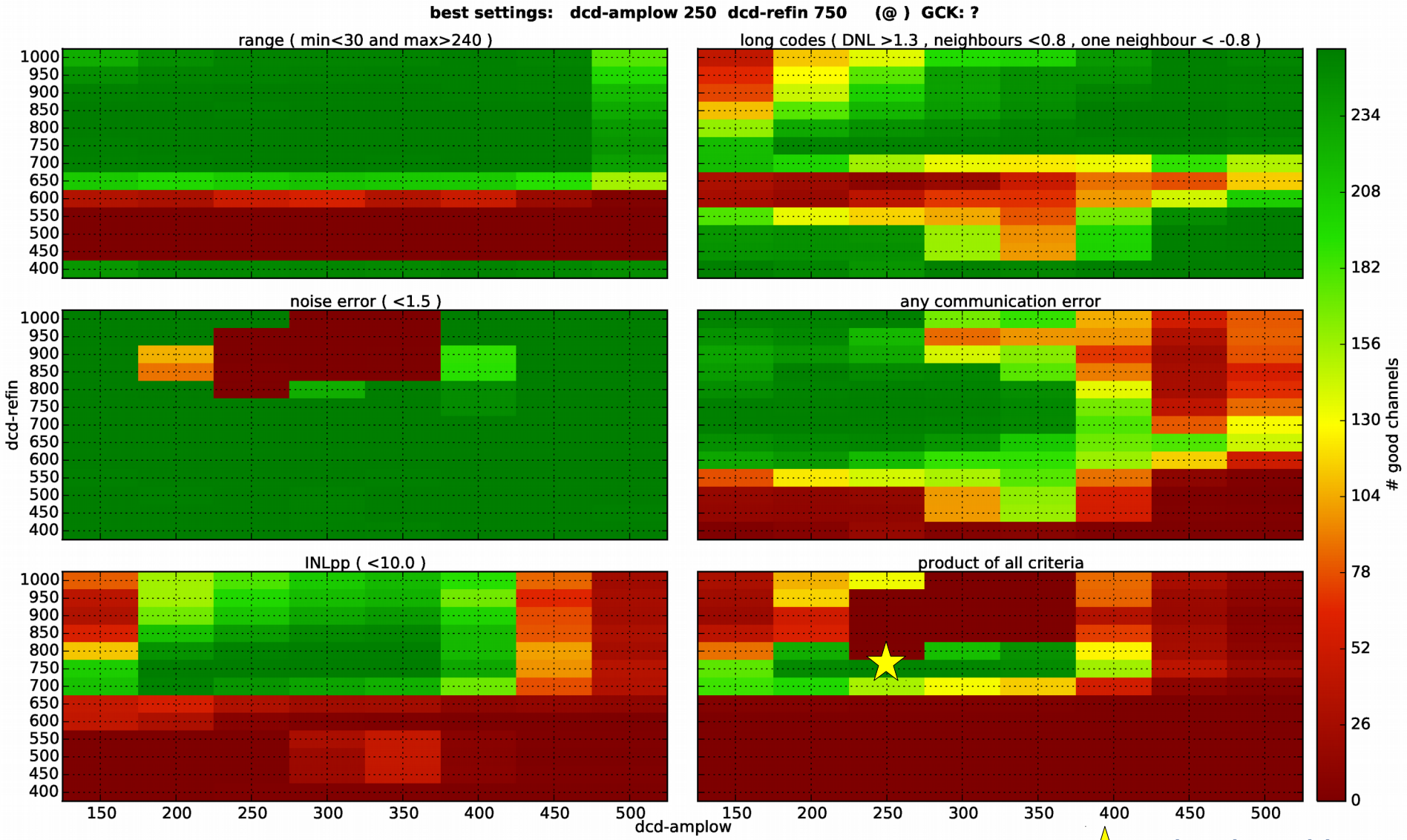
H5.0.13 (DCD4.1) Optimization:
IPSource-IPSource2



★ optimal working point

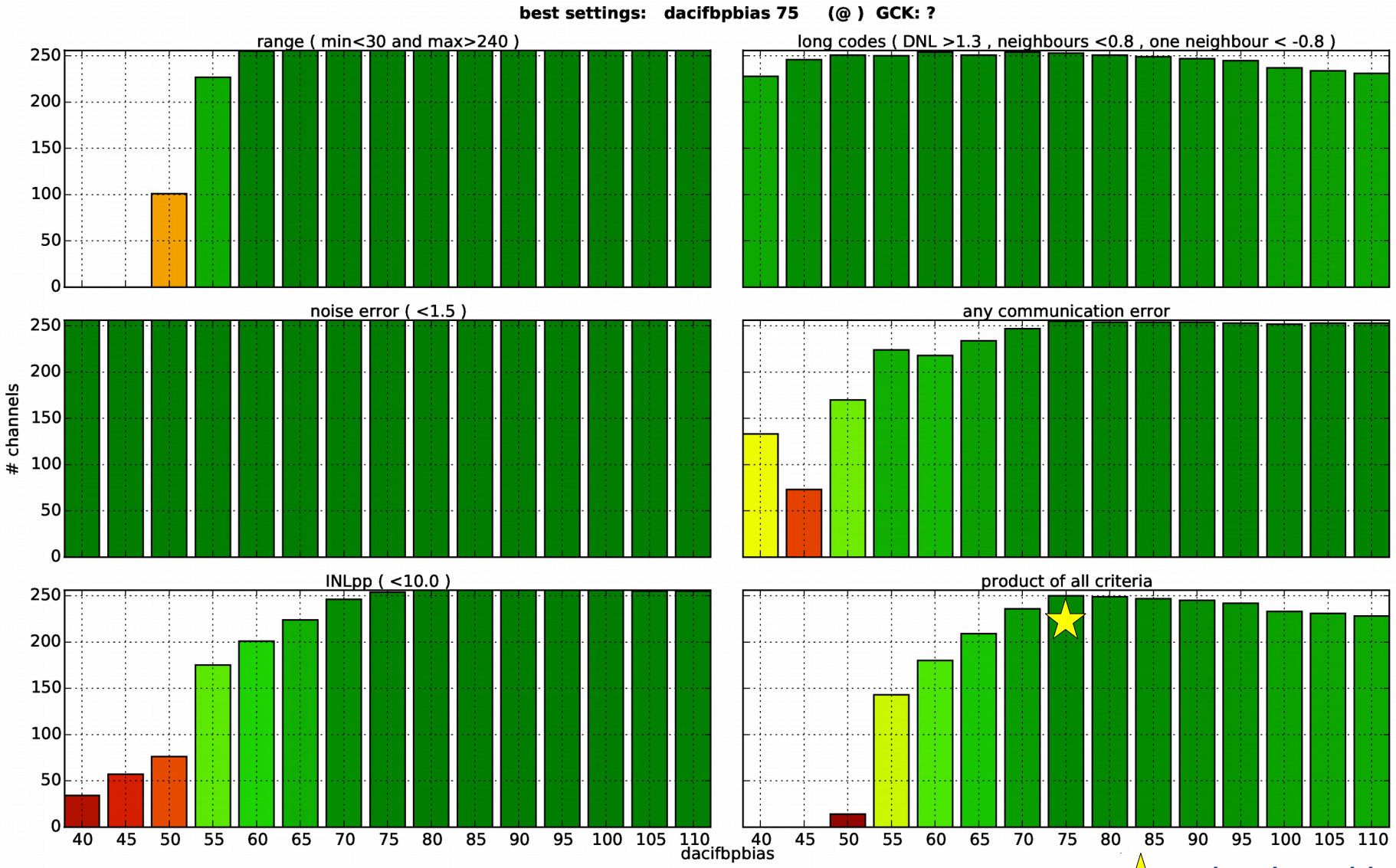
- narrow window for the optimal IPSource, IPSource2 values
- large enough to find stable setting

H5.0.13 (DCD4.1) Optimization:
RefIn-AmpLow



- RefIn very much constrained
  - scan with finer step size around 700-750 mV
- AmpLow with broad good region

H5.0.13 (DCD4.1) Optimization: IFBPBias



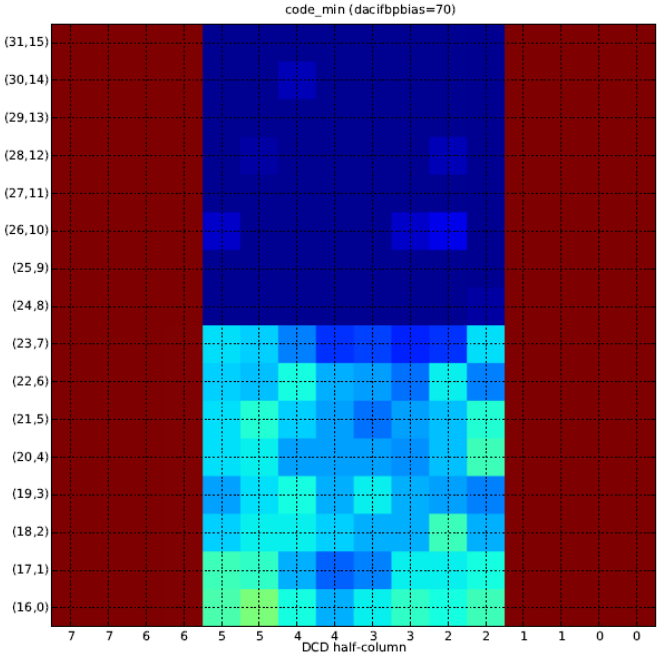
★ optimal working point

- find an optimal IFBPBias value with a large number of good channels

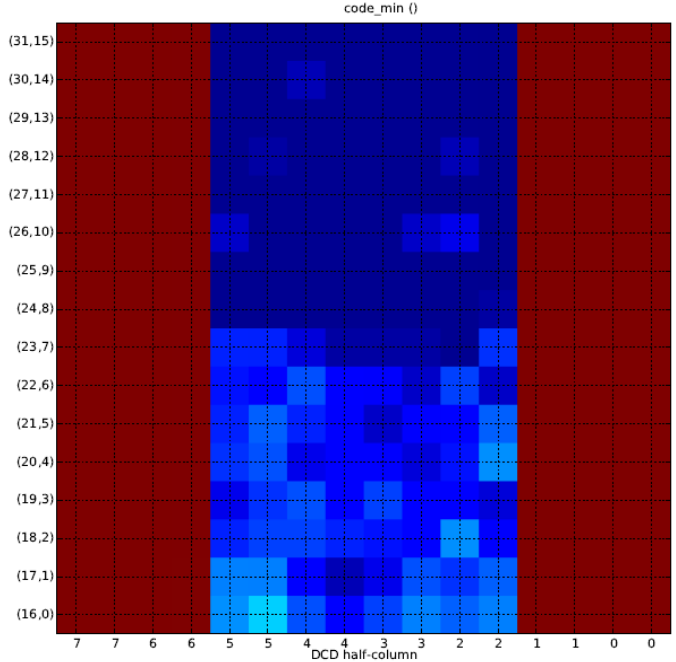
IPSourceMiddle Improvements

- IPSourceMiddle improves top/bottom inhomogeneity
- need to add IPSourceMiddle to the standard optimization parameters

IPSource/IPSourceMiddle: 75/75



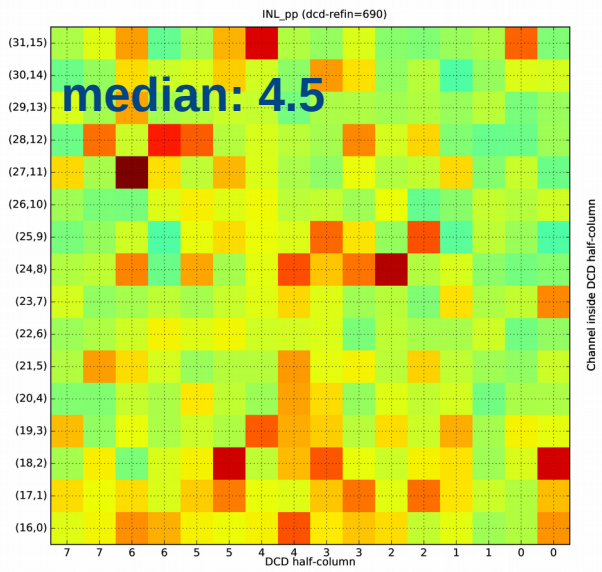
IPSource/IPSourceMiddle: 75/72



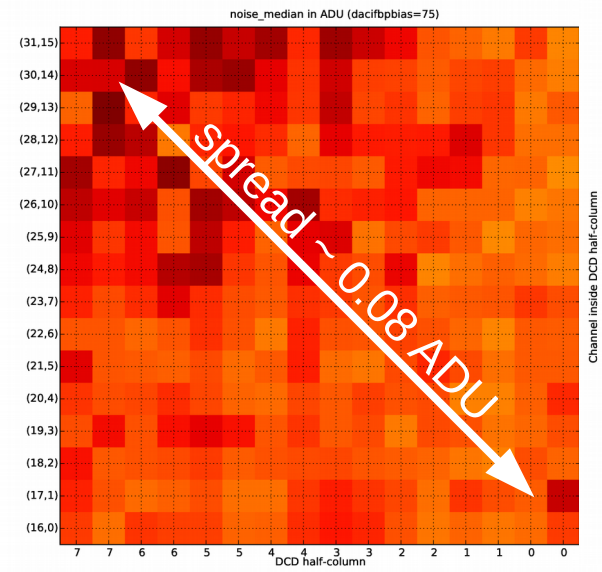
DCD pin-out map of the minimal code measured in the channels ADC curve

H5.0.13 (DCD4.1) Optimization Result

- found optimal working point for DCD4.1 on H5.0.13
- all channels are good, performance within specifications
  - all channels have INLpp < 8 ADU
  - all channels show noise < 0.55 ADU
  - gain similar for all channels

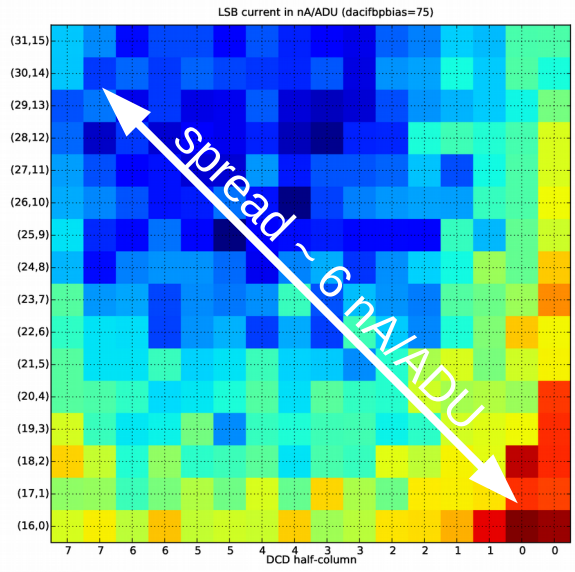


INLpp < 8 for all channels



noise < 0.55 for all channels

En30, ~80 nA/ADU



min to max gain variation ~10%

Hybrid5 Overview

- optimal working points table

Module	IPSource	IPSource2	IFBPBias	RefIn [mV]	AmpLow [mV]	gain/Clock	comment
H5.0.24 (DCD4.1)	70	60	75	690	200	En30, 76MHz	DHE source
H5.0.13 (DCD4.1)	**70**	**60**	**75**	**690**	**200**	**En30, 76MHz**	**DHE source**
H5.0.14 (DCD4.2)	**75**	**65**	**70**	**680**	**200**	**En30, 76MHz**	**DHE source, same for gate source**
H5.0.15 (DCD4.2)	70	55	60	700	200	En30, 76MHz	strange gain behaviour
H5.0.26 (DCD4.2)	70	60	70	650	200	?	
DCDpp							
H5.0.06 (DCDpp)	*100*	*80*	*90*	*850*	*350*	*HighGain, 62MHz*	*with matrix*
H5.0.07 (DCDpp)	*90*	*70*	*85*	*950*	*400*	*HighGain, 62MHz*	*without matrix*

- all DCD4.1 and DCD4.2 have very similar optimal working points

improved optimization procedure correct setting of VNSubIn, fine RefIn stepping

Hybrid5 Overview

- channel statistics table

Module	scanned	good	range err.	bit err.	comp. err.	INL err.	quality (good/all)
H5.0.24 (DCD4.1)	256	249	1	0	2	4	0.97
H5.0.13 (DCD4.1)	**256**	**256**	**0**	**0**	**0**	**0**	**1.00**
H5.0.14 (DCD4.2)	**256**	**256**	**0**	**0**	**0**	**0**	**1.00**
H5.0.15 (DCD4.2)	256	252	0	0	0	0	1.00
H5.0.26 (DCD4.2)	256	247	0	9	0	0	0.96
DCDpp							
H5.0.06 (DCDpp)	*256*	*249*	*2*	*5*	*0*	*?*	*0.97*
H5.0.07 (DCDpp)	*43*	*39*	*0*	*4*	*0*	*?*	*0.88*

- all DCD4.1 and DCD4.2 perform well at optimal working point

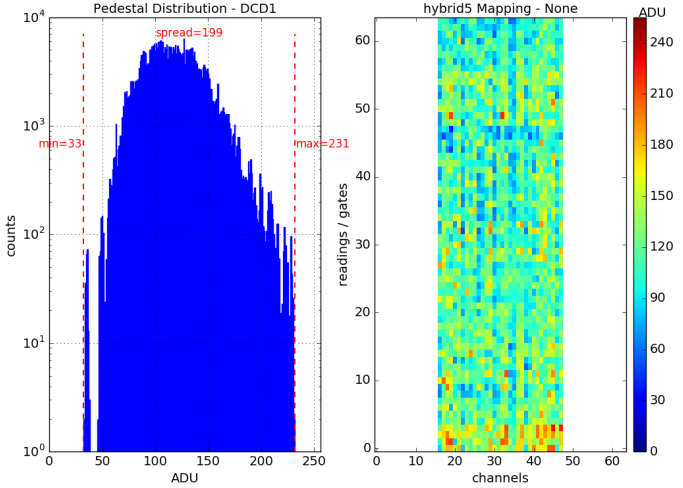
improved optimization procedure correct setting of VNSubIn, fine RefIn stepping

Source Measurements with DCD4.2, PXD9-6 Matrix and SWB18v2.1

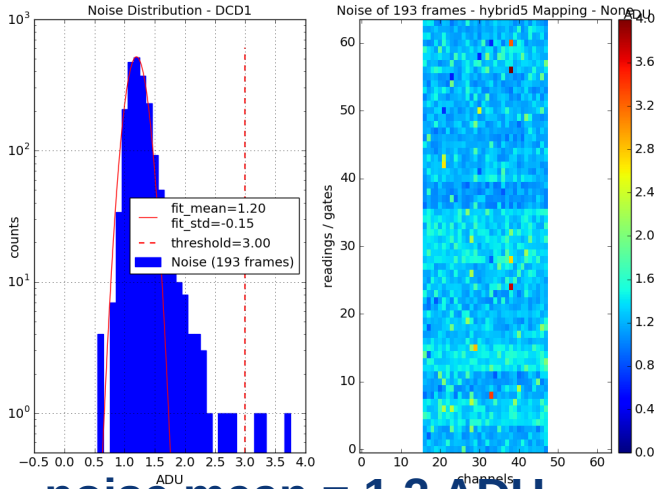
Analog Common Mode Correction

- pedestals and noise measured on H5.0.14 with DCD4.2

without any common mode correction



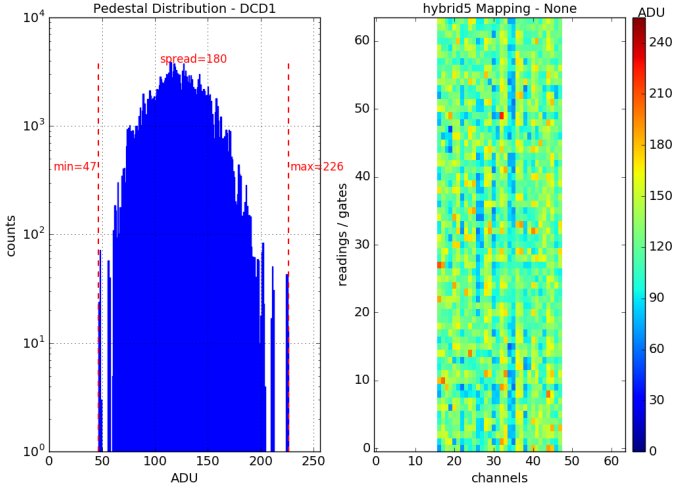
min-max pedestal = 199 ADU



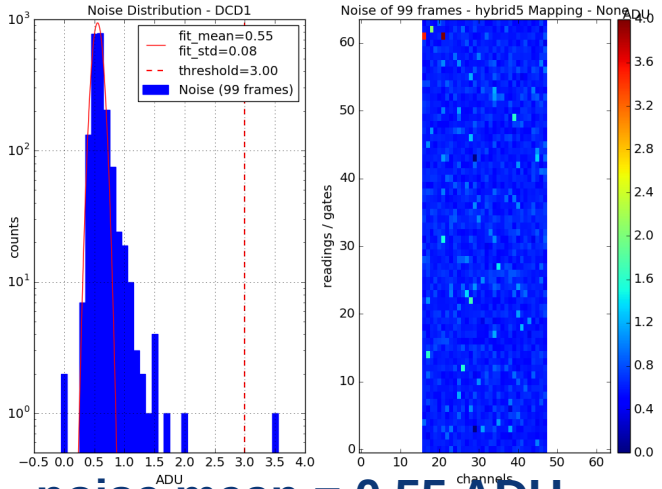
noise mean = 1.2 ADU
noise RMS = 0.15 ADU

ACMC on

with analog common mode correction



min-max pedestal = 180 ADU

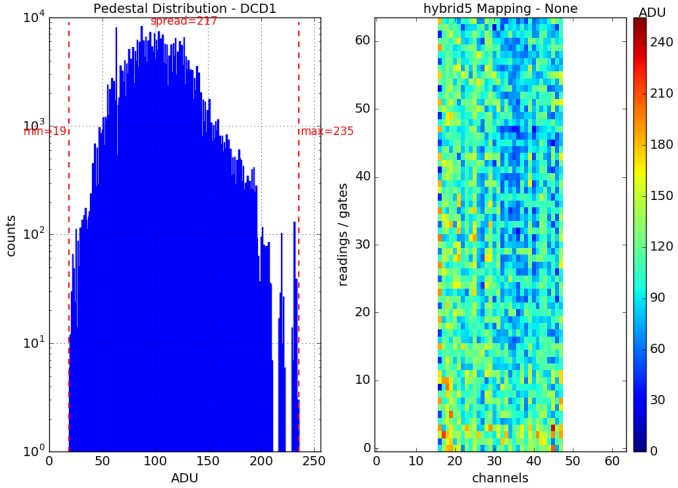


noise mean = 0.55 ADU
noise RMS = 0.08 ADU

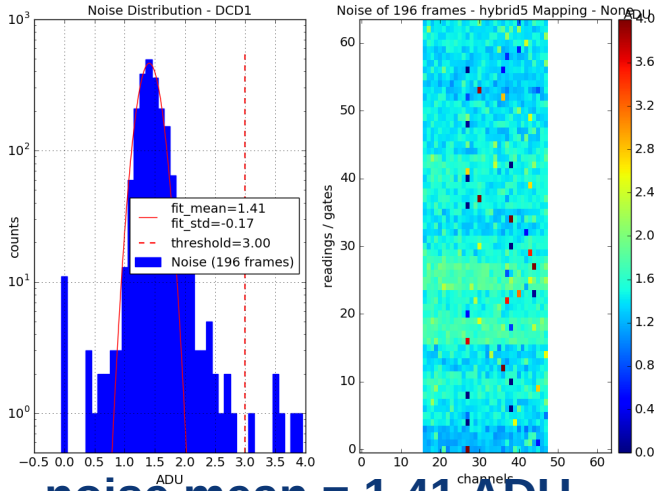
2bit DAC Offset Correction

- pedestals and noise measured on H5.0.24 with DCD4.1

without pedestal correction



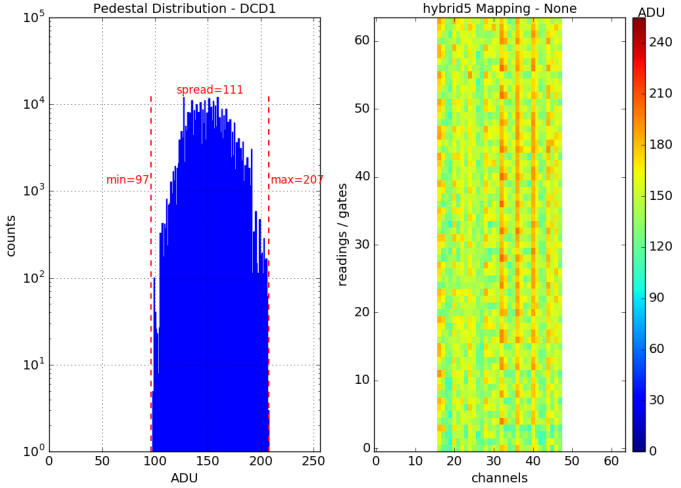
min-max pedestal = 217 ADU



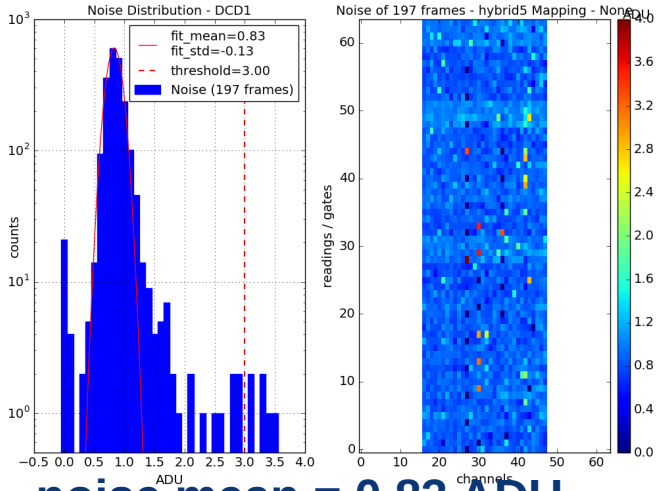
noise mean = 1.41 ADU
noise RMS = 0.17 ADU

2bit DAC corr.

with 2bit DAC offset correction



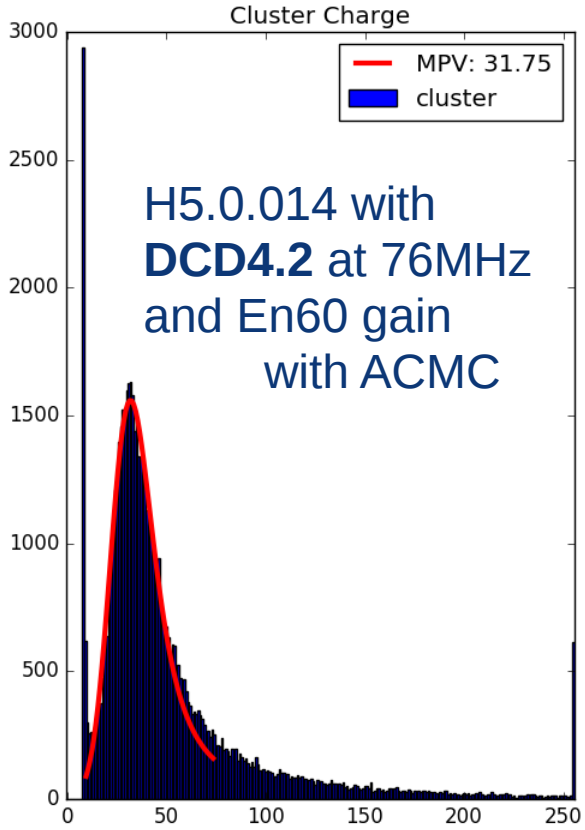
min-max pedestal = 111 ADU

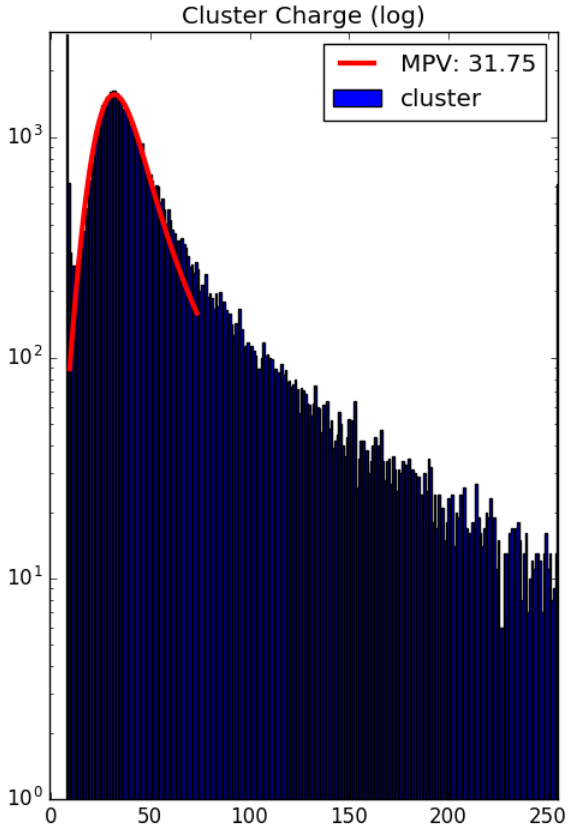


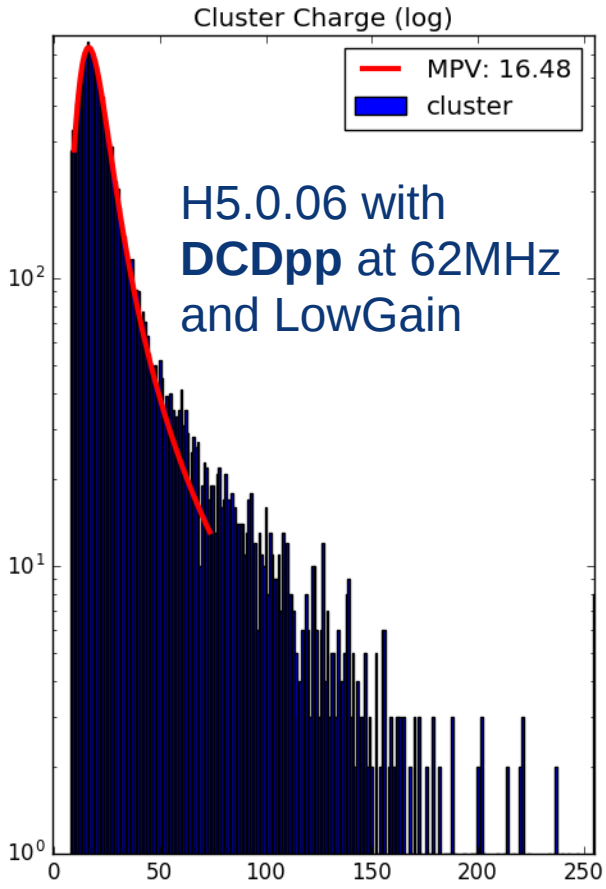
noise mean = 0.83 ADU
noise RMS = 0.13 ADU

Sr90 Signal Spectrum

- Sr90 spectrum measured with H5.0.14 with **DCD4.2** at gain En60
- compare to DCDpp measurement







MPV = 31.75 ADU

SNR = 57.73

gate length = 5 µm

g_q ~ 730 pA/e

MPV = 16.48 ADU

SNR = 30.52

gate length = 6 µm

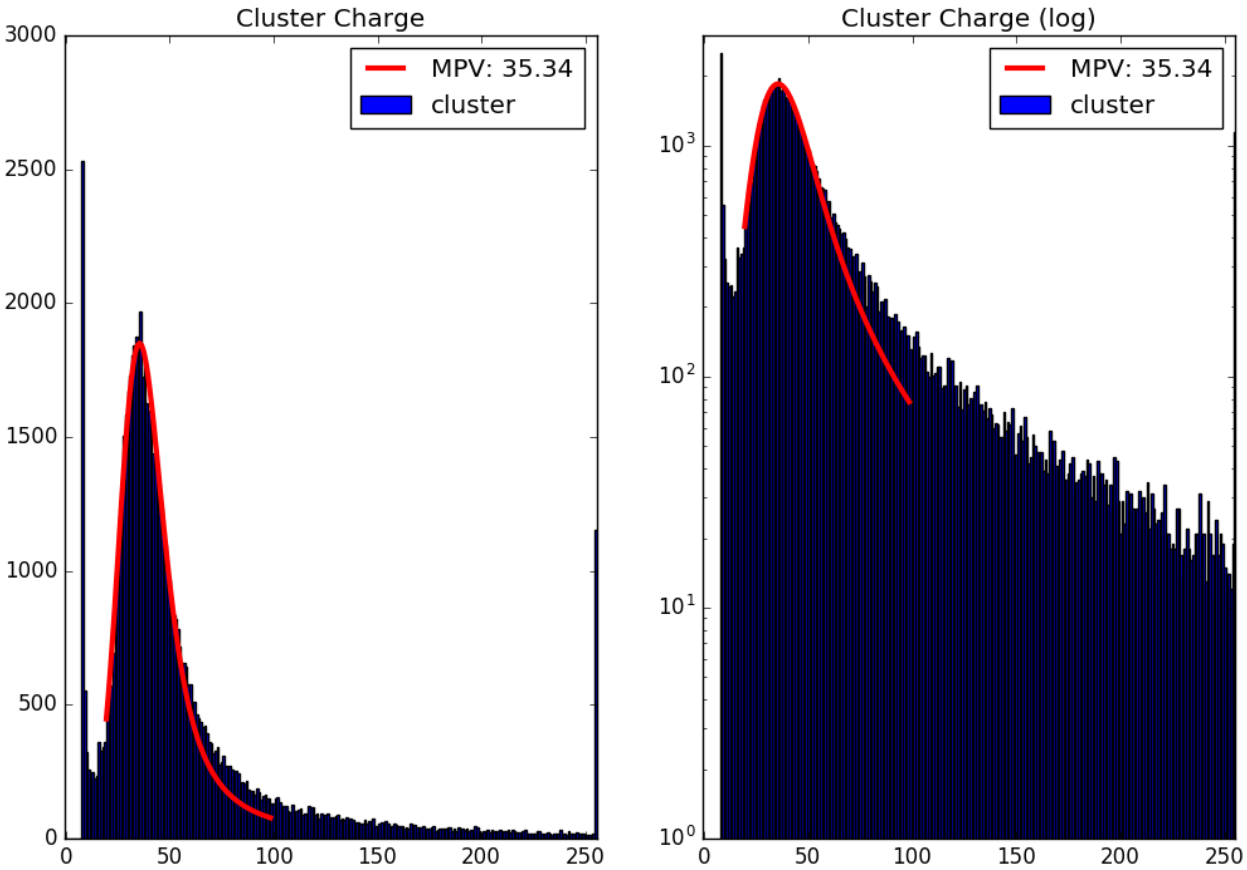
g_q ~ 380 pA/e

Sr90 Signal Spectrum

- Sr90 spectrum measured with H5.0.24 with **DCD4.1** at gain En60
- done with ACMC and 2bit DAC offset at full speed (GCK 76MHz)!

H5.0.024 with **DCD4.1** at 76MHz and En60 gain

SWB18v2



MPV = 35.34 ADU

SNR = 56.13

gate length = 5 µm

g_q ~ 780 pA/e

Conclusion

Conclusion

- DCD4.x gain implementation confirmed
- all Hybrid5 boards with DCD4.1 and DCD4.2 could be optimized
- after optimization both DCD4.x performance within specifications
- ACMC and 2bit DAC offset functional on both DCD4.x
- Sr90 source spectrum measured with a SNR of 57
- up to now both DCD4.1 and DCD4.2 seem to be fully functional
    - **both new DCD designs seem to be applicable for the final modules**
- ToDo:
    - source measurements with ACMC, 2-bit DAC offset and gated mode

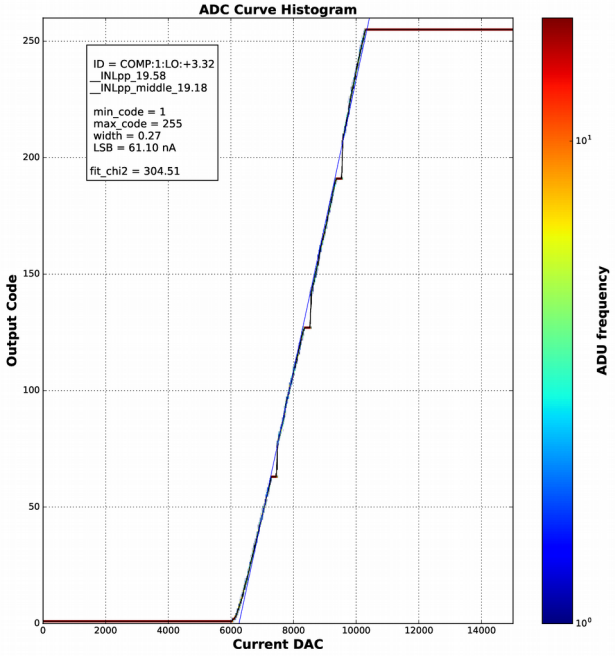
BACKUP

ACMC Observations

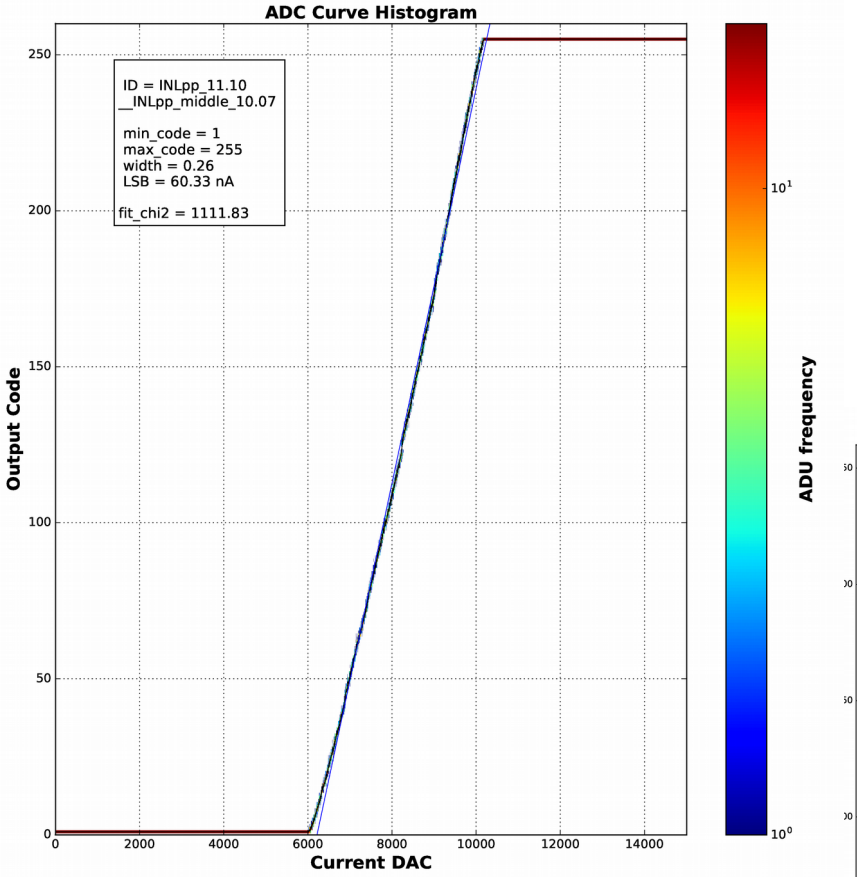
- on DCDpp
  - with ACMC on and matrix on, need to adjust IPAddOut to shift pedestal distribution in dynamic range
  - when matrix blocked: need to increase IPAddIn
    - why does IPAddIn have an effect at all? should be compensated by ACMC just as VNSubIn
- on DCD4.2
  - when ACMC turned on, no need to adjust IPAddOut/In

H5.0.24 (DCD4.1) Bad Channels

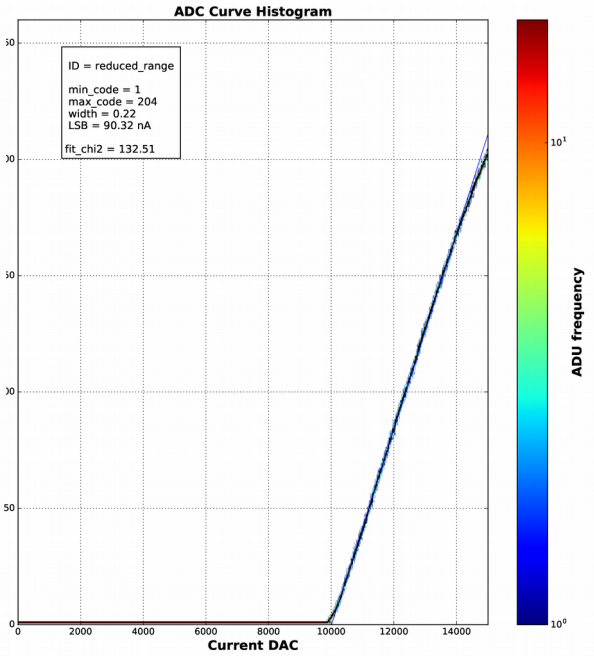
long codes (DNL > 10)



high INL (INLpp 11.10)



reduced range

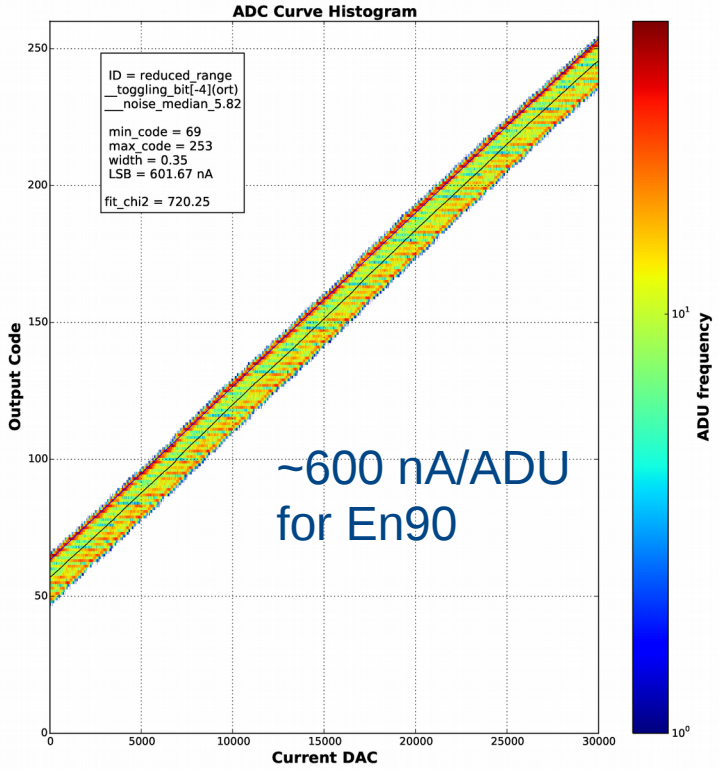


H5.0.15 (DCD4.2) Problems

- ADC curves show very large DAC offsets
  - several µA offset before ADC curve starts
  - VNSubIn/Out and IPAddIn/Out all 0
- for gain EN30 and extended DHE current source DAC range
  - could perform ADC optimization, optimal working point with good performance
- for lower gains (En60, En90)
  - ADC curves slopes extremely small

    in the order of 600-1200 nA/ADU

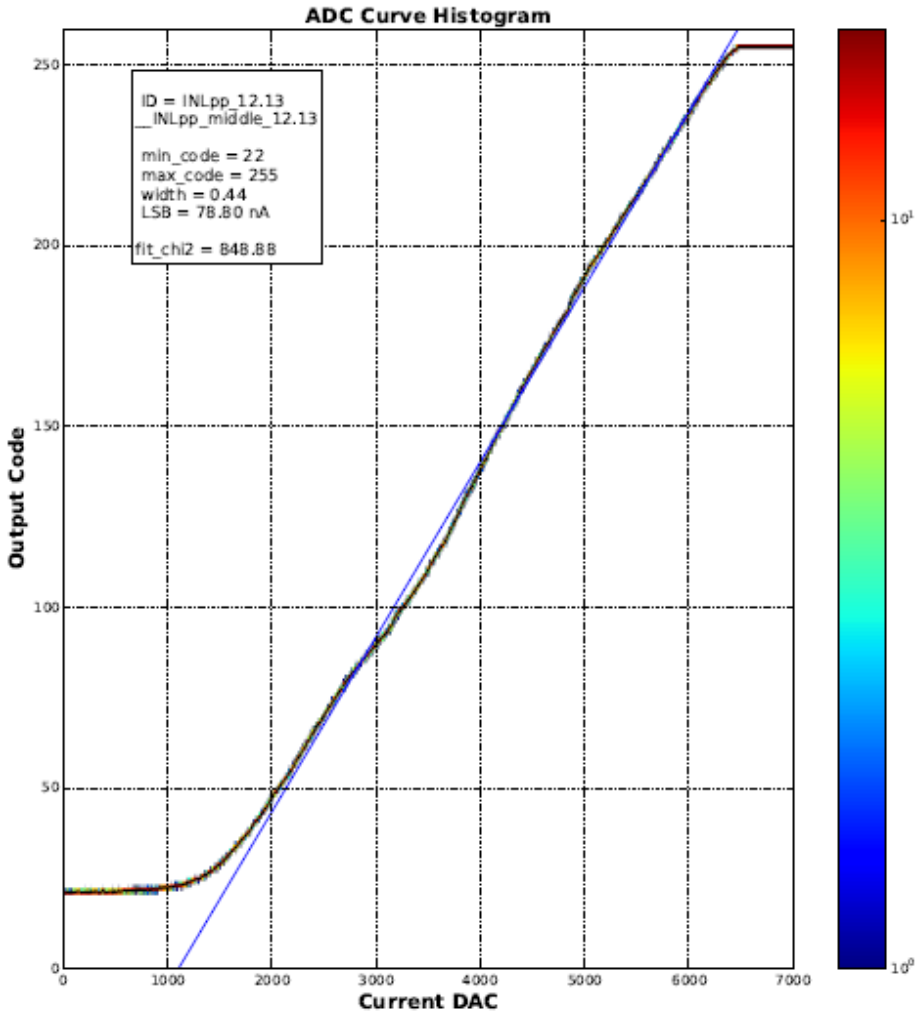
    and noise of > 6 ADU



Gate-On vs DHE Current Source

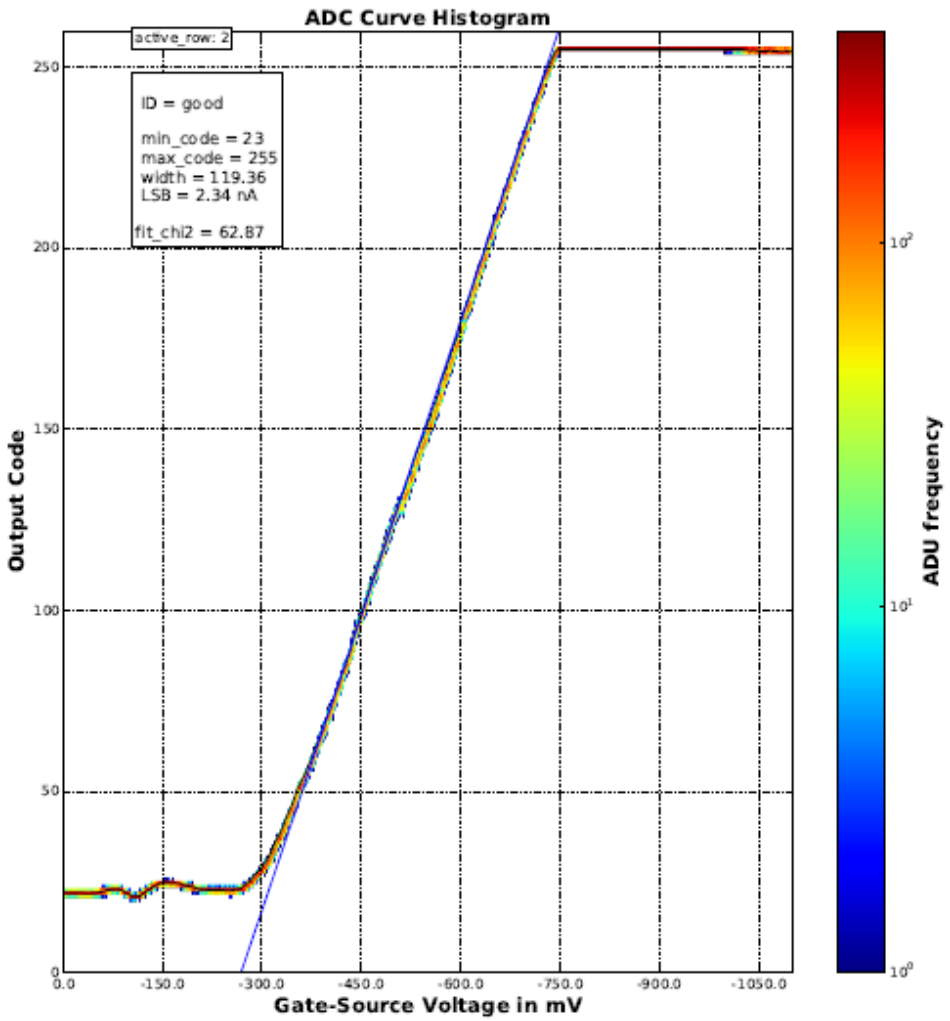
DHE Source

channel112_dacifbpbias-070__INLpp_12.13__INLpp_middle_12.13



Gate-On Source

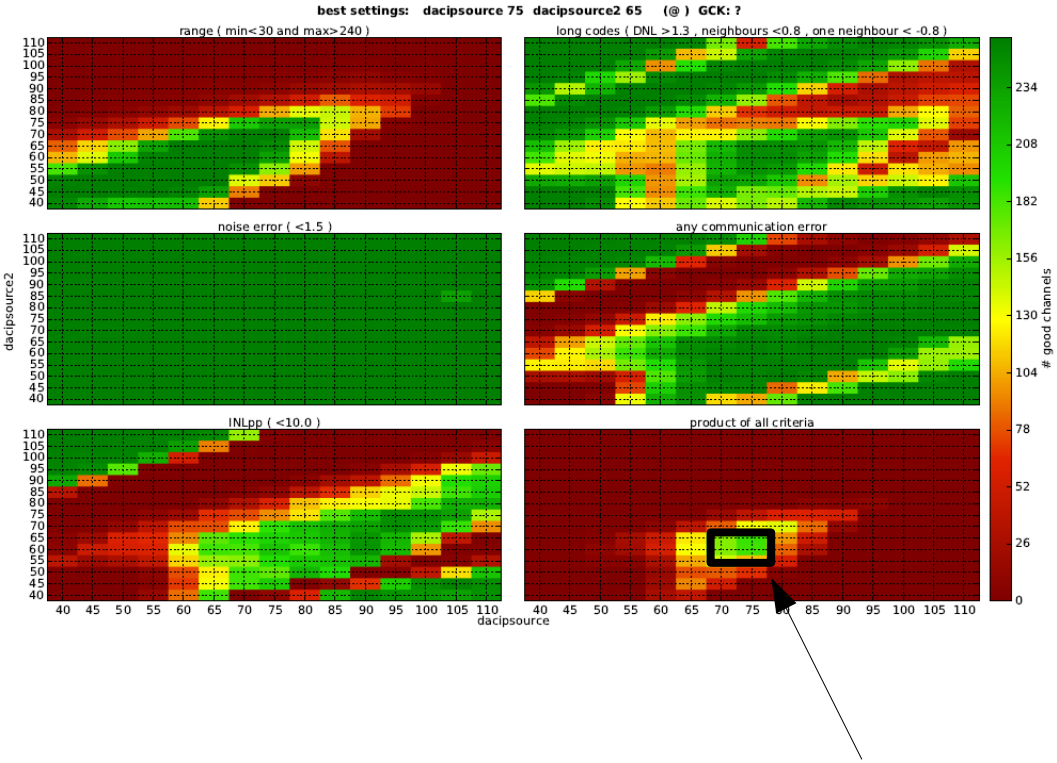
channel112_dacifbpbias-070



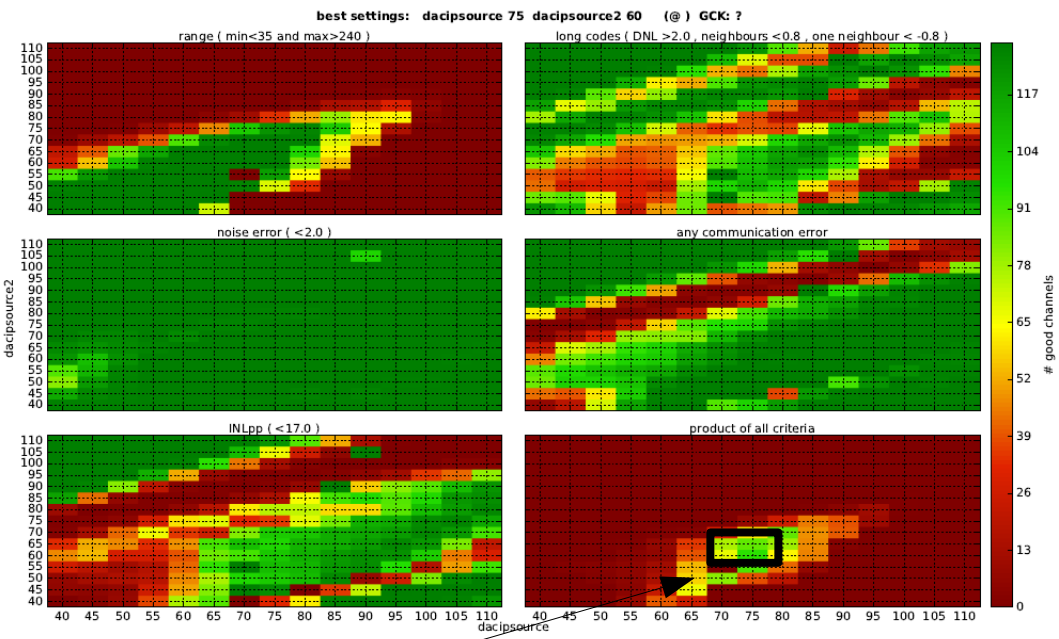
- same optimal working points are found with Gate-On source measurements

Gate-On vs DHE Current Source

DHE Source



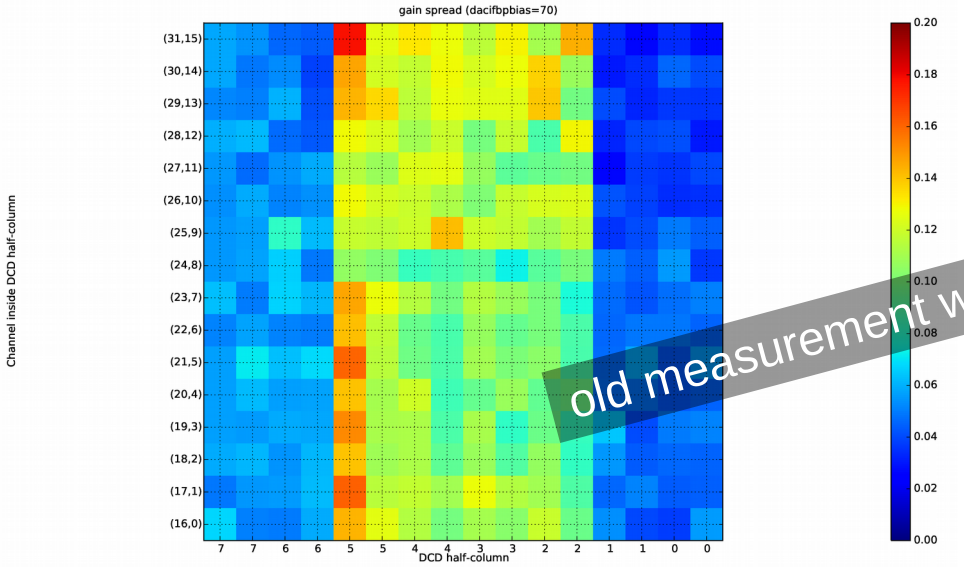
Gate-On Source

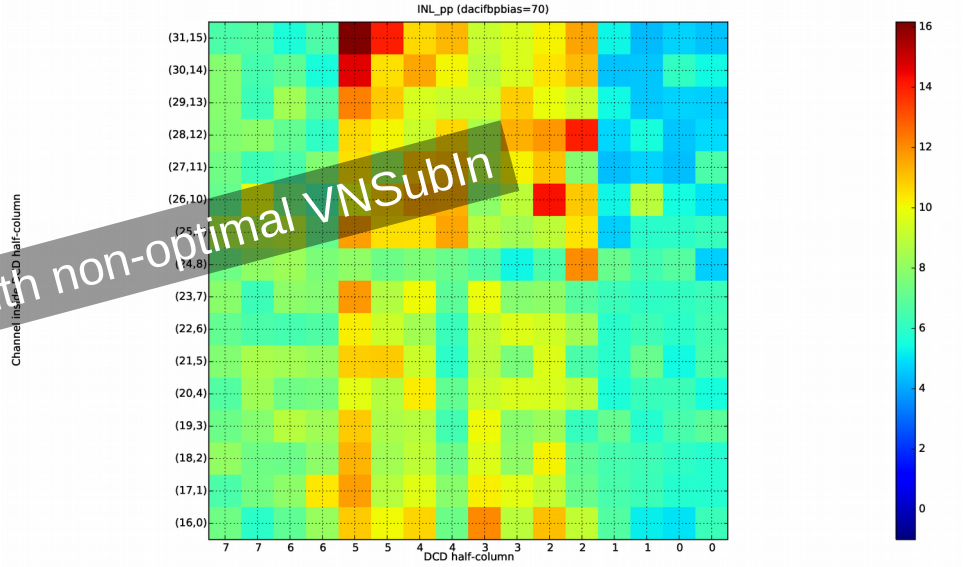


very similar region around
best working point

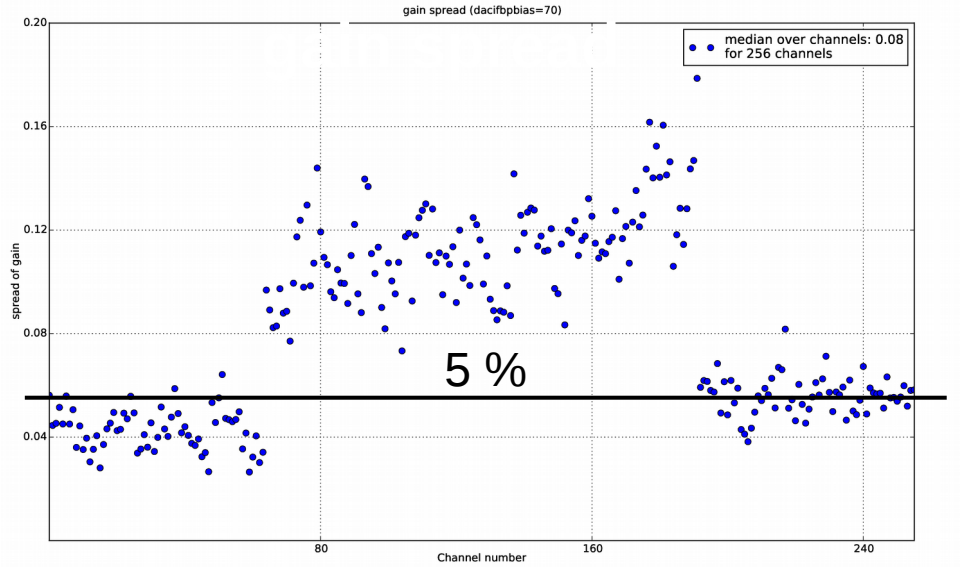
- similar for RefIn-AmpLow and IFBPBias sweeps

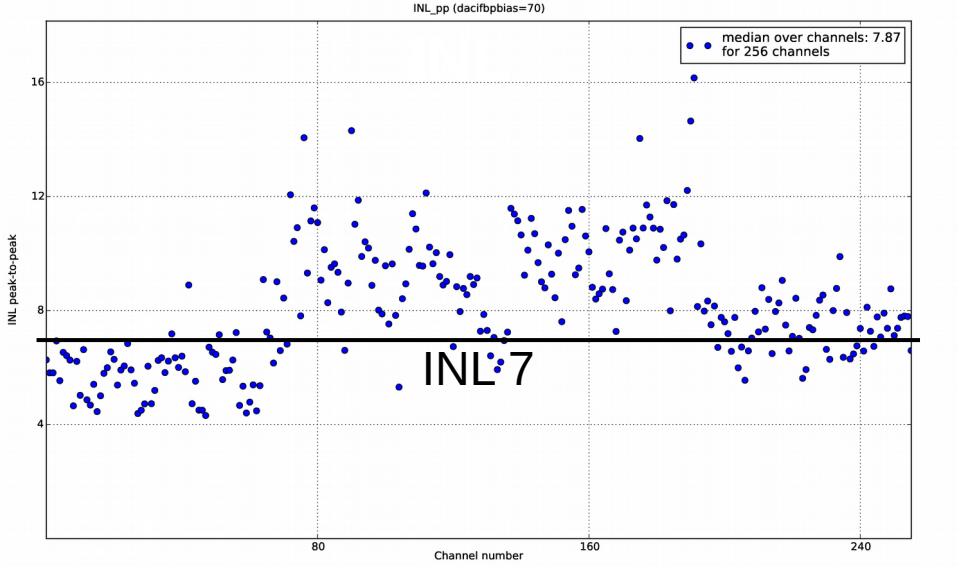
INLpp and Gain Spread





old measurement with non-optimal VNSubIn



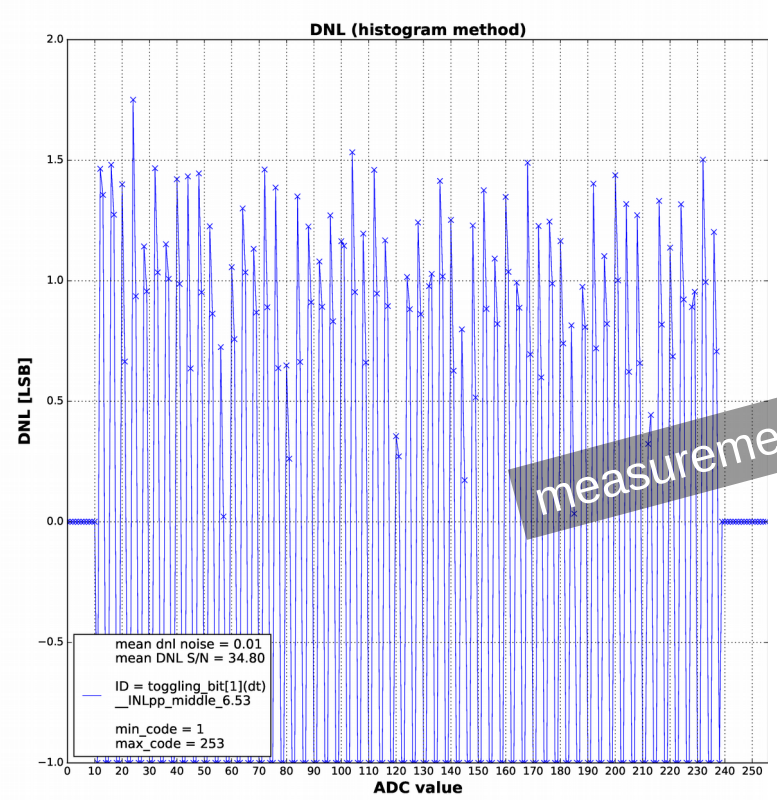


→ requiring a gain spread <= 5 % , INLpp values up to 7-8 are still ok

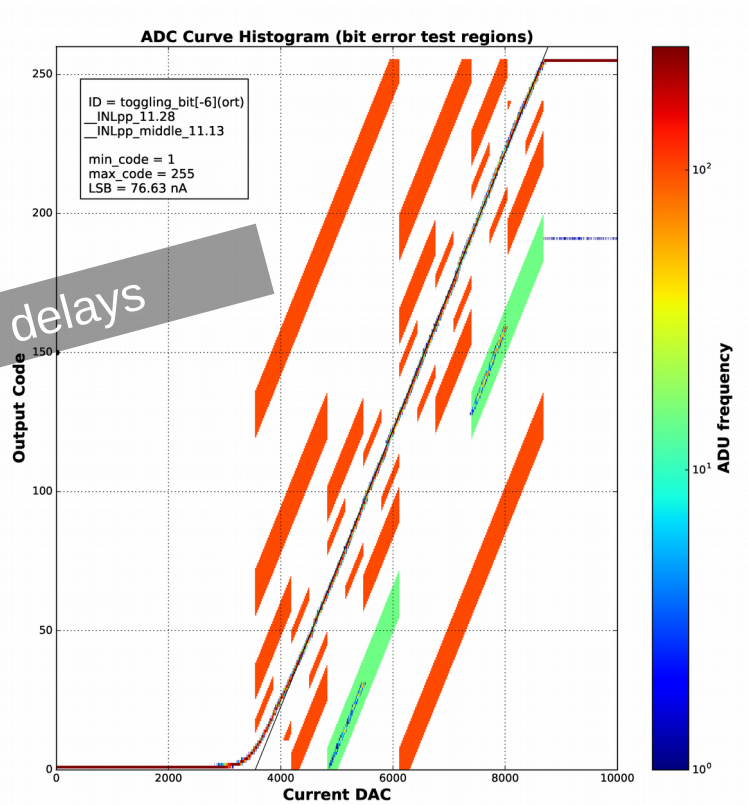
ADC Optimization Criteria

- check ADC curve for noise, INLpp, long codes, code range and **bit errors**

Bit1 error recognized in DNL topology



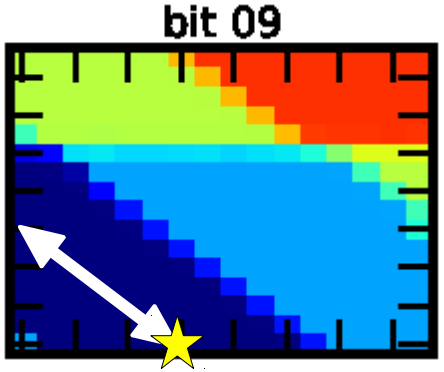
Bit6 error recognized via ADC curve outliers



measurement with non-optimal delays

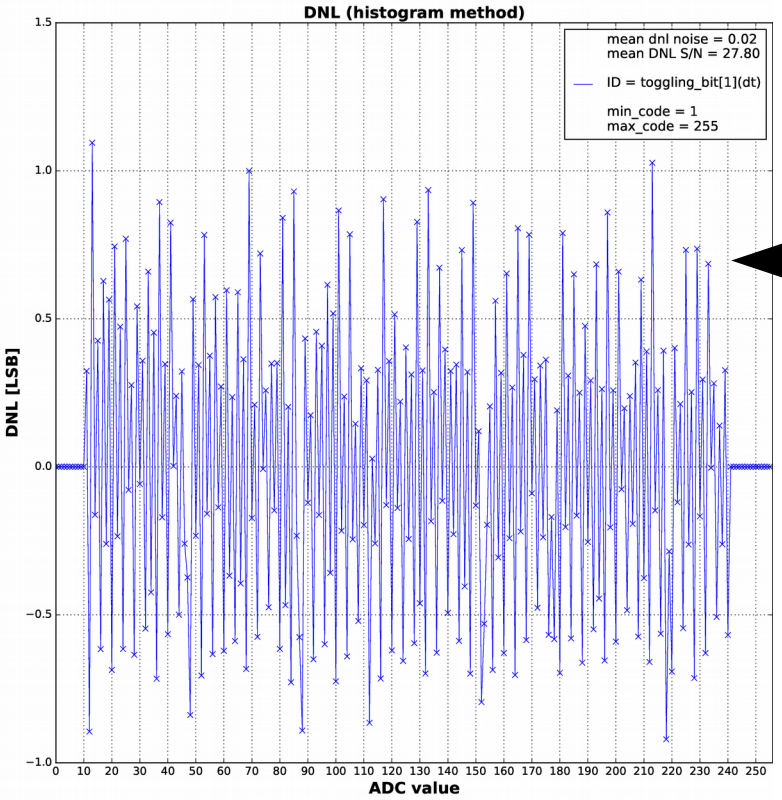
- bit errors show specific topology in the DNL
  - confirmed by simulation
  - distinct from long code topologies

Fine RefIn Tweaking



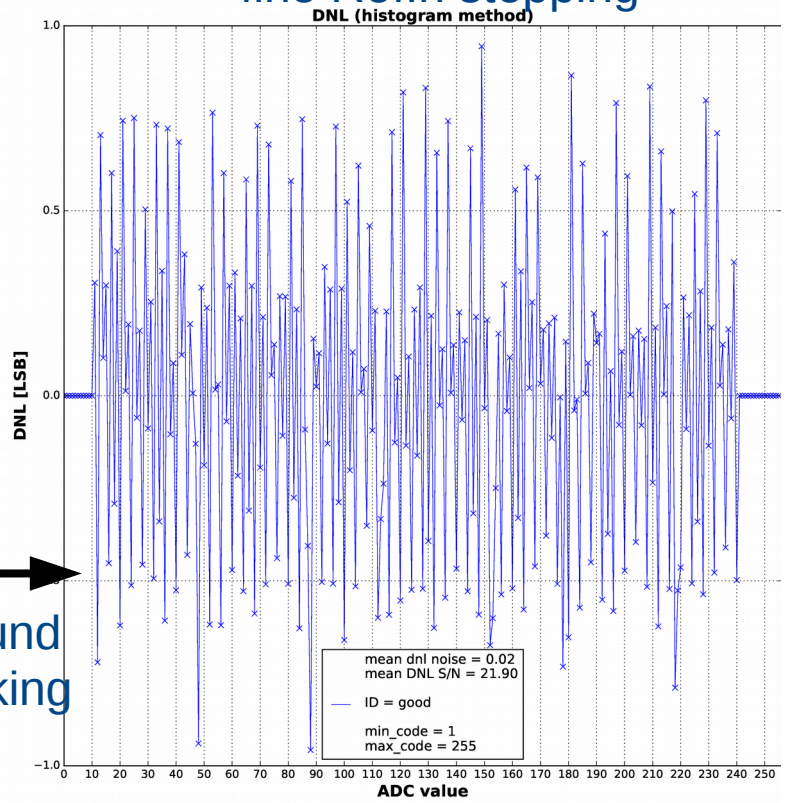
- Bit1 error topologies
  - do not change with different delay optimization
  - small change with RefIn voltage
    - performed a fine RefIn stepping optimization

H5.0.13 (DCD4.1), ch 60, normal optimization



Bit1 error found
does not change with
different delays

H5.0.13 (DCD4.1), ch 60,
fine RefIn stepping



Bit1 error no longer found
due to fine RefIn tweaking