DHPT 1.2 Status

VXD Workshop, Santander

September 14-16, 2016

Overview

- DHPT 1.2 chips delivered end of July (100 pcs.)
- Started with test on probe station (needle card)
- DHE software needed to be changed because of wrong JTAG ID (bug in DHPT JTAG register implementation)
- Used DHH emulator for first tests (not having full coverage)

Bugs fixed in DHPT 1.2

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CML Driver

Test Results

- CML driver power routing
  - Ground rail (VSS) had a too high wiring resistance (~30 Ohm), parasitic extraction did not spot this because of substrate model
  - Rerouting of power nets → $R_{VSS} < 0.2$ Ohm

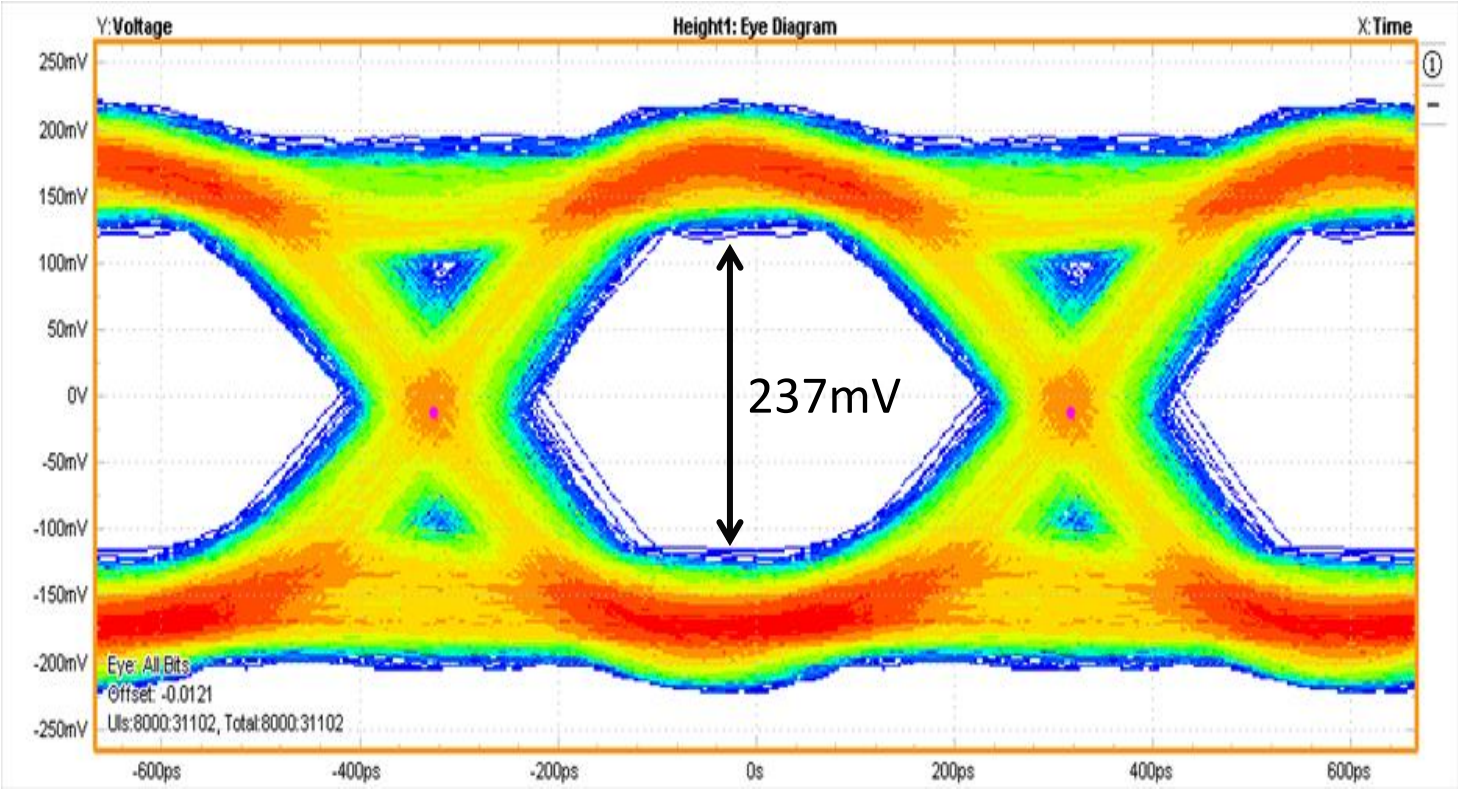
✓

- CML driver bias routing
  - Removed ESD resistor in bias connection and reduced parasitic resistance → increase of bias current, less sensitivity to voltage supply

✓

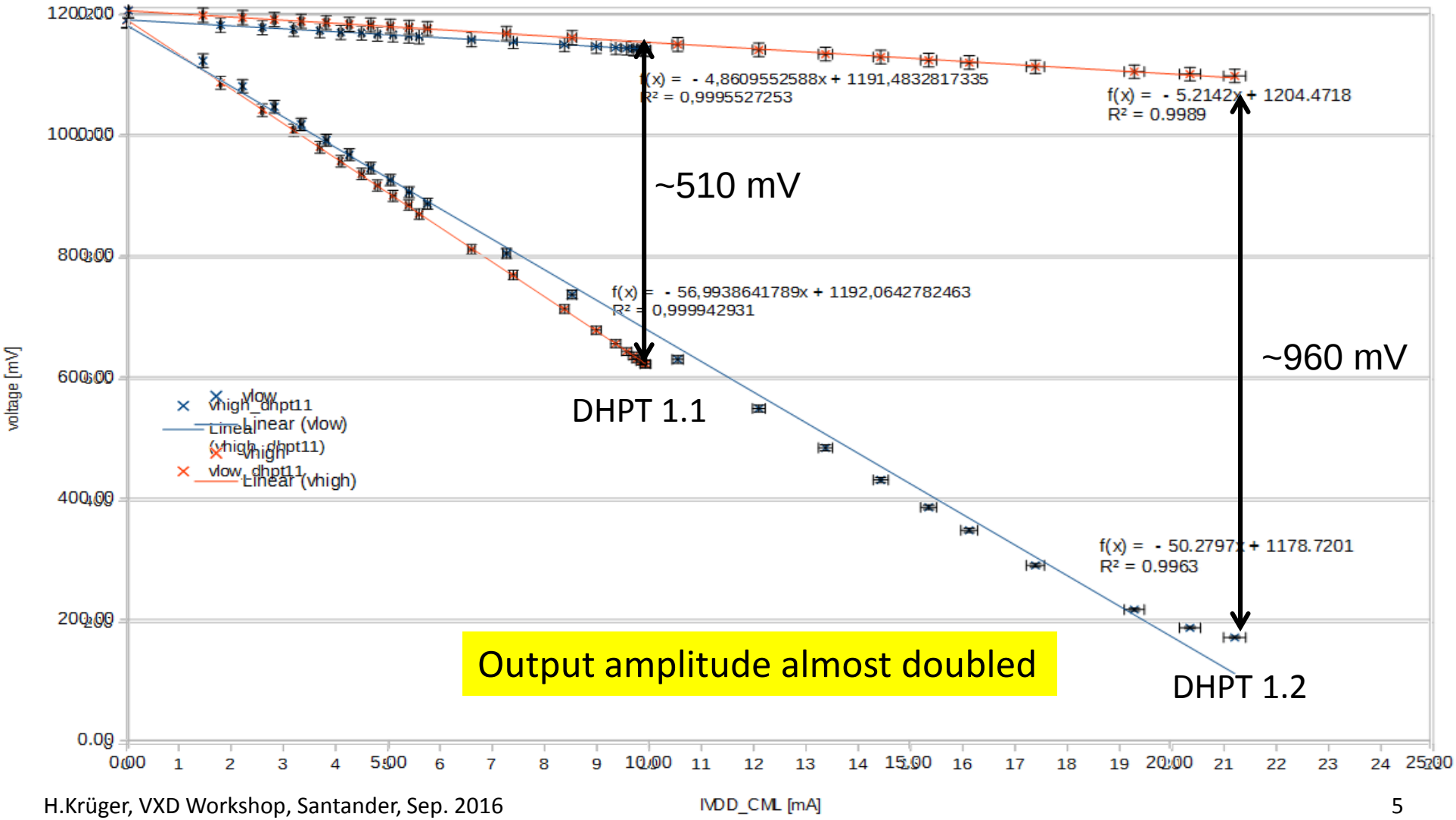
CML Driver Performance

- Eyediagram with 10m Infinband cable
  - IBIAS = 20, IBIASD = 60, Pll_cml_dly =2 (still a lot of headroom)



CML Performance Comparison

- CML output high and low level as a function of IBIAS (w/o termination)



Bugs fixed in DHPT 1.2

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Digital core

	Test Results
• Mem dump – Data had some low probability to show corrupted values for the first few pixels when output was set to 800 MHz and clock compensation was on → fixed in HDL code	pending
• Internal system clock phase – The core clock started with an arbitrary phase after power-on → added controlled reset (delayed GCK) to the internal clock divider	✓
• Gated mode sequence put out first word twice – Fixed HDL code	✓

Enhancements for DHPT 1.2

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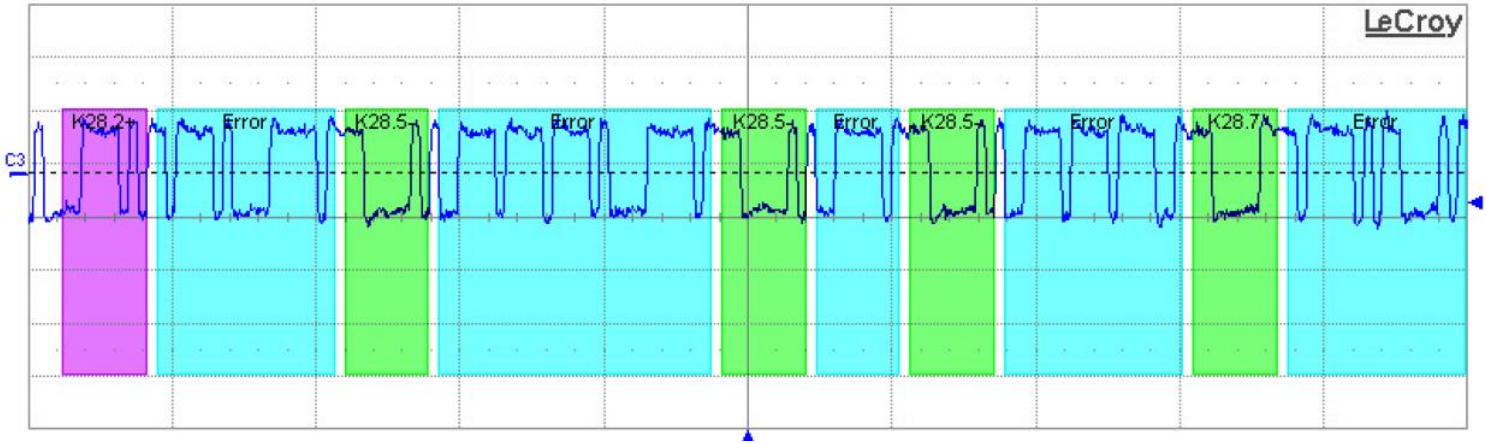
Digital core

	Test Results
• JTAG USERID changed: allows recognition of DHPT version – Implementation failure: used forbidden ID = xxx2 → (bit 0 of the IDCODE has to be 1)	X
• Gated mode: DATA_IN for the switcher can be selected to be controlled from either the *normal mode* sequence of the *gated mode* sequence (was *normal mode* only)	✓
• Added the DHPT ID in the memory dump frame header	pending
• Memory dump start address configurable	pending
• Bias register for LVDS receivers has fixed minimum value	✓

Data Link Synchronization

- We have seen an issue with the data link between DHE and DHPT 1.2
- DHPT 1.2 puts out invalid symbols → link does not synchronize



DHPT 1.2 data link @ DHE

- Very recent finding, need to cross-check with DHH emulator
- Behavior not reproducible in simulation (full layout, all corners)

Summary & Outlook

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- DHPT 1.2 changes
  - Power routing if the CML driver fixed successfully
  - Re-synthesized the digital core (bug fixes and enhancements)
  - Update of JTAG User ID introduced a bug in this register (User ID = 0 like DHP 0.2)

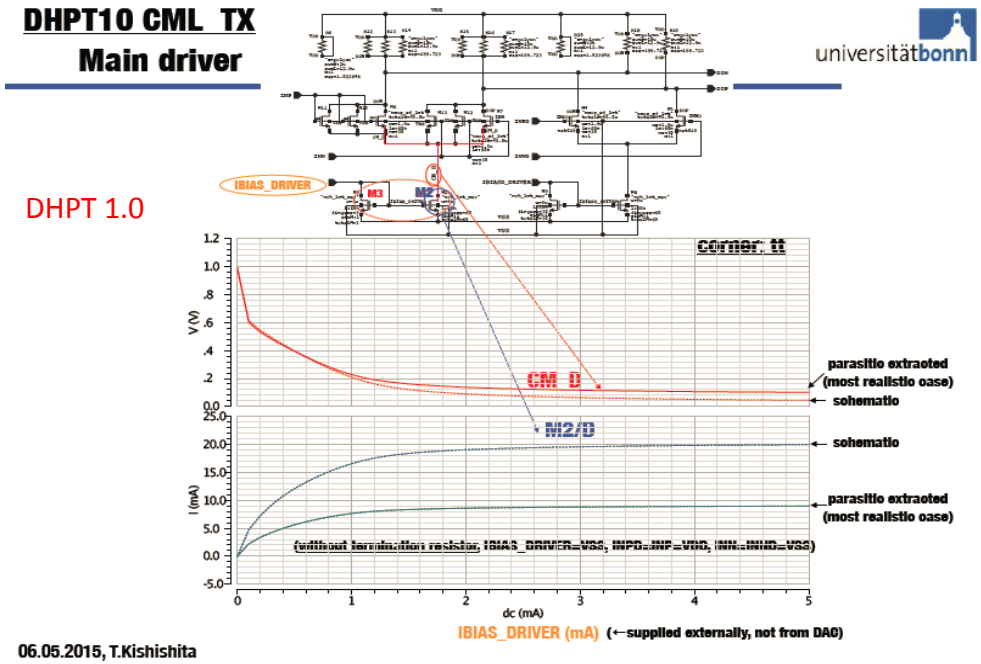
- Functional test (ongoing)
  - Functional test on probe station, test PCB, and hybrid 5
  - Issue with the data link synchronization needs to be understood

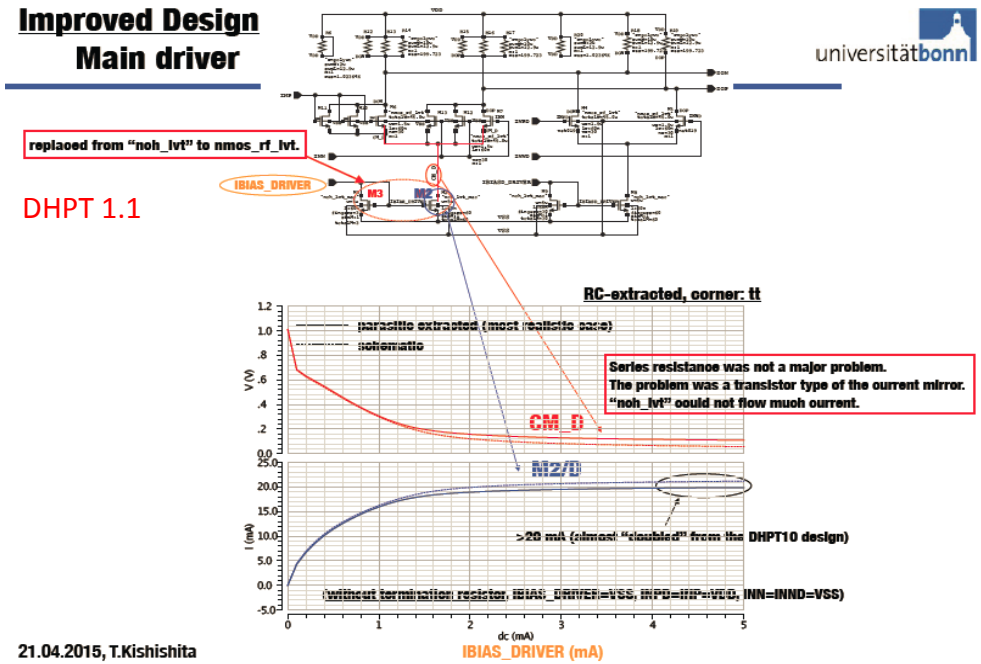
- Mass production/testing
  - Decision for DHPT 1.2 as the production chip
  - Then: Order of 9 additional wafers (1000 chips in total)
  - Two new needle cards for probe station testing are available
  - Estimated testing throughput: ~50 chips per week

BACKUP

DHPT CML Driver

- Changes from DHPT1.0 to DHPT1.1

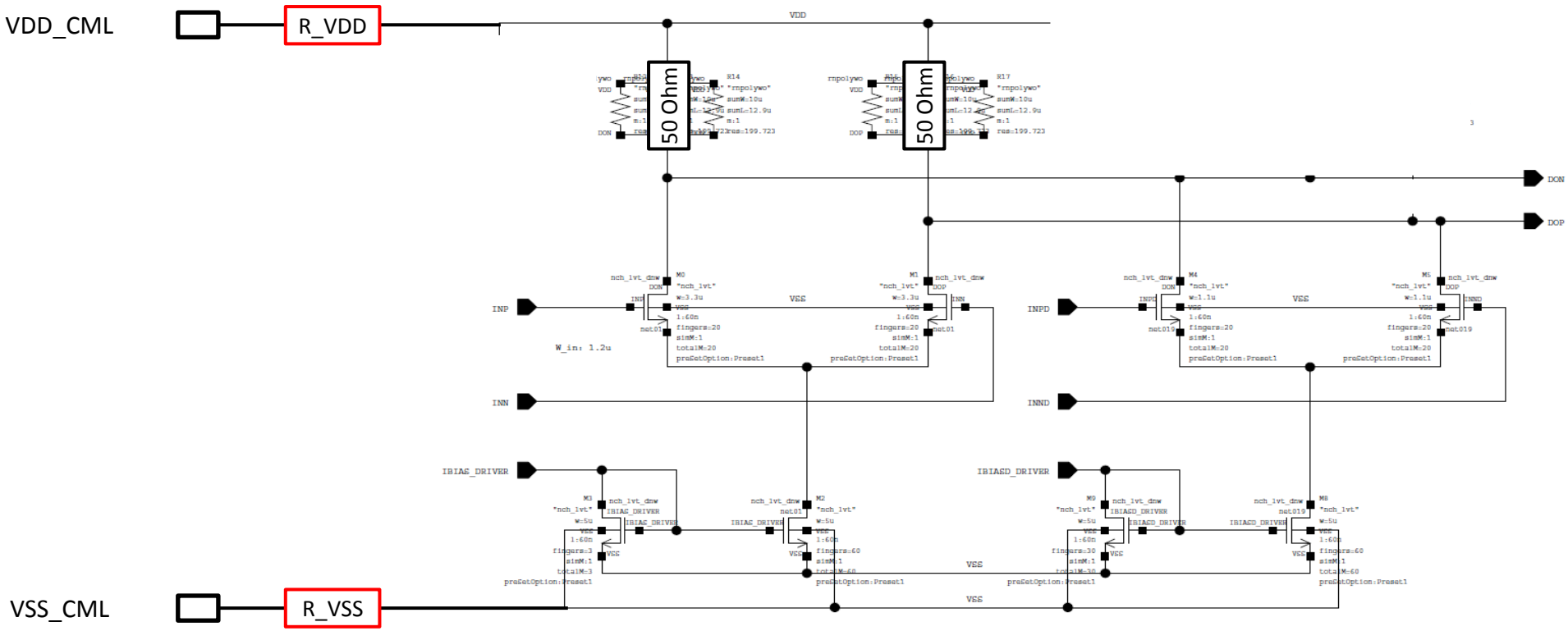




- Layout extracted with all parasitic elements
- Current in the main stage expected to be ~20mA after improvement of the transistor layout
- However measurements on DHPT 1.1 indicated ~10mA only

DHPT CML Driver

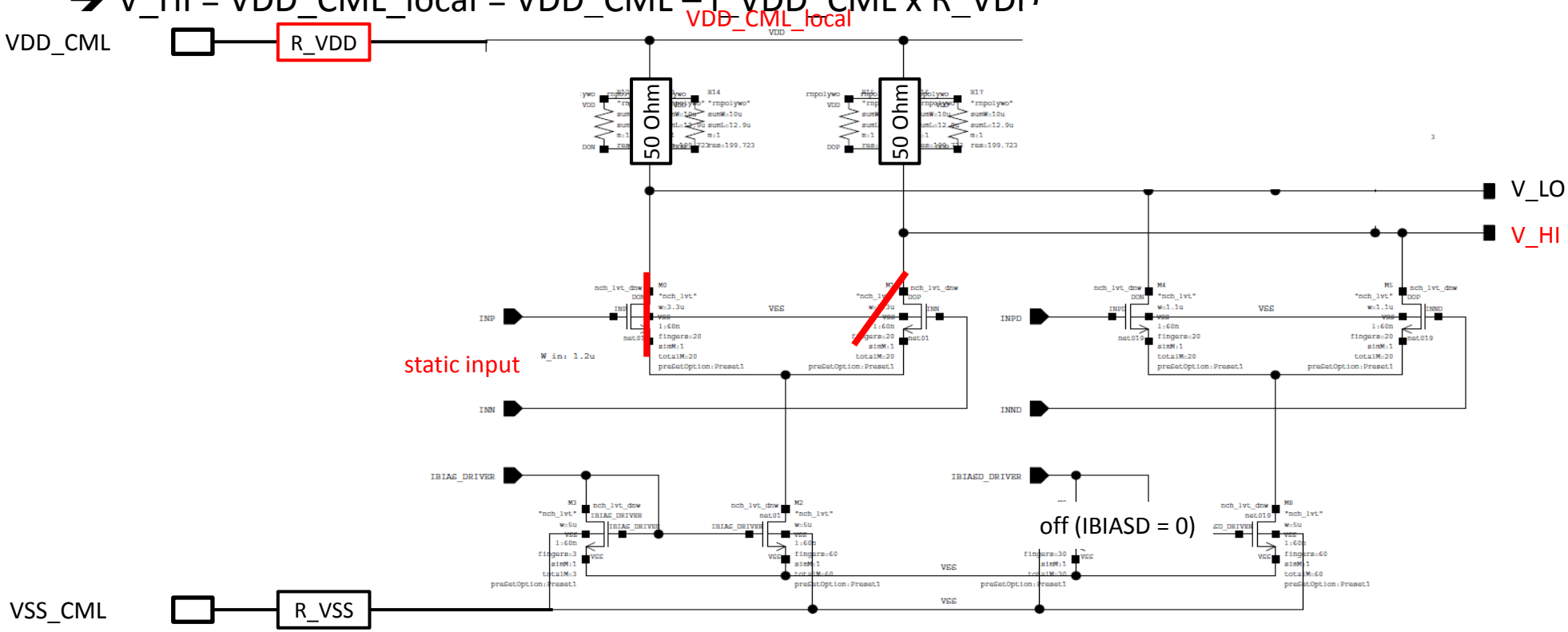
- Possible explanation: layout extraction underestimated the **parasitic** resistances R_VDD and R_VSS on the power lines



Measurement of the Parasitic Resistance R_VDD

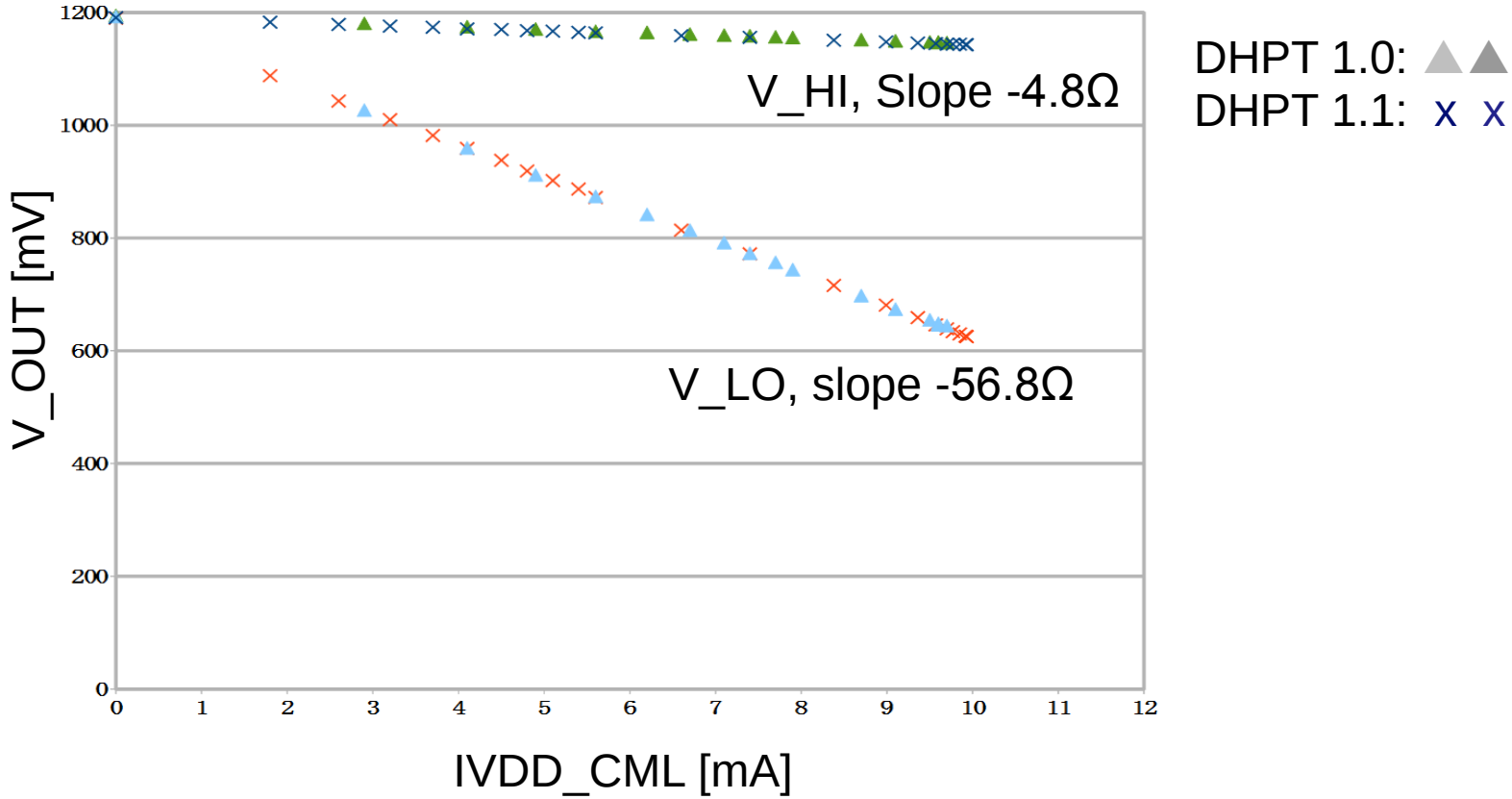
- Measure V_HI as a function of I_VDD_CML by changing IBIAS
  - no termination at driver output
  - no data line switching

➔ V_HI = VDD_CML_local = VDD_CML – I_VDD_CML x R_VDD



Measurement of the Parasitic Resistance R_VDD

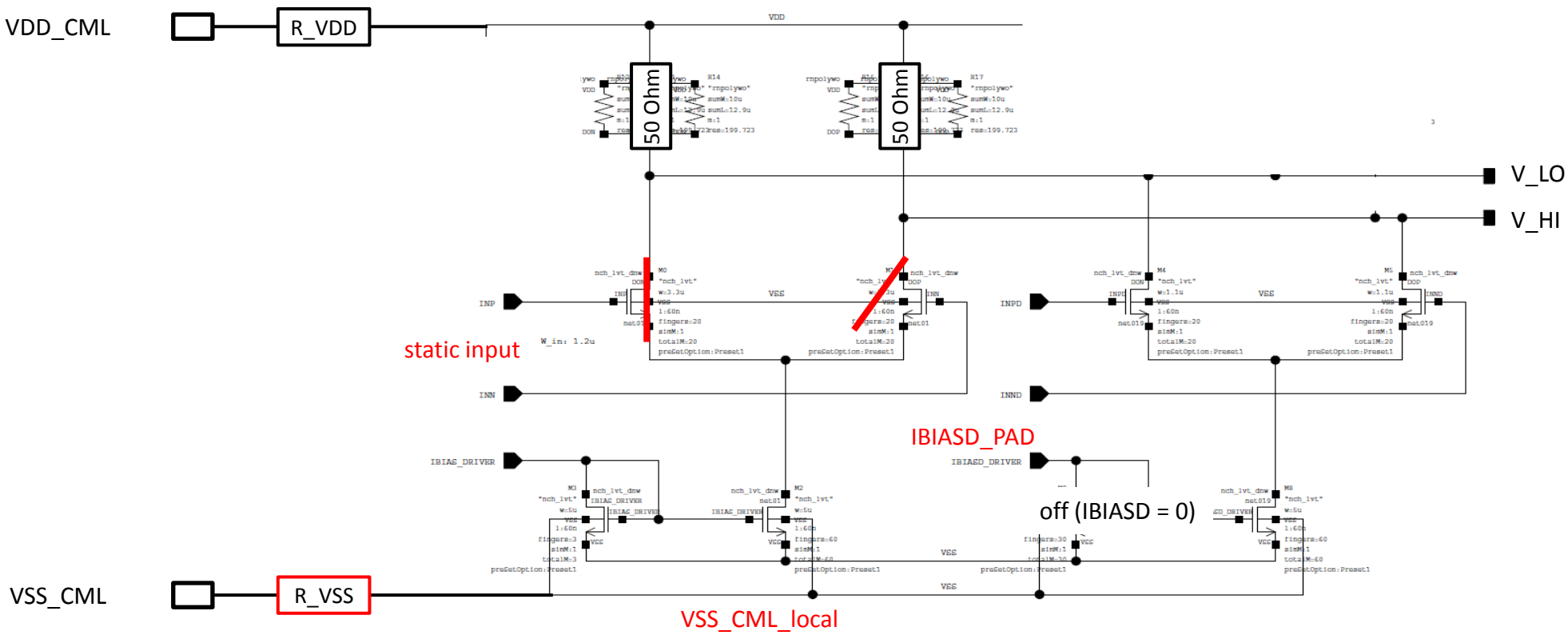
- Measurements indicate a parasitic resistance of about 5 Ohm in the VDD_CML line
- This is in agreement with the extraction of the parasitic elements of the layout, however this does not explain the loss of drive strength.



Measurement of the Parasitic Resistance R_VSS

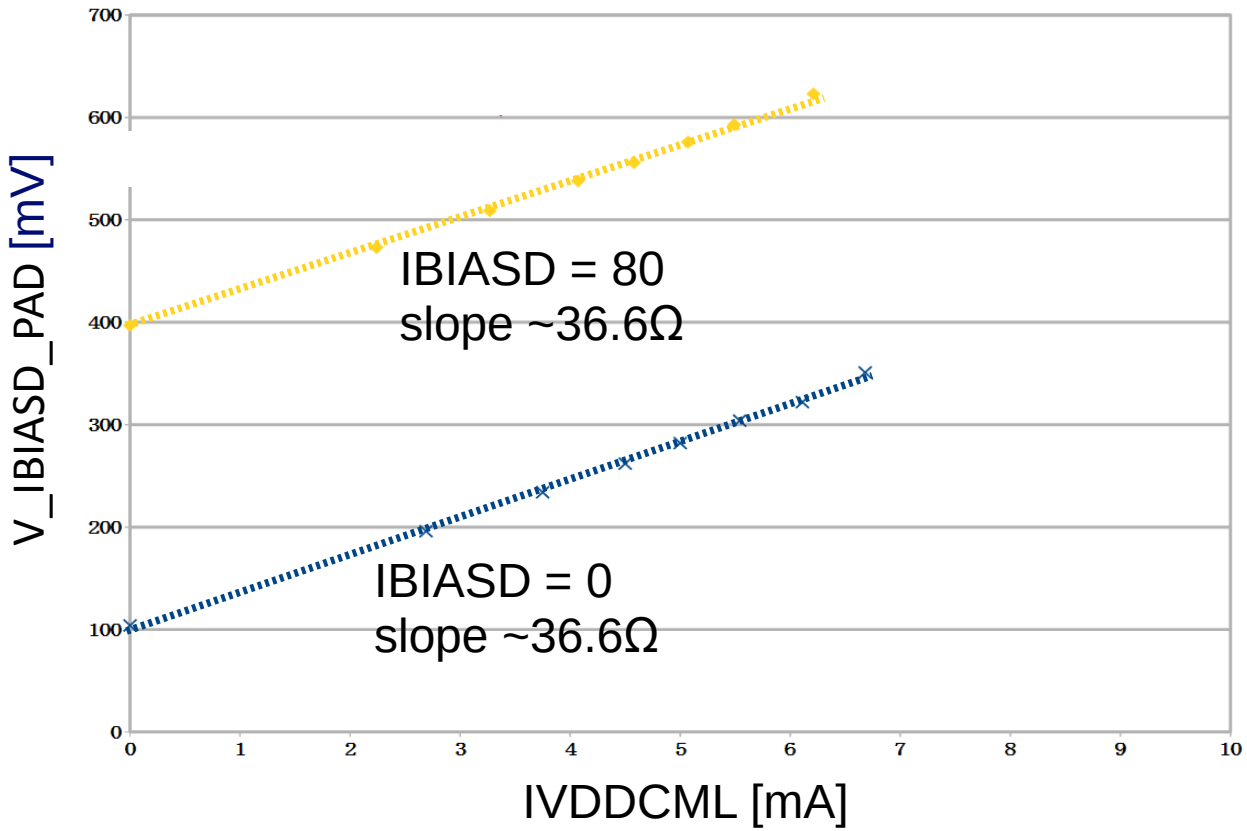
- Measure V_IBIASD_PAD as a function of I_VDD_CML by changing IBIAS, no termination at driver output

➔ V_IBIASD_PAD = VSS_CML_local + const = VSS_CML + I_VDD_CML x R_VSS



Measurement of the Parasitic Resistance R_VSS

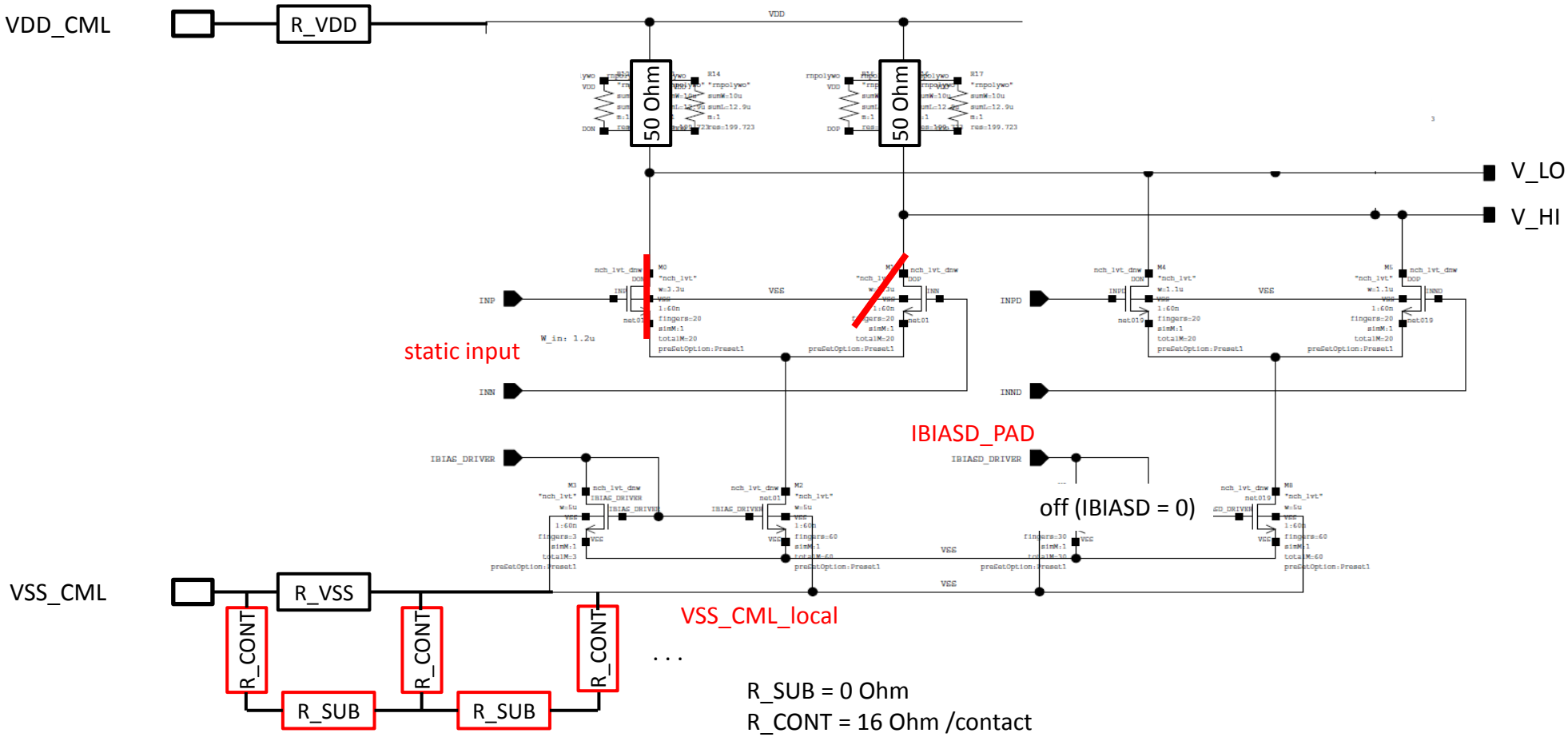
- Measurements indicate a parasitic resistance of about 36 Ohm in the VSS_CML line
- This is **not in agreement** with the simulation of the extracted layout which also shows ~5 Ohm parasitic resistance



Issue with the RC-extraction of the layout

- The extraction tool models the silicon substrate as a perfect conductor (R_SUB = 0 Ohm) and VSS_CML ins connected to the bulk with a lot of substrate contacts

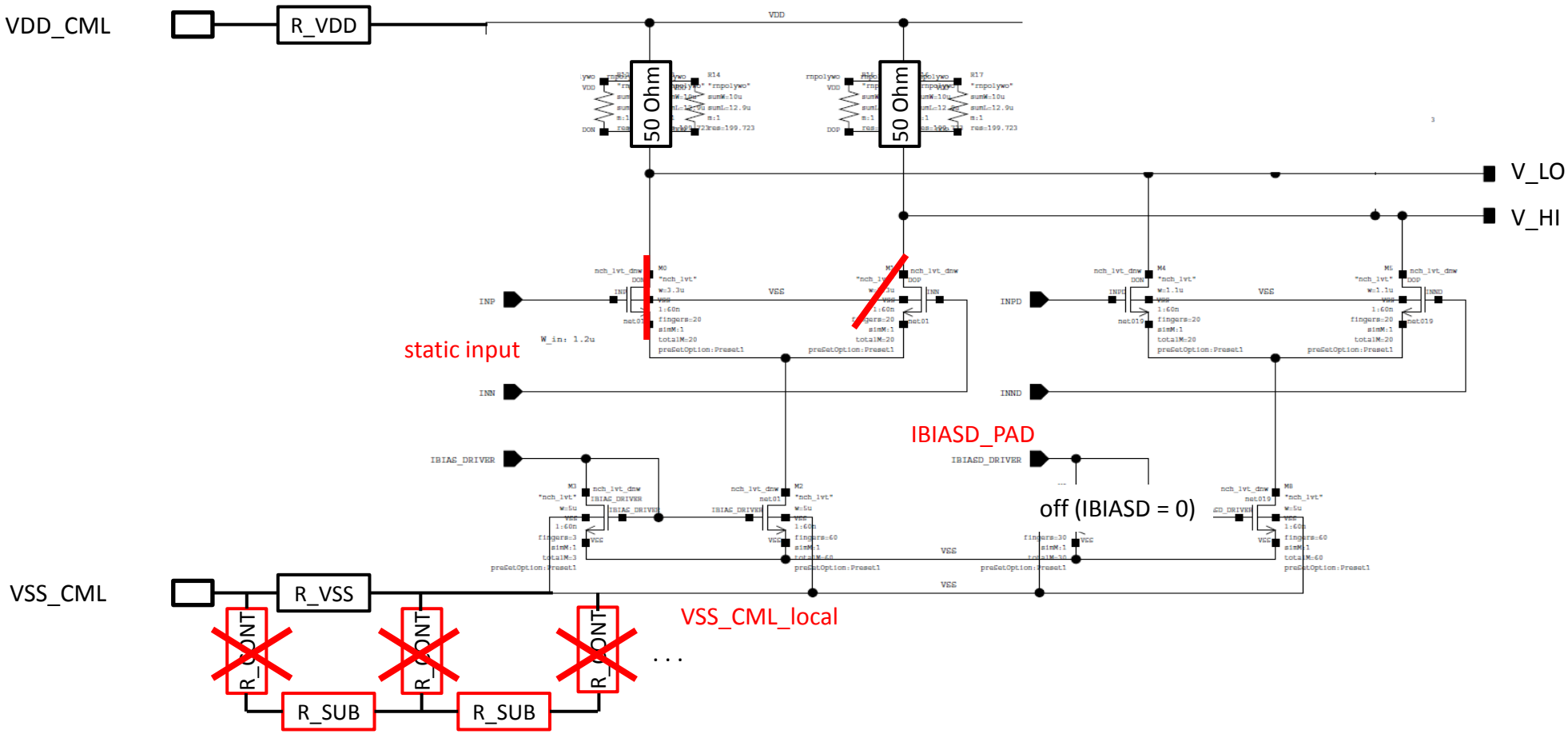
➔ Underestimation of the resistance in VSS_CML



Proof of the Explanation

- We removed the substrate contacts in the layout and extracted the parasitics again

➔ R_VSS_CML ~ 30 Ohm



CML_TX Layout toward DHPT12

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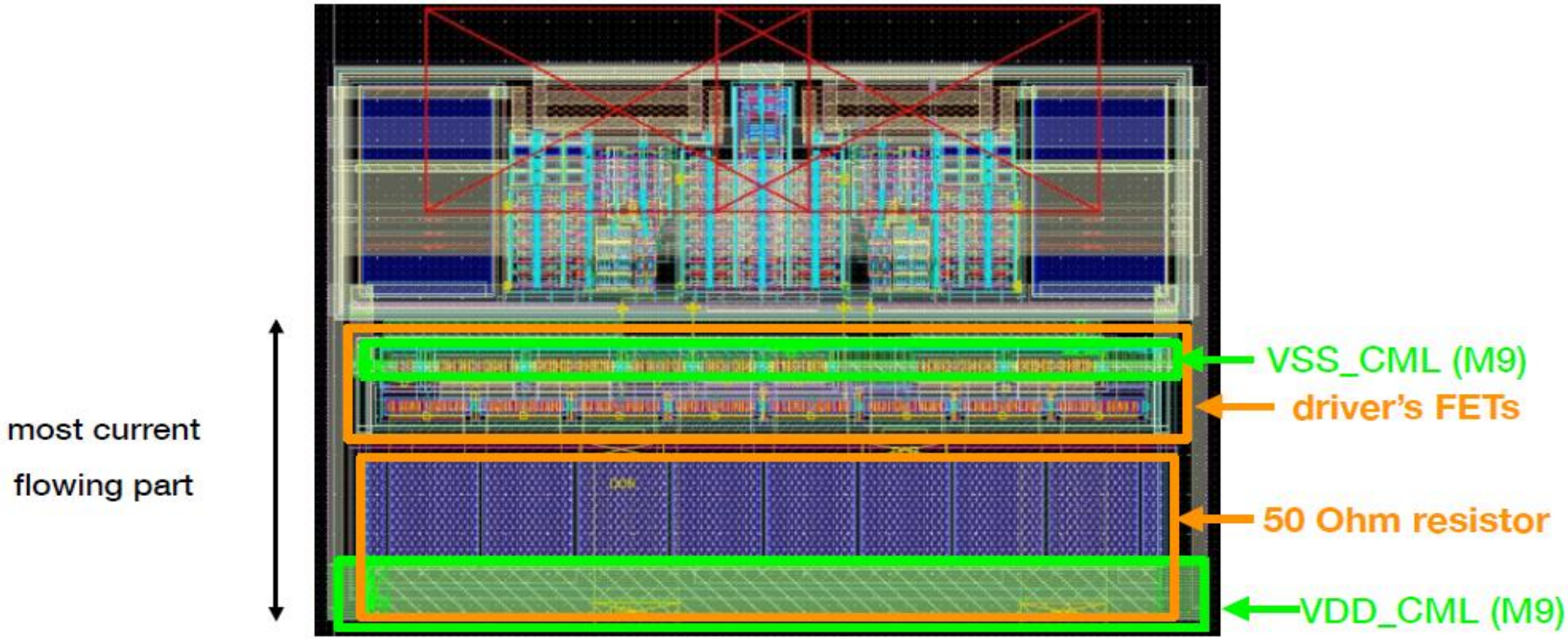
- vertical connection (M2→M9 for VDD_CML and M4→M9 for VSS_CML
- separate VSS and PSUB for Driver current mirror and switches
- avoid M1 connection between separate circuit blocks



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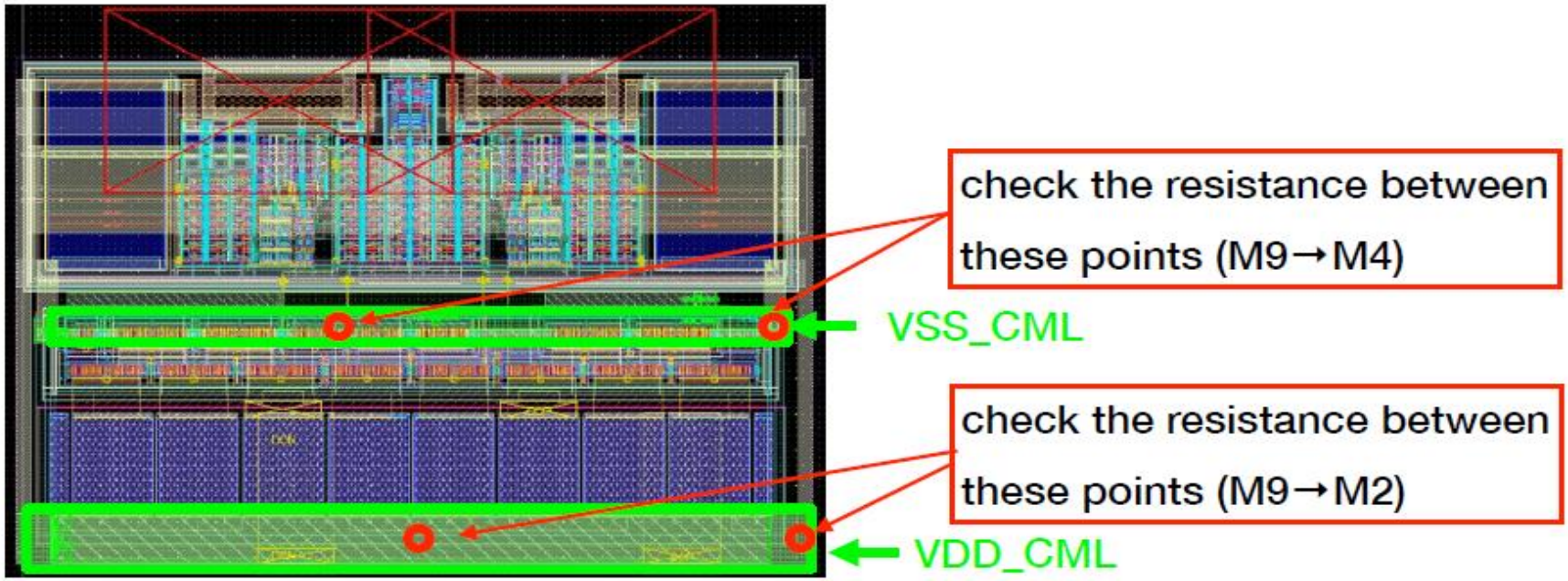
Serial-Resistance



	Assura, typical	Assura, worst	Calibre, typical
VDD_CML	49.3 mΩ	66.5 mΩ	53.0 mΩ
VSS_CML	114.1 mΩ	151.4 mΩ	115.2 mΩ

ΔR_{serial}: ~30% corner dependence, and ~10% between Assura and Calibre

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