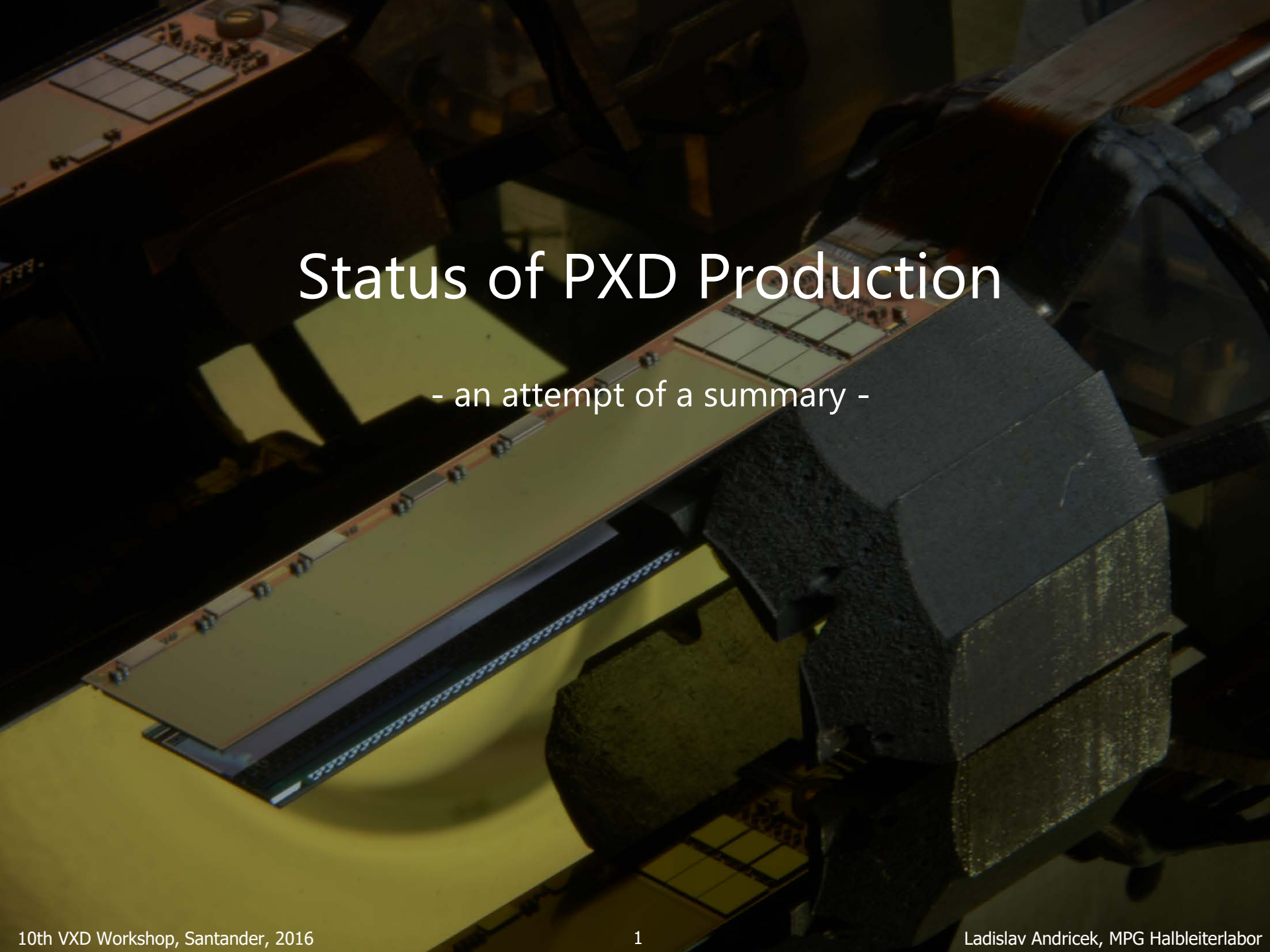


Status of PXD Production

- an attempt of a summary -

PXD Parallel Sessions on Wednesday

SC+DQM Overview
Santander

SL7-Testsetup
Santander

DHH Powersupply-Control Implementation
Santander

IPMI for ONSEN and DATCON
Santander

First experiences with EVB-DQM
Santander

BonnDAQ
Santander

Documentation: Whitebook
Santander

Status of PXD9 Production — *Rainer RICHTER*
Santander 09:30 - 09:50

Status PXD9 Probe Card — *Marca Josep BORONAT AREVALO*
Santander 09:50 - 10:10

PXD9 EMI Study — *Dr. Fernando ARTECHE*
Santander 10:10 - 10:30

Gated mode on H5 — *Carlos MARINAS*
Santander 11:00 - 11:20

PXD9 Gated Mode — *Dr. Eduard PRINKER*
Santander 11:20 - 11:40

PXD9 module testing preparations — *Felix MÜLLER*
Santander 11:40 - 12:00

DCDB4.x Analog Perfromance — *Mr. Philipp WIEDUWILT*
Santander 12:00 - 12:20

DCDB4.x Digital Performance — *Mr. Harrison SCHREECK*
Santander 12:20 - 12:40

DHPT1.2 Measurements — *Hans KRÜGER*
Santander 12:40 - 13:00

Status Switcher Bumping — *Laci ANDRICEK*
Santander 14:30 - 14:45

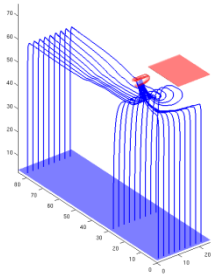
Testing ASICs at KIT — *Richard LEYS*
Santander 14:45 - 15:00

Power Supplies, Kapton & Cables — *Stefan RUMMEL*
Santander 15:15 - 15:35

DHH System and Optical Link — *Igor KONOROV*
Santander 15:35 - 16:00

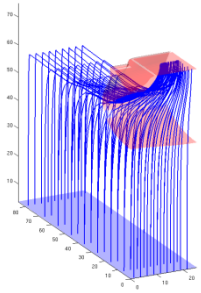
DEPFET shutter at SuperKEKB

Normal charge collection

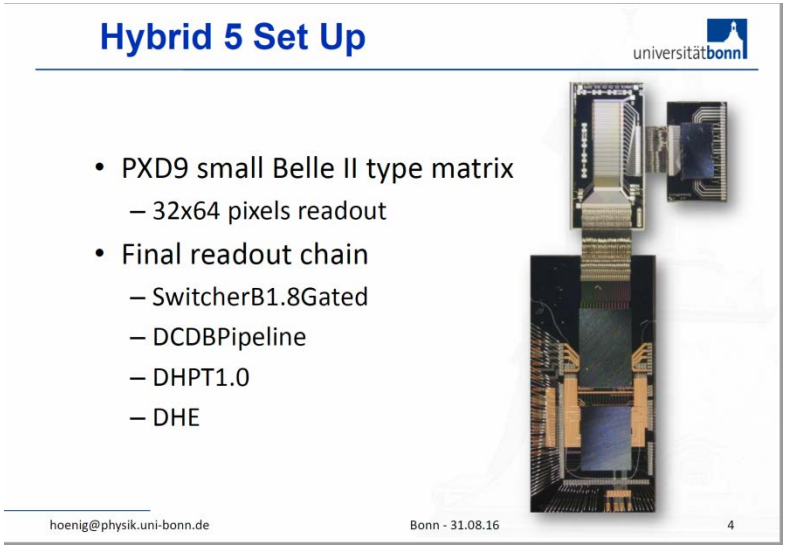


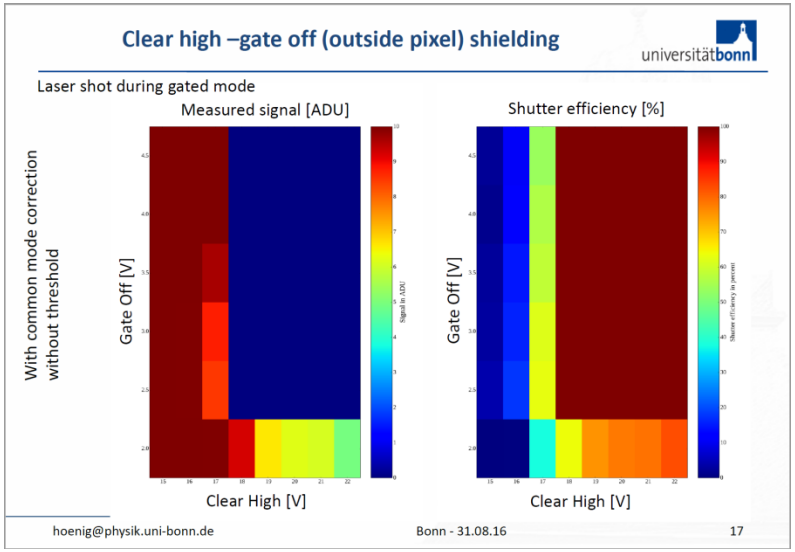
» Vgs=4V, Vclear=5V
» all signal charge collected in internal gate

Gated mode



» Vgs=4V, Vclear=20V
» all signal charge dumped to *Clear*

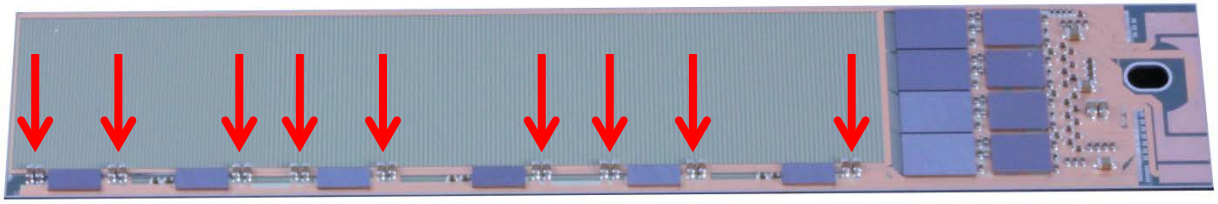




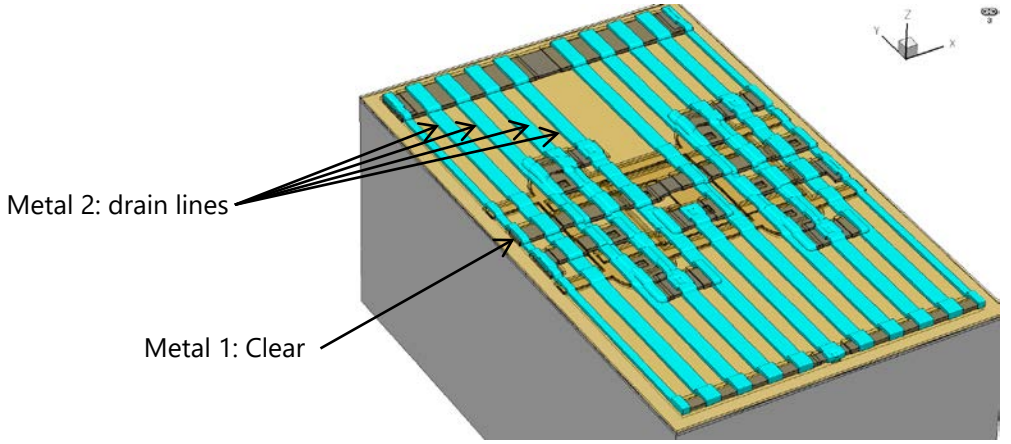
Challenge: switch all *Clear* contacts in the matrix from ~5V → ~20V
shown on small matrix, but as expected, it's more difficult on the pilot modules

Two main aspects of the gated mode

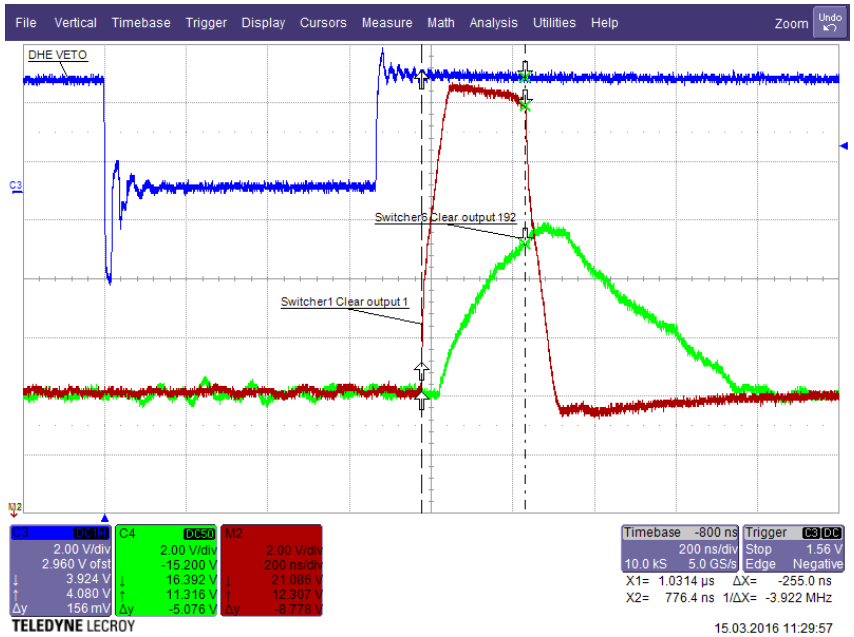
- **Fast switching of the clear signal (5V→20V)**
  - 26nF of the entire matrix → 135pF for one SWB channel (~4nF for one SWB)
  - To reduce peak current
    - Switch in groups: each SWB has **4 groups**, switched on and off consecutively
  - Provide current by local capacitors: each SWB has 100nF SMDs placed on the balcony

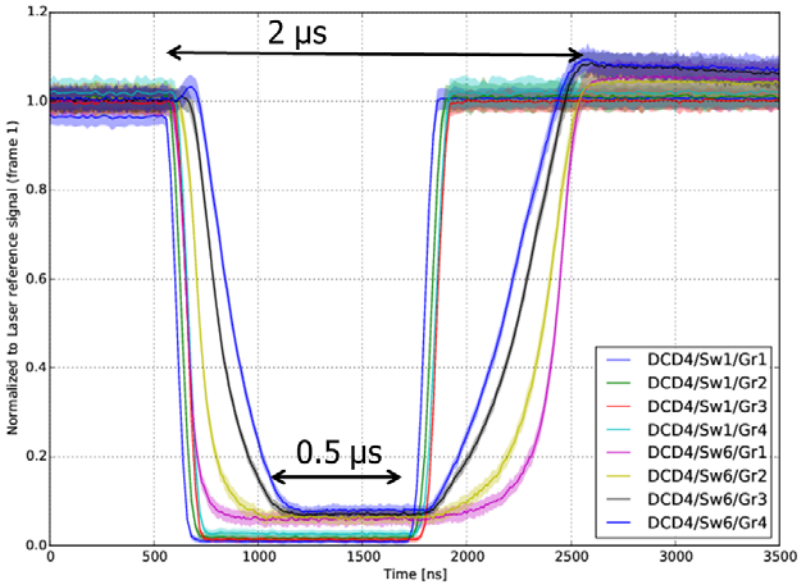


- **Analogue part of the DCD gets „upset“ during gated mode**
  - Capacitive coupling between Clear and Drain lines (input of the DCD)
  - Voltage drop on supply due to high transient currents



Direct measurement of the *Clear* pulse



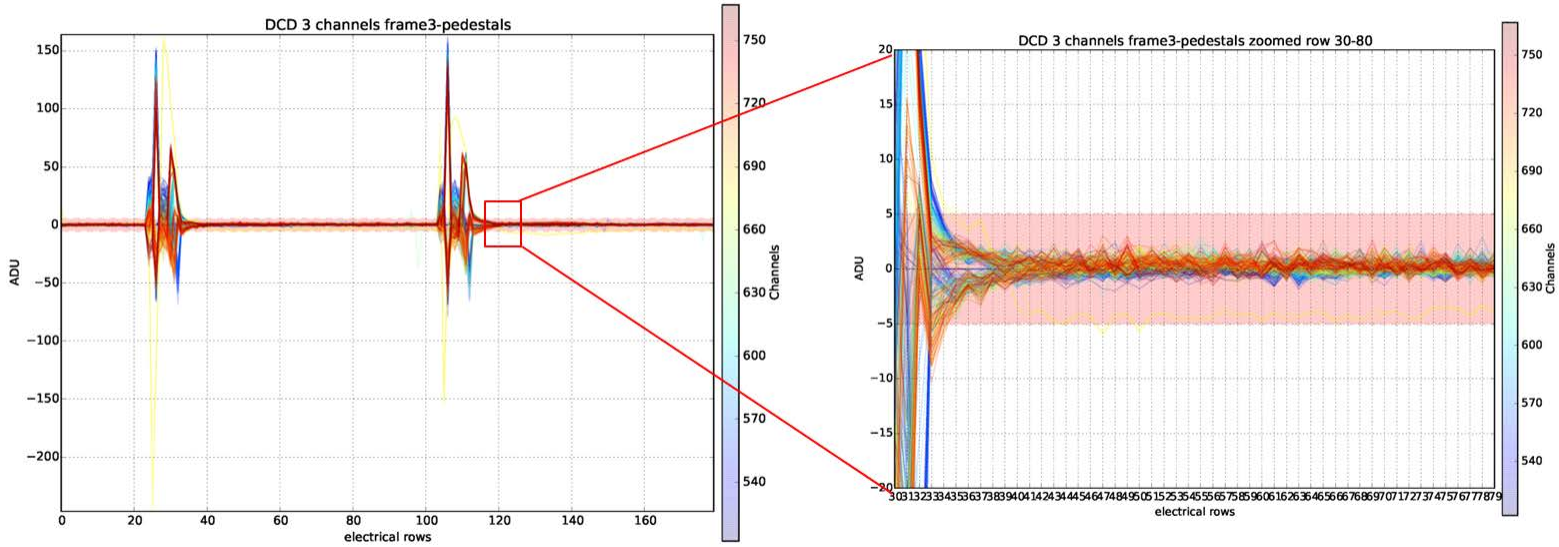


Two reasons for this identified

1. voltage drop along Vsub line on the balcony (SWB) causes worse behaviour of output driver of last SWB
2. poor quality of the decoupling caps on the balcony (minor influence..)

changes triggered by pilot module testing

- **Gated mode**
  - SWB V_sub net changes **– done**
  - Add more caps on Kapton, and possibly at docks patch panel – off-module, in progress



- **Standard operation**
  - Improvement of line/space for data lines between DCD/DHP **- done**
  - Reduction of line resistance of the SWB Clear strobe **- done**

- **No more modification of the on-module periphery required**
- **Continue sensor processing……..**

PXD9 Sensor Production: 29 Wafers

- PXD9-6: 3 wafers pilot run
  - First module assembly, DESY test, gated mode tests .....
- PXD9-7: 4 wafers pre-production
  - Lessons from pilot run incorporated (improved periphery routing)
  - Modules for Beast2, module pre-production ....
  - **Status: finished, ready for assembly**
- PXD9-8: 9 wafers, main production I
  - Final modules, in two sub-batches for copper process and thinning
  - **Status -8a: Phase III – back thinning done**
  - **Status -8b: Phase II – finished, ready for back thinning procedure, start phase III**
- PXD9-9: 6 wafers, main production II
  - Final modules
  - **Status: Phase II – Metal2 done, currently being measured on probe station**
- PXD9-10: 7 wafers, contingency...
  - **Status: Phase I finished -** in stand-by before Phase II, to start next week

PXD9-6 and -7 – pilot and pre-production

▷ Percentage of live pixels

	Pilot run			Pre-production			
	W30	W35	W36	**W31**	**W37**	**W38**	**W40**
IF	0*	98.44	98.96	98.8	98.4	98.8	100.0
OF1	100.00	98.44	98.96	99.0	98.1	0	99.5
OF2	99.48	98.96	99.48	99.0	0	0	99.3
OB1	97.72	99.40*	0	99.4	98.4	97.9	100.0
OB2	99.48	0	98.96	99.5	99.5	0	99.9
IB	97.92	0	99.48	100.0	99.0	99.0	100.0
Total	**83.3%**	**66.6%**	**83.3%**	**100%**	**83.3%**	**50%**	**100%**

**failure due to operator error during testing*

- **34/42 (80.1%) working sensors**
- **25/42 (59.5%) prime grade sensors (>99% pixels)**
- 9/42 (21.4%) second grade sensors

PXD9-8 – first production batch

▷ Percentage of live pixels

	W32	W33	W41	W42	W43	W44	W45	W46	W47
IF	100	0	99.5	99.3	100	99.0	99.5	99.5	99.5
OF1	99.5	100	99.5	0	100	100	99.5	100	98.5
OF2	100	100	0	100	0	100	100	99.9	0
OB1	0	100	0	99.5	0	99.0	0	99.5	0
OB2	100	0	0	100	99.9	100	100	100	0
IB	100	0	100	100	100	100	100.	99.5	99.5
Total	**83.3%**	**50%**	**50%**	**83.3%**	**66.7%**	**100%**	**83.3%**	**100%**	**50%**

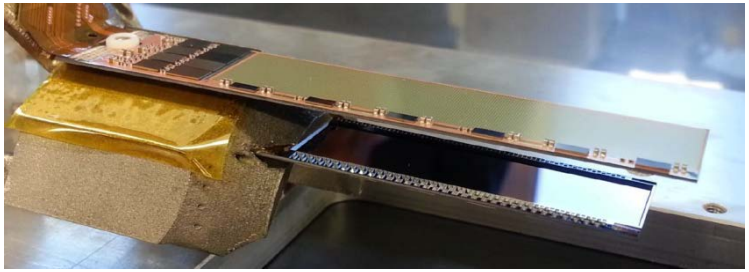
Combined production run yield PXD9-7 and -8

- **74/96 (87.5%) working sensors**
- **64/96 (66.7%) prime grade sensors (>99% pixels)**

Yield is better than expected already now enough sensors for phase 2 and 3!

ASICs

- April beam test at DESY was done with:
  - DCDB4: "old" DCDBpipeline with known minor shortcomings
  - DHPT1.1: latest DHPT submitted autumn 2015
  - SwitcherBv2.0: last samples of the "old" version

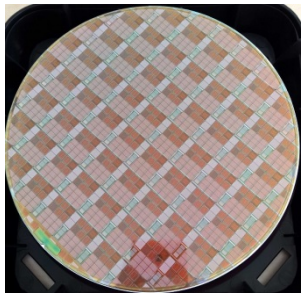


- Main issues with this chip set
  - Data transfer problems between DCD and DHP
  - Off-Module data transfer (DHP related)
  - **Still: successful and stable operation in the beam at 20% lower frame rate**

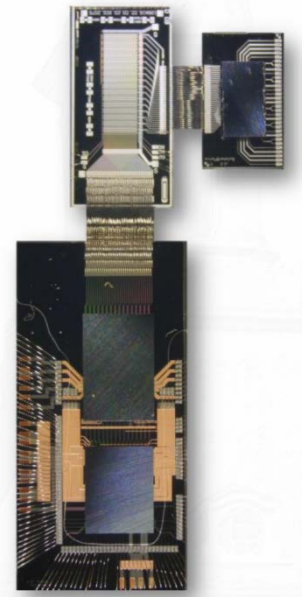
- New (final) chip versions to overcome communication and stability problems
  - DCDB4.1 and DCDB4.2
  - DHPT1.2
  - SwitcherBv2.1

DCDB4.1 and DCDB4.2

DCDB4.1 features:



- ▷ Parallel sampling mode for probe tests at full speed via JTAG, needle pads
- ▷ Programmable LVDS current (2 levels)
- ▷ Programmable RefLVDS (2 levels, normal and by ~30mV increased)
- ▷ Gain settings and other minor adjustments



DCDB4.2 features:

- ▷ Same as DCDB4.1
- ▷ Additionally new test pattern for better data transfer adjustment
- ▷ And changed layout of ADC transistors to avoid “long codes”

:- Both chip types are positively tested on the probe station at KIT
at Bonn and Goettingen
:- comprehensive test programme on H5 paired with DHPT1.1/SWB2.1 and DEPFET matrix

DCDB4.x Analogue Performance

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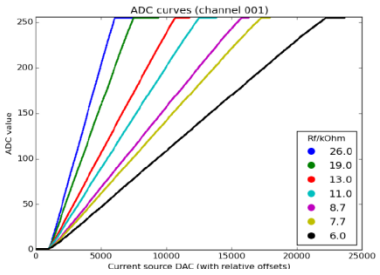
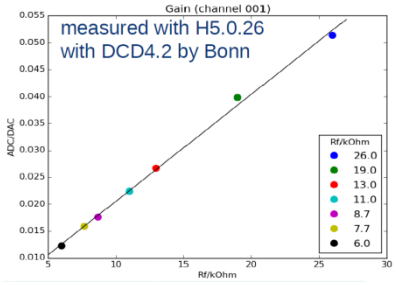
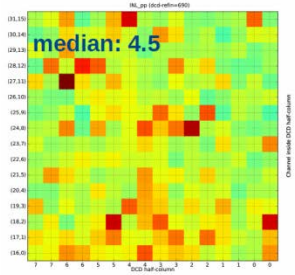
DCD4.x Testing Procedure

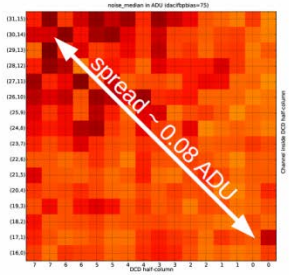
- test DCD4.1 and DCD4.2 functionality on Hybrid5 level
- confirm that stable operation is possible with both DCD designs
  - check correct implementation of gains ✓
  - check that ADCs operation can be optimized within specifications
    - INLpp < 8 ADU within +-100 ADC ✓
    - noise < 1.0 ADU ✓
    - no long codes above 6 ADU ✓
    - no bit errors visible in ADC curves ✓
    - gains should be homogeneous among all DCD channels ✓
      - adjust with new IPSourceMiddle DAC ✓



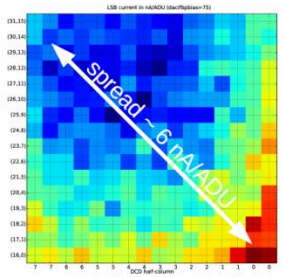




INLpp < 8 for all channels



noise < 0.55 for all channels



min to max gain variation ~10%

Sr90 spectra: DCDB4.1/DHPT1.1/SWB2.1 +PXD9

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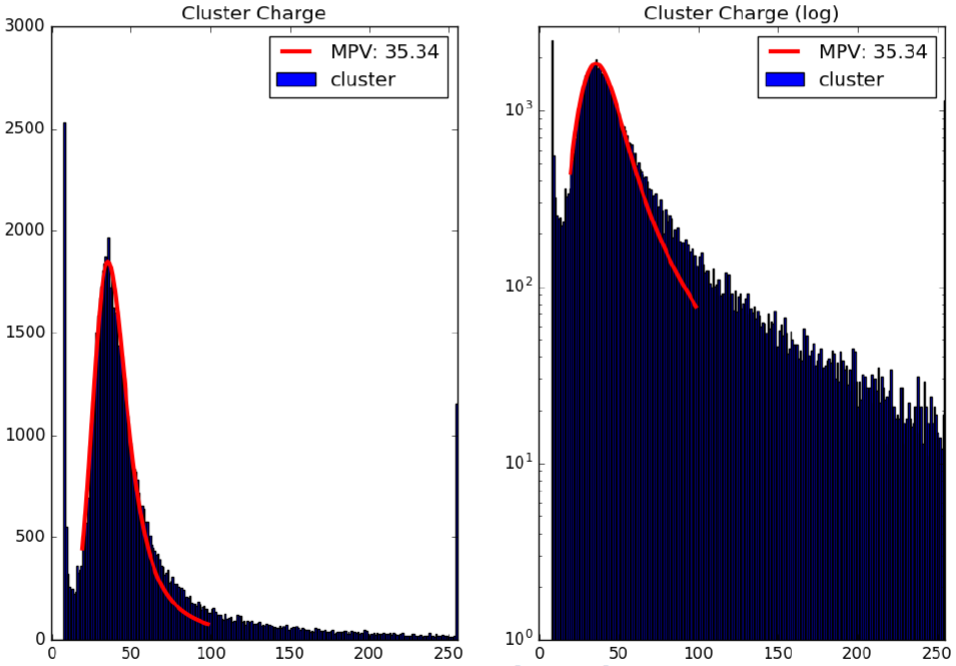
Sr90 Signal Spectrum

- Sr90 spectrum measured with H5.0.24 with **DCD4.1** at gain En60
- done with ACMC and 2bit DAC offset at full speed (GCK 76MHz)!

H5.0.024 with **DCD4.1** at 76MHz and En60 gain

SWB18v2



MPV = 35.34 ADU

SNR = 56.13

gate length = 5 µm

g_q ~ 780 pA/e

Sr90 spectra: DCDB4.2/DHPT1.1/SWB2.1 +PXD9

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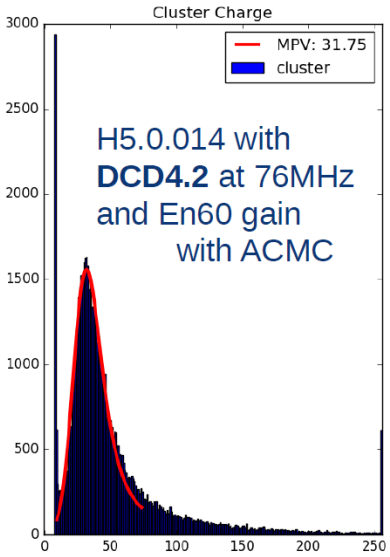
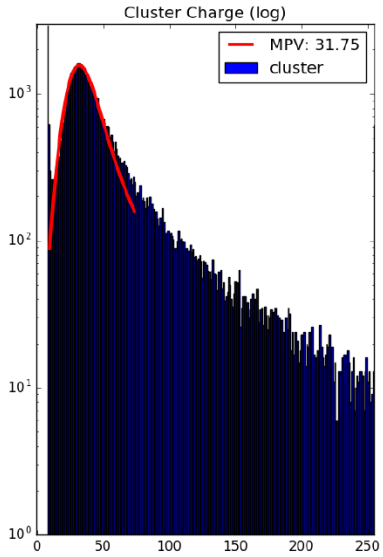
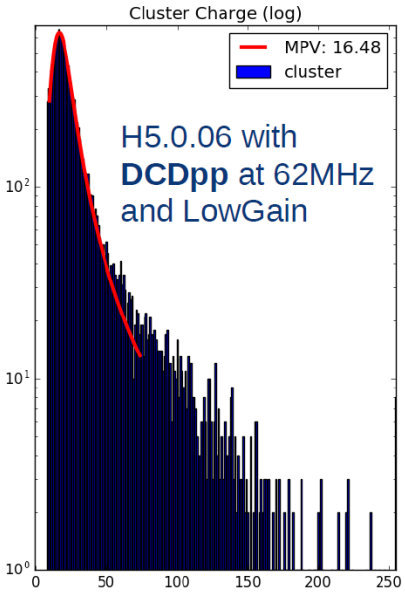
Sr90 Signal Spectrum

- Sr90 spectrum measured with H5.0.14 with **DCD4.2** at gain En60
- compare to DCDpp measurement







MPV = 31.75 ADU

SNR = 57.73

gate length = 5 µm

g_q ~ 730 pA/e

MPV = 16.48 ADU

SNR = 30.52

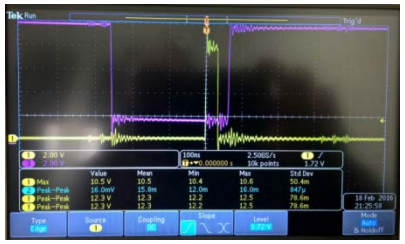
gate length = 6 µm

g_q ~ 380 pA/e

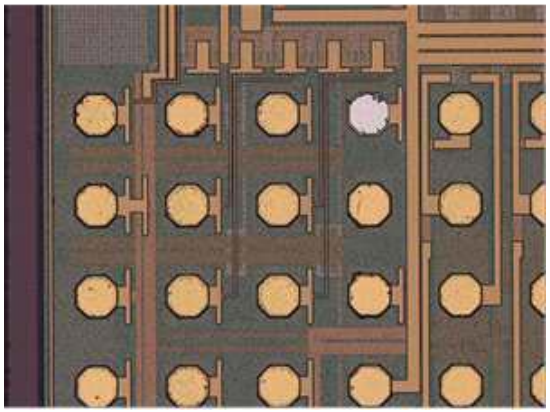
Final chip: decision to equip Phase 2 modules with DCDB4.2
Pre-testing on probe station scheduled

SwitcherBv2.1

- SwitcherBv2.1 is positively tested on probe station and on hybrid level
  - Chips work as expected
  - First samples bumped and placed on pilot module (DCDB4 and DHPT1.1)
  - In operation with DCDB4.x on H5 level (see previous slides..)
  - Additional 500 chips received from foundry



- Bumping (UBM process) causes problems with the new Switcher
- On one pad – the substrate pad – and only on this pad
  - Very little or no Nickel deposition



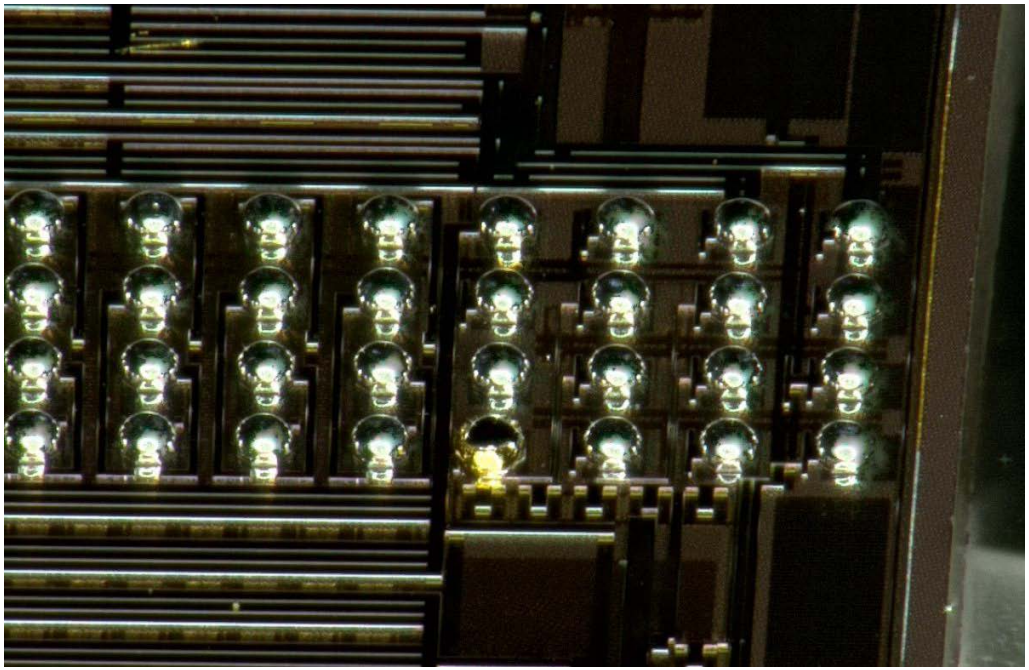
- Main difference to old Switcher
  - Chip is wider…
  - Different passivation (1µm Nitride/Oxide <-> PI)
  - Guard ring of the chip exposed, connected to bulk

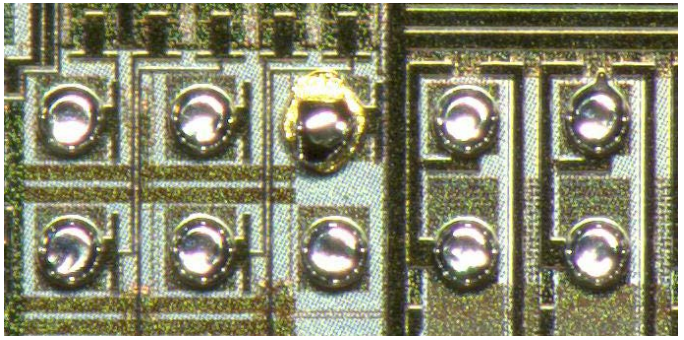
→ Different electrochemical potential causes reduced Ni growth on substrate

→ Solution: isolate chip edge! First trials by manual coating chip by chip …
  - → **Successful but very time consuming process with bad yield**
  - → **Batch process established, successful first trial, but failed finally due to process instabilities**

Repair: single pad balling

- Selected optically good chips
- It worked – sort of…

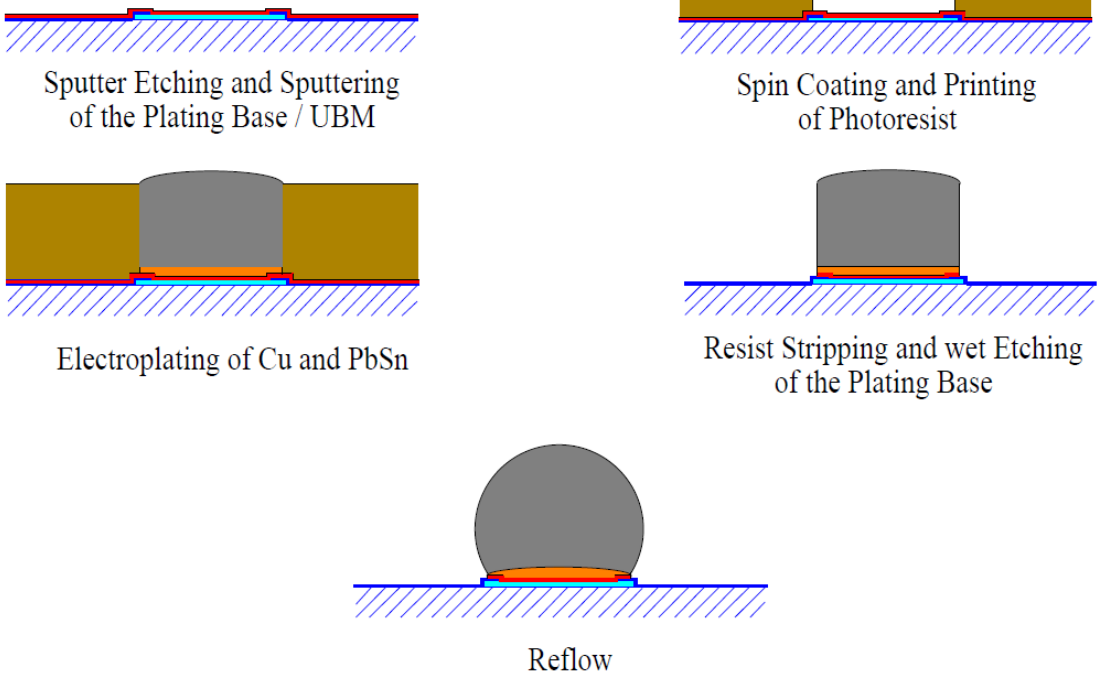




- Balls are all about 40-50 µm, as the others
- Mostly central ….
- Need for testing → KIT
- Have now: 16 Au-stud chips, 12 from first batch w/ manual PR coating

Bumping on “wafer level” at IZM

- Assemble a “wafer” by pick-and-place of Switchers to support with alignment marks
  - Accuracy ~few microns, subsequent wafer level lithography possible
  - Possibility to apply standard technology bumping by electro-plating



- Tests at IZM are ongoing … litho processes to be done this week

DHPT1.2

- DHPT1.2 submitted April 27 to correct two minor bugs in the DHPT1.1
  - Improvement of the long term reliability of the off-module driver (CML)
  - Better definition of the clock phase at start up

- 100 chips received of July
  - Probe station tests
  - Assembly of H5 with DCDB4
  - **Testing is ongoing….**

Bugs fixed in DHPT 1.2

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CML Driver

Test Results

- CML driver power routing
  - Ground rail (VSS) had a too high wiring resistance (~30 Ohm), parasitic extraction did not spot this because of substrate model
  - Rerouting of power nets → R_{VSS} < 0.2 Ohm

✓

- CML driver bias routing
  - Removed ESD resistor in bias connection and reduced parasitic resistance → increase of bias current, less sensitivity to voltage supply

✓

- Internal system clock phase
  - The core clock started with an arbitrary phase after power-on
    → added controlled reset (delayed GCK) to the internal clock divider

✓

CML Performance Comparison

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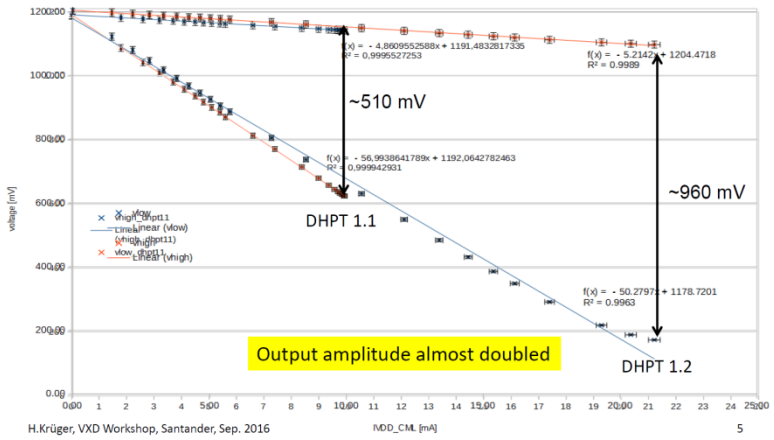
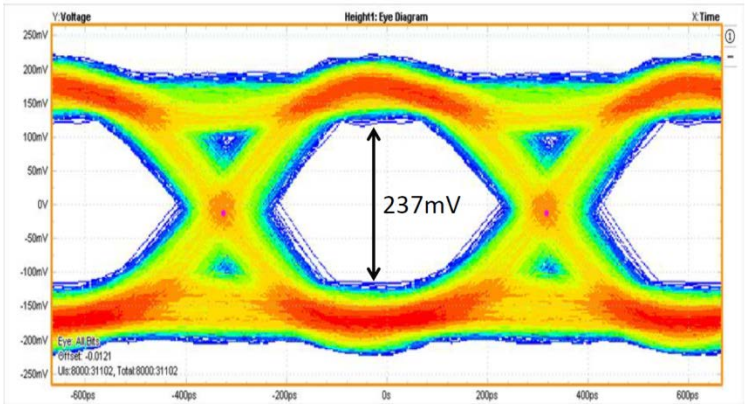
- CML output high and low level as a function of IBIAS (w/o termination)

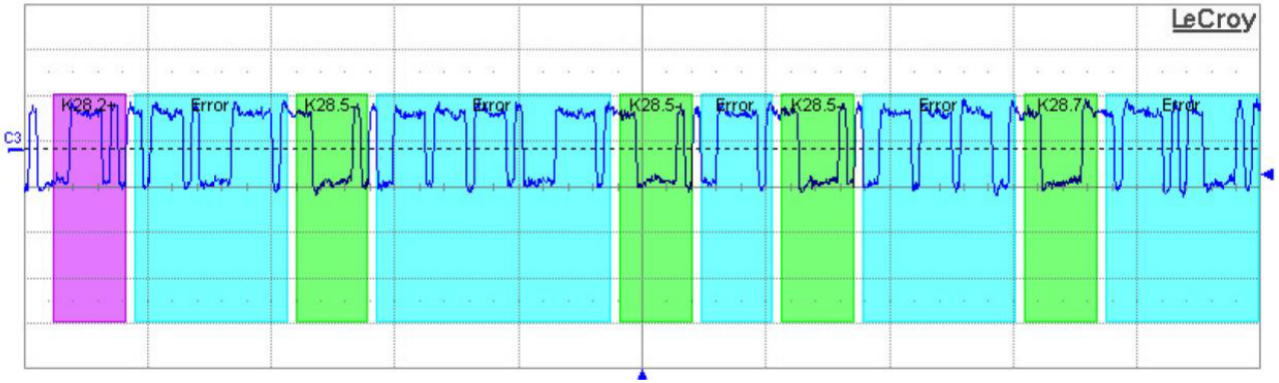




▷ **Testing is ongoing….**

Data Link Synchronization

- We have seen an issue with the data link between DHE and DHPT 1.2
- DHPT 1.2 puts out invalid symbols → link does not synchronize



DHPT 1.2 data link @ DHE

- Very recent finding, need to cross-check with DHH emulator
- Behavior not reproducible in simulation (full layout, all corners)

:- no final conclusion yet
:- two more weeks for evaluation, then decide which chip to place on Phase 2 modules
:- fall-back: DHPT1.1

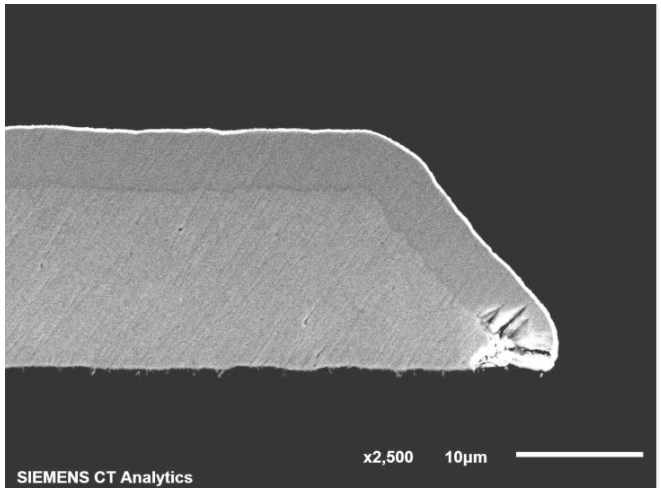
Kapton cable

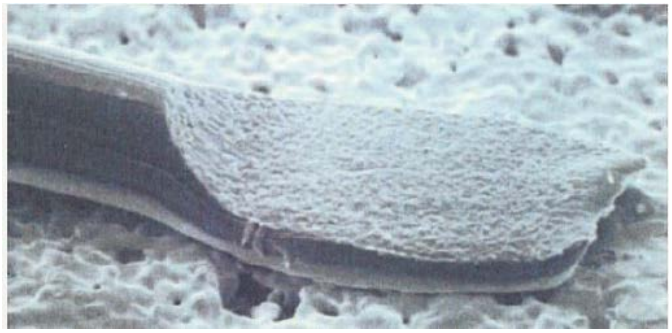
- Slight quality issues with Taiyo, but mostly the costs forced us to qualify a new vendor
- Prototyping was done, testing included
  - ↳ Electrical, mechanical, metallurgy, bondability …

Criteria

Criterium	Taiyo – L2bwd V1.1, L1bwd V2.0 2015-05, 2016-03	Kaupke – L1fwd V2.0 2016-03
Mechanics		
• X-Y Dimensions	• OK	• OK
• Z Dimension flex	• 300 µm, 430 µm at vias at bond area	• OK (350 µm)
• Z Dimension rigid	• OK (1 mm)	• OK (1 mm)
Material		
• Quality of bond pads	• Fair in latest production	• OK
• Pull-Test on bond wires	• OK (4.9 g)	• OK (6.1 g)
• Shape after bending	• Some deformation	• Some deformation
• Damages after bending	• OK	• OK
Electrical		
• R of power lines (130 µm)	• 10.8 Ω/m	• 8.5 Ω/m
• R of diff. lines	• 16.4 Ω/m	• 17.3 Ω/m
• Z of diff. lines	• ≈ 90 Ω	• ≈ 93 Ω
• Attenuation of diff. lines	• 11.7 dB/m	• 10.2 dB/m
Logistic		
• Production Time	• 6 – 8 weeks	• 6 – 8 weeks
• Test Protocol	• Partly unclear, Z0 per lot	• Promised: E-Test + Z0

M. Fras, MPI for Physics, Munich — Belle-II PXD9 Kapton Cable: Taiyo vs. Kaupke — 21 Apr 2016 / Page 2





:- 5 sets of kapton cables received
:- layout improved (only one connector on patch panel)

Ladder assembly procedure

Flip Chip of ASICs (~240°C):

- Bumped ASICs have the same solder balls (SAC305)
  - ↳ DHP bumping at TSMC, DCD bumping via Europractice
  - ↳ SWB bumping on chip level at IZM Berlin
- Flip Chip of PXD modules at IZM Berlin

SMD placement (~200°C):

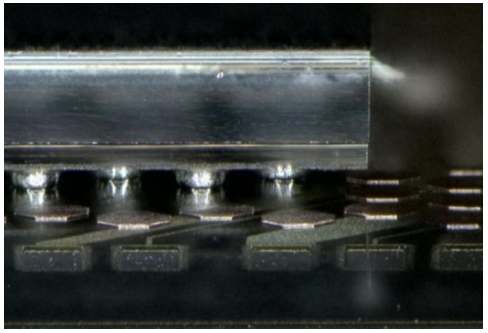
- Passive components (termination resistors, decoupling caps)
- Dispense solder paste/jetting of solder balls, pick, place and reflow
  - ↳ PbSn 37/63 solder

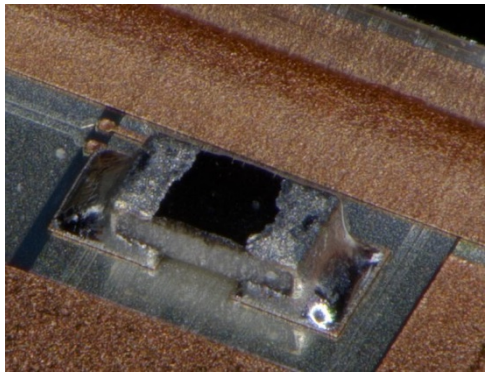
Kapton attachment (~170°C), wire bonding:

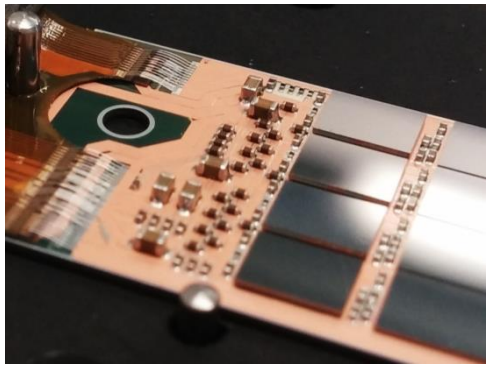
- Solder paste printing on kapton,
  - ↳ SnBi solder
- Wire-bond, wedge-wedge, 32 µm Al bond wires

Ladder gluing:

- Manuel procedure established
- Qualification of automated assembly pending







An incomplete list of topics I'm not covering here

There are many other important topics towards next DESY test, phase 2, and beyond

- ▷ EMI tests have been done at ITAinnova

- ▷ Power supplies are in production, first units are already available
- ▷ For power cables, a new more reliable vendor with agreed QC has been found
- ▷ Test systems for series module testing in construction
- ▷ …

Summary

- Sensor production ahead of schedule
  - Yield better than expected….
- New versions of DCDB4.x fully functional
  - Ready for Phase 2 module assembly after pre-test
- New SWBv2.1 fully functional
  - Tested on H5 level
  - Issue with bumping on chip level, necessity to change technology →IZM
  - Bumped chips for phase 2 modules are being pre-tested on probe station
- DHPT1.2 still under test
  - Off-module link shows initial problems with synchronization to DHH system
  - Under investigation
- Start Phase 2 module assembly as soon as SWB2.1 and DCDB4.2 pre-test are done
  - Expected to be in 2-3 weeks
  - If DHPT1.2 not ready, use DHPT1.1
  - Goal: have all modules available mid November

Schedule spring 2016