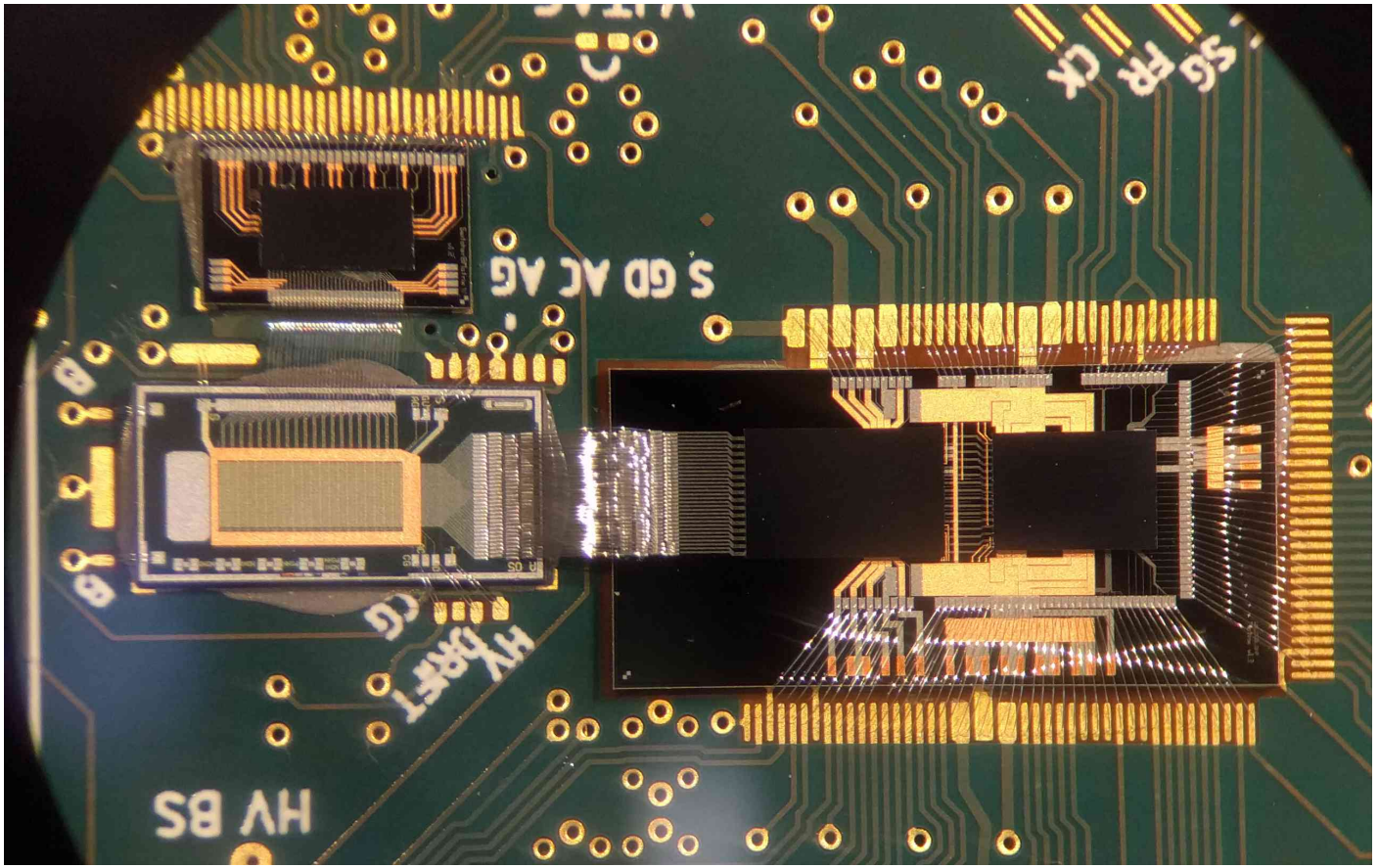
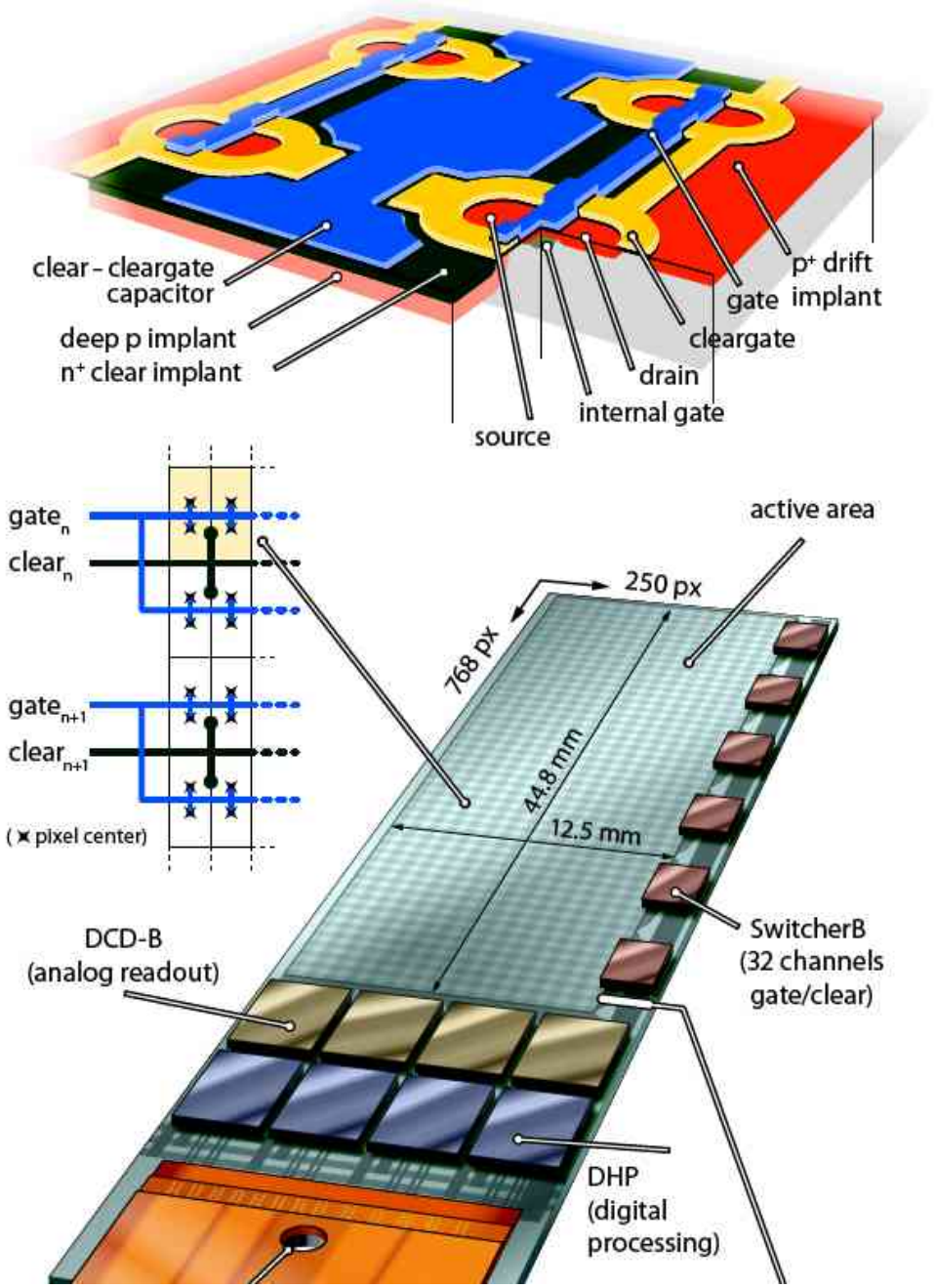
H5_0_24 with DCDB4.1

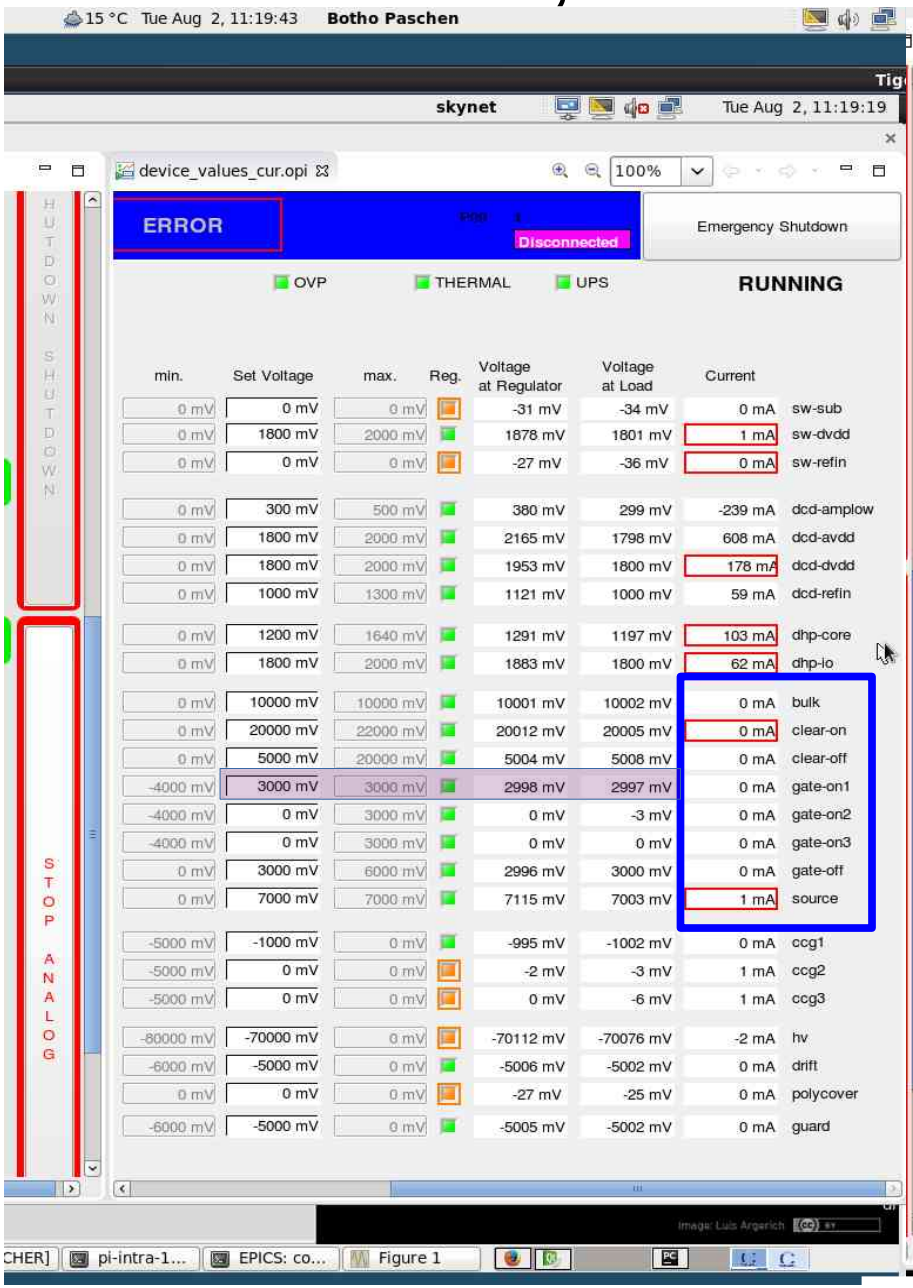


DEPFET matrix

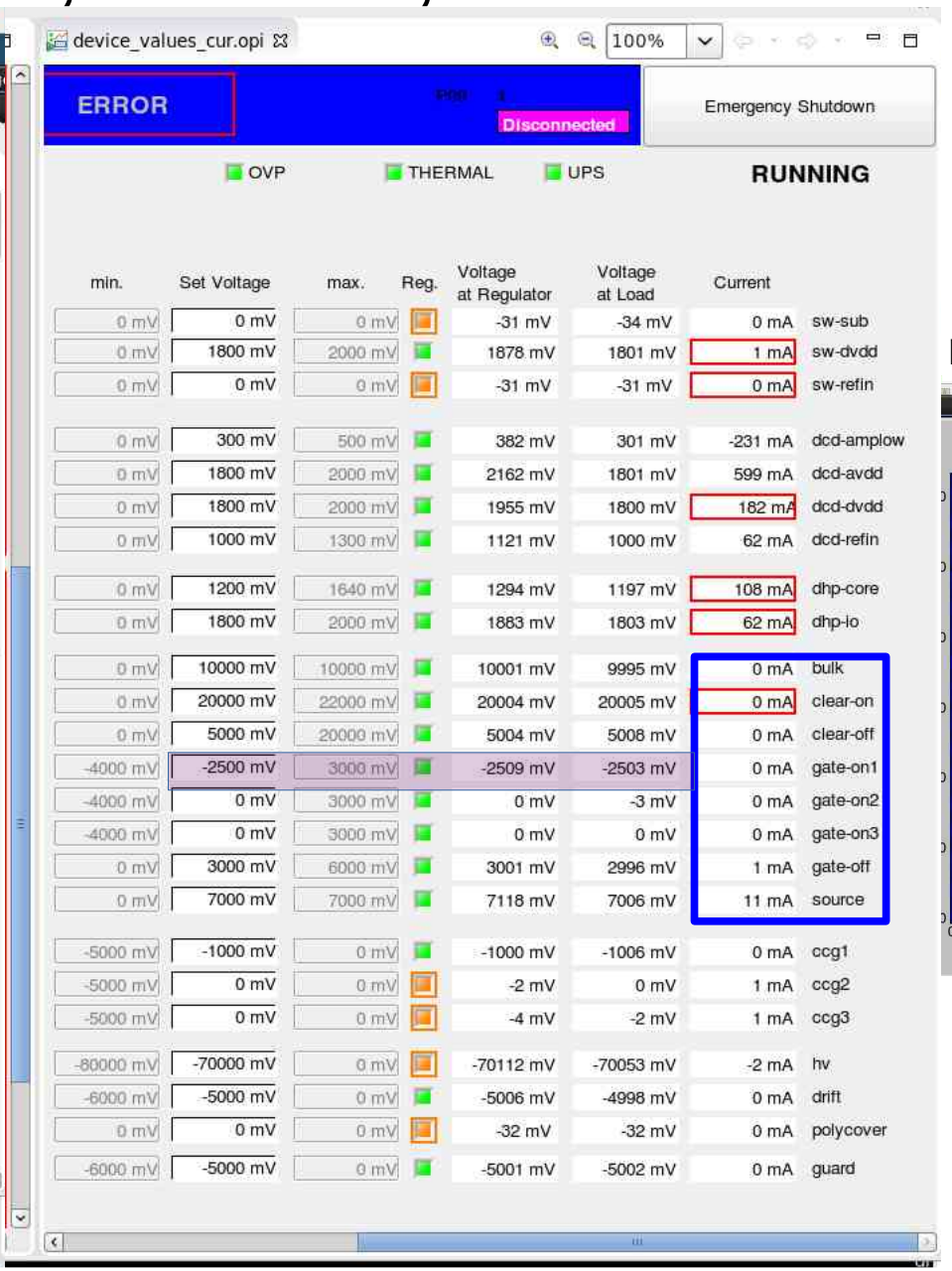


H5_0_24
DHPT1.1, DCDB4.1, SWB2.1, W35-A05

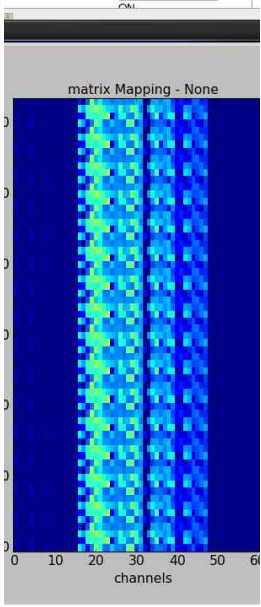
- GCK 62 MHz
- delays set
- ADC curves fine



Gate-On = 3000 → no currents



memdump



Gate-On = -2500 → no clear and gate currents
source = 11 mA in the dark, goes to 25 mA limit with light

H5_0_26 with DCDB4.2

H5_0_26
DHPT1.1, DCDB4.2, SWB2.1, W35-F00

- GCK 62 MHz
- delays set
- ADC curves fine

Set Voltage	max.	Reg.	Voltage at Regulator	Voltage at Load	Current	
0 mV	0 mV		-31 mV	-24 mV	0 mA	sw-sub
1800 mV	2000 mV		1878 mV	1801 mV	1 mA	sw-dvdd
0 mV	0 mV		-31 mV	-22 mV	0 mA	sw-refin
200 mV	500 mV		261 mV	200 mV	-295 mA	dcd-amplow
1800 mV	2000 mV		2175 mV	1801 mV	650 mA	dcd-avdd
1800 mV	2000 mV		1950 mV	1803 mV	178 mA	dcd-dvdd
650 mV	1300 mV		756 mV	648 mV	26 mA	dcd-refin
1200 mV	1640 mV		1294 mV	1197 mV	109 mA	dhp-core
1800 mV	2000 mV		1880 mV	1803 mV	62 mA	dhp-io
0 mV	10000 mV		-1 mV	3 mV	-1 mA	bulk
0 mV	22000 mV		2 mV	4 mV	0 mA	clear-on
0 mV	20000 mV		6 mV	3 mV	0 mA	clear-off
0 mV	3000 mV		1 mV	0 mV	0 mA	gate-on1
0 mV	3000 mV		0 mV	0 mV	0 mA	gate-on2
0 mV	3000 mV		-3 mV	-3 mV	0 mA	gate-on3
0 mV	6000 mV		0 mV	0 mV	0 mA	gate-off
0 mV	7000 mV		791 mV	683 mV	0 mA	source
0 mV	0 mV		2 mV	-7 mV	0 mA	ccg1
0 mV	0 mV		-7 mV	-3 mV	1 mA	ccg2
0 mV	0 mV		-8 mV	-6 mV	1 mA	ccg3
0 mV	0 mV		-33 mV	-69 mV	0 mA	hv
0 mV	0 mV		0 mV	0 mV	1 mA	drift
0 mV	0 mV		-27 mV	-25 mV	0 mA	polycover
0 mV	0 mV		-24 mV	-28 mV	0 mA	guard

1. ASICs on, matrix off

2. Bulk = 10 V → OK

1800 mV	2000 mV	1880 mV	1800 mV	62 mA	dhp-io
10000 mV	10000 mV	10001 mV	10002 mV	0 mA	bulk
0 mV	22000 mV	-5 mV	4 mV	0 mA	clear-on
0 mV	20000 mV	-2 mV	12 mV	0 mA	clear-off
0 mV	3000 mV	1 mV	0 mV	0 mA	gate-on1
0 mV	3000 mV	0 mV	4 mV	0 mA	gate-on2
0 mV	3000 mV	0 mV	0 mV	0 mA	gate-on3
0 mV	6000 mV	0 mV	-4 mV	0 mA	gate-off
0 mV	7000 mV	660 mV	561 mV	0 mA	source
0 mV	0 mV	-6 mV	-3 mV	0 mA	ccg1
0 mV	0 mV	-2 mV	-3 mV	1 mA	ccg2
0 mV	0 mV	-4 mV	-2 mV	1 mA	ccg3
0 mV	0 mV	-77 mV	-69 mV	0 mA	hv
0 mV	0 mV	-4 mV	0 mV	1 mA	drift
0 mV	0 mV	-32 mV	-32 mV	0 mA	polycover

3. clear-on = 12 V → clear-off goes to 9 V, current between clear-on, clear-off?

1800 mV	2000 mV	1883 mV	1800 mV	62 mA	dhp-io
10000 mV	10000 mV	10001 mV	10002 mV	0 mA	bulk
12000 mV	22000 mV	12011 mV	11996 mV	4 mA	clear-on
0 mV	20000 mV	8963 mV	8965 mV	-2 mA	clear-off
0 mV	3000 mV	1 mV	-7 mV	0 mA	gate-on1
0 mV	3000 mV	0 mV	0 mV	0 mA	gate-on2
0 mV	3000 mV	-3 mV	0 mV	0 mA	gate-on3
0 mV	6000 mV	3 mV	0 mV	0 mA	gate-off
0 mV	7000 mV	399 mV	297 mV	0 mA	source
0 mV	0 mV	-1 mV	-3 mV	0 mA	ccg1
0 mV	0 mV	1 mV	-3 mV	1 mA	ccg2
0 mV	0 mV	0 mV	-2 mV	1 mA	ccg3
0 mV	0 mV	-33 mV	-92 mV	0 mA	hv
0 mV	0 mV	-4 mV	0 mV	1 mA	drift
0 mV	0 mV	-32 mV	-25 mV	0 mA	polycover

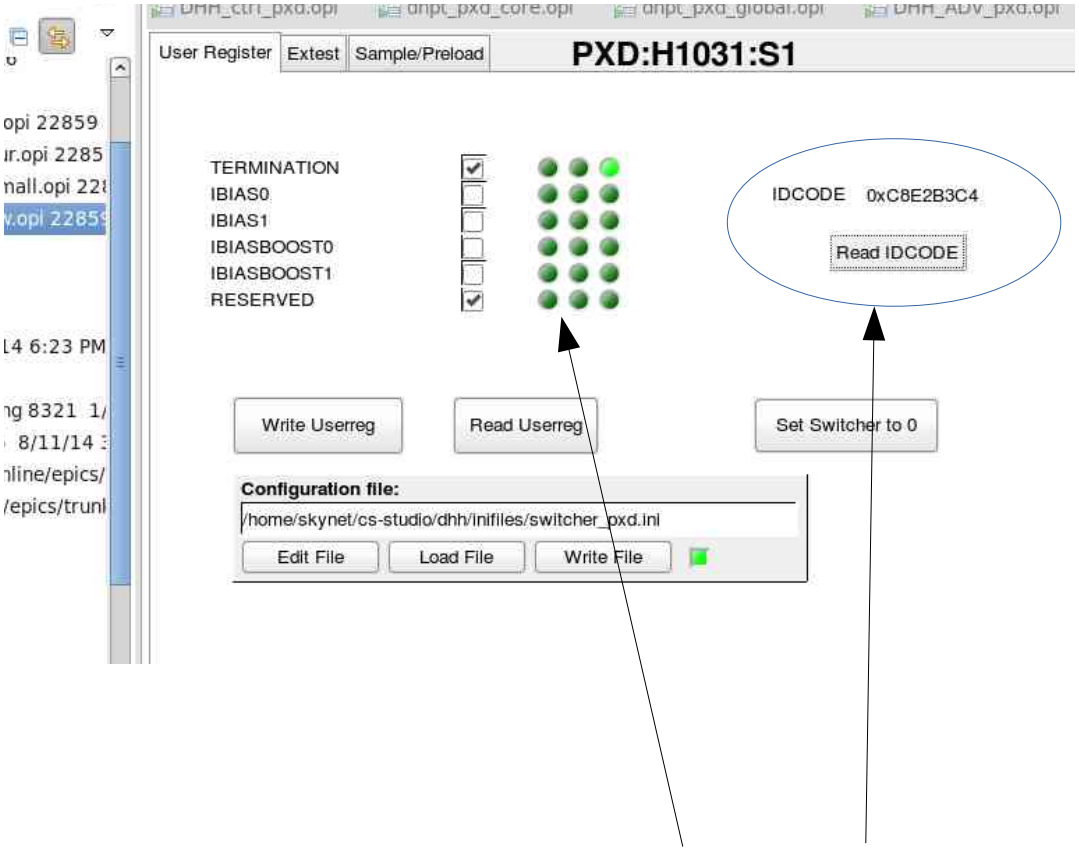
H5_0_26
DHPT1.1, DCDB4.2, SWB2.1, W35-F00

- GCK 62 MHz
- delays set
- ADC curves fine

4. clear-off = 5 V → okay?

1800 mV	2000 mV	1883 mV	1800 mV	62 mA	dhp-io
10000 mV	10000 mV	10005 mV	10009 mV	0 mA	bulk
12000 mV	22000 mV	12011 mV	12004 mV	8 mA	clear-on
5000 mV	20000 mV	4996 mV	5008 mV	-6 mA	clear-off
0 mV	3000 mV	1 mV	4 mV	0 mA	gate-on1
0 mV	3000 mV	-5 mV	-3 mV	0 mA	gate-on2
0 mV	3000 mV	-7 mV	-3 mV	0 mA	gate-on3
0 mV	6000 mV	0 mV	0 mV	0 mA	gate-off
0 mV	7000 mV	363 mV	259 mV	0 mA	source
0 mV	0 mV	2 mV	0 mV	0 mA	ccg1
0 mV	0 mV	-2 mV	-3 mV	1 mA	ccg2
0 mV	0 mV	-4 mV	-2 mV	1 mA	ccg3
0 mV	0 mV	-55 mV	-69 mV	0 mA	hv
0 mV	0 mV	-4 mV	-4 mV	1 mA	drift
0 mV	0 mV	-27 mV	-32 mV	0 mA	polycover

As soon as clear-off is set, switcher JTAG can not be read and written stably anymore...



wrong IDCODE read out
wrong register content read out

H5_0_26
DHPT1.1, DCDB4.2, SWB2.1, W35-F00

- GCK 62 MHz
- delays set
- ADC curves fine

4. clear-off = 5 V → okay?

1800 mV	2000 mV	1883 mV	1800 mV	62 mA	dhp-io
10000 mV	10000 mV	10005 mV	10009 mV	0 mA	bulk
12000 mV	22000 mV	12011 mV	12004 mV	8 mA	clear-on
5000 mV	20000 mV	4996 mV	5008 mV	-6 mA	clear-off
0 mV	3000 mV	1 mV	4 mV	0 mA	gate-on1
0 mV	3000 mV	-5 mV	-3 mV	0 mA	gate-on2
0 mV	3000 mV	-7 mV	-3 mV	0 mA	gate-on3
0 mV	6000 mV	0 mV	0 mV	0 mA	gate-off
0 mV	7000 mV	363 mV	259 mV	0 mA	source
0 mV	0 mV	2 mV	0 mV	0 mA	ccg1
0 mV	0 mV	-2 mV	-3 mV	1 mA	ccg2
0 mV	0 mV	-4 mV	-2 mV	1 mA	ccg3
0 mV	0 mV	-55 mV	-69 mV	0 mA	hv
0 mV	0 mV	-4 mV	-4 mV	1 mA	drift
0 mV	0 mV	-27 mV	-32 mV	0 mA	polycover

6. increase clear-on/off current limit to 15 mA → okay?

650 mV	1300 mV	753 mV	650 mV	27 mA	dcd-refin
1200 mV	1640 mV	1294 mV	1202 mV	109 mA	dhp-core
1800 mV	2000 mV	1880 mV	1800 mV	62 mA	dhp-io
10000 mV	10000 mV	10005 mV	10002 mV	0 mA	bulk
20000 mV	22000 mV	20012 mV	20013 mV	11 mA	clear-on
5000 mV	20000 mV	5004 mV	5000 mV	-9 mA	clear-off
0 mV	3000 mV	-3 mV	0 mV	0 mA	gate-on1
0 mV	3000 mV	0 mV	0 mV	0 mA	gate-on2
0 mV	3000 mV	-3 mV	-3 mV	0 mA	gate-on3
0 mV	6000 mV	3 mV	0 mV	0 mA	gate-off
0 mV	7000 mV	284 mV	190 mV	0 mA	source
0 mV	0 mV	-1 mV	-3 mV	0 mA	ccg1
0 mV	0 mV	-2 mV	-7 mV	1 mA	ccg2
0 mV	0 mV	4 mV	-6 mV	1 mA	ccg3
0 mV	0 mV	-55 mV	-69 mV	0 mA	hv
0 mV	0 mV	-4 mV	-4 mV	1 mA	drift
0 mV	0 mV	-32 mV	-32 mV	0 mA	polycover

5. clear-on = 20 V → clear-on/off in 10 mA current limit

1800 mV	2000 mV	1880 mV	1800 mV	64 mA	dhp-io
10000 mV	10000 mV	10001 mV	10002 mV	0 mA	bulk
20000 mV	22000 mV	18733 mV	18735 mV	11 mA	clear-on
5000 mV	20000 mV	4996 mV	5008 mV	-9 mA	clear-off
0 mV	3000 mV	-3 mV	4 mV	0 mA	gate-on1
0 mV	3000 mV	0 mV	-3 mV	0 mA	gate-on2
0 mV	3000 mV	-3 mV	0 mV	0 mA	gate-on3
0 mV	6000 mV	-5 mV	0 mV	0 mA	gate-off
0 mV	7000 mV	297 mV	193 mV	0 mA	source
0 mV	0 mV	2 mV	0 mV	0 mA	ccg1
0 mV	0 mV	-7 mV	-3 mV	1 mA	ccg2
0 mV	0 mV	0 mV	-6 mV	1 mA	ccg3
0 mV	0 mV	-55 mV	-69 mV	0 mA	hv
0 mV	0 mV	-4 mV	-4 mV	1 mA	drift
0 mV	0 mV	-32 mV	-25 mV	0 mA	polycover

7. everything on, gate-on = 3 V

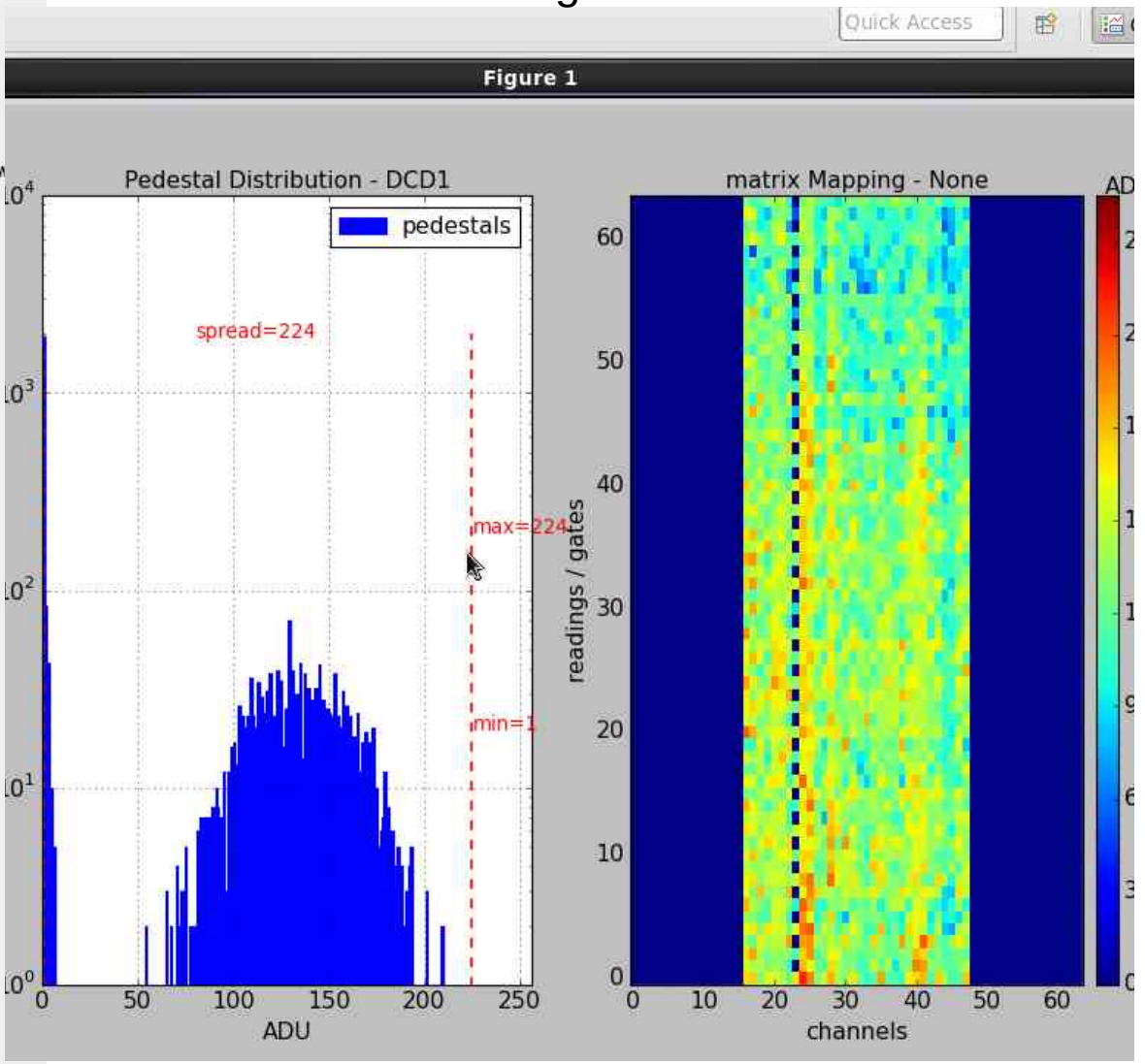
1800 mV	2000 mV	1883 mV	1803 mV	62 mA	dhp-io
10000 mV	10000 mV	10005 mV	10002 mV	0 mA	bulk
20000 mV	22000 mV	20012 mV	20013 mV	11 mA	clear-on
5000 mV	20000 mV	4987 mV	5008 mV	-10 mA	clear-off
3000 mV	3000 mV	2998 mV	3001 mV	1 mA	gate-on1
3000 mV	3000 mV	3001 mV	2997 mV	0 mA	gate-on2
3000 mV	3000 mV	2998 mV	3001 mV	0 mA	gate-on3
3000 mV	6000 mV	2996 mV	2996 mV	1 mA	gate-off
7000 mV	7000 mV	7105 mV	7003 mV	4 mA	source
-1000 mV	0 mV	-1004 mV	-1002 mV	0 mA	ccg1
0 mV	0 mV	1 mV	0 mV	1 mA	ccg2
0 mV	0 mV	-4 mV	-2 mV	1 mA	ccg3
-70000 mV	0 mV	-70112 mV	-70053 mV	-2 mA	hv
-5000 mV	0 mV	-5006 mV	-5002 mV	0 mA	drift
0 mV	0 mV	-27 mV	-32 mV	0 mA	polycover

H5_0_26
DHPT1.1, DCDB4.2, SWB2.1, W35-F00

8. everything on, gate-on = -2.5 V

Set Voltage	max.	Reg.	Voltage at Regulator	Voltage at Load	Current	
0 mV	0 mV		-31 mV	-34 mV	0 mA	sw-sub
1800 mV	2000 mV		1878 mV	1803 mV	1 mA	sw-dvdd
0 mV	0 mV		-22 mV	-31 mV	0 mA	sw-refin
200 mV	500 mV		277 mV	200 mV	-227 mA	dcd-amplow
1800 mV	2000 mV		2152 mV	1801 mV	585 mA	dcd-avdd
1800 mV	2000 mV		1955 mV	1805 mV	185 mA	dcd-dvdd
650 mV	1300 mV		761 mV	650 mV	33 mA	dcd-refin
1200 mV	1640 mV		1297 mV	1200 mV	112 mA	dhp-core
1800 mV	2000 mV		1883 mV	1803 mV	65 mA	dhp-io
10000 mV	10000 mV		9996 mV	10002 mV	0 mA	bulk
20000 mV	22000 mV		20020 mV	20005 mV	11 mA	clear-on
5000 mV	20000 mV		4996 mV	5000 mV	-10 mA	clear-off
-2500 mV	3000 mV		-2504 mV	-2503 mV	-6 mA	gate-on1
0 mV	3000 mV		0 mV	-3 mV	0 mA	gate-on2
0 mV	3000 mV		-3 mV	0 mV	0 mA	gate-on3
3000 mV	6000 mV		3005 mV	3004 mV	9 mA	gate-off
7000 mV	7000 mV		7113 mV	7006 mV	19 mA	source
-1000 mV	0 mV		-1000 mV	-998 mV	0 mA	ccg1
0 mV	0 mV		-7 mV	-3 mV	1 mA	ccg2
0 mV	0 mV		-4 mV	2 mV	1 mA	ccg3
-70000 mV	0 mV		-70090 mV	-70053 mV	-2 mA	hv
-5000 mV	0 mV		-5006 mV	-5002 mV	0 mA	drift
0 mV	0 mV		-32 mV	-25 mV	0 mA	polycover
-5000 mV	0 mV		-5001 mV	-5002 mV	0 mA	guard

memdump, at least looks like something...



H5_0_26 DHPT1.1, DCDB4.2, SWB2.1, W35-F00

comparison

H5_0_07 DHPT1.0, DCDBpp, SWBG, W30...

Set Voltage	max.	Reg.	Voltage at Regulator	Voltage at Load	Current	
0 mV	0 mV		-31 mV	-34 mV	0 mA	sw-sub
1800 mV	2000 mV		1878 mV	1803 mV	1 mA	sw-dvdd
0 mV	0 mV		-22 mV	-31 mV	0 mA	sw-refin
200 mV	500 mV		277 mV	200 mV	-227 mA	dcd-amplow
1800 mV	2000 mV		2152 mV	1801 mV	585 mA	dcd-avdd
1800 mV	2000 mV		1955 mV	1805 mV	185 mA	dcd-dvdd
650 mV	1300 mV		761 mV	650 mV	33 mA	dcd-refin
1200 mV	1640 mV		1297 mV	1200 mV	112 mA	dhp-core
1800 mV	2000 mV		1883 mV	1803 mV	65 mA	dhp-io
10000 mV	10000 mV		9996 mV	10002 mV	0 mA	bulk
20000 mV	22000 mV		20020 mV	20005 mV	11 mA	clear-on
5000 mV	20000 mV		4996 mV	5000 mV	-10 mA	clear-off
-2500 mV	3000 mV		-2504 mV	-2503 mV	-6 mA	gate-on1
0 mV	3000 mV		0 mV	-3 mV	0 mA	gate-on2
0 mV	3000 mV		-3 mV	0 mV	0 mA	gate-on3
3000 mV	6000 mV		3005 mV	3004 mV	9 mA	gate-off
7000 mV	7000 mV		7113 mV	7006 mV	19 mA	source
-1000 mV	0 mV		-1000 mV	-998 mV	0 mA	ccg1
0 mV	0 mV		-7 mV	-3 mV	1 mA	ccg2
0 mV	0 mV		-4 mV	2 mV	1 mA	ccg3
-70000 mV	0 mV		-70090 mV	-70053 mV	-2 mA	hv
-5000 mV	0 mV		-5006 mV	-5002 mV	0 mA	drift
0 mV	0 mV		-32 mV	-25 mV	0 mA	polycover
-5000 mV	0 mV		-5001 mV	-5002 mV	0 mA	guard

min.	Set Voltage	max.	Reg.	Voltage at Regulator	Voltage at Load	Current	
0 mV	0 mV	0 mV		-17 mV	-21 mV	0 mA	sw-sub
0 mV	1800 mV	2000 mV		1893 mV	1800 mV	1 mA	sw-dvdd
0 mV	0 mV	0 mV		-15 mV	-11 mV	0 mA	sw-refin
0 mV	400 mV	500 mV		458 mV	398 mV	-218 mA	dcd-amplow
0 mV	1900 mV	2000 mV		2325 mV	1903 mV	666 mA	dcd-avdd
0 mV	2100 mV	2100 mV		2279 mV	2098 mV	202 mA	dcd-dvdd
0 mV	875 mV	1300 mV		873 mV	875 mV	104 mA	dcd-refin
0 mV	1540 mV	1640 mV		1673 mV	1540 mV	154 mA	dhp-core
0 mV	2000 mV	2000 mV		2110 mV	2001 mV	95 mA	dhp-io
0 mV	10000 mV	10000 mV		10003 mV	10002 mV	0 mA	bulk
0 mV	19000 mV	22000 mV		19004 mV	18995 mV	6 mA	clear-on
0 mV	6000 mV	20000 mV		6002 mV	6002 mV	-5 mA	clear-off
-4000 mV	-2500 mV	3000 mV		-2504 mV	-2505 mV	-4 mA	gate-on1
-4000 mV	0 mV	3000 mV		0 mV	-1 mV	0 mA	gate-on2
-4000 mV	0 mV	3000 mV		-1 mV	-1 mV	0 mA	gate-on3
0 mV	3000 mV	6000 mV		3001 mV	2997 mV	6 mA	gate-off
0 mV	7000 mV	7000 mV		7152 mV	7003 mV	18 mA	source
-5000 mV	-1000 mV	0 mV		-1001 mV	-1007 mV	1 mA	ccg1
-5000 mV	0 mV	0 mV		-5 mV	-3 mV	1 mA	ccg2
-5000 mV	0 mV	0 mV		4 mV	-5 mV	1 mA	ccg3
-80000 mV	-70000 mV	0 mV		-70003 mV	-69927 mV	0 mA	hv
-6000 mV	-5000 mV	0 mV		-5003 mV	-5006 mV	0 mA	drift
0 mV	0 mV	0 mV		-7 mV	-2 mV	0 mA	polycover
-6000 mV	-5000 mV	0 mV		-4997 mV	-5001 mV	0 mA	guard

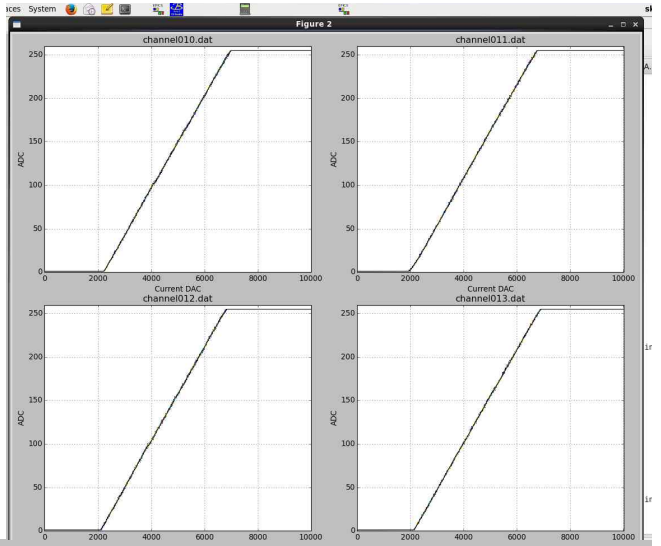
H5_0_14 with DCDB4.2

H5_0_14
DHPT1.1, DCDB4.2, SWB2.1, W35-A02

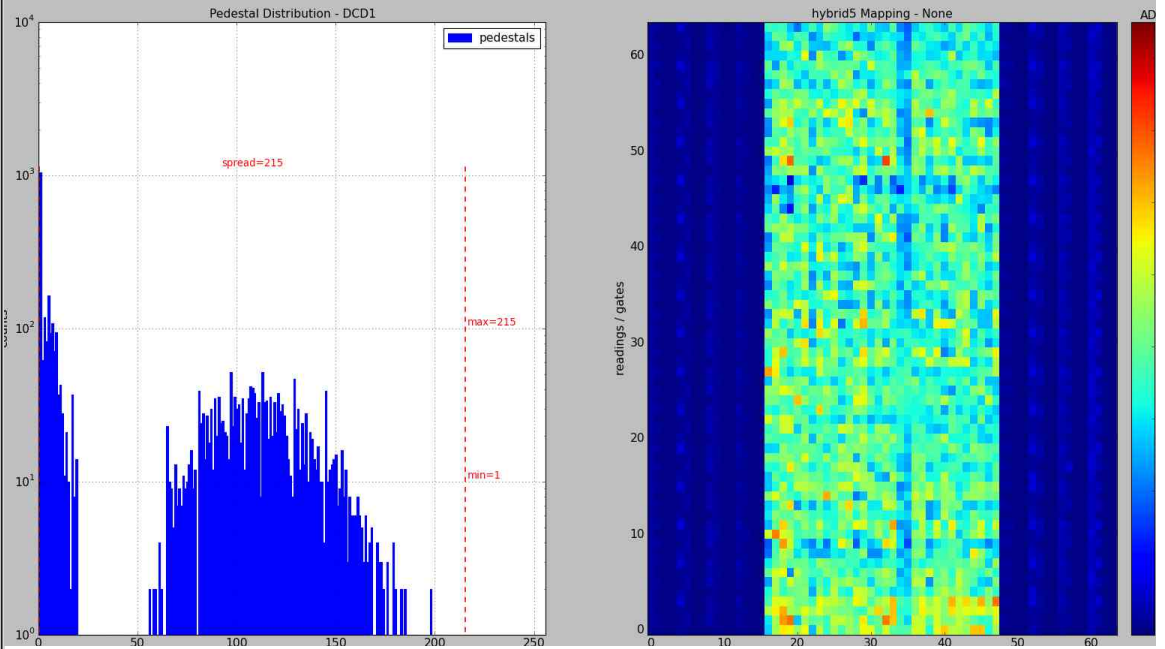
everything on, gate-on = -2.5 V

	Set Voltage	max.	Reg.	Voltage at Regulator	Voltage at Load	Current	
0 mV	0 mV	0 mV		-41 mV	-29 mV	0 mA	sw-sub
0 mV	1800 mV	2000 mV		1878 mV	1798 mV	1 mA	sw-dvdd
0 mV	0 mV	0 mV		-27 mV	-27 mV	0 mA	sw-refin
0 mV	200 mV	500 mV		277 mV	200 mV	-240 mA	dcd-amplow
0 mV	1800 mV	2000 mV		2165 mV	1798 mV	604 mA	dcd-avdd
0 mV	1800 mV	2000 mV		1958 mV	1805 mV	184 mA	dcd-dvdd
0 mV	650 mV	1300 mV		766 mV	650 mV	36 mA	dcd-refin
0 mV	1200 mV	1640 mV		1294 mV	1200 mV	112 mA	dhp-core
0 mV	1800 mV	2000 mV		1880 mV	1803 mV	64 mA	dhp-io
0 mV	10000 mV	10000 mV		10005 mV	10009 mV	0 mA	bulk
0 mV	20000 mV	22000 mV		20012 mV	20005 mV	11 mA	clear-on
0 mV	5000 mV	20000 mV		4996 mV	5008 mV	-9 mA	clear-off
0 mV	-2500 mV	3000 mV		-2509 mV	-2499 mV	-6 mA	gate-on1
0 mV	0 mV	3000 mV		0 mV	0 mV	0 mA	gate-on2
0 mV	0 mV	3000 mV		-3 mV	-3 mV	0 mA	gate-on3
0 mV	3000 mV	6000 mV		3005 mV	3000 mV	9 mA	gate-off
0 mV	7000 mV	7000 mV		7120 mV	7006 mV	22 mA	source
0 mV	-1000 mV	0 mV		-1000 mV	-998 mV	0 mA	ccg1
0 mV	0 mV	0 mV		1 mV	-3 mV	1 mA	ccg2
0 mV	0 mV	0 mV		0 mV	-2 mV	1 mA	ccg3
0 mV	-70000 mV	0 mV		-70090 mV	-70053 mV	-2 mA	hv
0 mV	-5000 mV	0 mV		-5006 mV	-5007 mV	0 mA	drift
0 mV	0 mV	0 mV		-27 mV	-25 mV	0 mA	polycover
0 mV	-5000 mV	0 mV		-4996 mV	-5002 mV	0 mA	guard

DCD settings exact copy from H5_0_26
optimization
→ looks good!



memdump



Switcher gain setting: en60 (Rf = 13 kOhm)
→ theoretical gain about 0.9

Switcher JTAG issue

- As soon as voltage is applied by PS to the clear-on contact, JTAG becomes unstable
  → Reading IDCODE or registers results in wrong results
  - if that happened, results are still wrong after powerdown → registers written by reading(?)
- If power ramped up and down and readout afterwards register still okay
  → preserved as long as not readout
- Possible problem: DCD is also in JTAG chain!

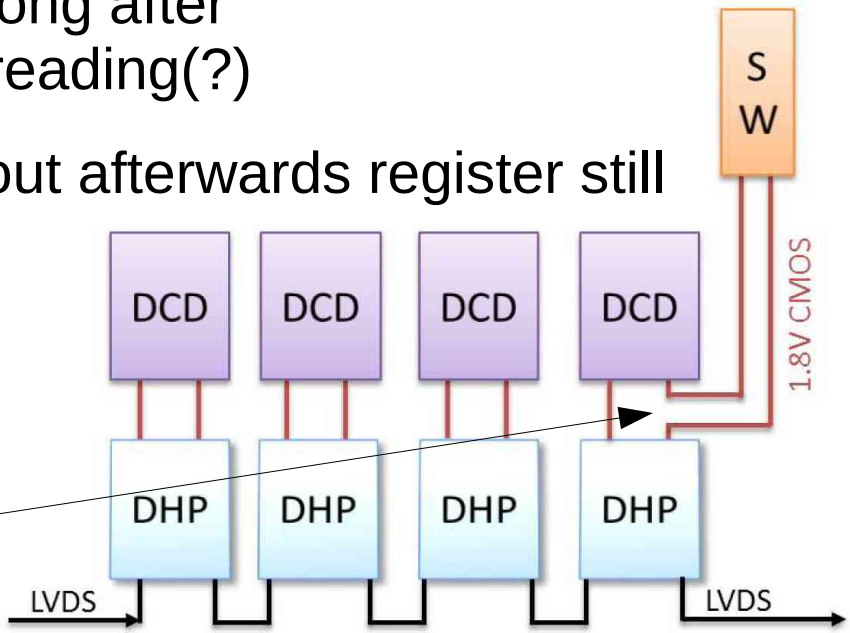
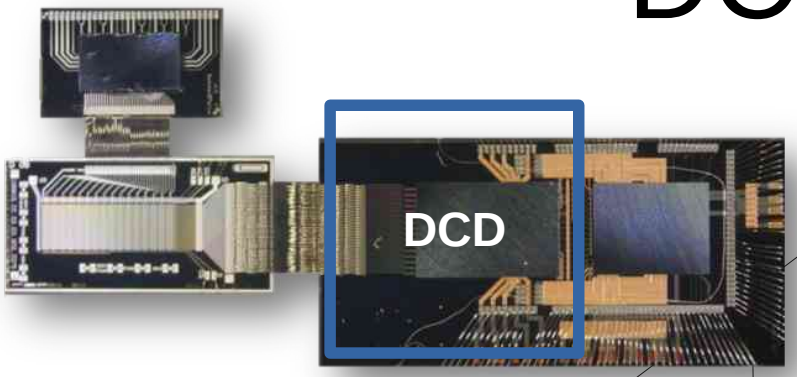


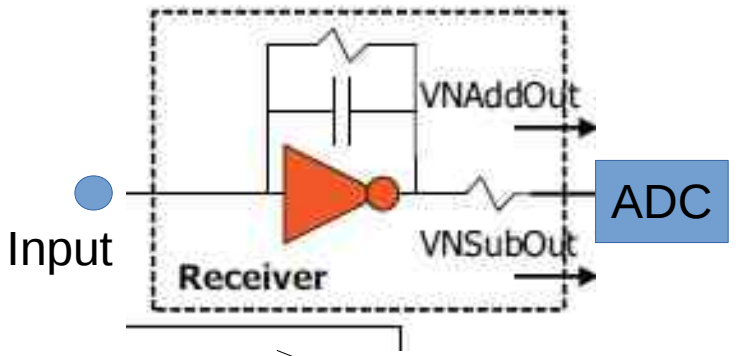
Figure 5: Global JTAG chain structure

- Possible Vsub problem?
  → connect back of switcher to GND for testing (Laci)

DCD channel



256 channels per DCD



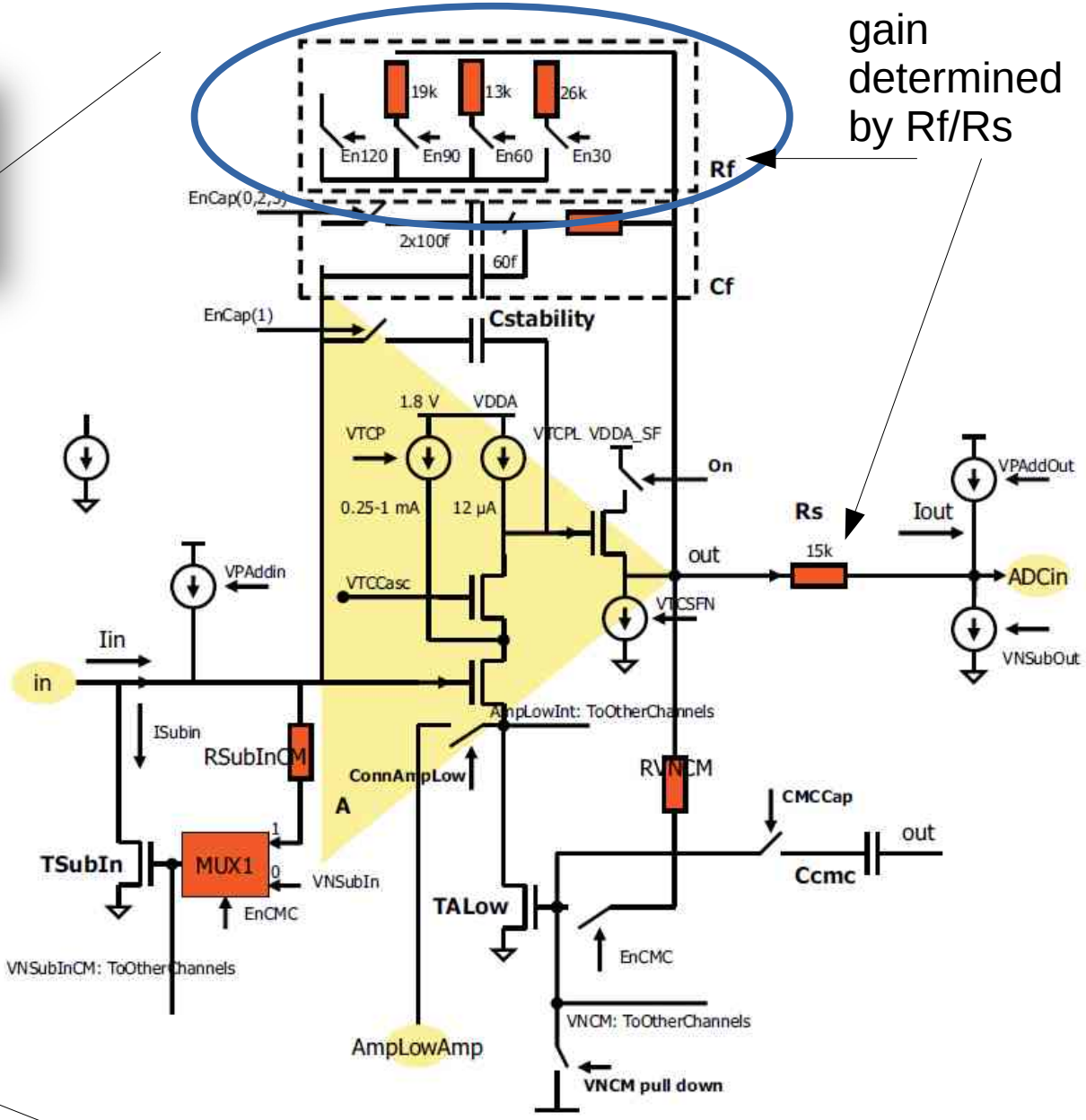


Figure 2.2: The receiver.

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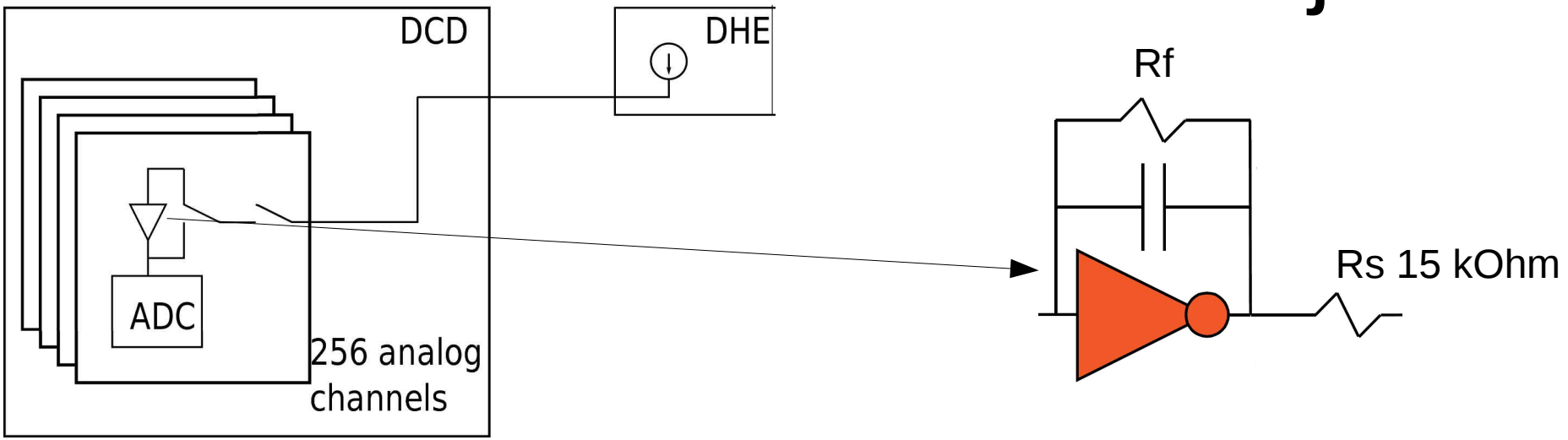
DCD channel test current injection



DCDB4.2 @ H5_0_26