

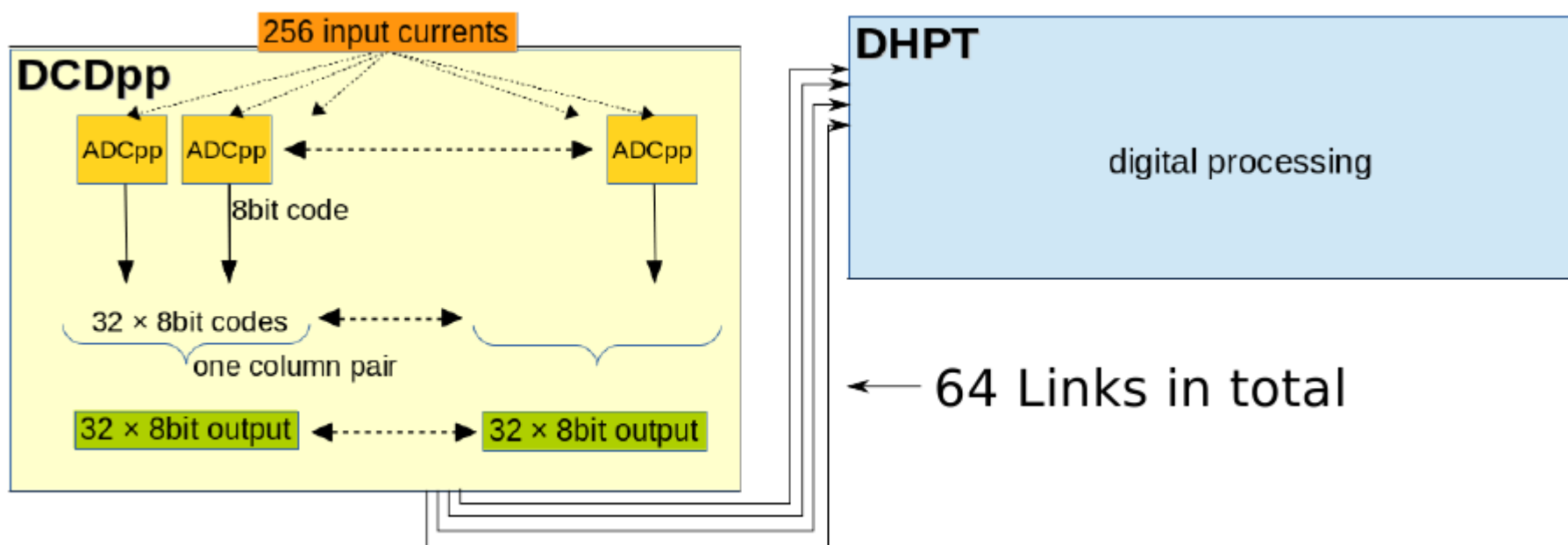
DCD4.1/DCD4.2 Review

Digital Performance

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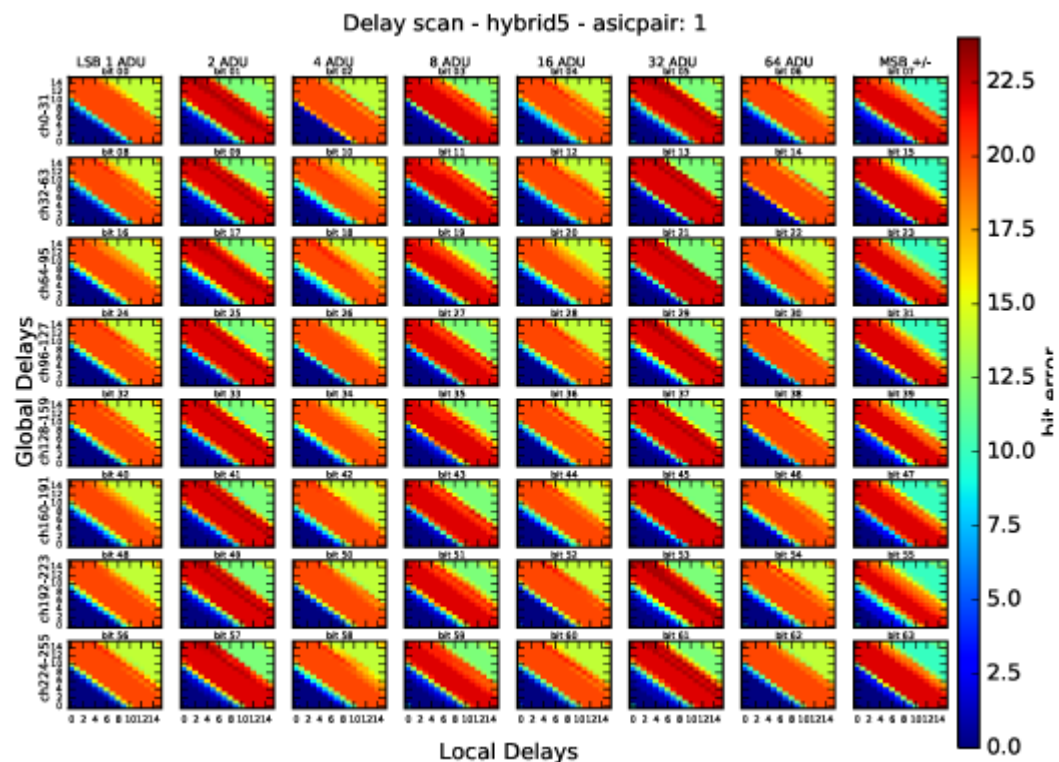
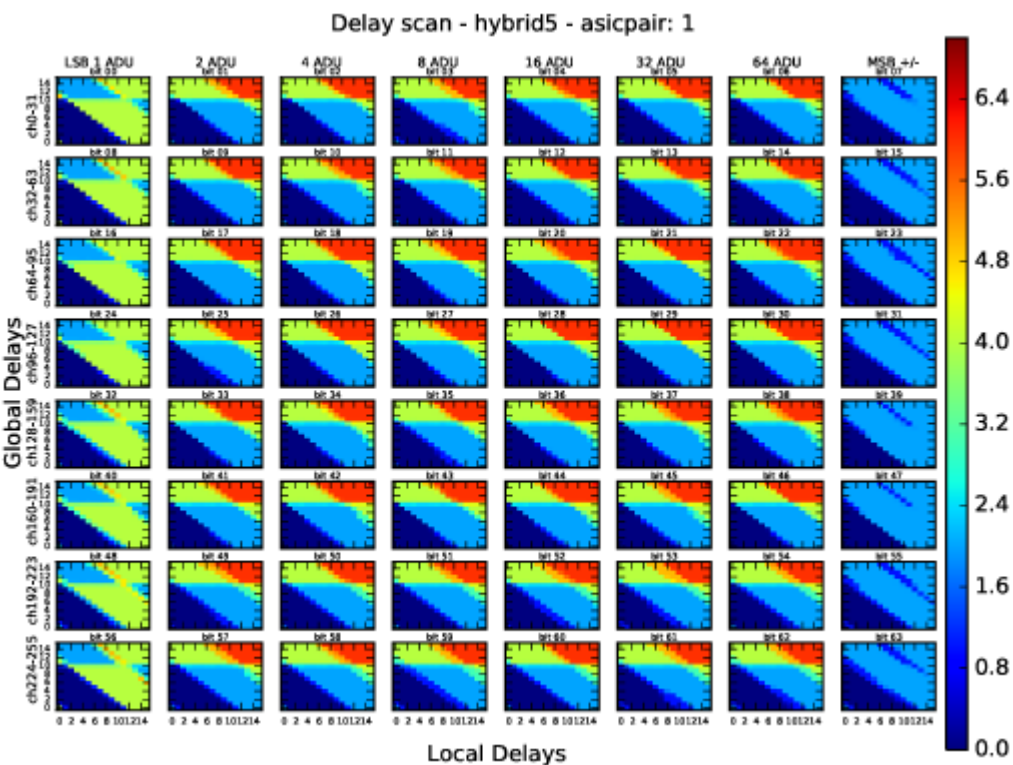


- 64 Links connect the DCD to the DHPT (8 x 8-Bit Link)
- For each link a local delay can be set to ensure a proper timing
- In addition to the local delays, a global delay can be set
- These delays have to be optimized

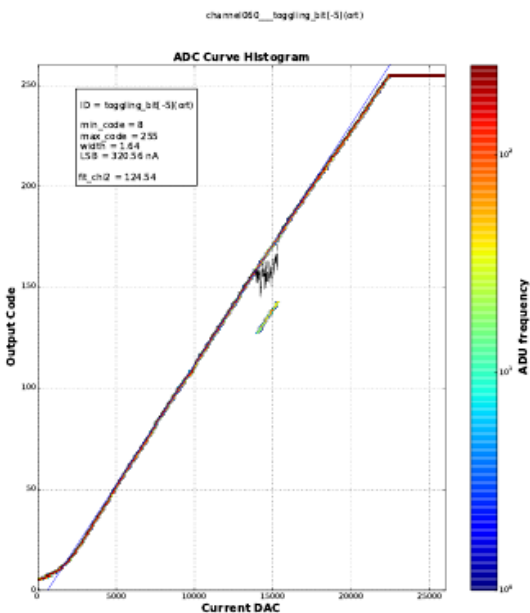
- Communication between DCD and DHP is tested by using a special test pattern
- DCD4.2 uses a new, more complicated test pattern
- DCD4.X feature a LVDS current boost to improve the communication

Test pattern is used to check the correct communication between DCD and DHP and choose the correct delay settings

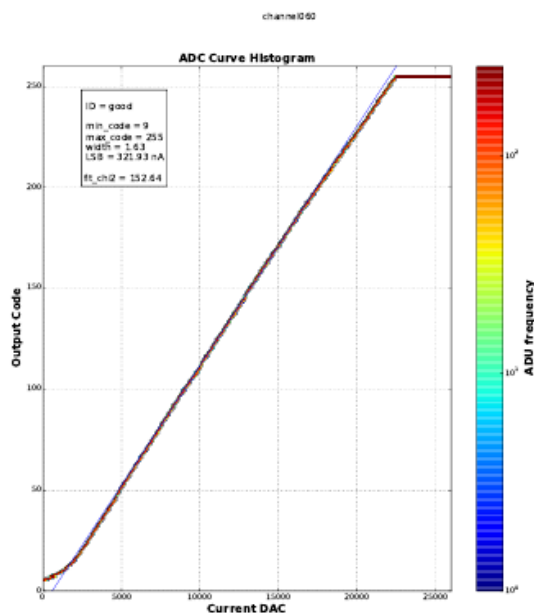
- DCD4.1
 - old, simple test pattern
 - LVDS current boost
- DCD4.2
 - new, complex test pattern
 - LVDS current boost



- Increase LVDS current from 1.3 to 1.8 mA
- Observation:
 - Communication is stabilized
 - „good“ region is broadened

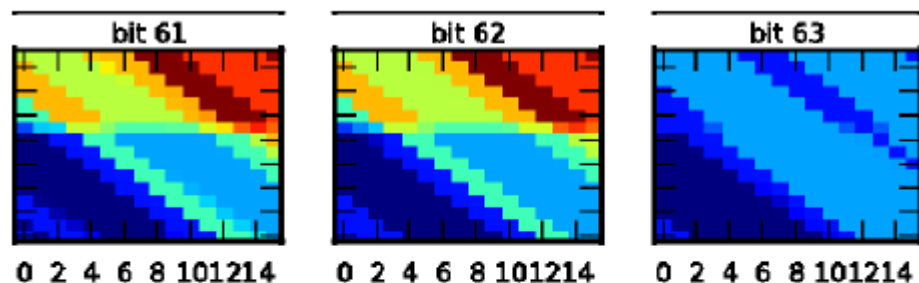


Without LVDS boost

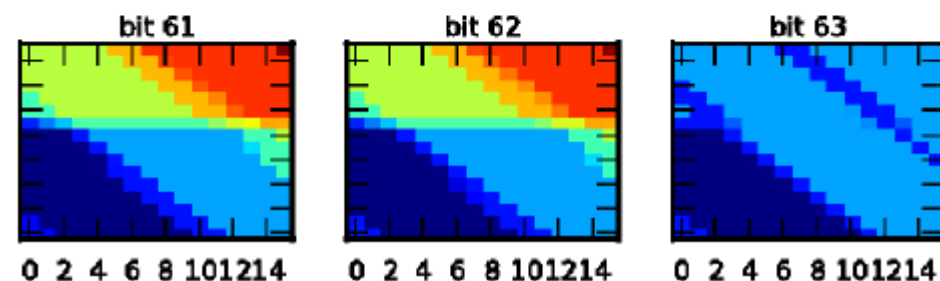


With LVDS boost

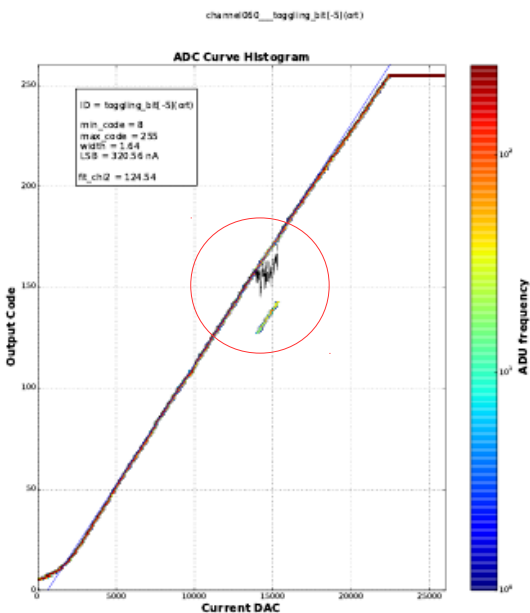
without LVDS boost



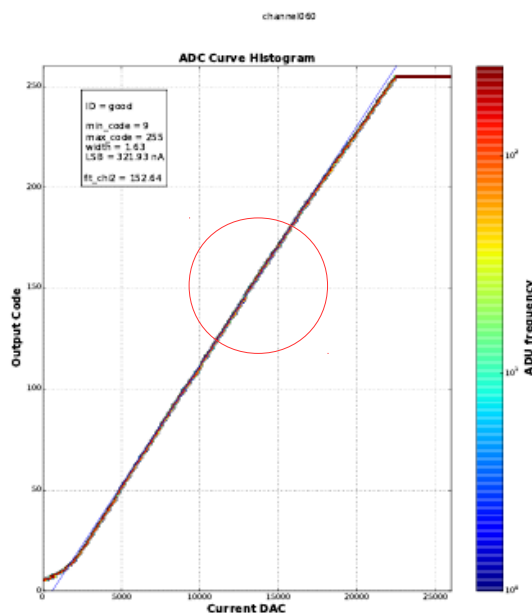
with LVDS boost



- Increase LVDS current from 1.3 to 1.8 mA
- Observation:
 - **Communication is stabilized**
 - „good“ region is broadened

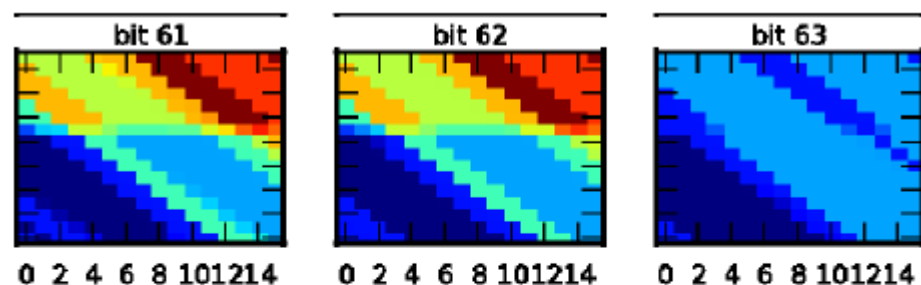


Without LVDS boost

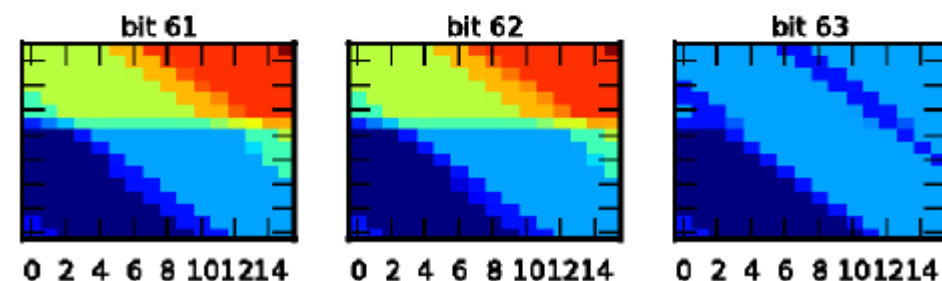


With LVDS boost

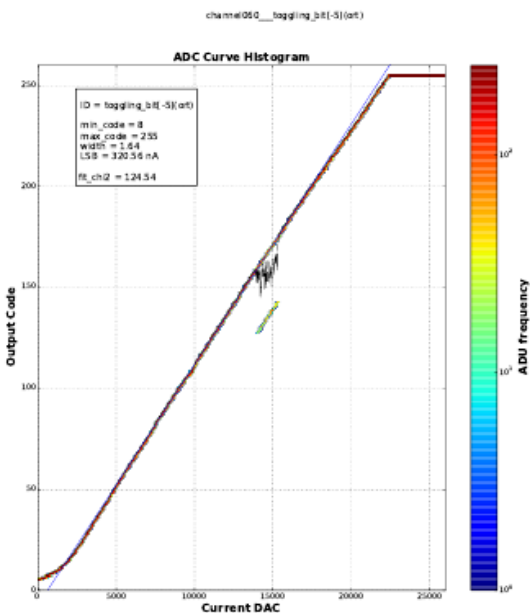
without LVDS boost



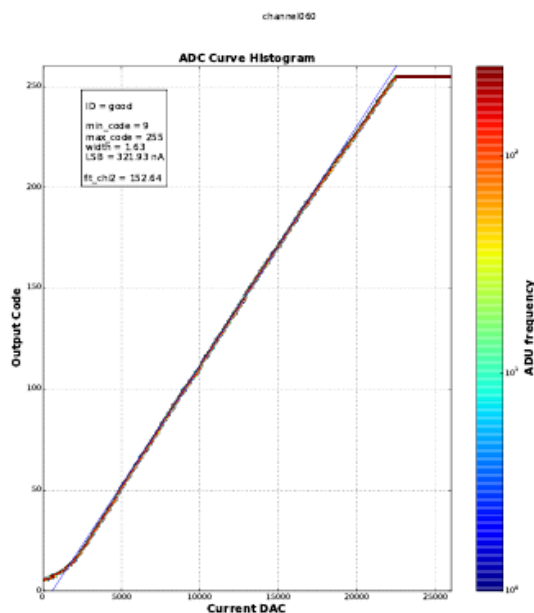
with LVDS boost



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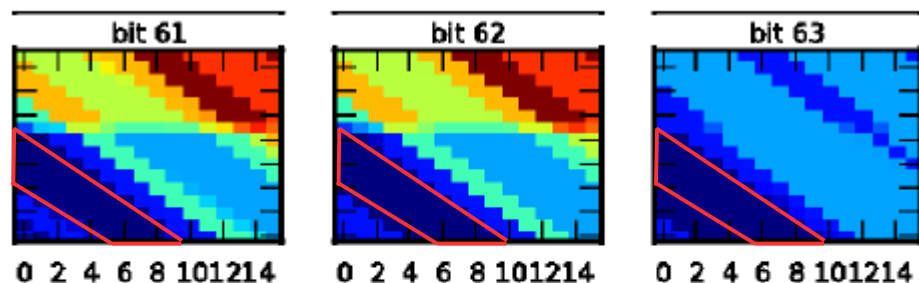


Without LVDS boost

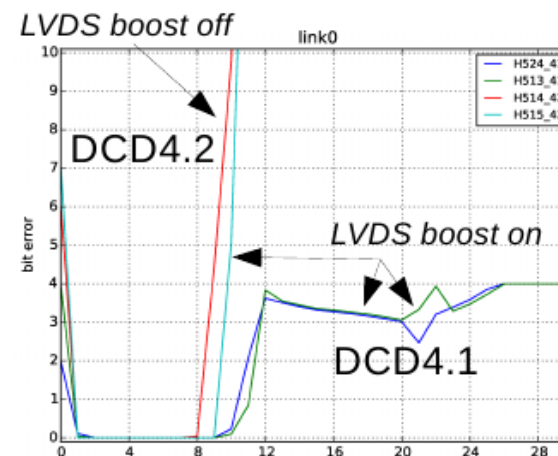
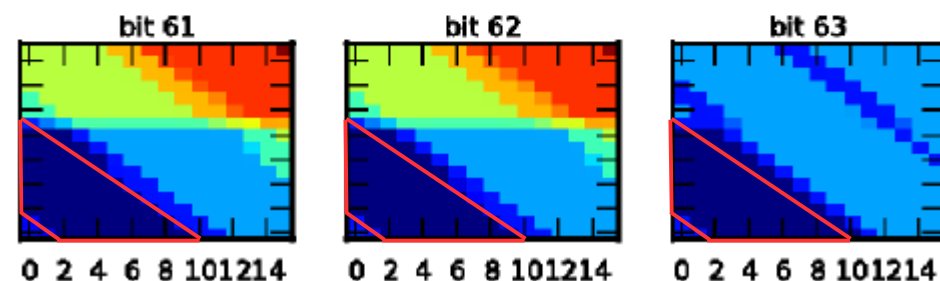


With LVDS boost

without LVDS boost

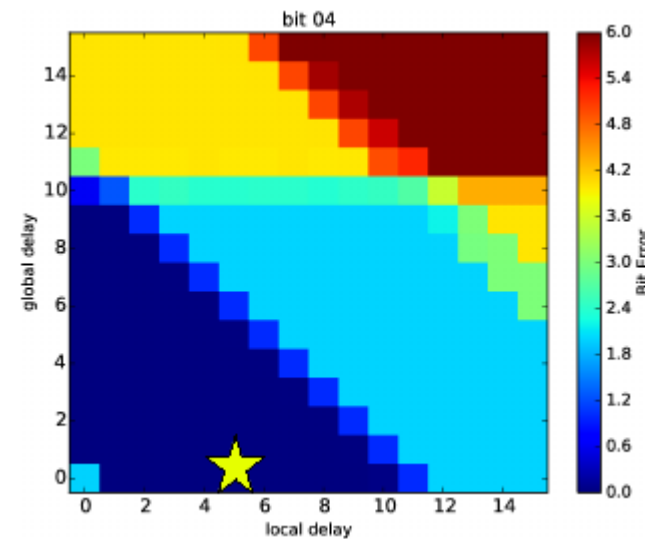


with LVDS boost

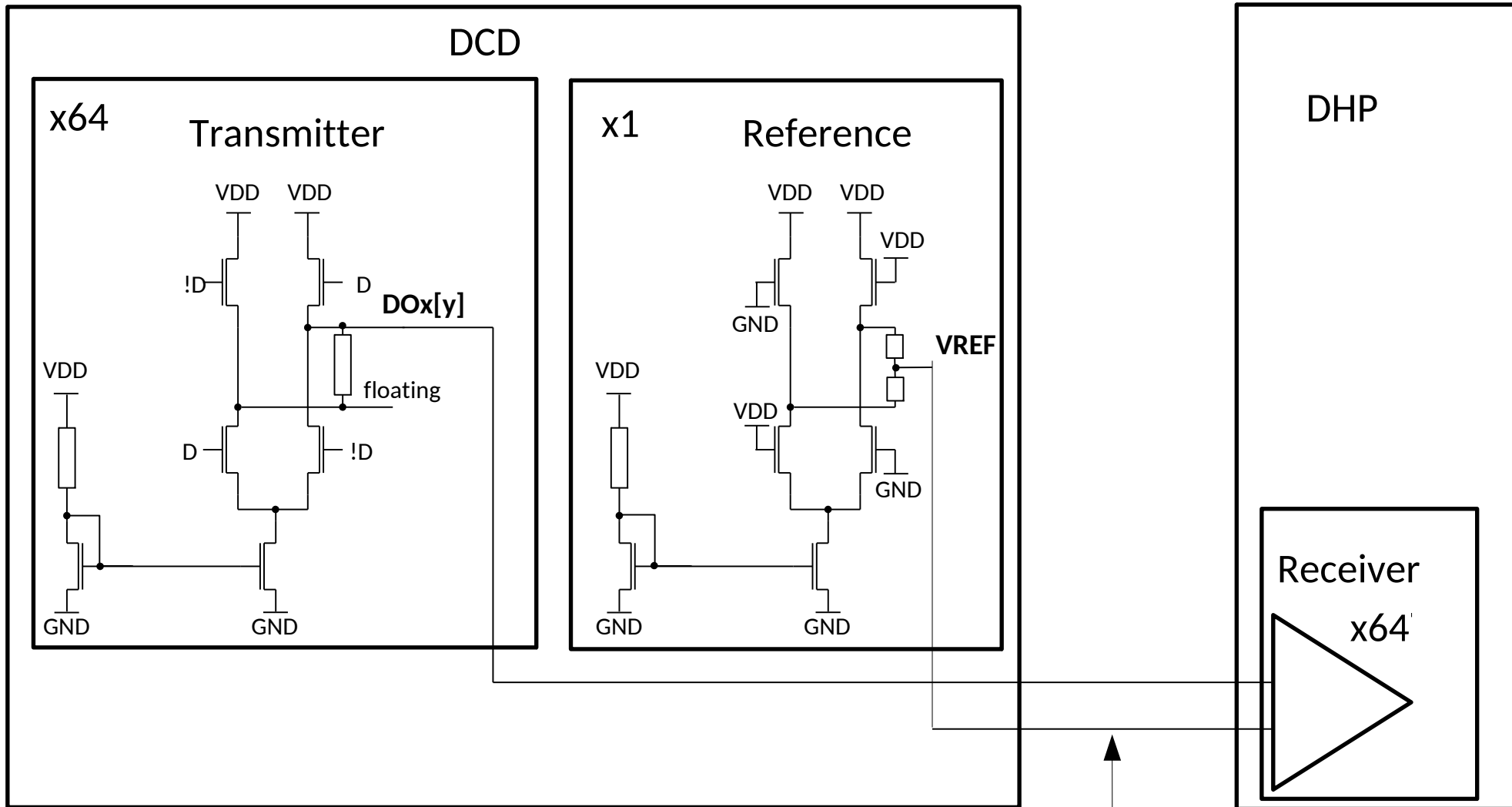


Module	Global delay	Local delay range
H5.0.24 (DCD4.1)	0	[4,6]
H5.0.13 (DCD4.1)	0	[4,6]
H5.0.14 (DCD4.2)	0	[2,4]
H5.0.15 (DCD4.2)	1	[3,4]

- Data link delays for all DCD4.1 and DCD4.2 were successfully optimized, delay values are similar
- Both test pattern can be used for the optimization
- LVDS boost improves communication

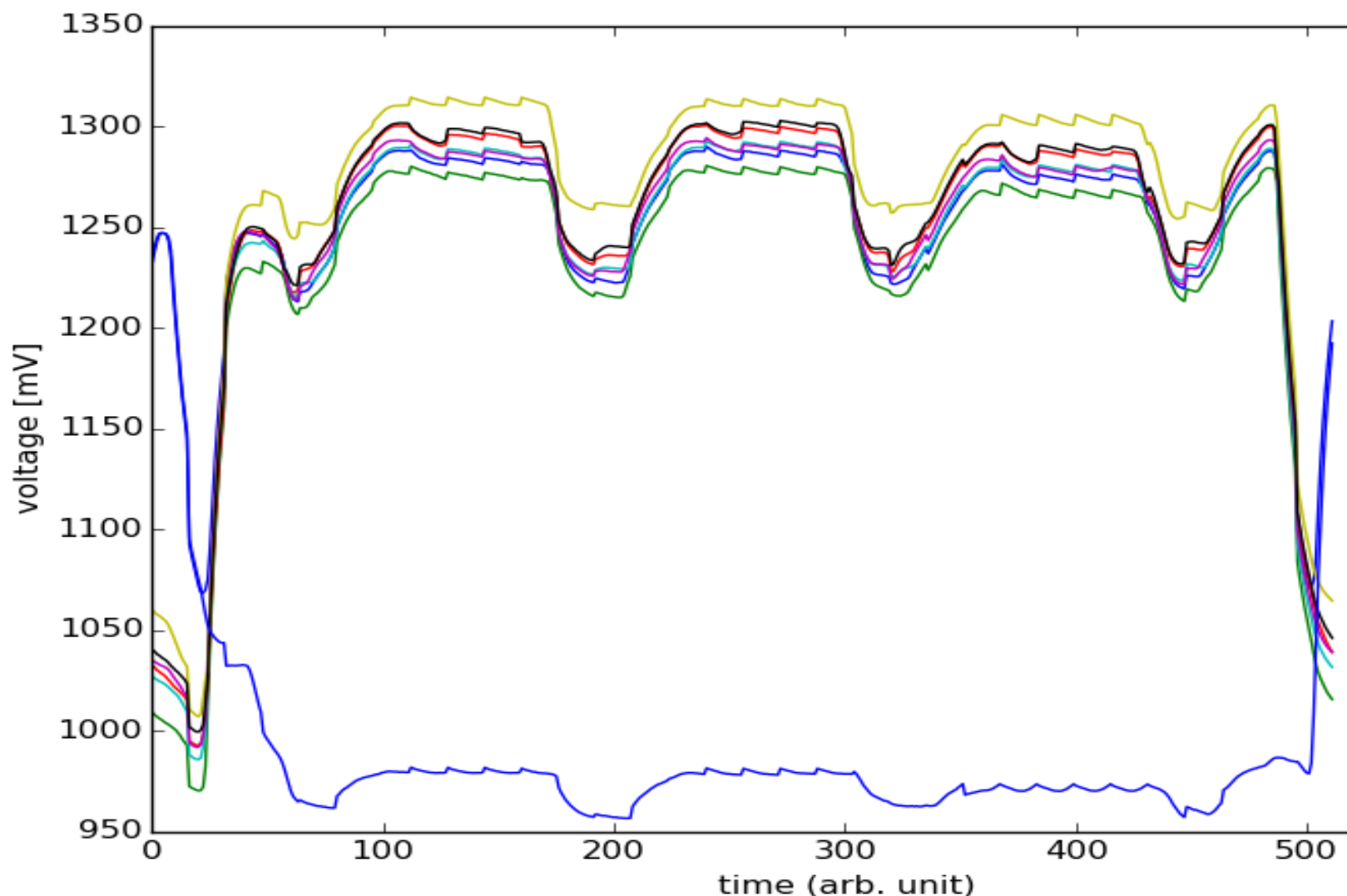



 Optimal setting



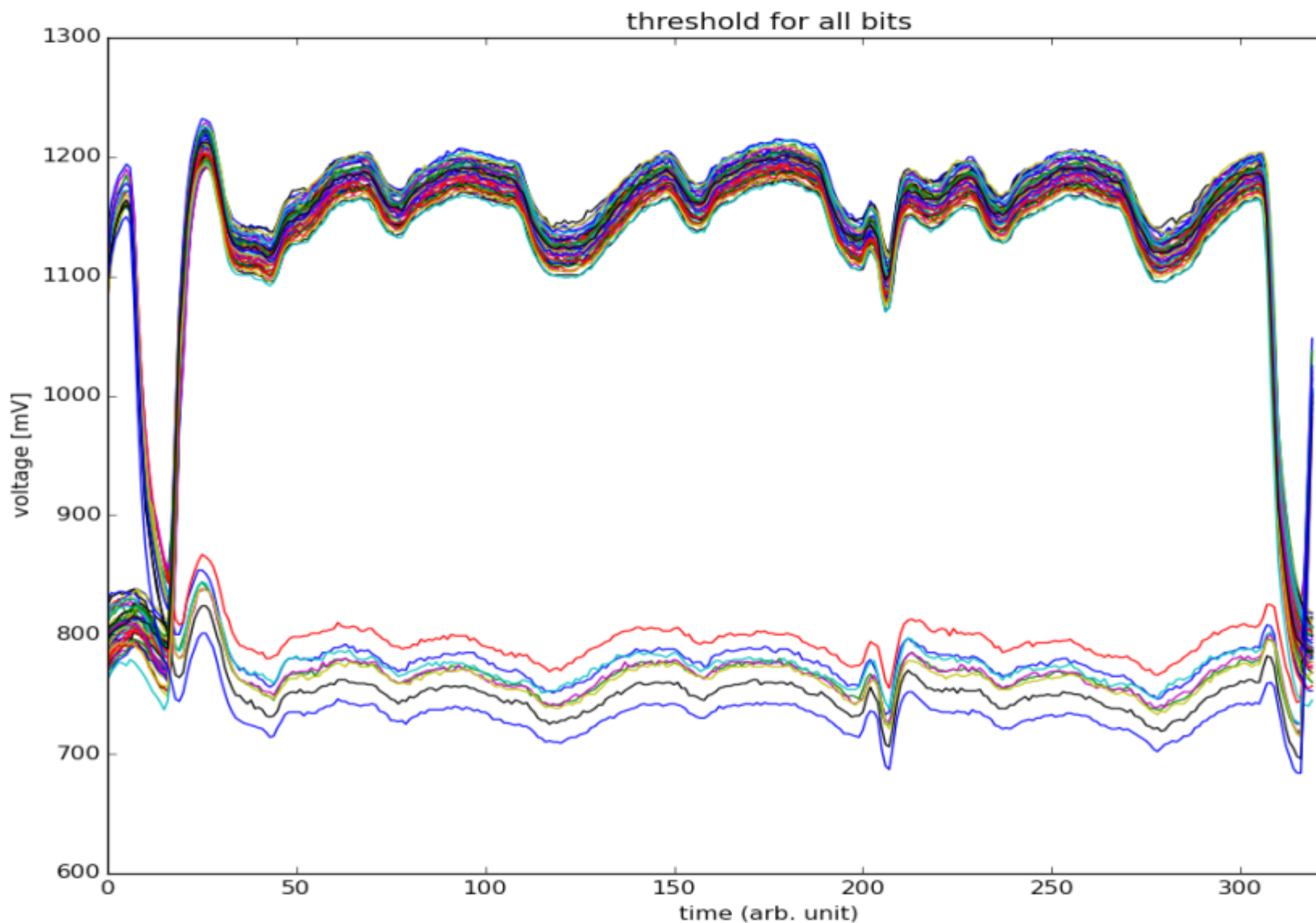
Reference Voltage can be changed from the outside

All bits of one link at 1.9V VDDD DCDpp 3, 250MHz, test pattern enabled



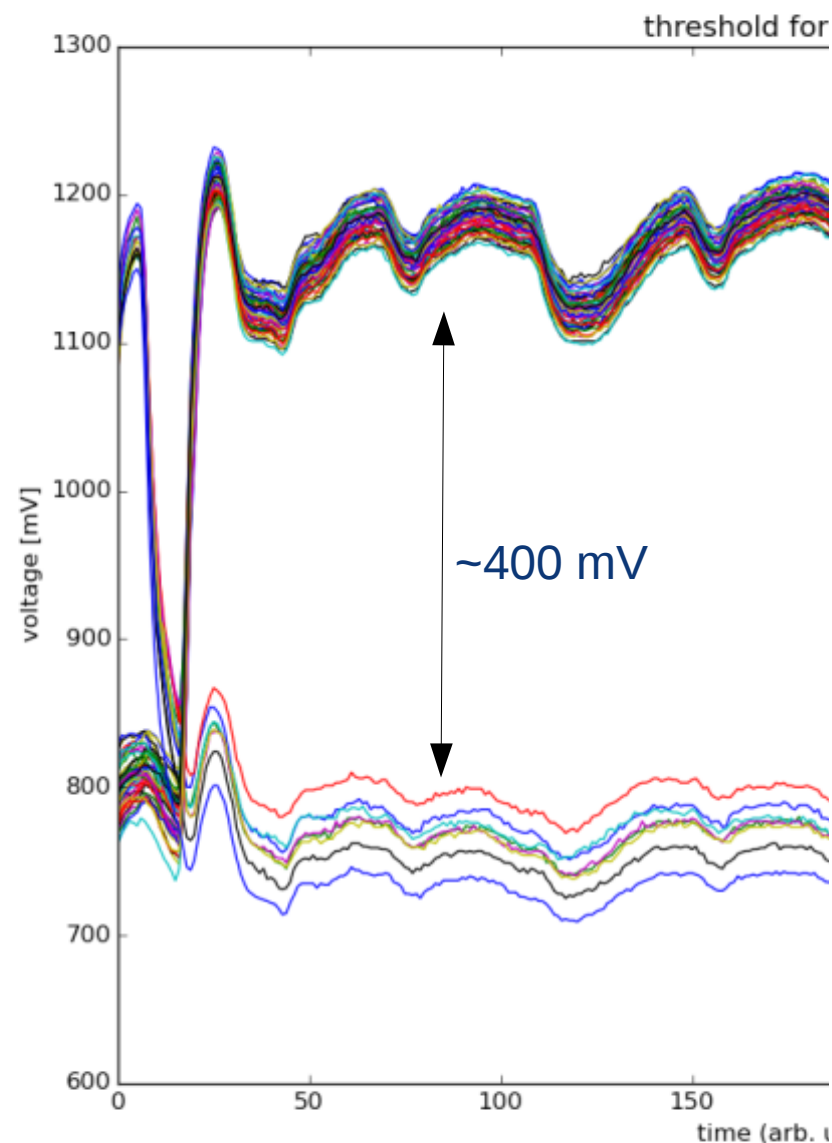
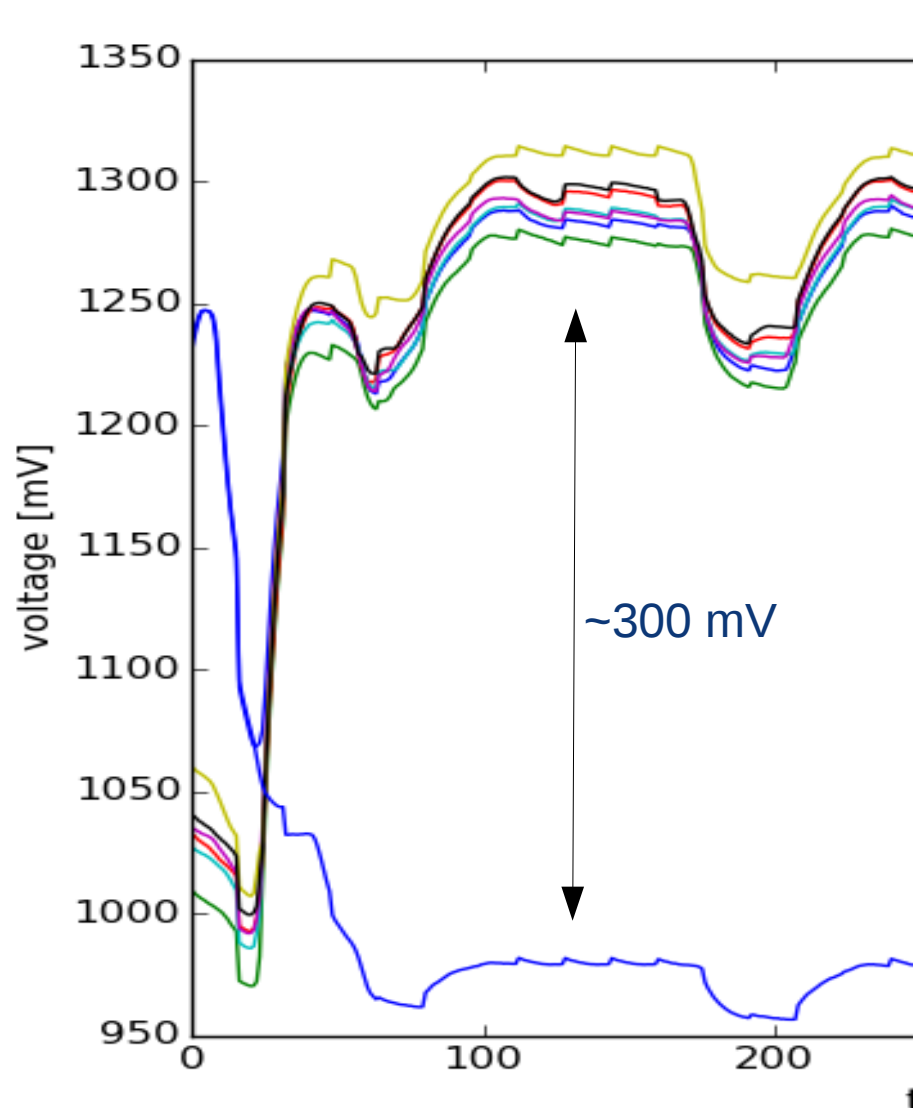
MSB	Bit 1-6	LSB
1	0	1
0	0	0
0	1	1
0	1	1
.	.	.
.	.	.
.	.	.
0	1	1
0	0	0

All bits of all links at 1.9V DVDD **DCDB4.1**, boost on, 305MHz

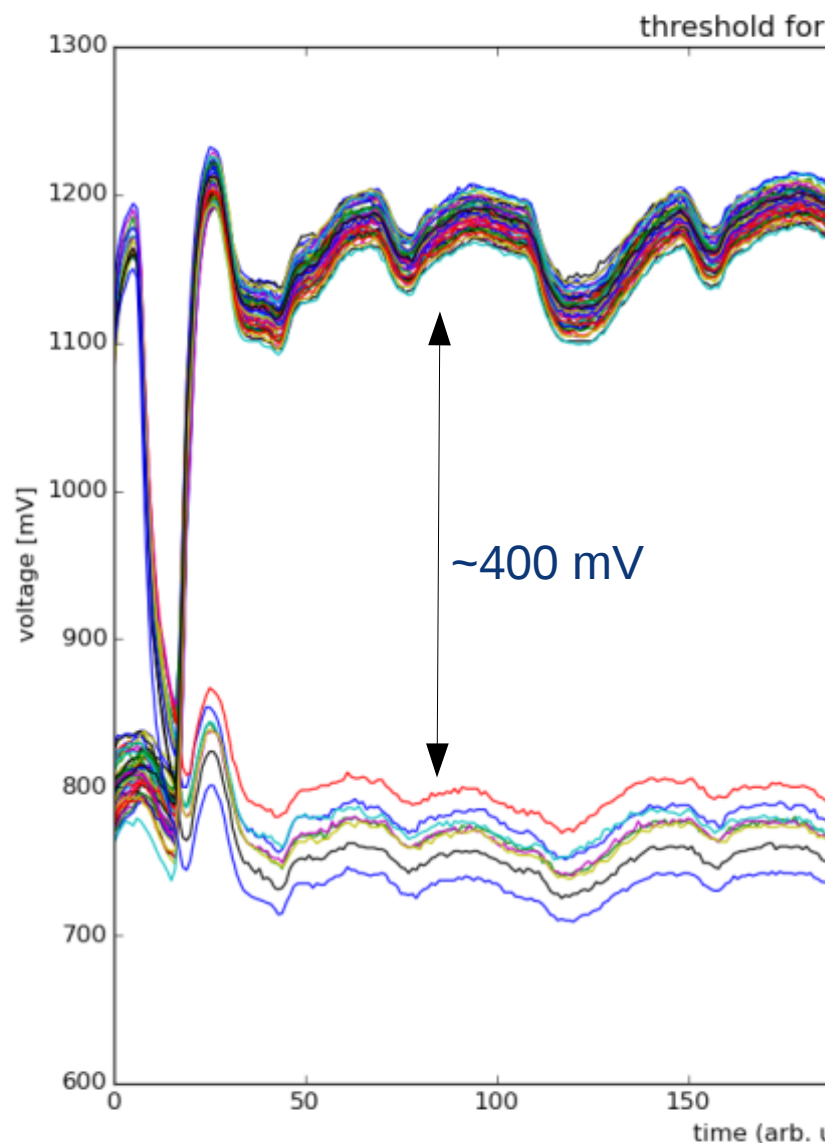
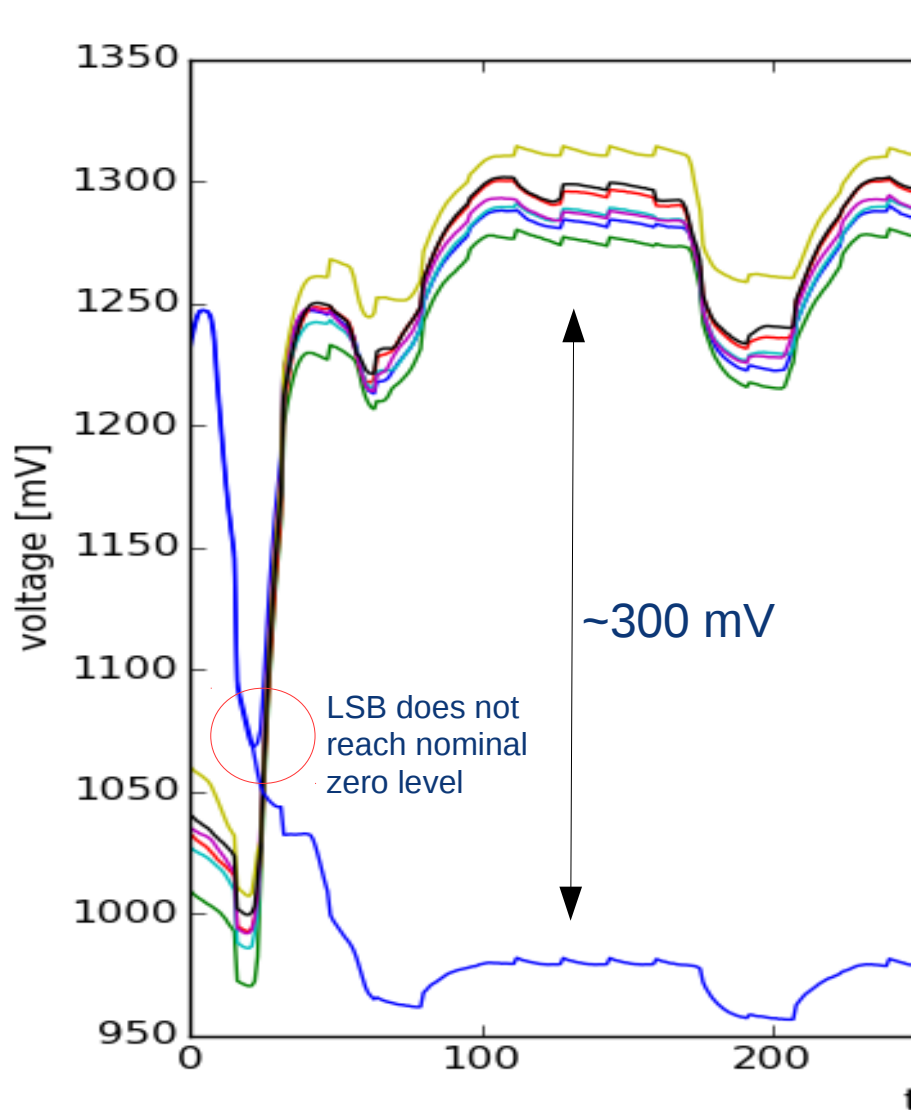


MSB	Bit 1-6	LSB
1	0	1
0	0	0
0	1	1
0	1	1
.	.	.
.	.	.
.	.	.
0	1	1
0	0	0

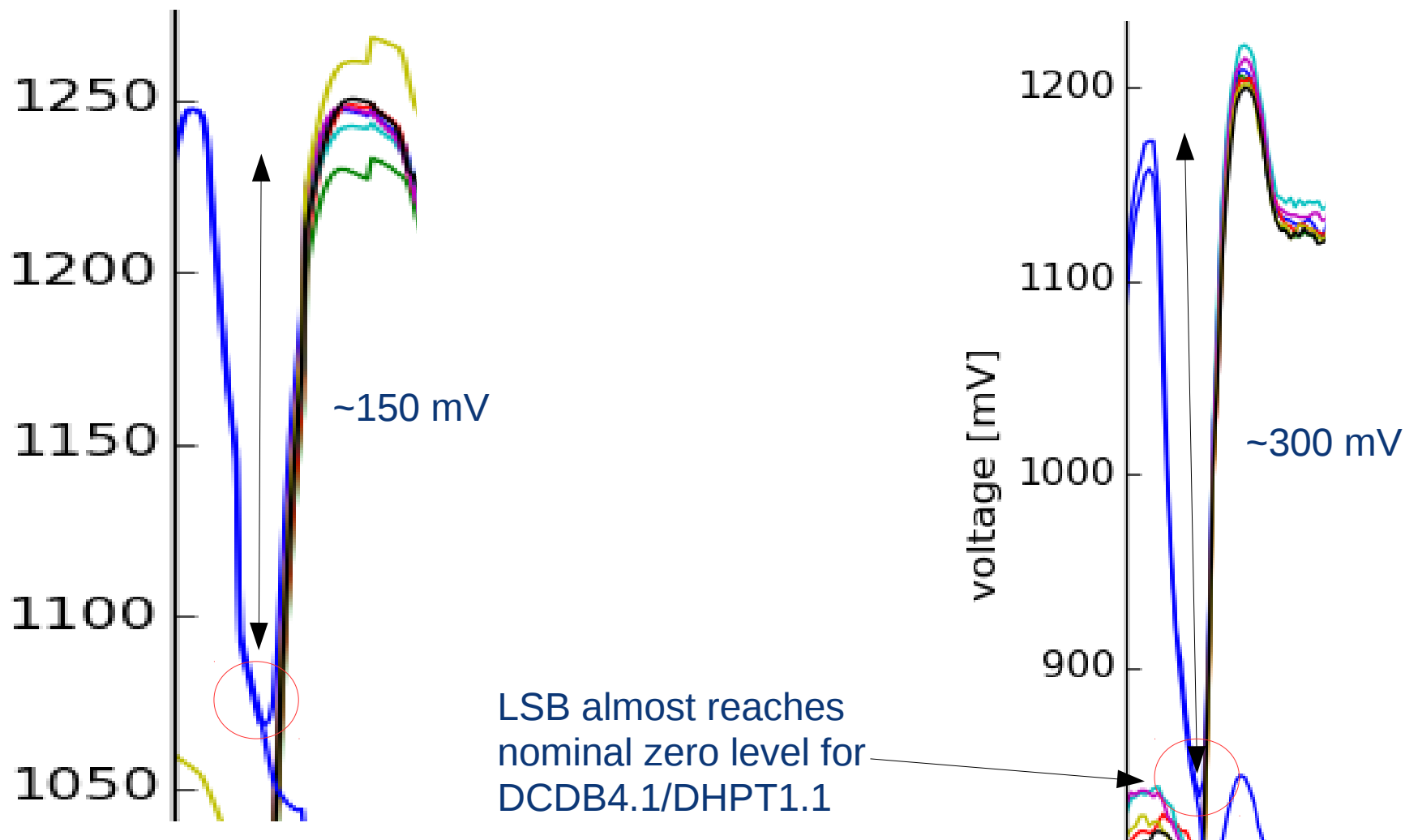
Comparison of DCDpp and DCDB4.1



Comparison of DCDpp and DCDB4.1

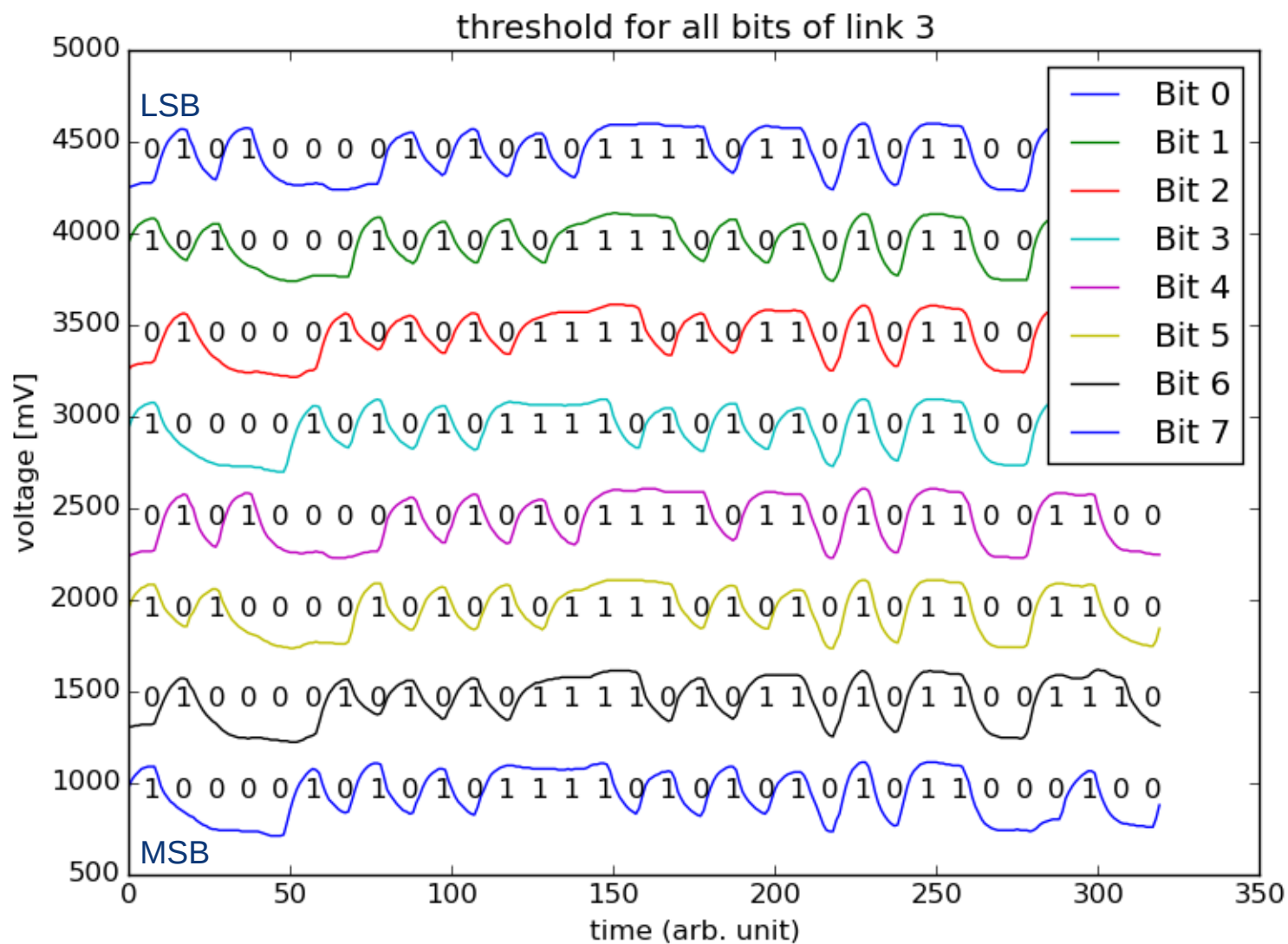


Comparison of DCDpp and DCDB4.1



DCDB4.2 lines stacked

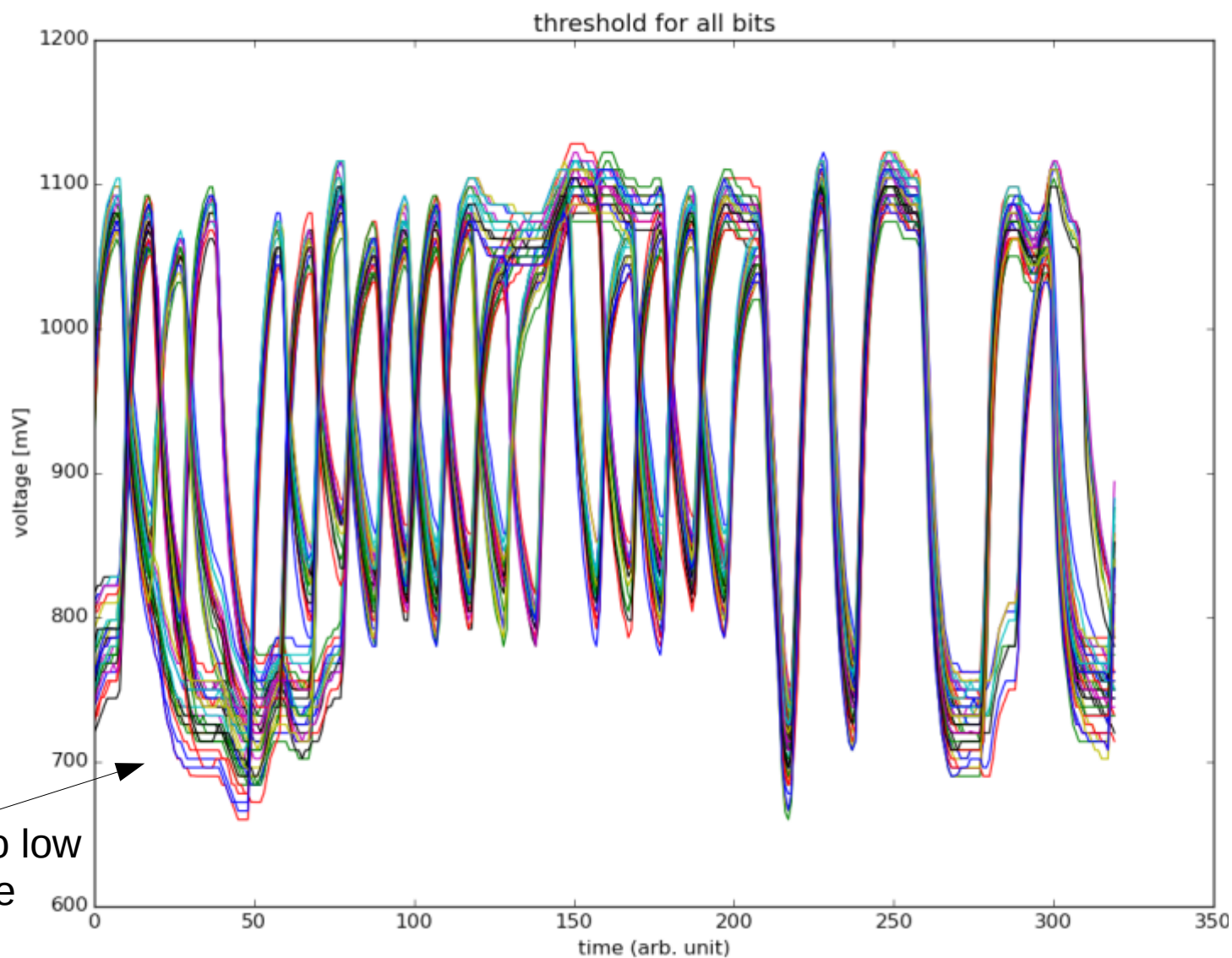
new test pattern



Index	MSB	LSB	Value
29	0	1 0 0 0 0 0 0	64
30	0	0 0 0 0 0 0 0	0
31	1	0 1 0 1 0 1 0	-86
0	0	1 0 1 0 1 0 1	85
1	0	0 1 0 0 0 1 0	34
2	0	0 0 1 0 0 0 1	17
3	0	0 0 0 0 0 0 0	0
4	1	0 0 0 1 0 0 0	-120
5	0	1 0 0 0 1 0 0	68
6	1	0 1 0 1 0 1 0	-86
7	0	1 0 1 0 1 0 1	85
8	1	0 1 0 1 0 1 0	-86
9	0	1 0 1 0 1 0 1	85
10	1	0 1 0 1 0 1 0	-86
11	1	1 0 1 1 1 0 1	-35
12	1	1 1 0 0 1 1 0	-18
13	1	1 1 1 1 1 1 1	-1
14	0	1 1 1 0 1 1 1	119

Index	MSB	LSB	Value
15	1	0 1 1 1 1 0 1	-69
16	0	1 0 1 0 1 0 1	85
17	1	0 1 0 1 0 1 0	-86
18	0	1 0 1 0 1 0 1	85
19	1	1 1 1 1 1 1 1	-1
20	0	0 0 0 0 0 0 0	0
21	1	1 1 1 1 1 1 1	-1
22	0	0 0 0 0 0 0 0	0
23	1	1 1 1 1 1 1 1	-1
24	1	1 1 1 1 1 1 1	-1
25	0	0 0 0 0 0 1 0	2
26	0	0 0 0 0 0 0 0	0
27	0	1 1 1 1 1 1 1	127
28	1	1 1 1 1 1 1 1	-1
29	0	1 0 0 0 0 0 0	64
30	0	0 0 0 0 0 0 0	0
31	1	0 1 0 1 0 1 0	-86
0	0	1 0 1 0 1 0 1	85

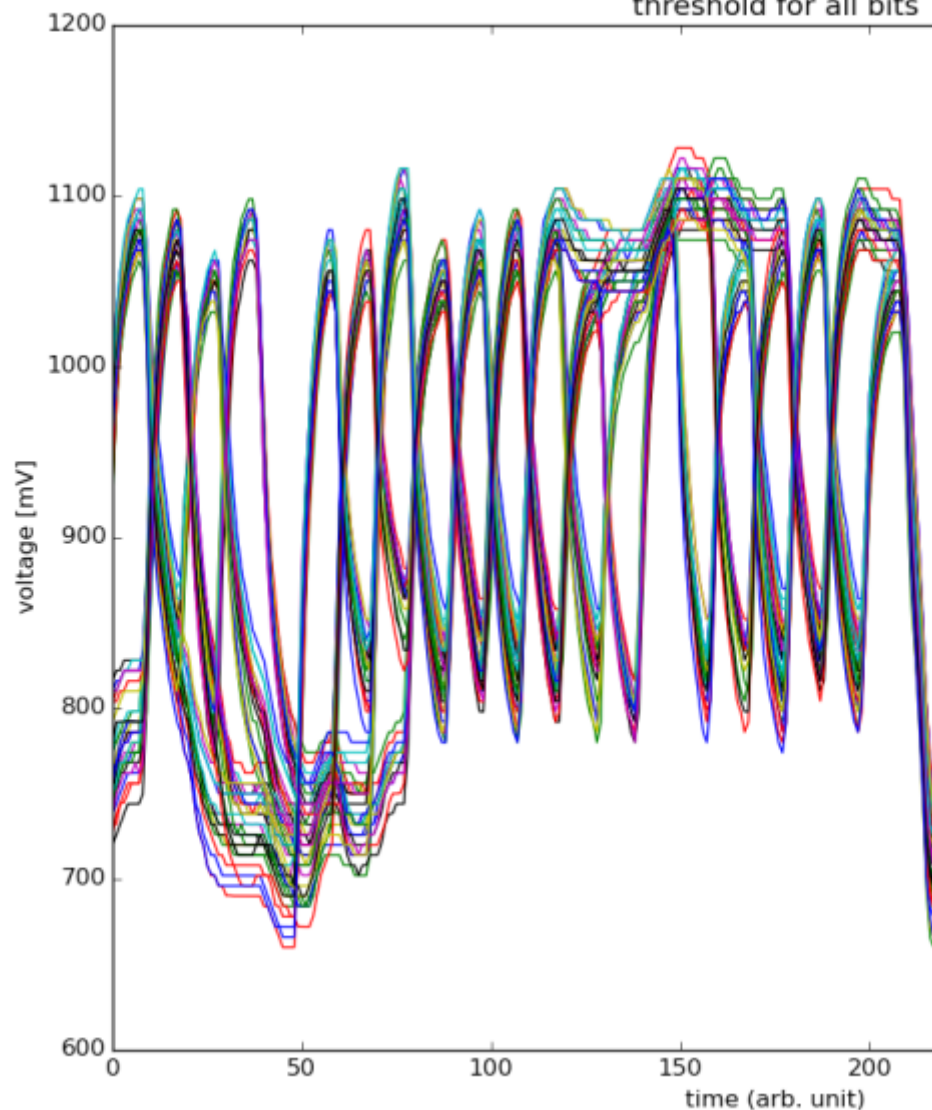
All bits of all links at 1.8V DVDD **DCDB4.2**, boost on, 305MHz



All bits of all links at 1.8V DVDD DCDB4.2, 305MHz

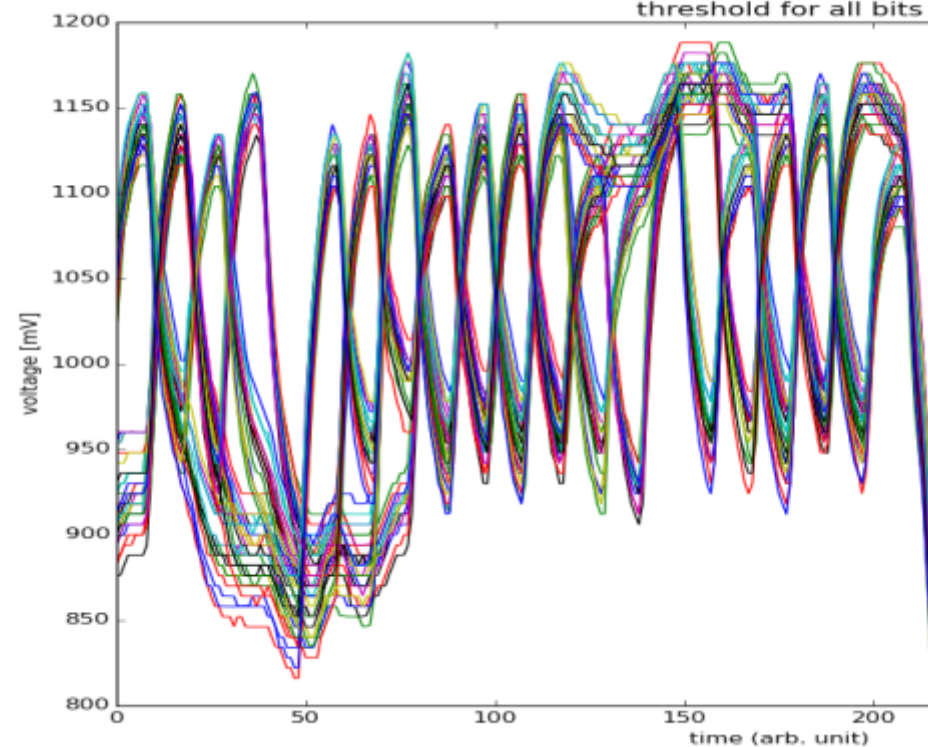
LVDS Boost On

threshold for all bits



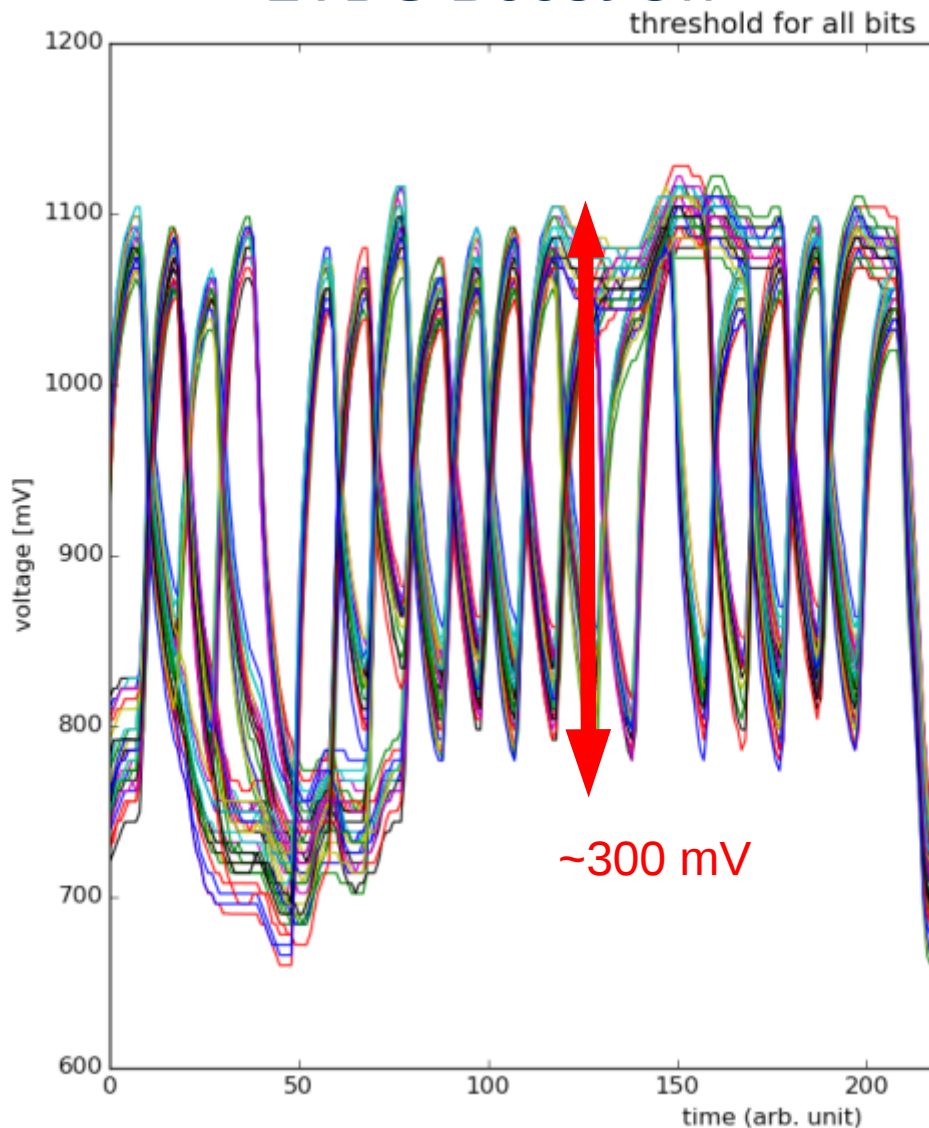
LVDS Boost Off

threshold for all bits

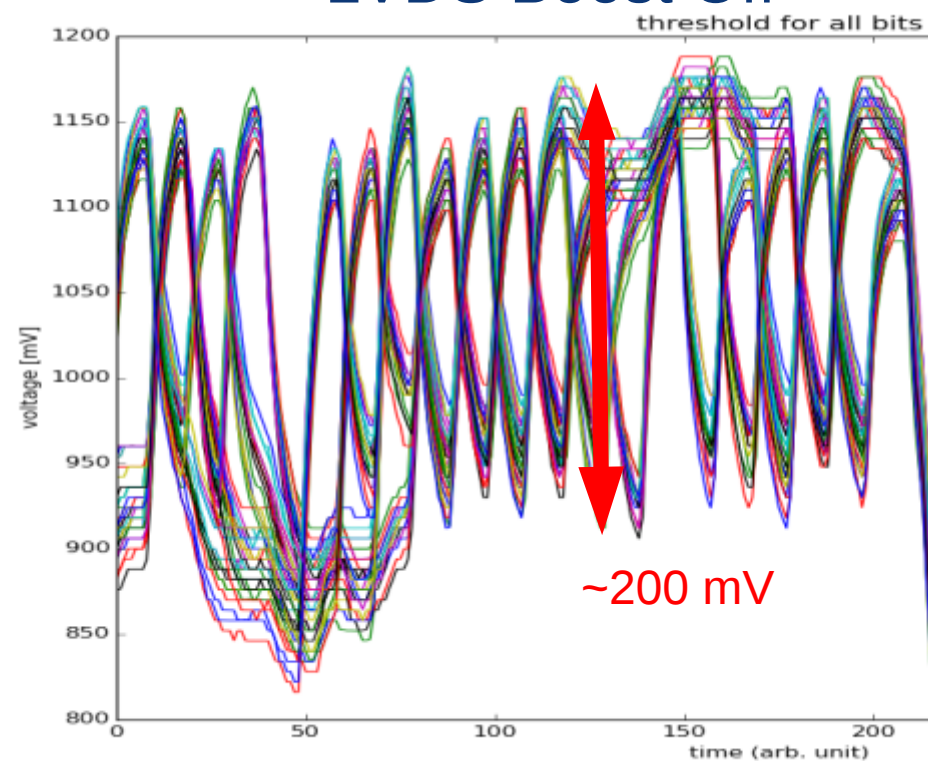


All bits of all links at 1.8V DVDD DCDB4.2, 305MHz

LVDS Boost On



LVDS Boost Off



- Both test pattern can be used to optimize the global/local delay settings
- The new LVDS boost implemented in DCD4.X helps to suppress bit errors and stabilize the communication
- The waveform is improved in comparison to the DCDpp
- Communication is significantly improved with DCD4.X