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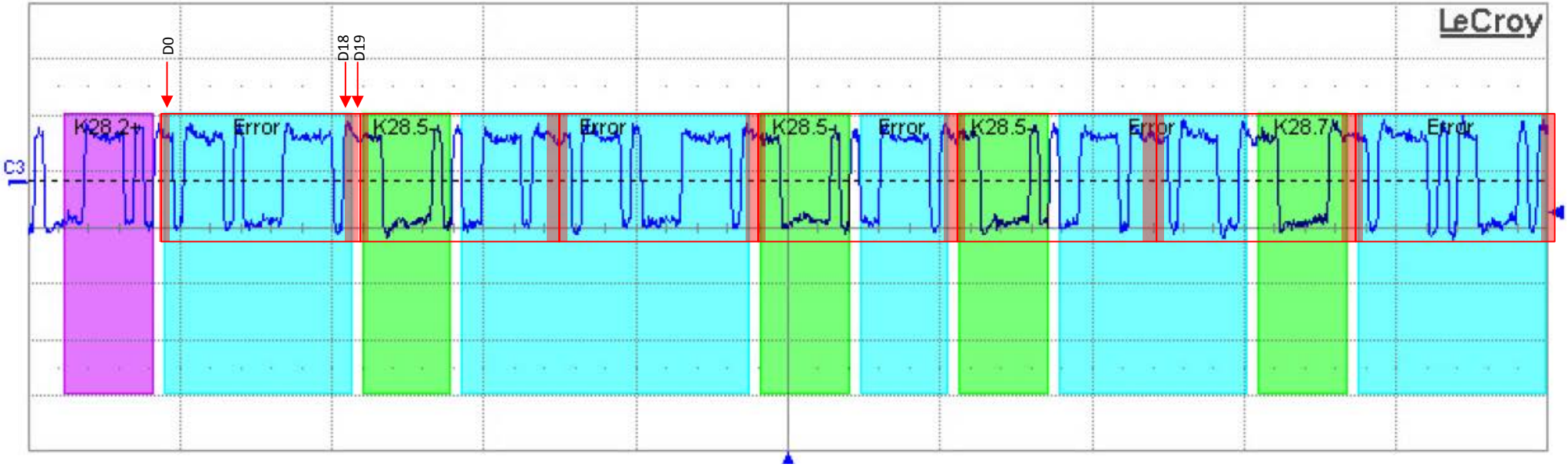
DHPT 1.2 Status

DEPFET-TB

Sep 27. 2016

Status

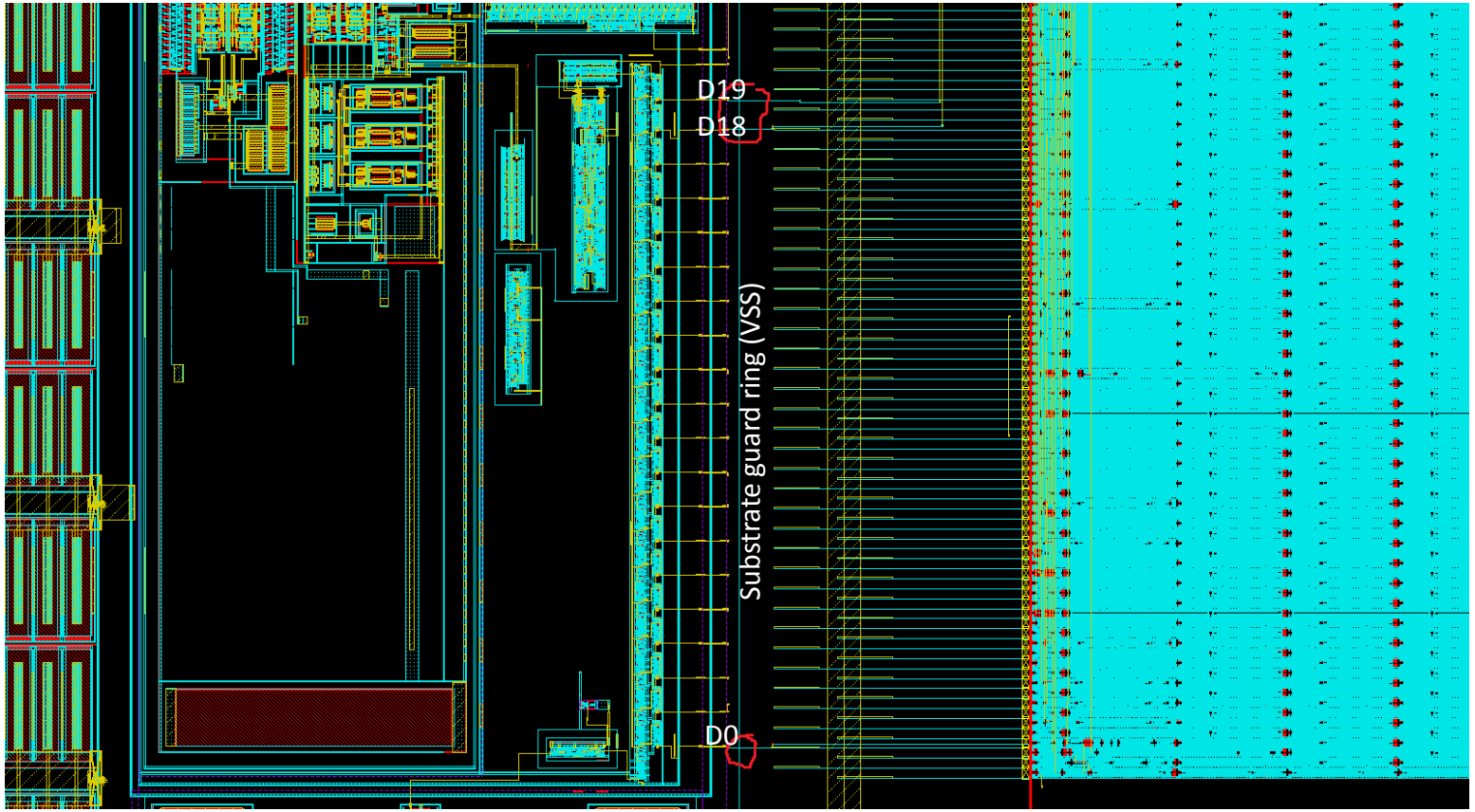
- DHPT 1.2 has a major bug: On the 20 bit data bus connecting the core to the serializer bits D[0], D[18], and D[19] are shorted to ground.
- The data link puts out invalid symbols rendering the DHHPT 1.2 unusable



DHPT 1.2 data link output: D[0], D[18], and D[19] of a 20 bit group are always 0 (inverted waveform)

Localization of the shorts

- The **auto routed data** lines are part of the **synthesized core**. Only D[0], D[18], and D[19] are routed on M1, all other bits use higher metal levels.
- The **substrate guard ring** on M1 was placed by hand in one of the **full custom cells**.
- The cells are combined at a later stage of the integration flow. Need LVS checks to spot and fix shorts.



Layout zoom: Data bus between digital core (right) and serializer (left), only M1 and M2 shown

Cause of events which lead to the mistake

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- Concurrent layout changes in a full custom layout cell containing the substrate guard ring and the synthesized core with routing between serializer and core caused the short.

- A LVS (layout versus schematic) check spotted this error and it was corrected by hand. A LVS clean layout was checked-in to our repository system.

- However, the layout submission was done from another machine (by another designer) where the design was not updated to the latest version from the repository server (human error).

Consequences

- The correct version of the layout (DHPT1.2B) has to be re-submitted end of September.
- No layout changes needed, since the correct layout has been in our repository all the time.
- However, functional test w/o data link and repeated simulations have been conducted to verify the chip as good as possible
  - The functionality of the data path, which cannot be tested due to the bug, has not been changed from DHPT 1.1 to DHPT 1.2

- Time line
  - DHPT 1.2B available end of December
  - Use DHPT 1.1 for production of beast modules (31pcs. @BN + 30 pcs. @HLL)
  - We could order 100 additional DHPT 1.1 chips. Do we need them (i.e. for ramp-up of pre-production)?

BACKUP

Bugs fixed in DHPT 1.2

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CML Driver

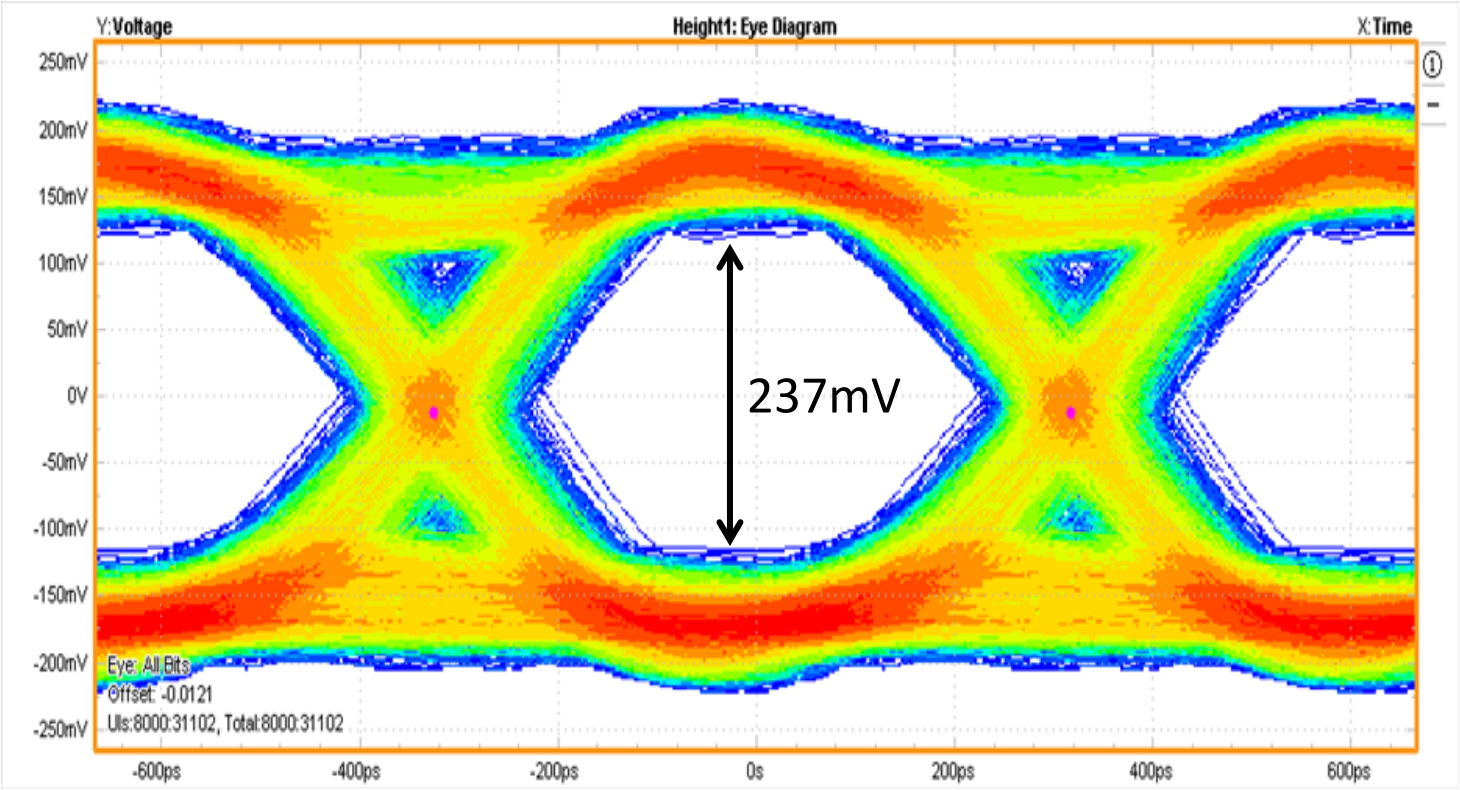
Test Results

- CML driver power routing
  - Ground rail (VSS) had a too high wiring resistance (~30 Ohm), parasitic extraction did not spot this because of substrate model
  - Rerouting of power nets → $R_{VSS} < 0.2$ Ohm

- CML driver bias routing
  - Removed ESD resistor in bias connection and reduced parasitic resistance → increase of bias current, less sensitivity to voltage supply

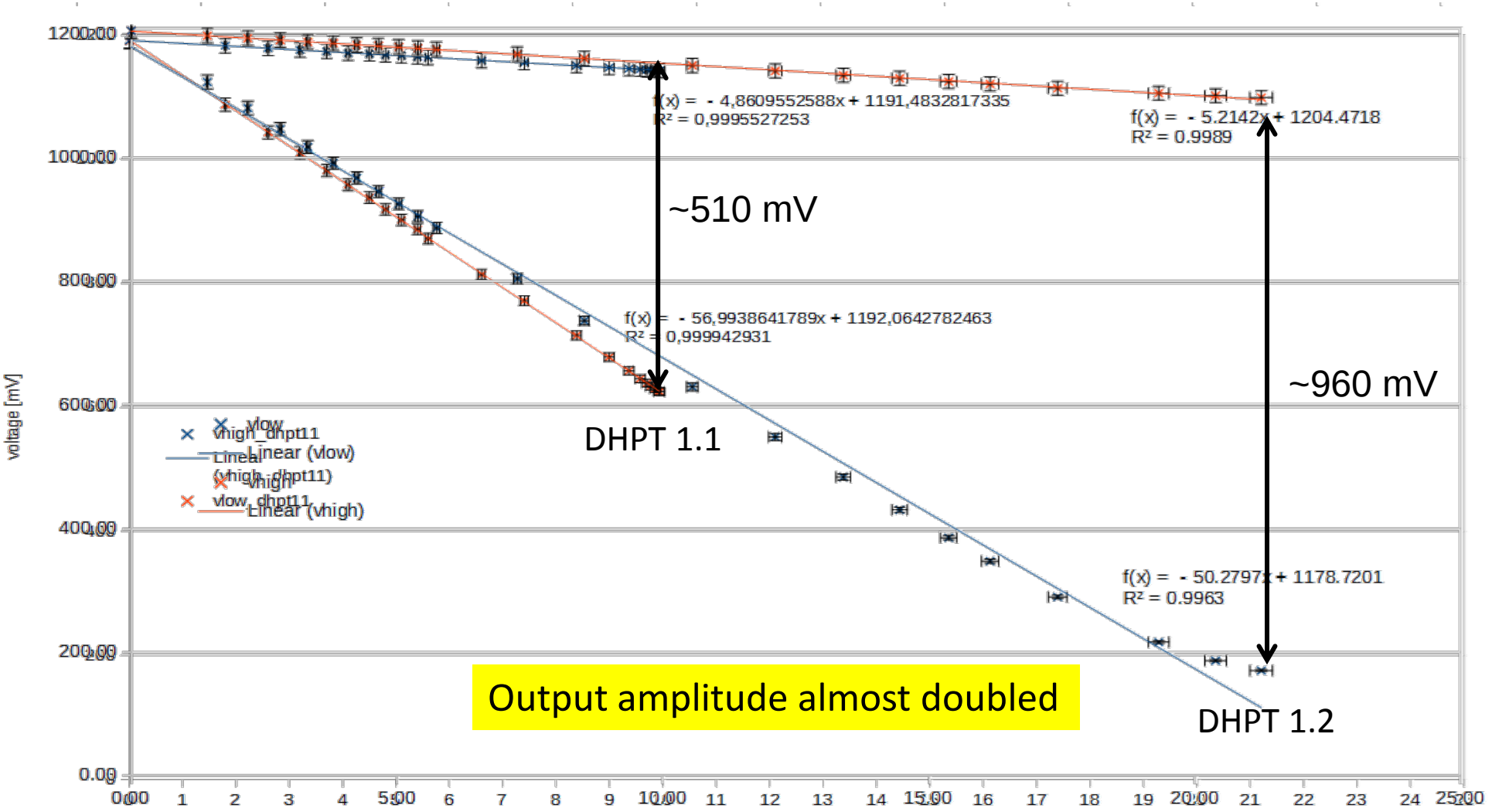
CML Driver Performance

- Eyediagram with 10m Infinband cable
  - IBIAS = 20, IBIASD = 60, Pll_cml_dly =2 (still a lot of headroom)



CML Performance Comparison

- CML output high and low level as a function of IBIAS (w/o termination)



Bugs fixed in DHPT 1.2

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Digital core

Test Results

- Mem dump
  - Data had some low probability to show corrupted values for the first few pixels when output was set to 800 MHz and clock compensation was on
    → fixed in HDL code

test not possible

- Internal system clock phase
  - The core clock started with an arbitrary phase after power-on
    → added controlled reset (delayed GCK) to the internal clock divider

- Gated mode sequence put out first word twice
  - Fixed HDL code

Enhancements for DHPT 1.2

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Digital core

	Test Results
• JTAG USERID changed: allows recognition of DHPT version – Implementation failure: used forbidden ID = xxx2 → (bit 0 of the IDCODE has to be 1)	X
• Gated mode: DATA_IN for the switcher can be selected to be controlled from either the *normal mode* sequence of the *gated mode* sequence (was *normal mode* only)	✓
• Added the DHPT ID in the memory dump frame header	test not possible
• Memory dump start address configurable	test not possible
• Bias register for LVDS receivers has fixed minimum value	✓