Characterization of the first full-sized DEPFET Modules for the Belle II Detector

B. Paschen for the DEPFET collaboration
SuperKEKB and the Belle II experiment

- **SuperKEKB**
  - Located at KEK, Japan
  - Upgrade of KEKB accelerator
  - Asymmetric e+e- collider
  - Peak *luminosity* $L = 8 \times 10^{35} / \text{cm}^2 / \text{s}$
    (40 times higher than KEKB, new record!)
  - $E_{\text{cm}} = m(Y(4s)) = 10.58 \text{ GeV}$
    $\rightarrow$ B-factory

- **Belle II**
  - Upgrade of Belle
  - Detector requirements:
    - Light material
    - **Vertexing capability**
    - Particle identification
    - Electromagnetic calorimeter
    - Data handling capabilities
The Belle II Vertex Detector (VXD)

- 4 layers double sided silicon strip (SVD)
  - R = 3.8 cm, 8.0 cm, 11.5 cm, 14 cm
  - Area ~ 1 m²
- 2 layers DEPFET pixel detector (PXD)
  - r = 1.4 cm, 2.2 cm
  - Area ~ 0.03 m²
Pixel Detector Requirements

Belle II PXD

- Occupancy: 0.4 hits/µm²/s
- Radiation: 2 Mrad/year
- Frame time: 20 µs
- Momentum range: Low momentum (< 1 GeV)
- Acceptance: 17°-155°
- Material budget: 0.2% X₀ per layer
- Resolution: 15 µm (50x75 µm²)

- Modest resolution (15 µm), dominated by multiple scattering → pixel size (50 x 75 µm²)
- Lowest possible material budget (0.2% X₀/layer)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services
The DEPFET Principle

- Field Effect Transistor (FET) on top of fully depleted silicon bulk
  - Quick charge collection (~ns)
- Charges collected in “internal gate”
  - Readout of modulated drain current → internal amplification
    \[ g_q = \frac{\partial I}{\partial q} \approx 500 \text{ pA/e}^- \]
- Periodical clearing of “internal gate” required

- Row-wise readout (rolling shutter)
  - Charge collection in “off-state” → Low sensor power consumption
  - Readout electronics outside of detector acceptance
The DEPFET Module

- High level of integration
  - Monolithic silicon module
  - Three regions:
    - Sensor (thinned, 75 μm)
    - Frame and balcony (420 μm)
    - End Of Stave (EOS) outside acceptance
  - 3 metal layers for interconnection
    - 2 Al + 1 Cu

- Three types of ASICs bump-bonded to module
  - 14 chips, ~3000 bumps in total

Switcher – row control

DCD – current digitizer

DHP – data handling and transmission (1.6 Gb/s)
Dedicated small Test System (Hybrid5)

- Dedicated small system for laboratory tests

- PCB with minimal number of ASICs for a full test system
- Latest iteration of ASICs is tested as well as matrix prototypes

DHP
(Data reduction)

DCD
(Drain current digitization)

Switcher
(Matrix steering)

Small matrix
(64 x 32 pixels / 16 gates, 128 drainlines)
ASIC optimization (Hybrid5)

- Timing optimization of ASIC communication with delay elements
- Small matrix (64 x 32 pixels / 16 gates, 128 drainlines)
- DHP (Data reduction)
- DCD (Drain current digitization)
- Switcher (Matrix steering)

- 256 analog channels per DCD → ADC transfer curves
Sensor optimization (Hybrid5)

- Optimization of DEPFET voltages for PXD9
  - Laser measurements
  - Source measurements

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- Laser focused through microscope
- \( \sim 3 \, \mu \text{m} \) spot size
- Laser moves over matrix – position resolution

\(~700 \, \text{pA/e}^-\)

\( ^{90}\text{Sr} \) source triggered

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Single and multi pix cluster

\[ g_Q \sim 700 \, \text{pA/e}^- \]

- multi pixel
- single pixel

\[ ^{90}\text{Sr} \] source triggered

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seed signal

cluster signal
Combined VXD Beam Test at DESY

- April 2016 at DESY
- 4 layers of SVD
- 2 PXD modules (backward direction)
  - CO₂ cooling in place
  - Integration of slow control
  - Integration of full data acquisition (DAQ) chain
Combined VXD Beam Test at DESY

- 4 GeV electron beam
- Triggered with 4 Scintillators
- Additional tracking with beam telescope

**Projected hit efficiencies:**

Average efficiency 99%
Outlook

- Four modules in preparation for “phase 2” test (BEAST)
- Commissioning of BEAST detector in spring 2017

Goal of Belle II

- 9 months/year
- 20 days/month

Slice of final VXD
(2 PXD + 4 SVD layers) + additional radiation detectors
Conclusion

- The first functioning Belle II PXD DEPFET modules have been characterized and tested at a beam test

- Lessons learned
  - Minor design changes in Module for final production

- Most recent iteration of ASICs verified with Hybrid 5 system
- Sensor optimized on Hybrid 5

- Production for BEAST and final experiment is ongoing

- Commissioning of first detector in experiment in spring 2017
- Commissioning of final detector with Belle II in 2018
# Backup - Yield of the Pilot Run

![Image](image_url)

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<th>W36</th>
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<td>98.96</td>
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<tr>
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<td>100.00</td>
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<tr>
<td>IB</td>
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<td>99.48</td>
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<tr>
<td><strong>Total</strong></td>
<td><strong>83.3%</strong></td>
<td><strong>66.6%</strong></td>
<td><strong>83.3%</strong></td>
</tr>
</tbody>
</table>

ratio of functional pixels
* destroyed by handling error
Peripherals and Routing

- Power distribution to ASICs
  - Line widths increased
  - SMD capacitors exchanged

- 300 MHz single ended signals
- 82 lines per ASIC pair
  - Cross talk observed
  - Routing spaced out

→ Design changes implemented in ongoing production
The DEPFET Collaboration @ Belle II

- Original collaboration: DEPFET pixel detector @ ILC (since 2002)
- Now: design, deliver and operate the PXD for Belle II

IHEP Beijing, China (Z.A. Liu)
Charles University, Prague, Czech Rep. (Z. Dolezal)
DESY Hamburg (C. Niebuhr)
University of Bonn (J. Dingfelder)
University of Hamburg (C. Hagner)
University of Heidelberg (P. Fischer)
University of Giessen (W. Kühn)
University of Göttingen (A. Frey)
University of Karlsruhe (T. Müller, I. Peric)
University of Mainz (C. Sfienti)
MPG Semiconductor Laboratory, Munich (J. Ninkovic)
Ludw.-Max.-University, Munich (T. Kuhr)
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Technical University, Munich (S. Paul, A.Knoll)
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IFIC, Valencia, Spain (J. Fuster)
University of Tabuk, Saudi Arabia (R. Ayad)

DEPFET@Belle II

Management:
Project Leader
C. Kiesling (MPI)

Technical Coord.
L. Andricek (HLL)

IB- Board
Chair: J. Dingfelder (Bonn)

Integration Coordinator
Shuji Tanaka (KEK)
Characterization in the Laboratory

- 256 analog channels per DCD
  - Transfer curves and parameter optimization

- Timing of ASIC communication
  - Delay elements optimization with bit error tests

![Graph showing ADC counts vs. injected current](image1.png)

![Heatmap showing delay scans](image2.png)
Matrix Tests in the Laboratory

- Illumination with visible light
- Illumination with red laser
- Cd radioactive source