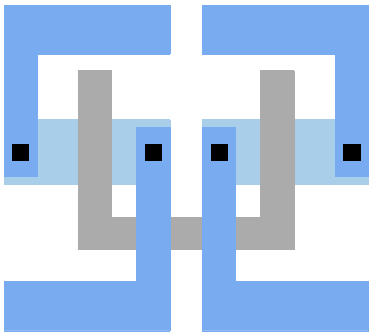
UNIVERSITÄT
HEIDELBERG

S3B Firmware Development & PXD5 Matrix Tests



Jochen Kinzel

jochen.kinzel@ziti.uni-heidelberg.de

2nd International Workshop on
DEPFET Detectors and Applications

Ringberg Castle

May, 5th 2009

Overview

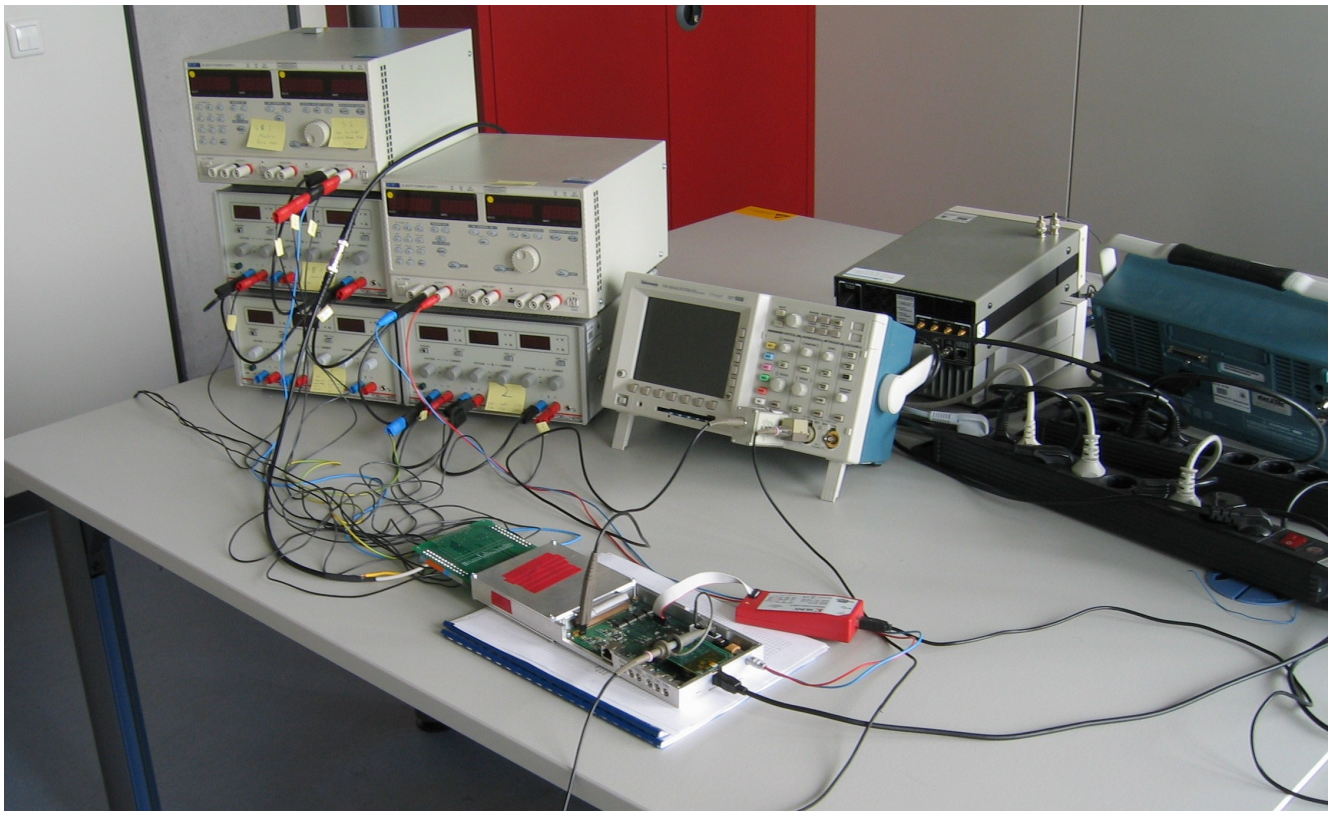
- Part I: S3B test environment development
  - S3B test environment in Mannheim
  - General information about the S3B
  - S3B firmware

- Part II: PXD5 matrix tests
  - Current state

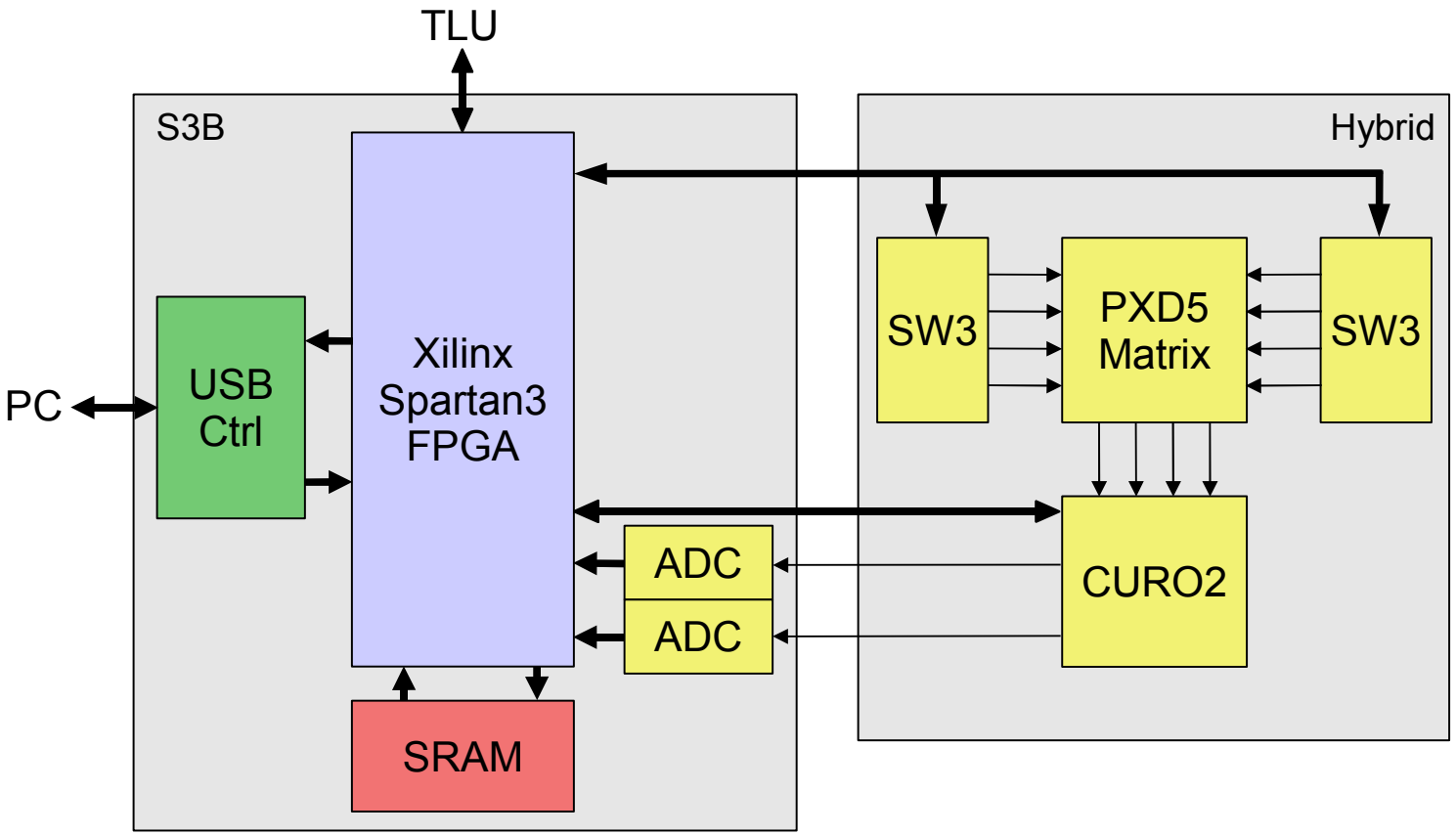
S3B Test Environment in Mannheim

The S3B test environment is running in Mannheim!

- Fully assembled hybrid board with a PXD5 matrix, two Switcher3s and a CURO2 chip
- S3B as hardware read out platform
- Data acquisition software (by Sergey Furletov, Uni Bonn) is set up and running

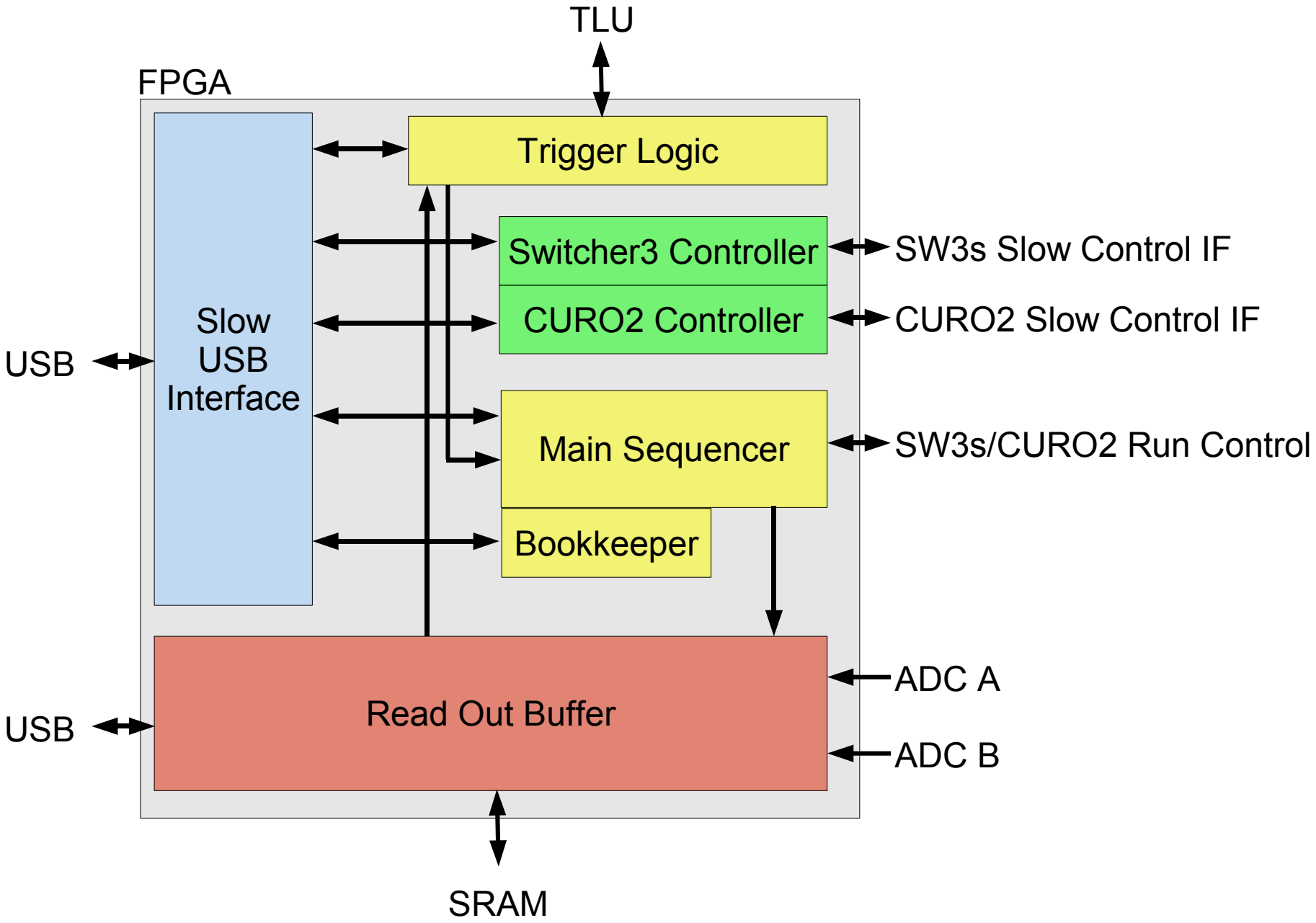


S3B: General Information



- FPGA controls the CURO2 and the two Switcher3 chips
- Raw analog pixel data is sampled by the CURO2 and digitalized by two ADCs
- Raw digital pixel data is processed by the FPGA. The SRAM is used for buffering
- USB 2.0 Controller establishes a communication channel to the host PC

S3B Firmware



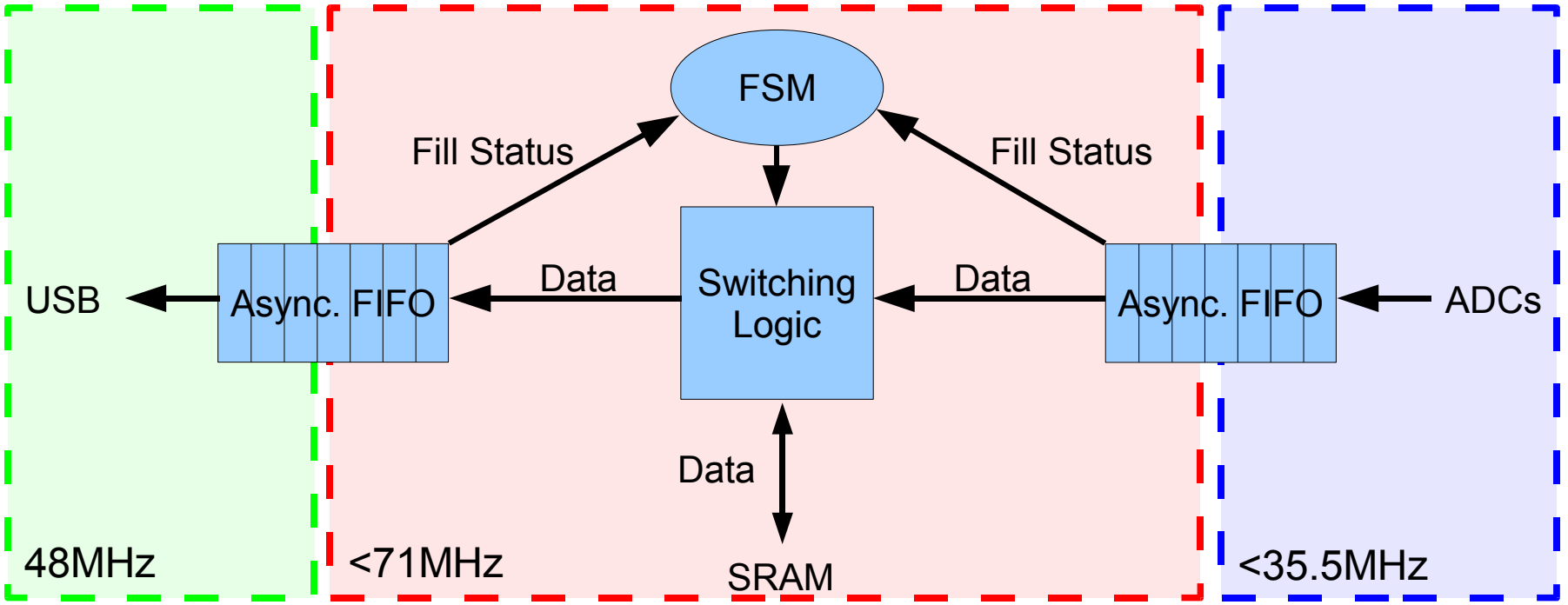
Switcher3 Integration

- Switcher3 controller module enables reading from and writing to the Switcher3's control registers and RAM
  - ➔ Simulated and tested

- Switcher3 controlling mechanisms are successfully integrated into the data acquisition software

- Complex abilities of the Switcher3's sequencer are currently not used
  - A very simple sequencer program makes it behave like a Switcher2
  - Only slight modifications in Main Sequencer programs necessary

Read Out Buffer for Non-Zero-Suppressed CURO Read Out



1. ADC values are stored into the input FIFO buffer
2. Data is forwarded to the SRAM
3. While no new ADC values are to be processed, Data from the SRAM can be transfered to the output FIFO buffer
4. Data in the output FIFO buffer is read by the host PC via USB

Important improvements:

a) Storing new ADC values is independent from reading data via USB

b) Reading and writing is done within the same clock domain

General issue:

With the deployed combination of FPGA and SRAM, a max. SRAM writing frequency of only ~71MHz is possible

→ max ADC clock frequency is ~35.5MHz

Overview

- Part I: S3B test environment development
  - S3B test environment in Mannheim
  - General information about the S3B
  - S3B firmware

- Part II: PXD5 matrix tests
  - Current state

Current state: static problems

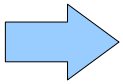
1. Broken column detected → solved by destroying the corresponding bond wire between the matrix and the CURO

First PXD5 Matrix Test Results

Current state: static problems

2. High current from U_source (matrix) to GND even if all DEPFET transistors should be switched off (33mA @ 7V U_source)

→ Not understood, not solved.



Target operating conditions are currently not applicable.
So testing the system's dynamic behavior is not possible.

Summary

S3B test environment:

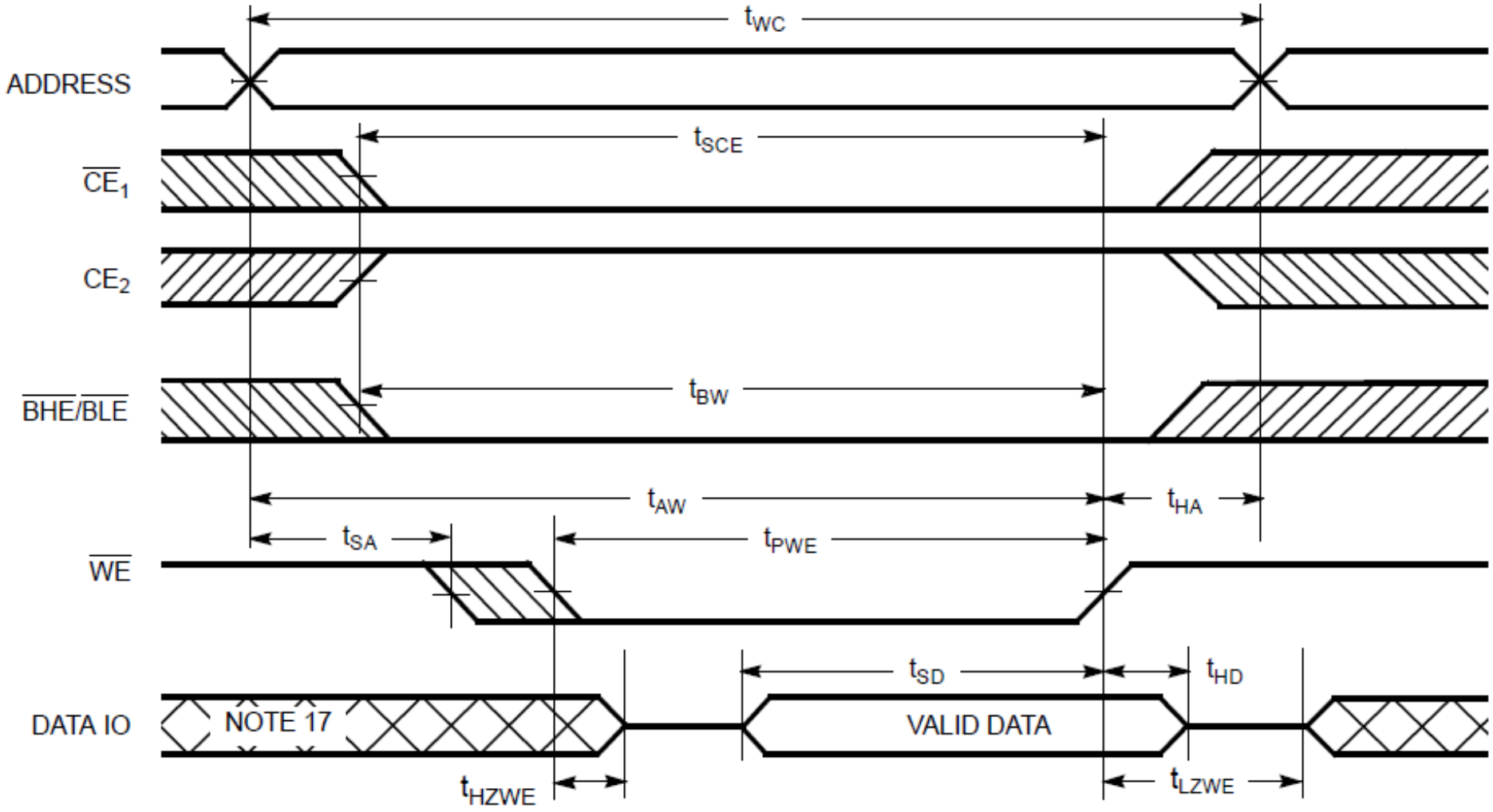
- S3B test environment is set up and running successfully in Mannheim
- S3B firmware is implemented – testing phase not finished yet

PXD5 matrix tests:

- First PXD5 matrix tests were not very successful due to static problems

Thank you!

SRAM Write Cycle Timing Diagram



Min values: t_{WC} 10ns, t_{SCE} 7ns, t_{AW} 7ns, t_{HA} 0ns, t_{SA} 0ns, **t_{PWE} 7ns**, t_{SD} 5.5ns, t_{HD} 0ns, t_{LZWE} 3ns, t_{BW} 7ns

Max values: t_{HZWE} 5ns