



Bump Bonding Status



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2nd International Workshop on DEPFET

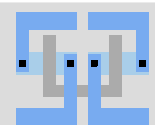
detectors and applications

Ringberg Castle

03. - 06.05.2009

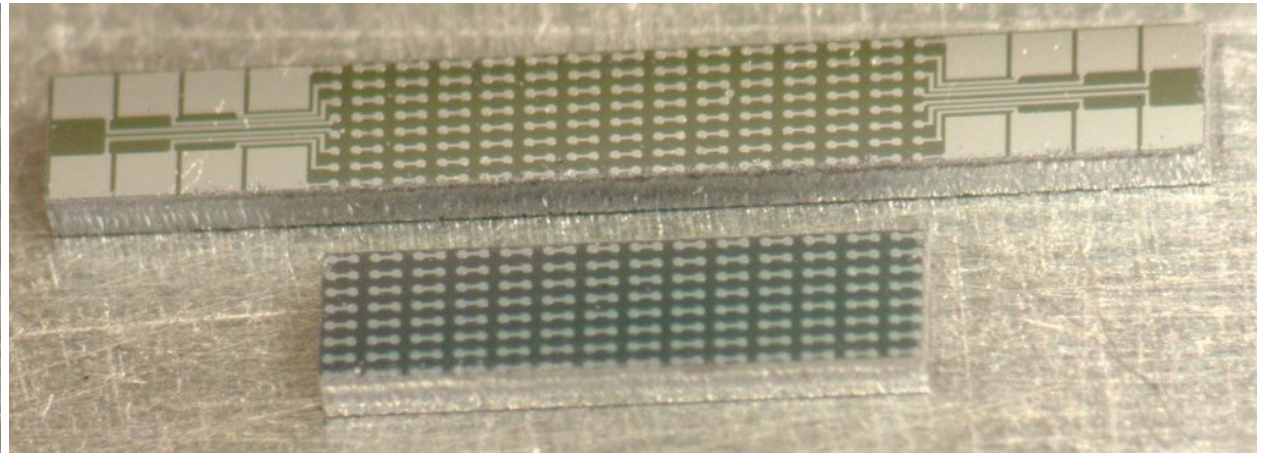
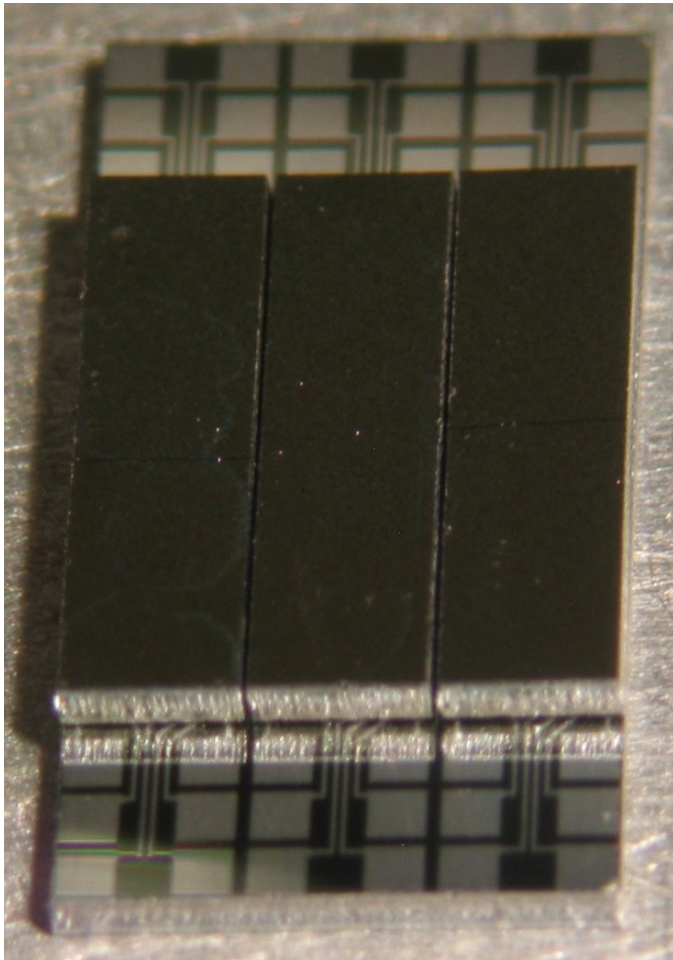
Content

- find minimum flip-chip force for gold in gold flipping
- destruction tests on PXD5 bumping teststructures
- destruction tests on UMC018 bumping teststructures
- preparations for evaluating solderball jetting



Bump Bonding Force Tests

- Dummy chips made in DEPFET technology
 - only 1 metal layer

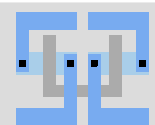


DCD dummy chip and substrate
224 pads

triple dummy substrate and chips

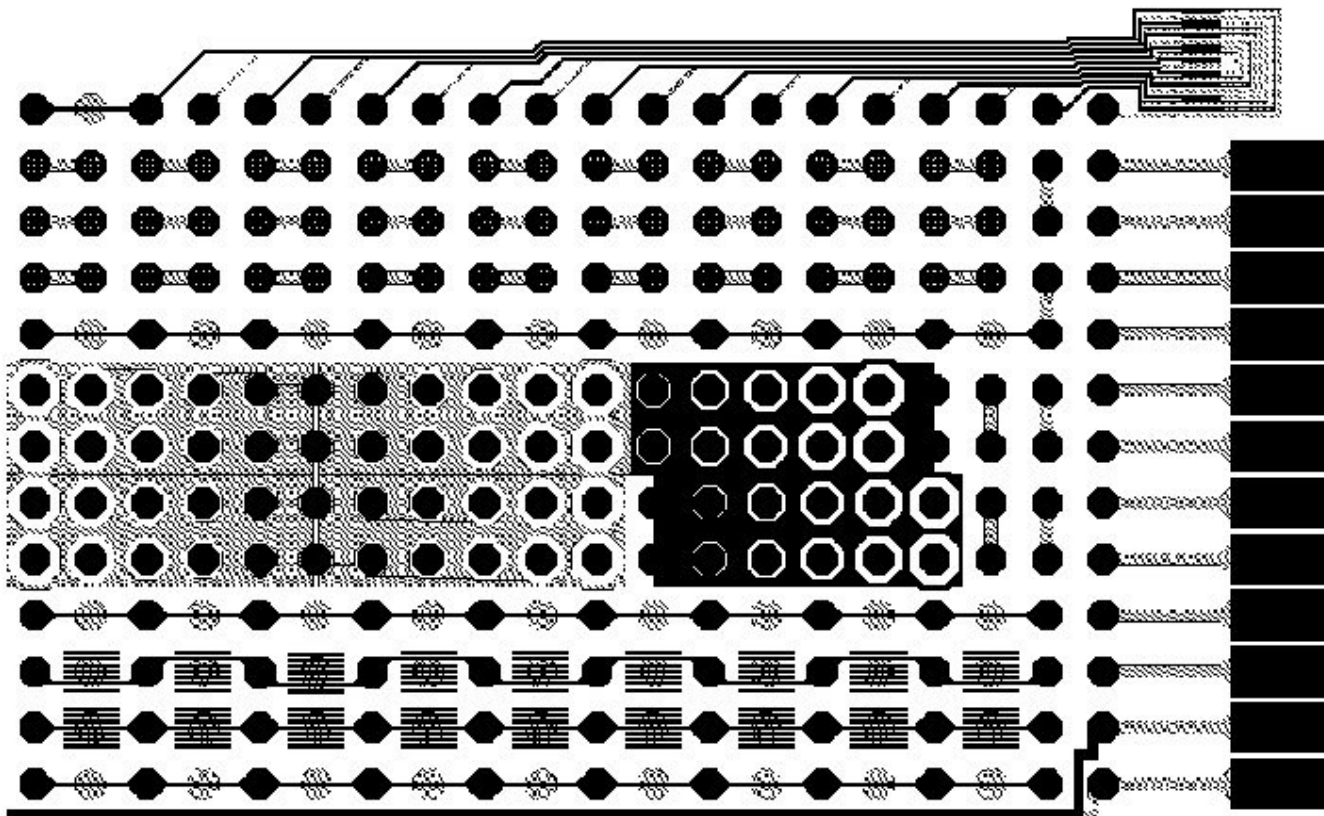
Bump Bonding Force Tests

- check how low flipchip force can be
 - 20 singles and 10 tripples flipped
 - “double bump”: bumps on chip and substrate
- single dummies:
 - 20g/bump
 - chip moves slightly sideways when bump-tails are touching
 - 1 of 180 snakes not connected
 - ok with 110gr/bump → bumpheight not uniform
 - 9g/bump coining + 20g/bump flipping
 - less chip movement
- tripple dummies:
 - flip-chip head larger then chip → all 3 chips pushed at once
 - need to increase force with every chip to ensure 20g/bumps (5kg, 10kg, 15kg)
 - Ineed chip-size head to get single dummy results
 - laser-cut chip edges not flat → some chips didn't fit

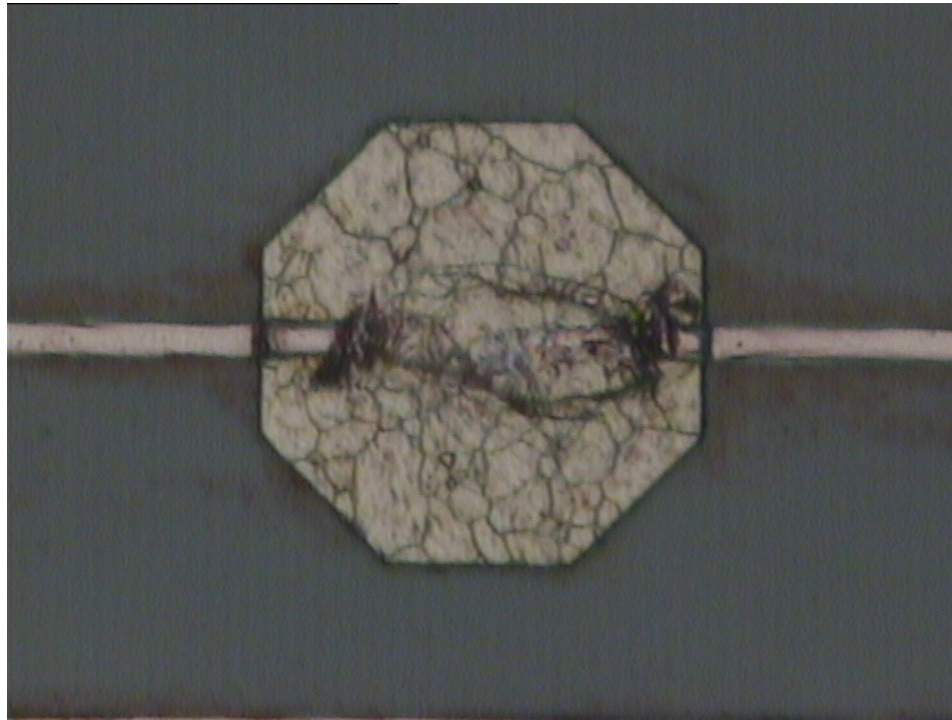


PXD5 Bumping Test Structures

- 6 test structures from PXD5 with 2 metal layer
 - test shorts between metal2 pad and metal1
 - 7 μm trace, 60 μm pad, 110 μm pitch
- measured resistance before and after bumping



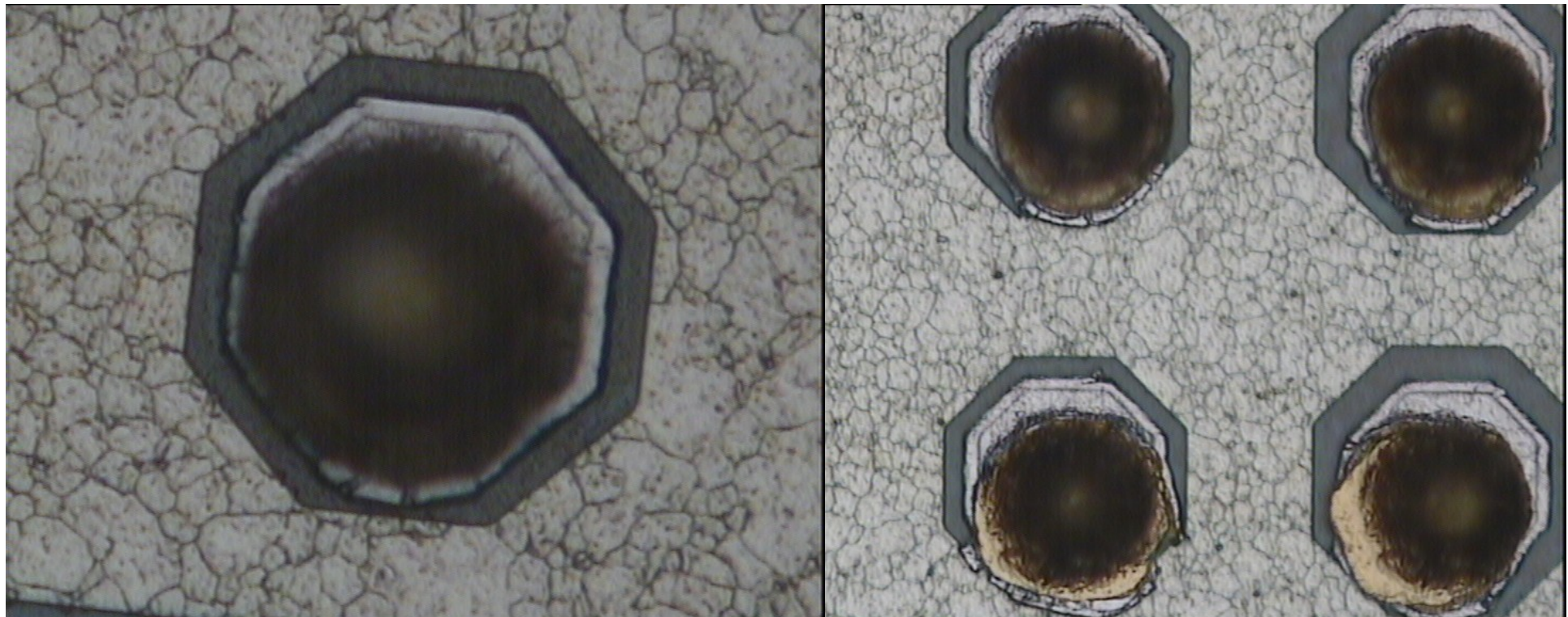
- Bumping on pads with a single trace was hardly possible
 - bonded bumps created shorts between trace and bump
 - removed bumps also removed trace
- Pads with multiple traces and 2 layered pads were bondable
- → metal layers in stream-out, stream-in procedure switched???
 - the trace should be below the pad according to Manuel's description



Pad after unsuccessful bumping

PXD5 Bumping Test Structures – Clearance

- bonding force while placing the bump squashes pad

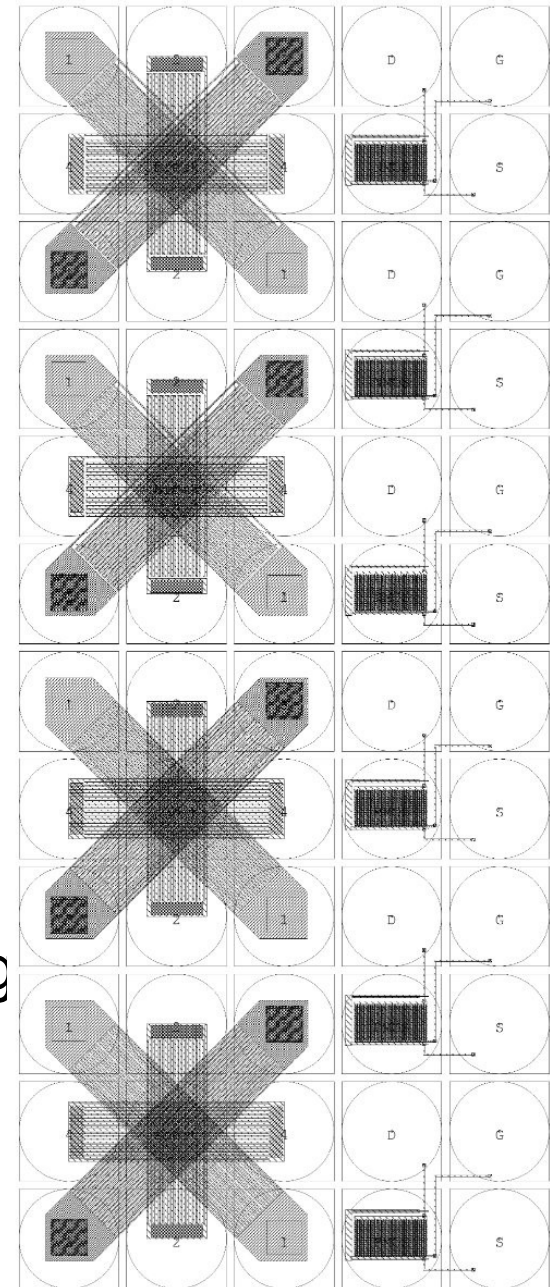


low power bonding; 4 μ m gap

high power bonding; 4 μ m + 8 μ m gap

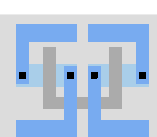
UMC018 Bump Teststructures

- 4 teststructures per chip
 - 2x poly - metal3 short test (parallel traces)
 - 2x poly - metal3 break test (snake structures)
 - 1 μ m width
- 6 transistors
 - 3x NMOS and 3x PMOS transistors
 - l=400nm, w=800 μ m
- metal crossings and transistors under pad
 - metal4 - metal6 used for pad
 - 65 μ m pad diameter
- measured resistance and characterized transistors before and after bumping and flipping
 - flipping simulated with glas plate



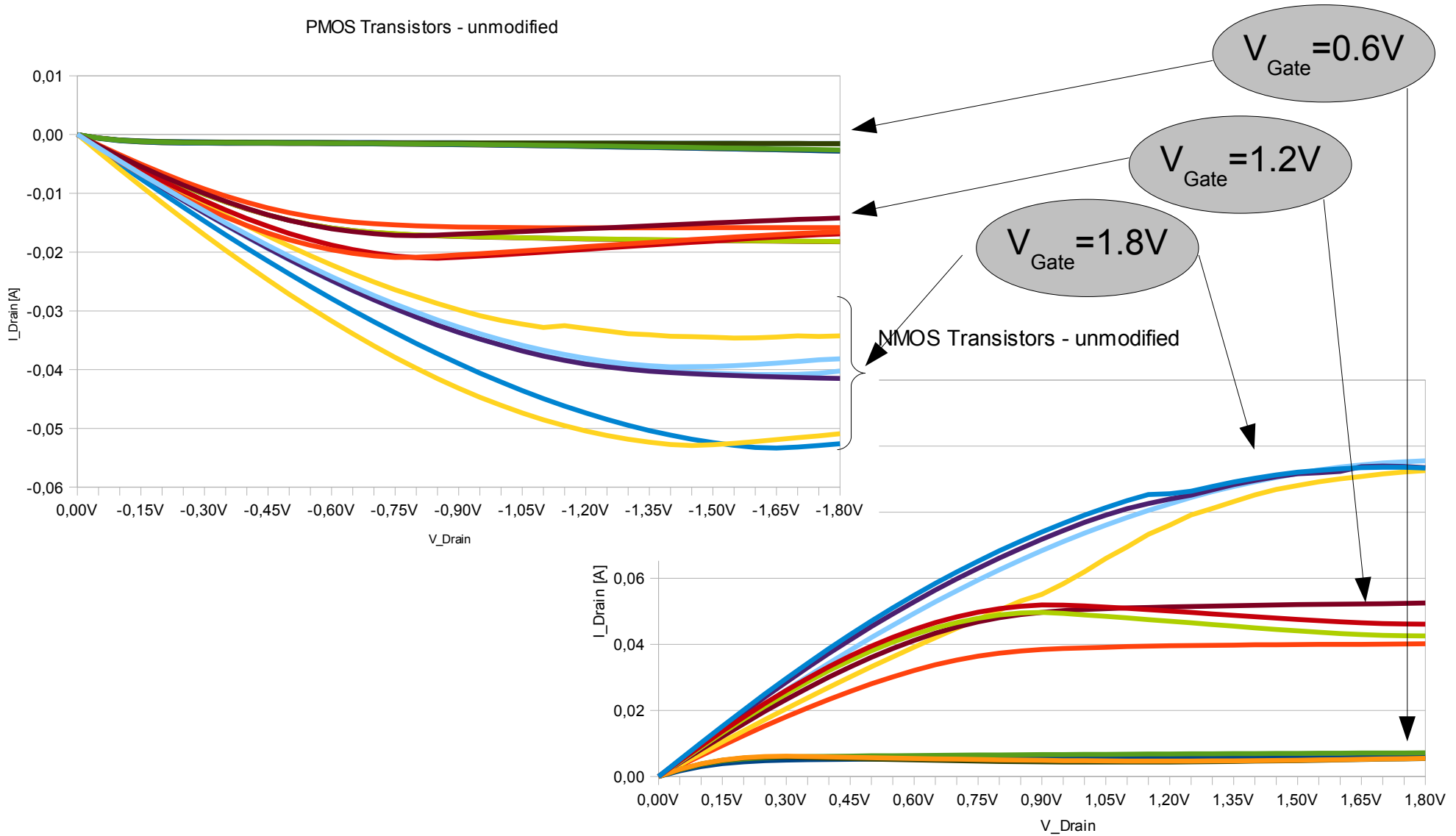
UMC018 Bump Teststructures

- no problems bumping on metal4 – metal6 pads
- no resistivity changes or shorts measured in layers poly – metal3

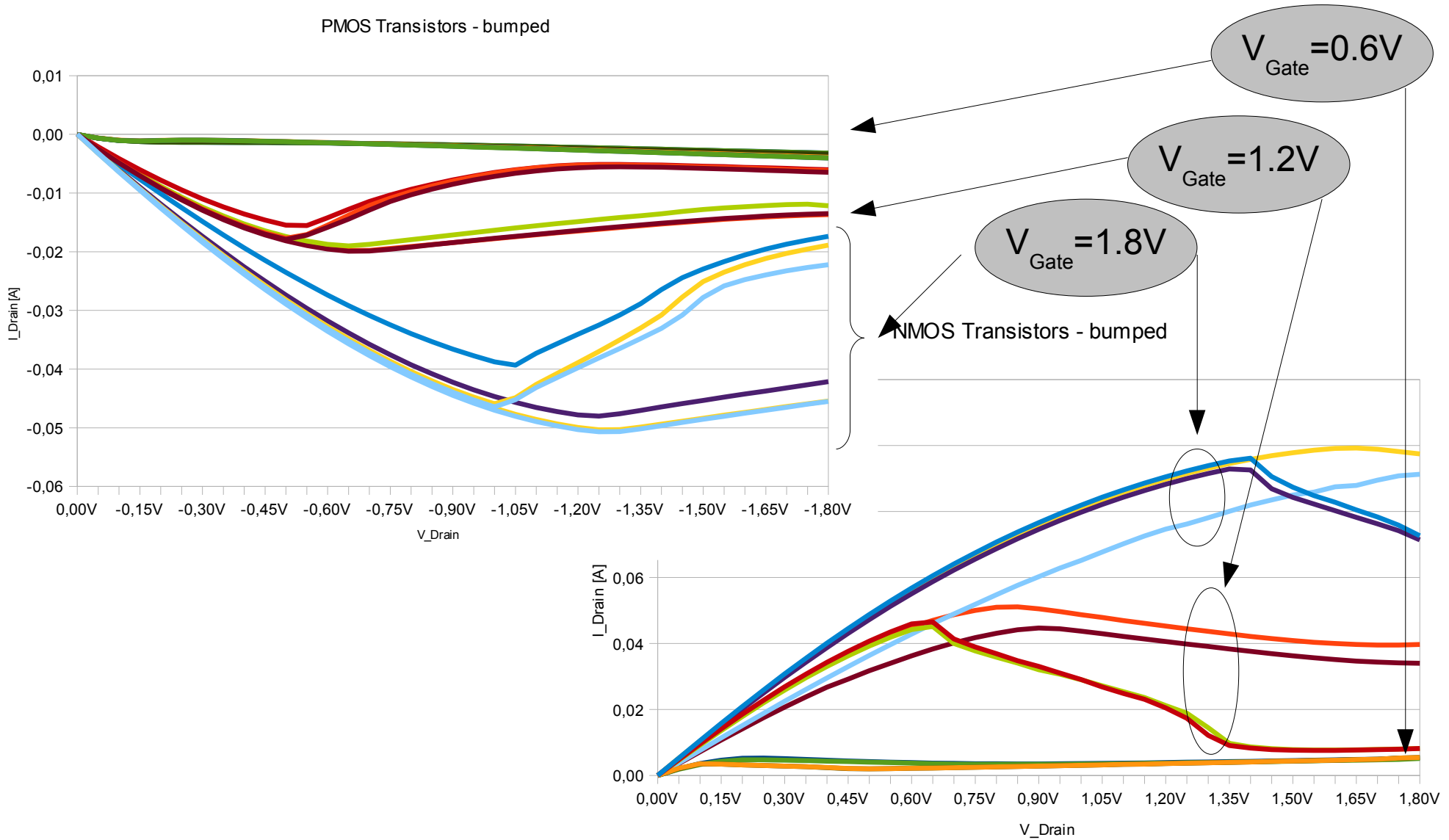


UMC018 Bump Teststructures

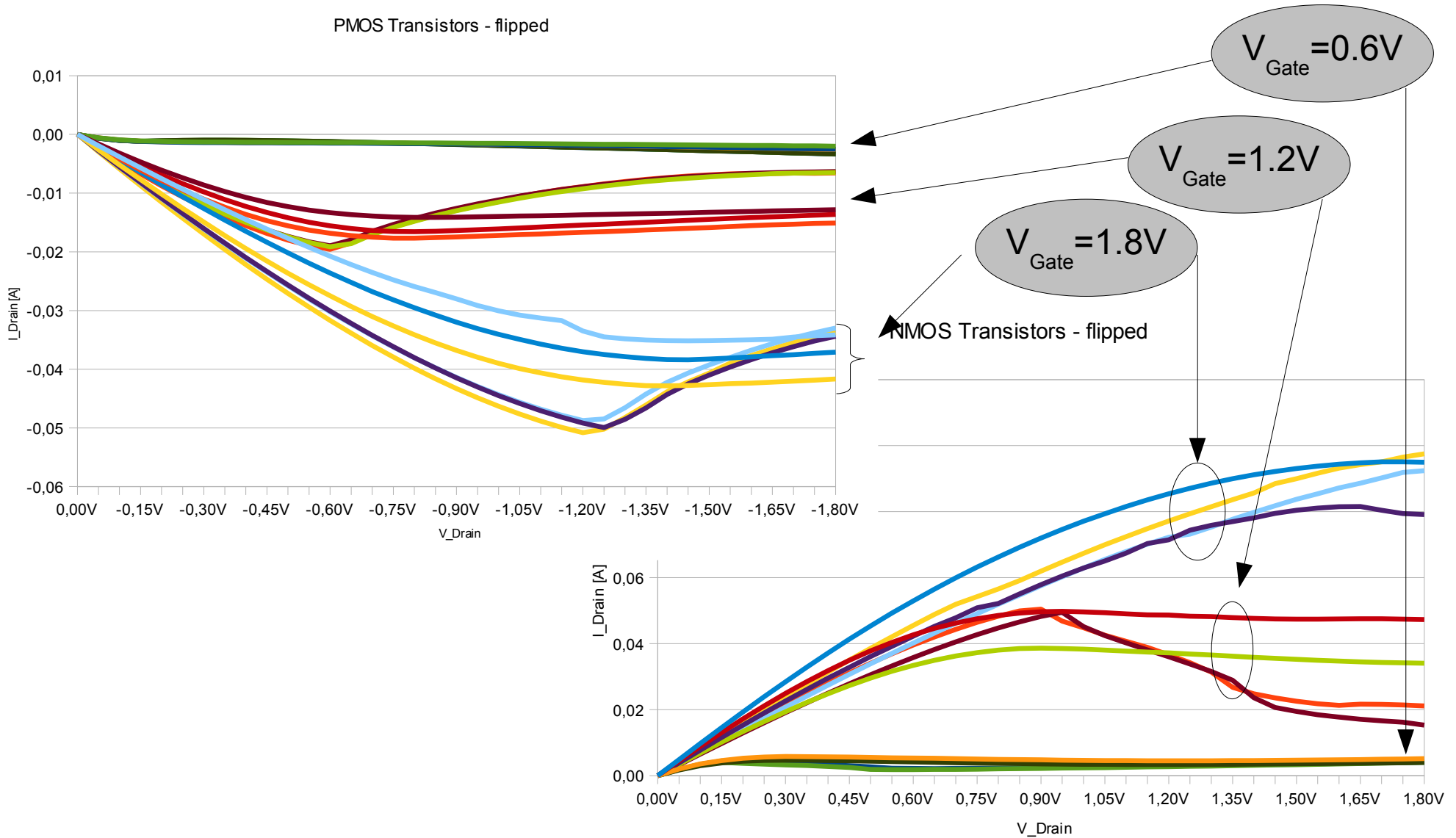
- 3x NMOS and 3x PMOS of 2 chips before bumping



- Transistors after bumping



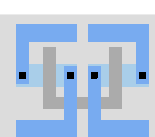
- Transistors after flipping



- coined bumps needed as UBM for jetting solderballs
 - 60 μ m flat
- 40g/bump coining
 - 40 μ m diameter of flat area
 - 70 μ m bump diameter
 - 20 μ m height
- 130g/bump coining
 - 60 μ m diameter of flat area
 - 70 μ m bump diameter
 - 10 μ m height

Solderball Jetting

- have sent some DCD dummies to PacTec for jetting solderballs
 - ~20 chips, singles and tripples
 - bumped and coined
- try soldering chips
- try rework of chips
 - Au bump with SnAg ball might be hard to rework
 - Pd bump with PbSn ball better → test Pd-bumping



- flipping Au-bumps with 20g/bump possible
- PXD5 bumping teststructures
 - trace below pad could not be tested
 - 6 μ m gap between 60 μ m pad and trace
- UMC018 teststructures
 - no effects on poly up to metal3
 - transistors change
- solderball jetting
 - coining of bumps for UBM with 130g/bump
 - waiting for return of balled dummies

Thank you!