DCD2 test system and results

Ringberg 05/2009

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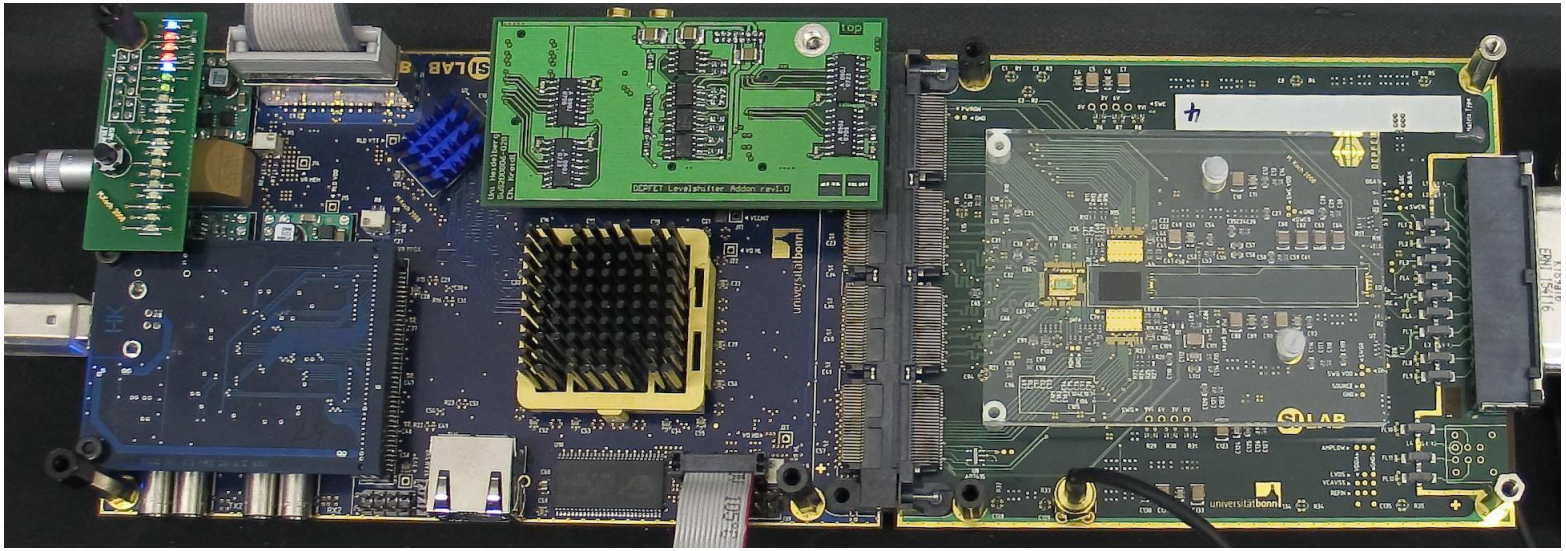
DCD2 test system



- high speed FPGA board
  - PC connectivity (USB)
  - data handling
  - DCD / Switcher3 connections
- level shifter add-on for Switcher3

- Hybrid
  - DCD2 tests
  - Switcher 3 Integration
  - standard & long matrix

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measurement setup

- things to remember:
  - DCD2 has 72 channels (24 designated ‘fast’; used here)
  - each channel has two ADCs, working interleaved (Left / Right ADC)
    - data separation is possible
  - ADC provides 8 bit resolution

- measure ADC response (digital out) with changing input current
  - use precision, low noise external current source; range 0-30µA, step 25nA
  - feed into regulated cascode
  - subtract some (fixed) current after cascode (utilize full ADC range)
  - take ≥ 1000 separate (L/R) samples for each current

- measure total range, gain, INL, DNL, noise

- results depend on specifically chosen bias settings

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measurement setup

- shown in the following plots
  - 2 data sets
    - supply voltage 1.8V
    - supply voltage 1.9V
  - displayed frequencies
    - channel frequency (1.25 … 12.5 MHz)
      - sampling time = (channel frequency)$^{-1}$
    - channel frequency × 8 = channel clock (10 … 100 MHz)
    - channel clock × 6 = readout clock (60 … 600 MHz)
  - data for separate and combined (L/R) ADCs

- power consumption (total)
  - @1.8V : 360mW
    - /72 = 5mW
  - @1.9V : 435mW
    - /72 = 6mW
  - only small frequency dependency

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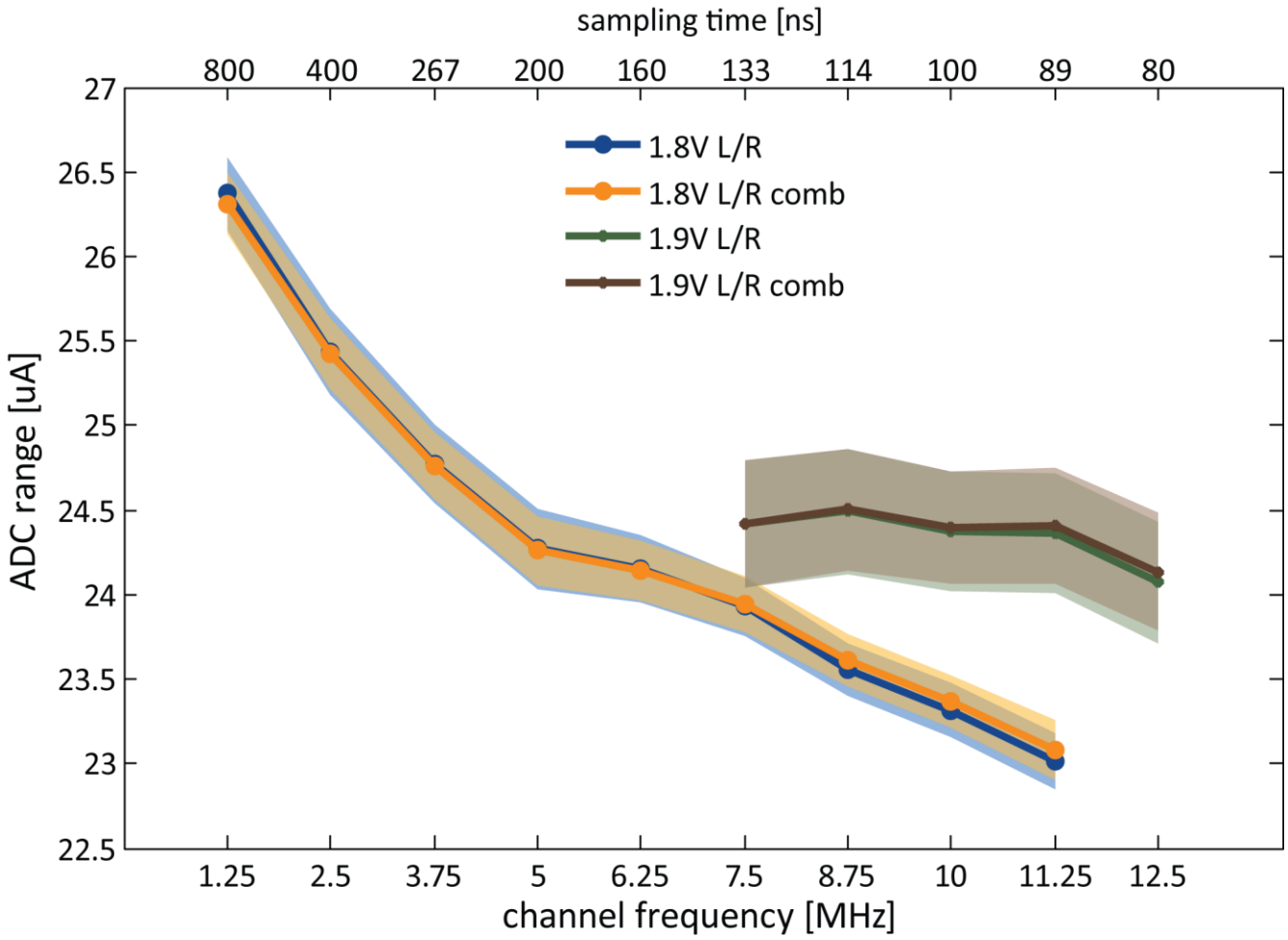
ADC range

- total range
  of ≈ 24µA achievable
  in all channels
  @ 12.5MHz



- range loss at higher frequencies → ADCs start losing codes
- can be ‘fixed’ with higher supply voltage

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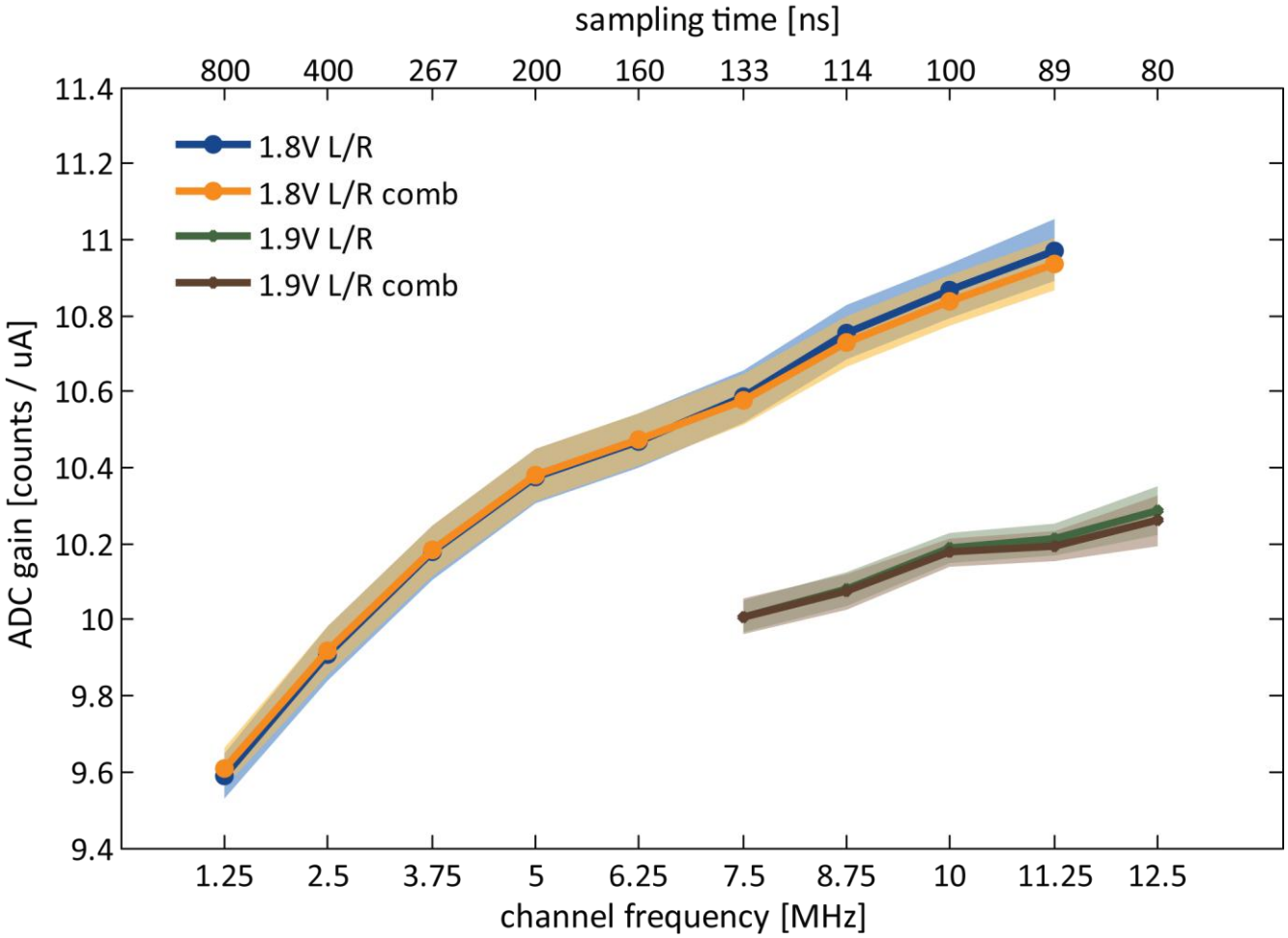
ADC gain

- best straight line fit (error-weighted) to data
- gain 10.2 ± 0.1 @ 12.5MHz



- remember: 1µA ≈ 10 ADC steps
- → 1 LSB ≈ 100nA

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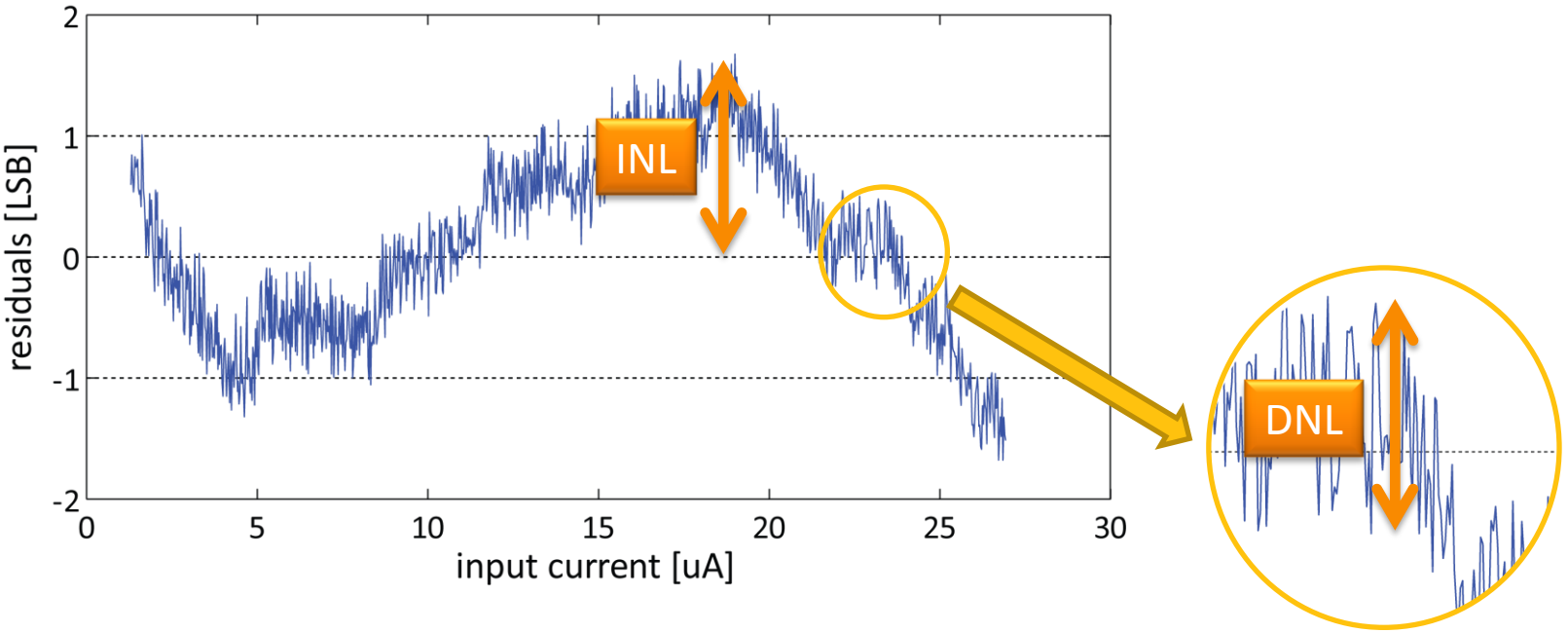
Residuals / INL / DNL

- subtract best-straight-line fit from data → residuals



- maximum integral non-linearity: max. distance data ↔ line fit
- maximum differential non-linearity: max. single step

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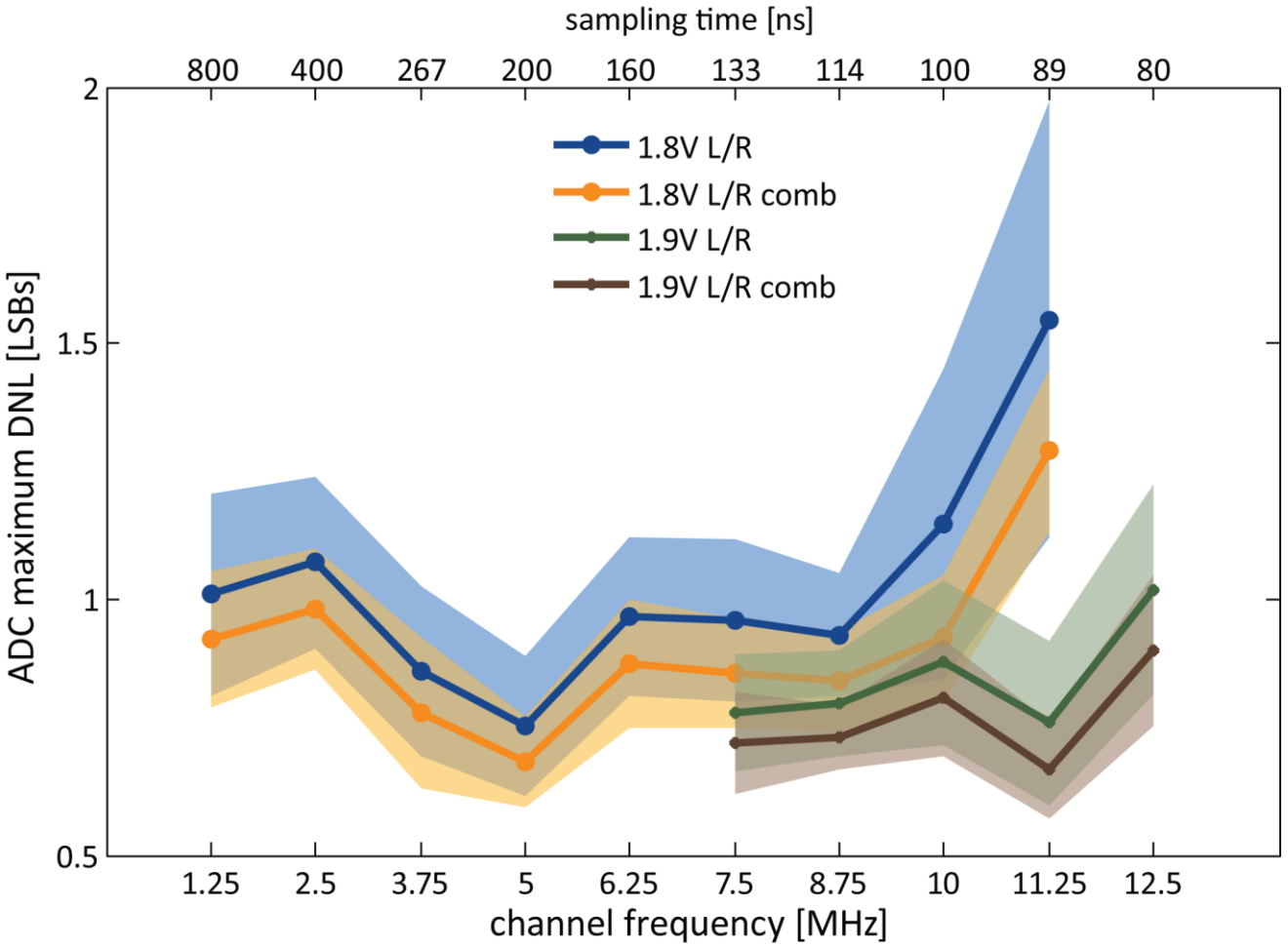
ADC maximum differential non-linearity (DNL)



- DNL > 1 can mean different things:
- ADC not monotonic, missing codes, misbehaved LSB …

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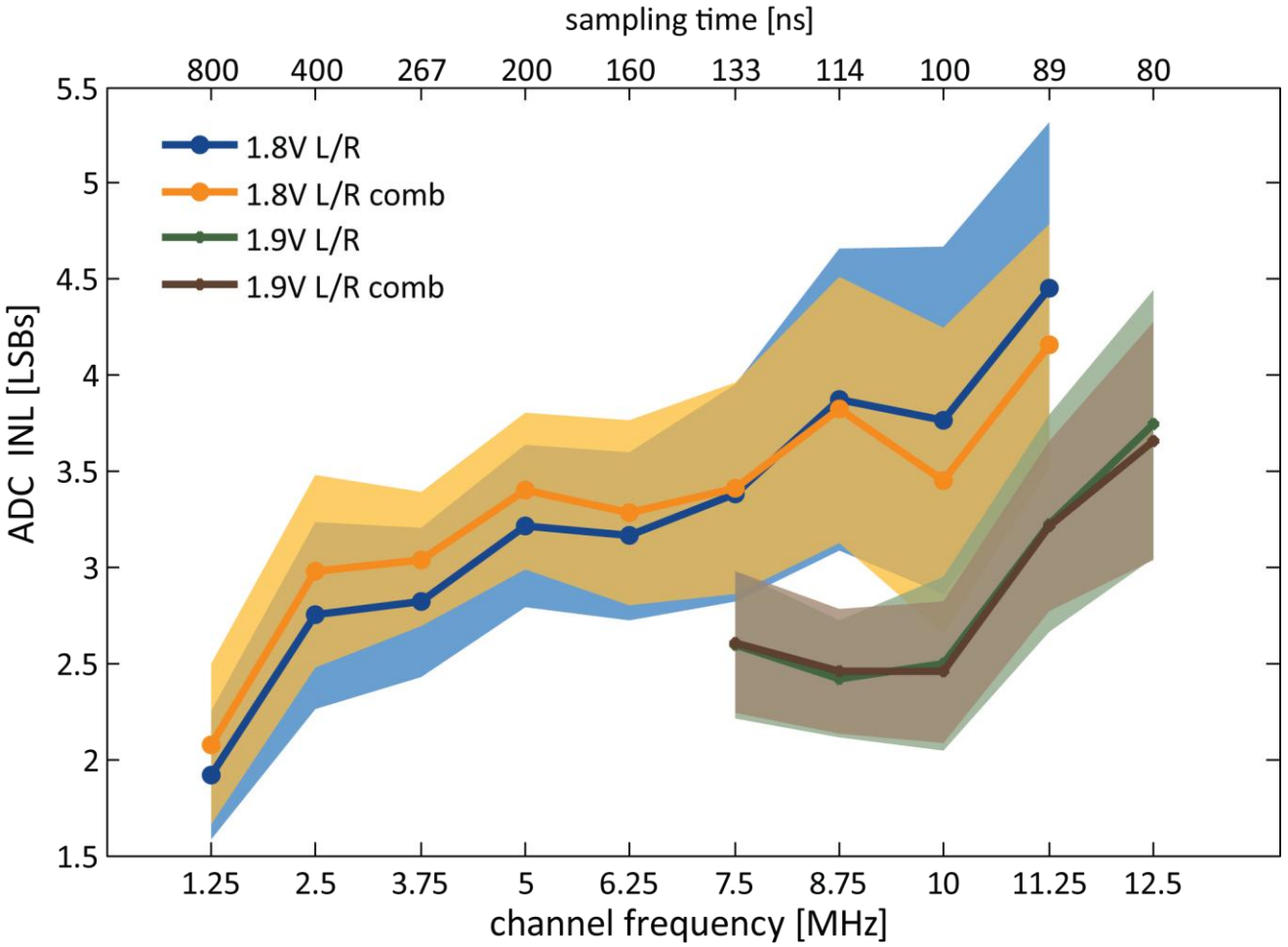
ADC maximum integral non-linearity (DNL)



- good measure of linearity

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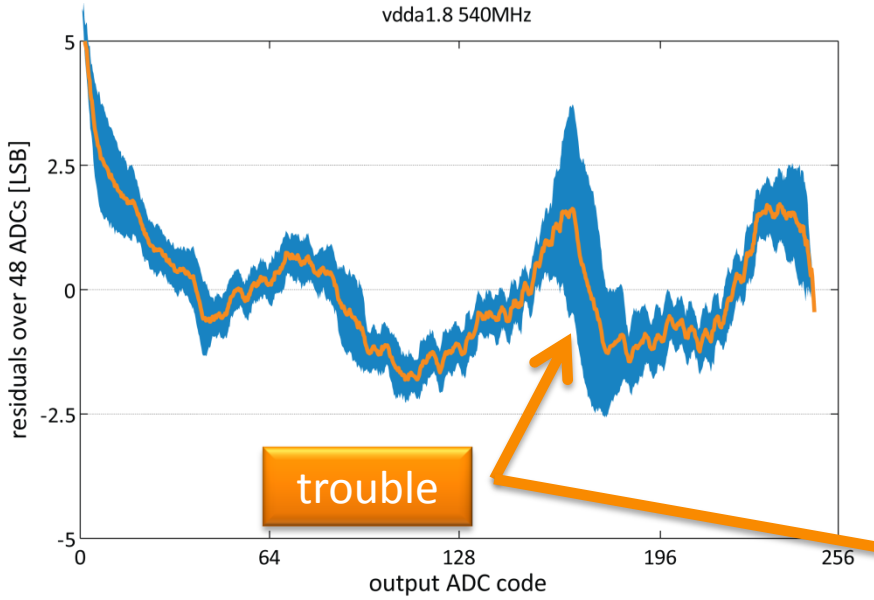
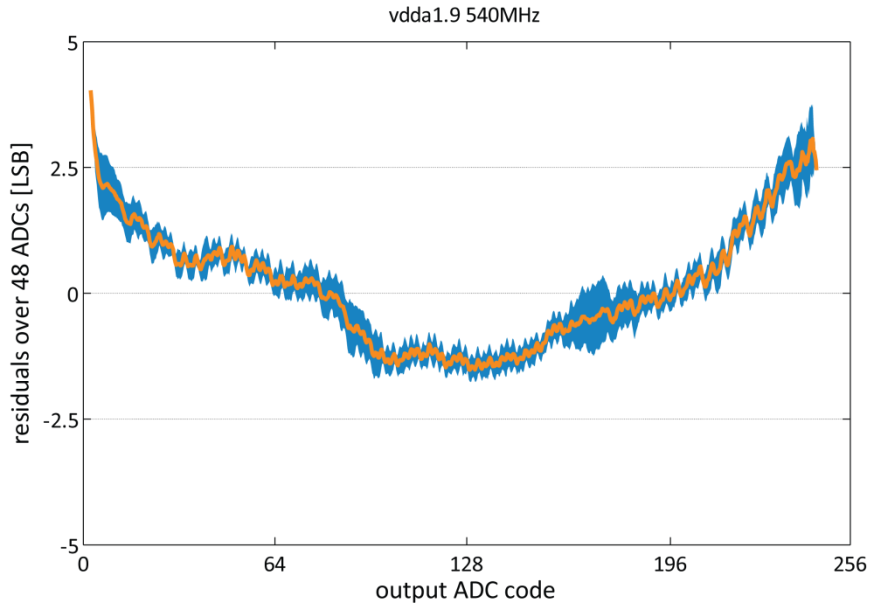
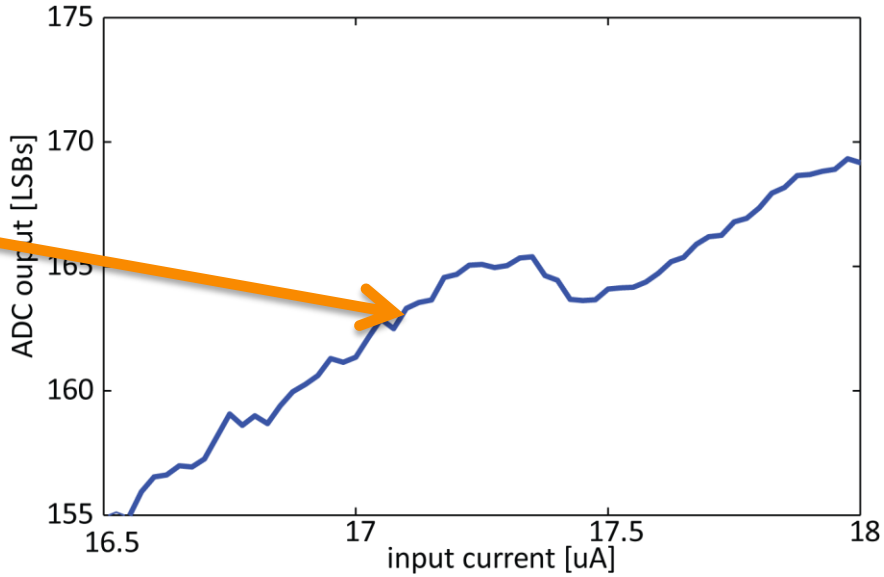
problems at higher frequencies





- residuals for 48 ADCs, 540MHz
  - top: VDD = 1.8V
  - bottom VDD = 1.9V
- step in ADC response



- very (±10mV) sensitive to supply voltages (RefIn, VDDx)

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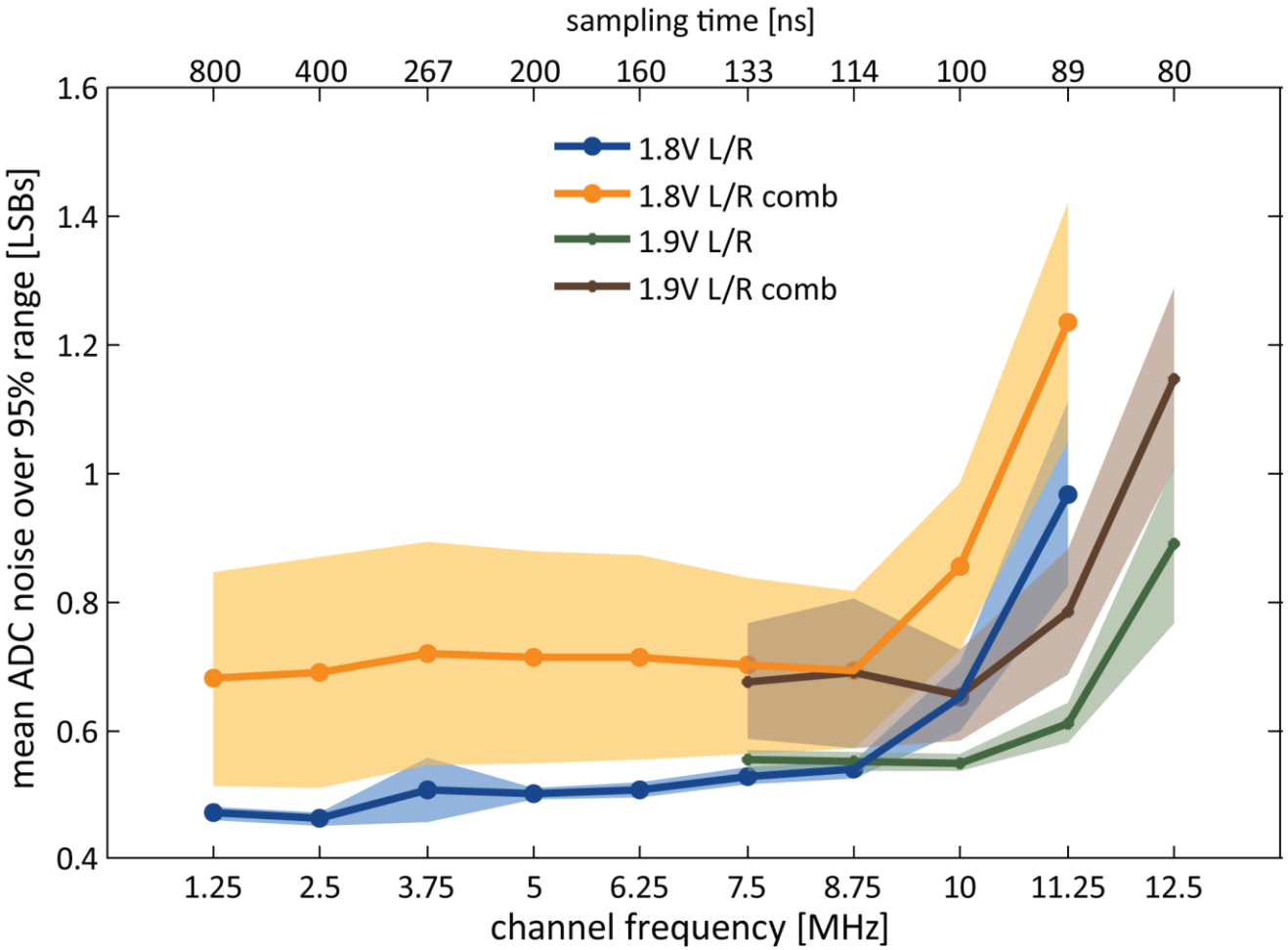
mean ADC noise

- noise over 95% of ADC input range
- **noise less 1 LSB @ 12.5MHz**
- noise consistent in all channels



- ➔ combining L/R ADCs increases noise and spread over channels

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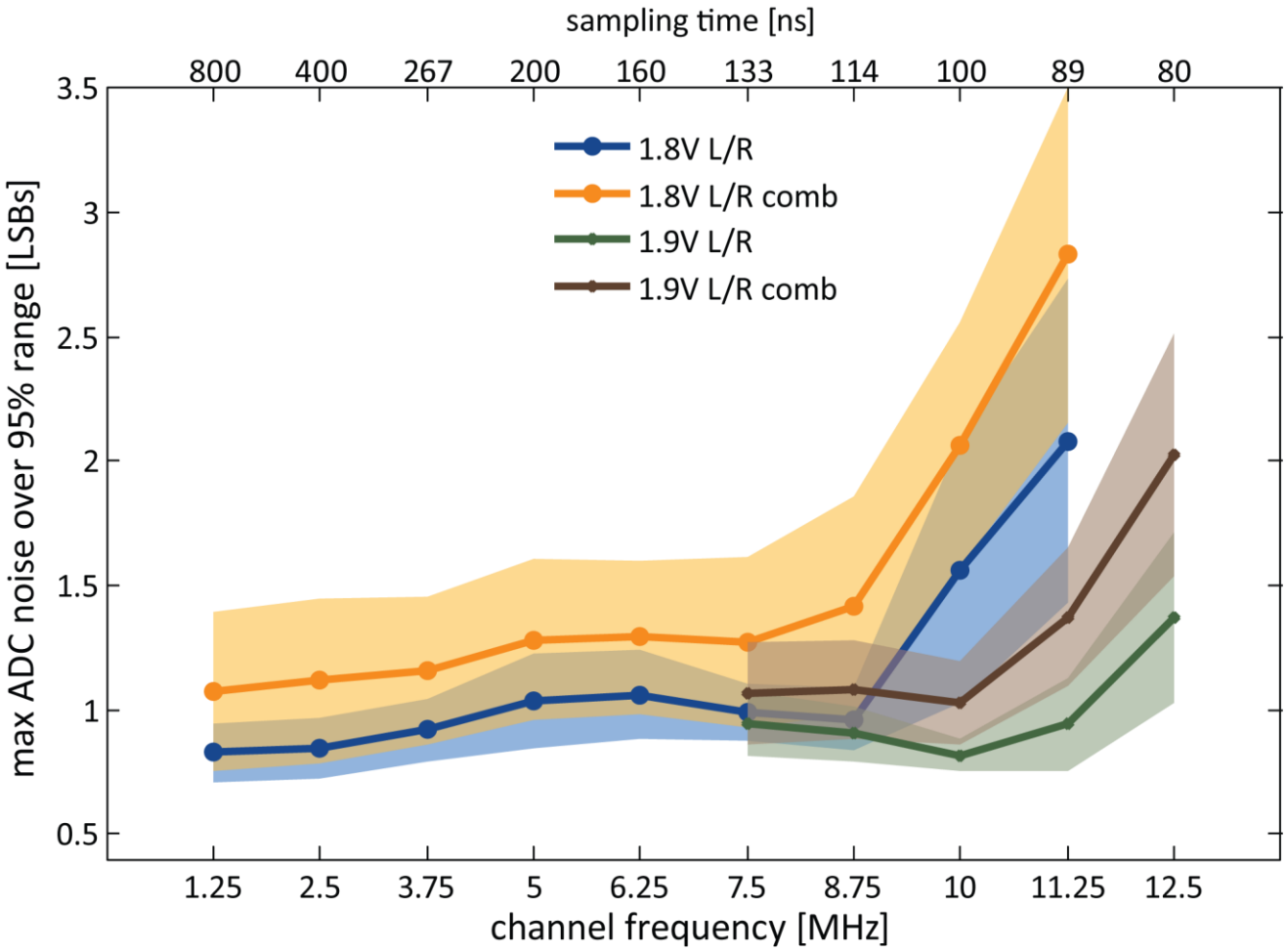
maximum ADC noise



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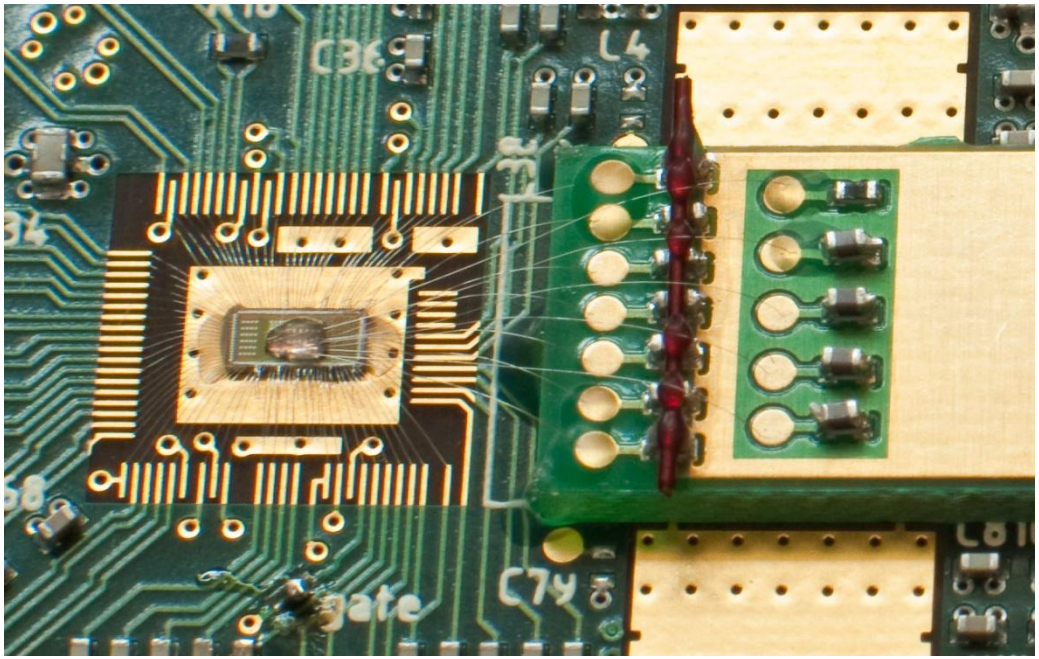
input capacitors

- measure noise vs. capacitance



- 11 values of input capacitance
- 4pF … 82pF
- bonded directly to DCD's input bump-pads

- noise (almost) independent of operating frequency

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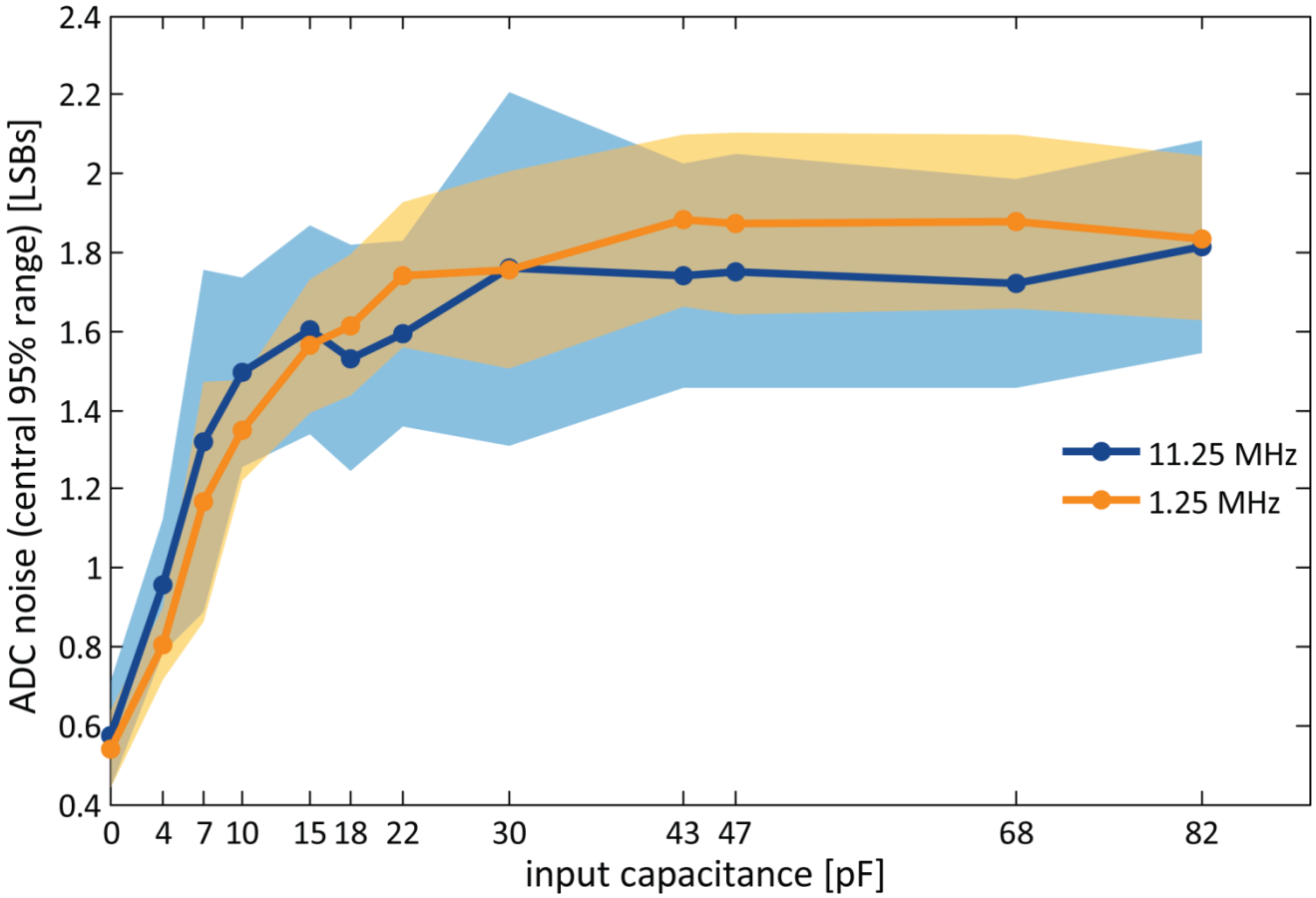
ADC noise with added capacitance

- note:
  noise no longer
  constant
  over range
  → high spread

- L/R channels
  not combined



- noise increase ×3 over capacitance range
- ➔ @60pF: ≈1.8LSB

- TODO: check gain/range with added capacitance

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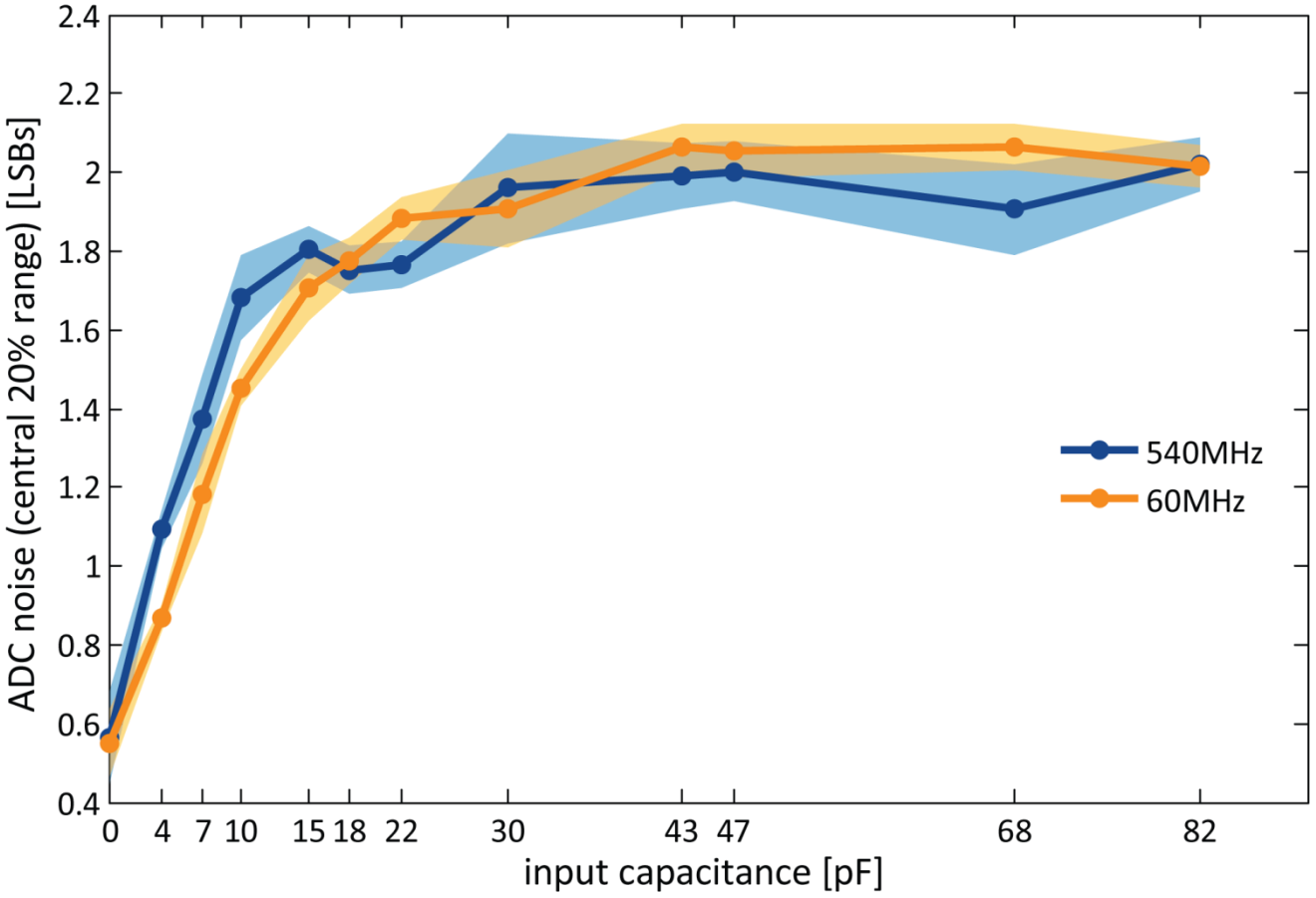
ADC noise with added capacitance – central 20% range



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Summary

- test system working reliable !

- ADC characteristics at 12.5MHz
  - total range of ≈ 24µA
  - gain ≈ 10 ± 0.1 LSBs / µA → LSB ≈ 100nA, small spread
  - DNL ≈ 1 LSB, INL < 4 LSB
  - noise: 0.9 LSB, ≈ 1.2 LSB with L/R ADCs combined
  - noise doubles with 60pF input capacitance

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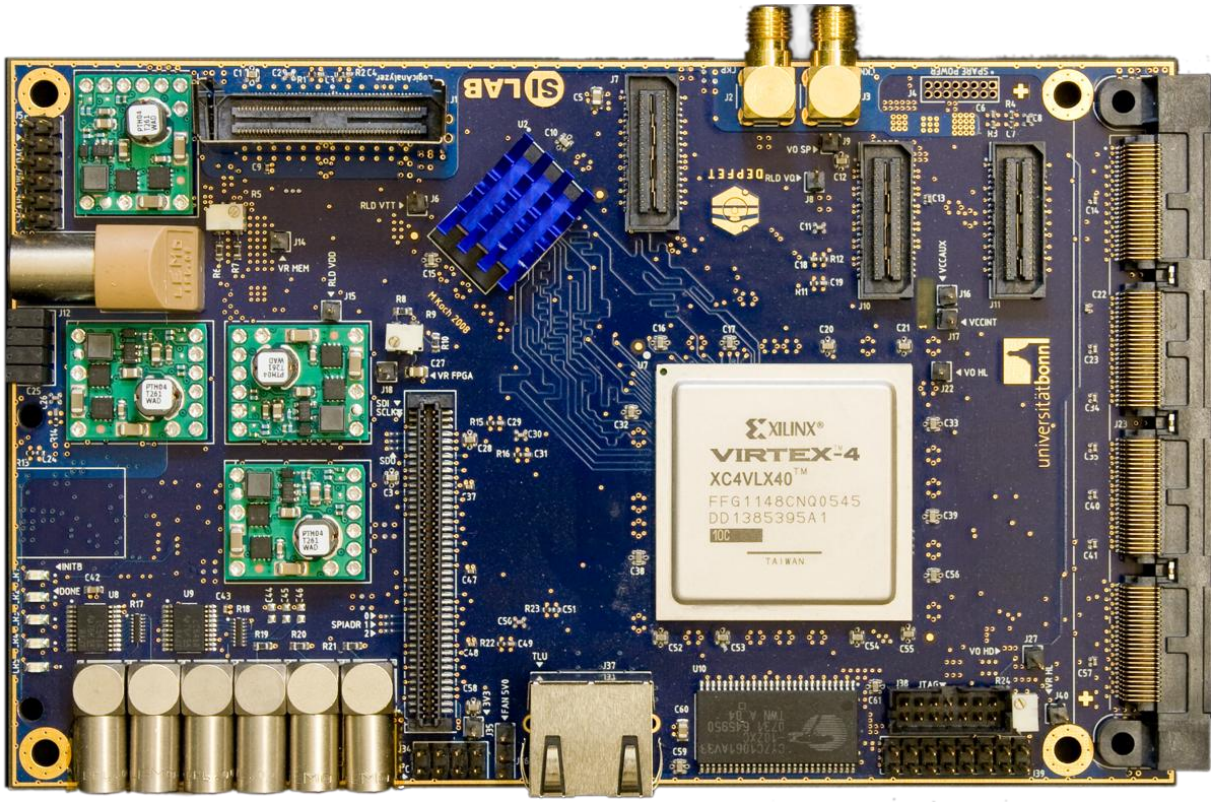
DCD2 Test system (FPGA PCB)

- XILINX Virtex 4 LX40-1148
- 288Mbit RLDRAM
- USB 2.0 connection
- 16Mbit async. SRAM
- EUDET TLU connection
- Multiple high speed connectors
- FPGA handles 600MHz data input from DCD
- No signal / power integrity issues so far



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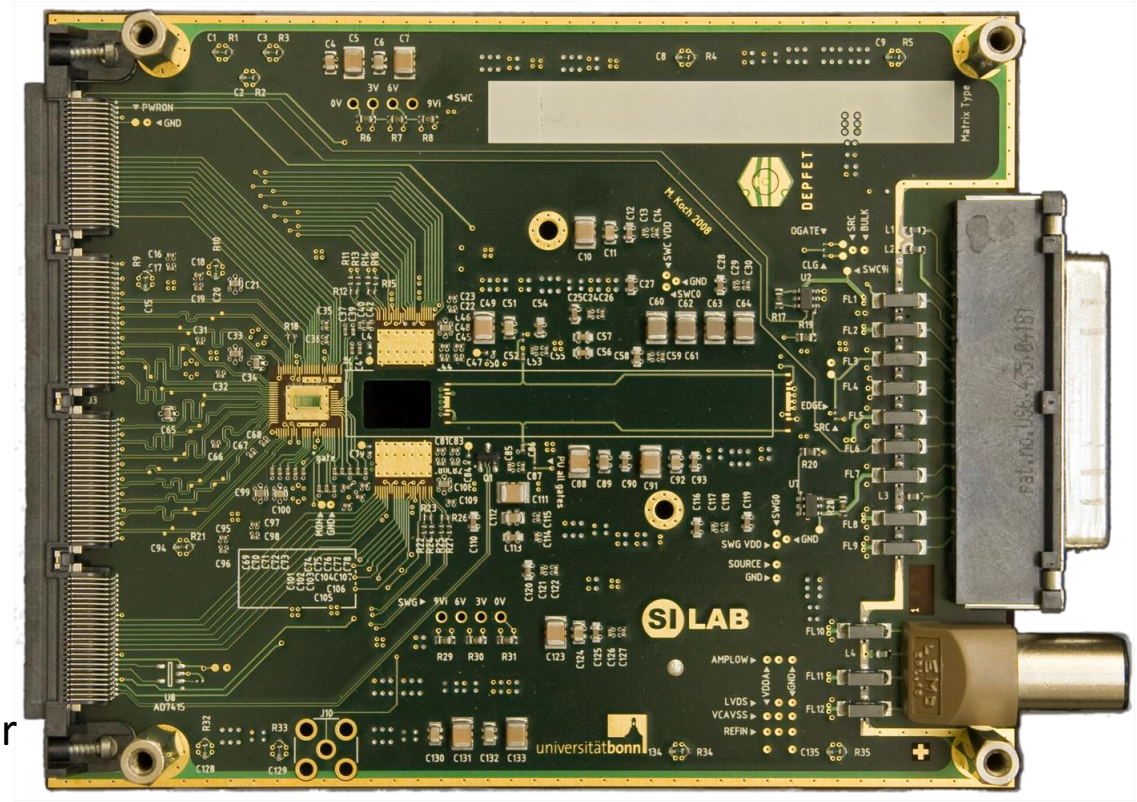
New Hybrid (Bonn v4)

- DCD2, Switcher3
- 128x128 matrix &
  256 x 1024 (2 Switcher)
- For Switcher 3:
  - 3V, 6V: res divider
  - CLK, Strobe: high speed
- For DCD2:
  - Matched high speed routing
  - Decoupling for DACs, Refs
- Temp Sensor (NPN & I2C)
- Samtec QTS/QSS-RA connector
  - → rigid connection to fpga
  - Longer cable possible



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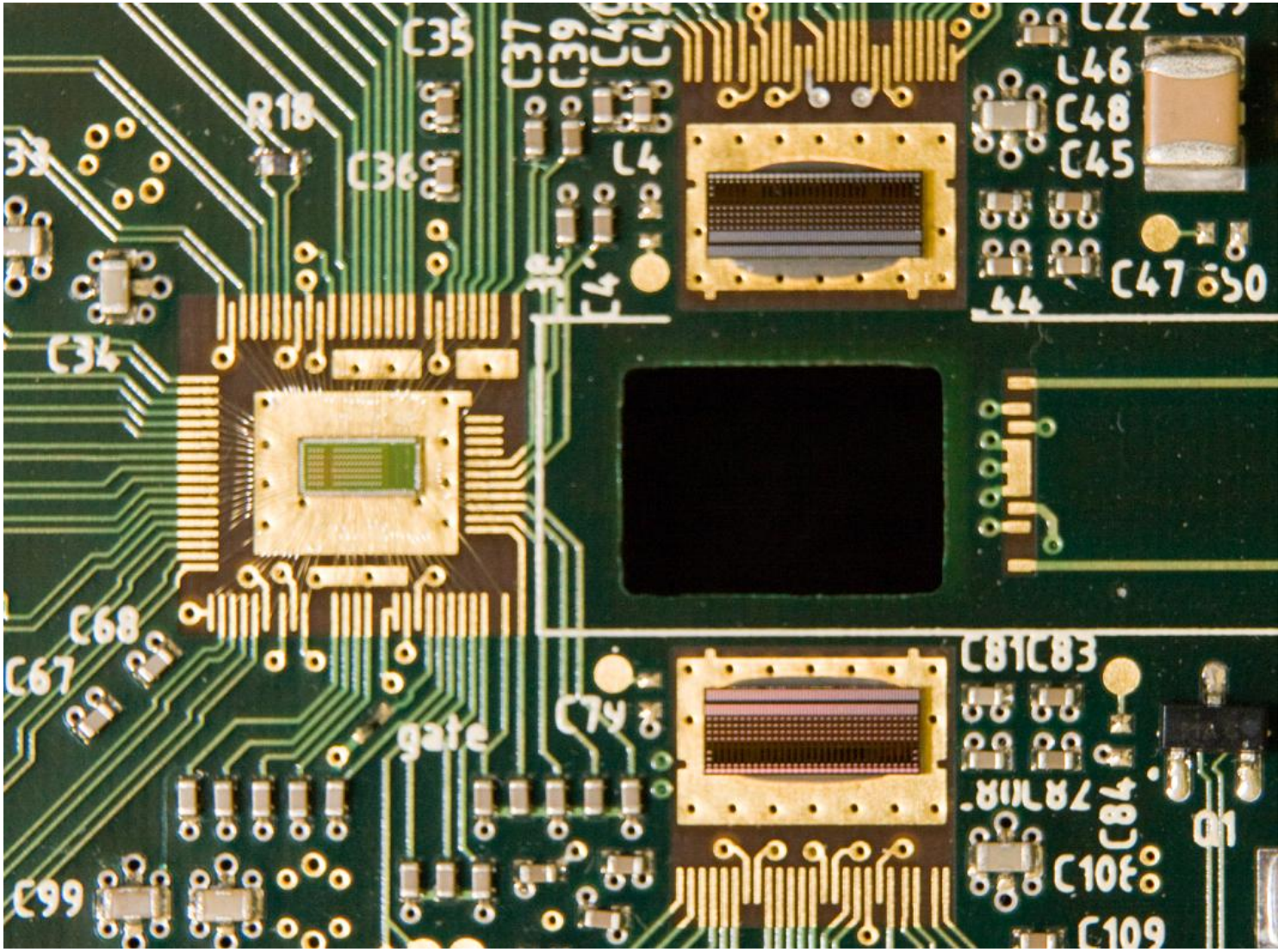
New Hybrid (Bonn v4) - chips



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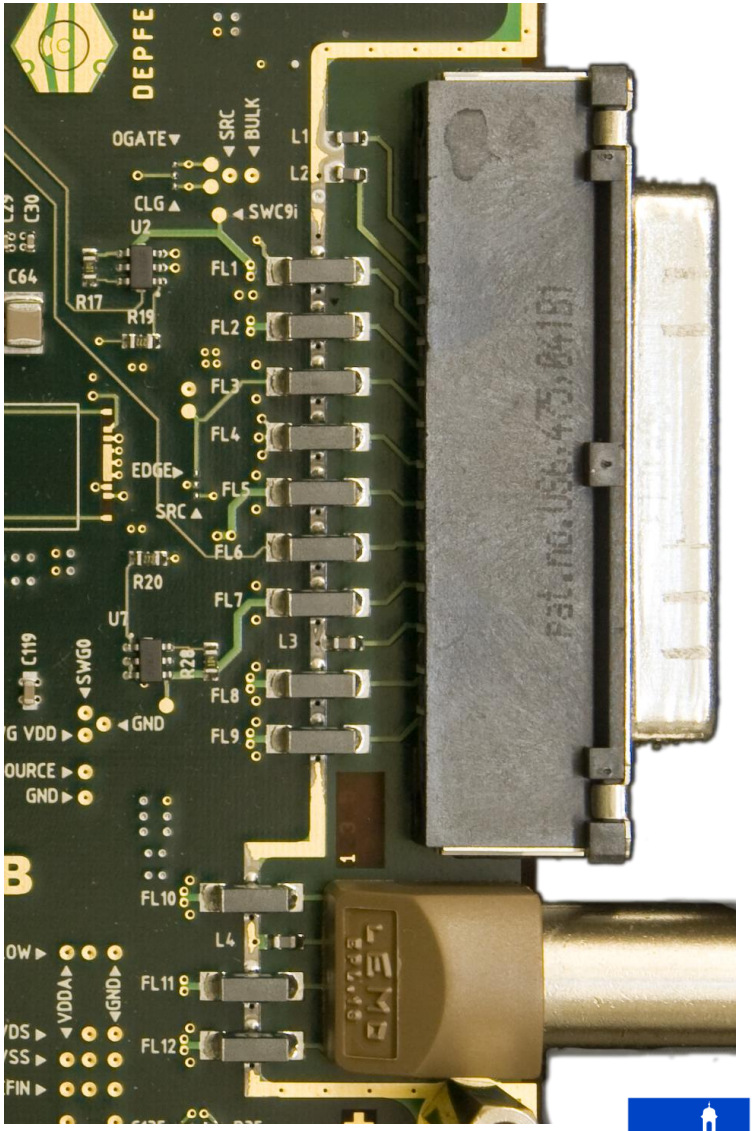
New Hybrid (Bonn v4) - power

- DSUB 25 connector for all power supplies
  (bad choice, nothing better available)
- Additional LEMO 6 pin for DCD only
  - Simplifies testing
- All referenced to GND
- All incoming power cons are filtered
  - LCL type for power, ACH4518-333
  - Ferrite for GND, BLM18SG121
  - RCRC for HV, 470k & 47n
- Switcher 3:
  - 9V supply can be turned of by FPGA, FDC6330
- Low impedance of power distribution system guaranteed by careful choice of capacitors, stackup, layout, simulation



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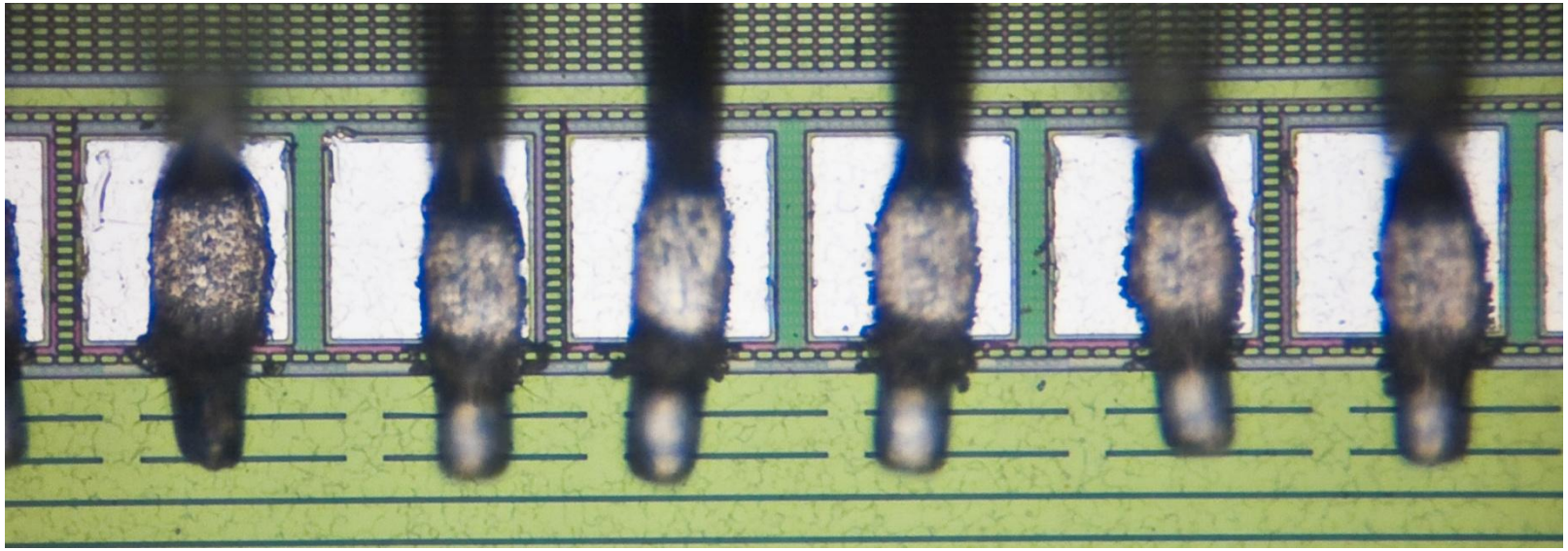
First DCD2 tests

- Bonding extremely difficult due to high number of small pads
- Lost ≈ 10 chips so far
  - But not completely clear if always problem of bonding
- After modification of bond-needles (partial) bonding is possible



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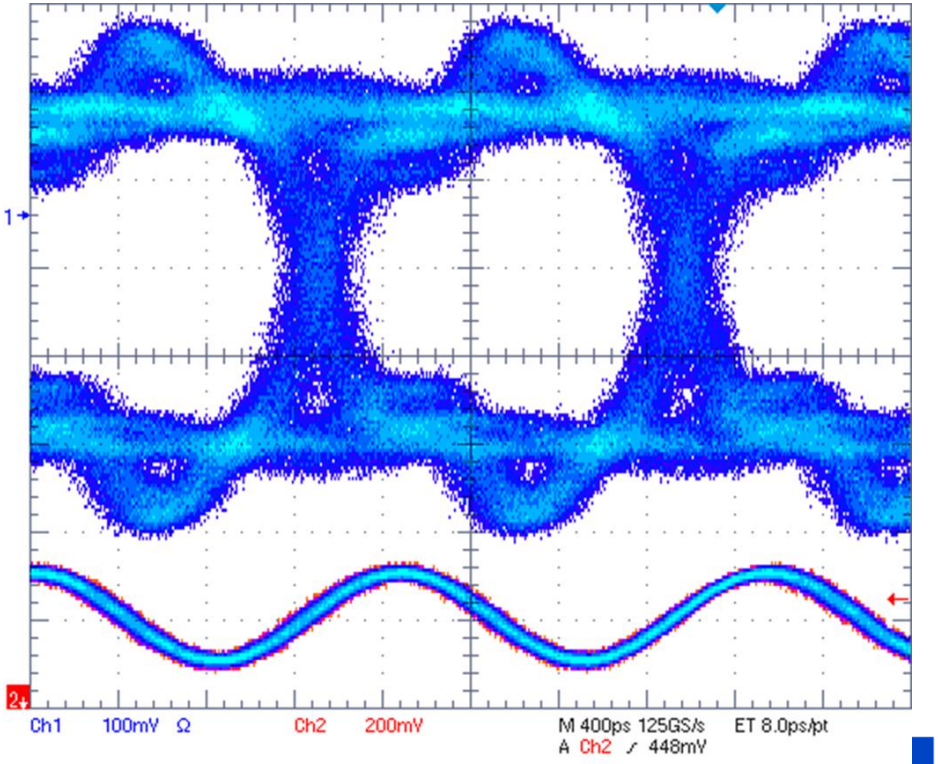
First DCD2 tests – digital only

- Digital part works @600MHz (@666 pulser maximum)

- 600MHz from DCD2 and CLK
- Measured under FPGA (vias)
- “Random” values from ADC
- 1GHz scope and diff probe
- True differential termination (Virtex4)
- Excellent signal quality

- Synchro signal ok!



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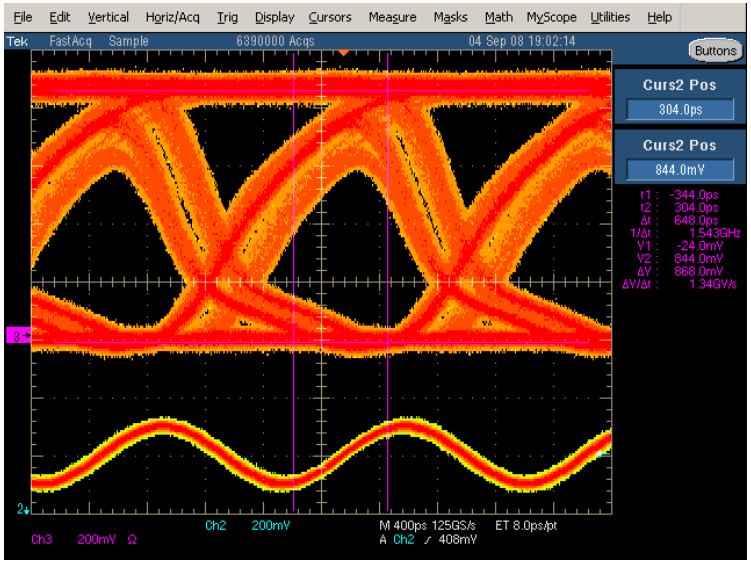
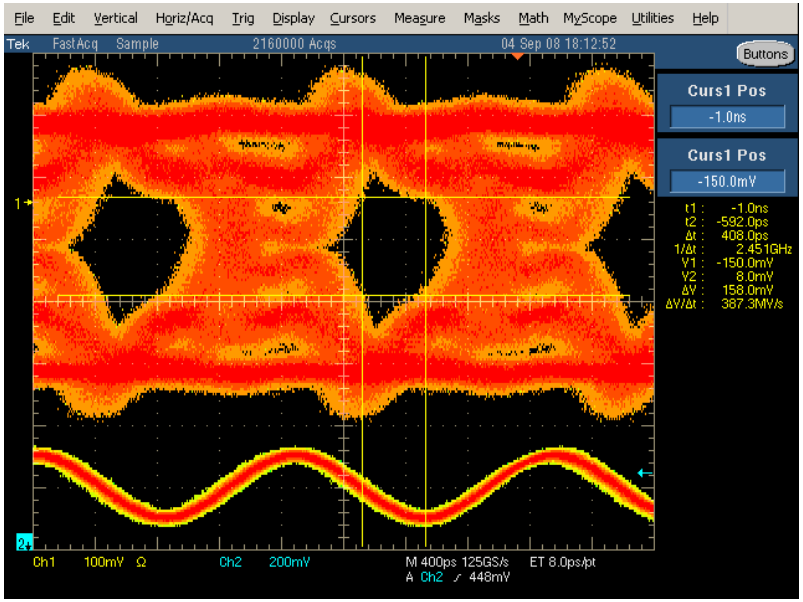
First DCD2 tests – digital only

- Good data (previous slide) going through the FPGA
- Single-ended, asymmetric termination
- Looks ugly, but proves the point





- Example of how things can go wrong
- 600MHz signal from DCD @FPGA, but:
- Symmetric split termination (DCI)
- Expected (Ivan's driver is asymmetric)

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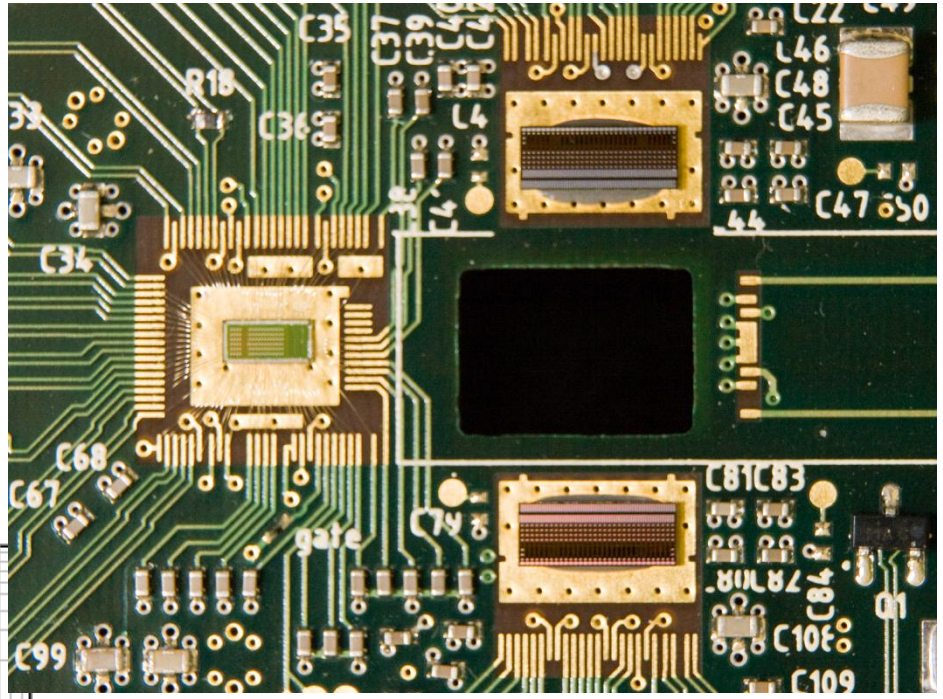
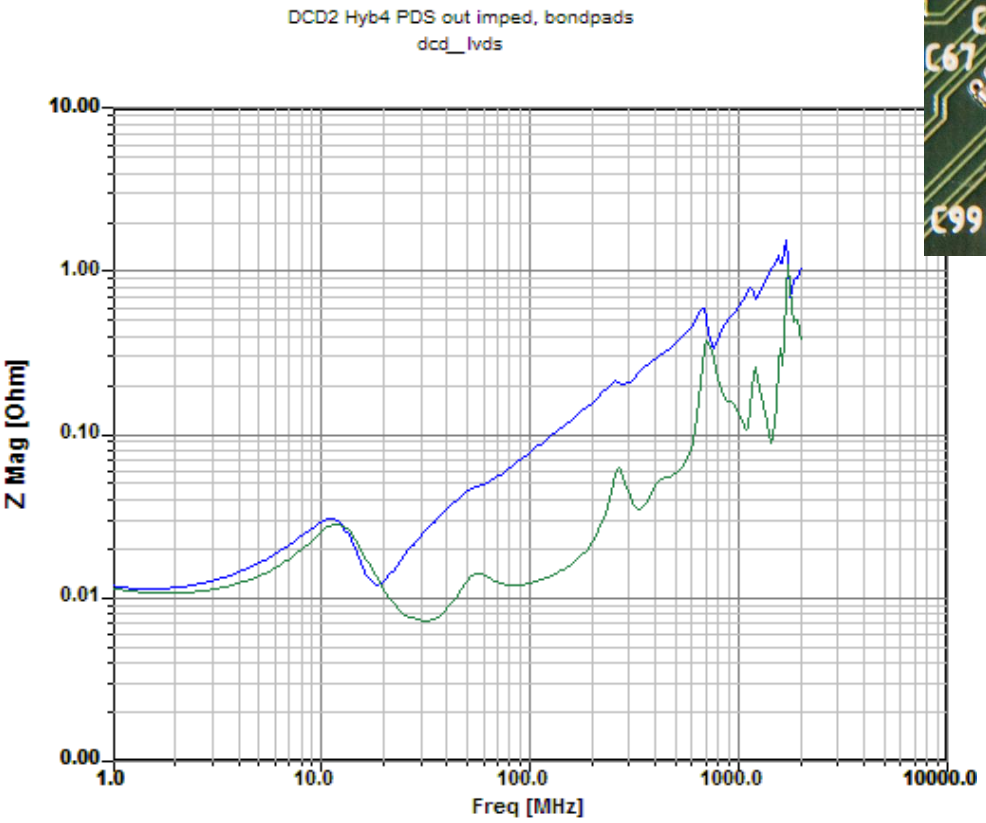
New Hybrid (Bonn v4) - power





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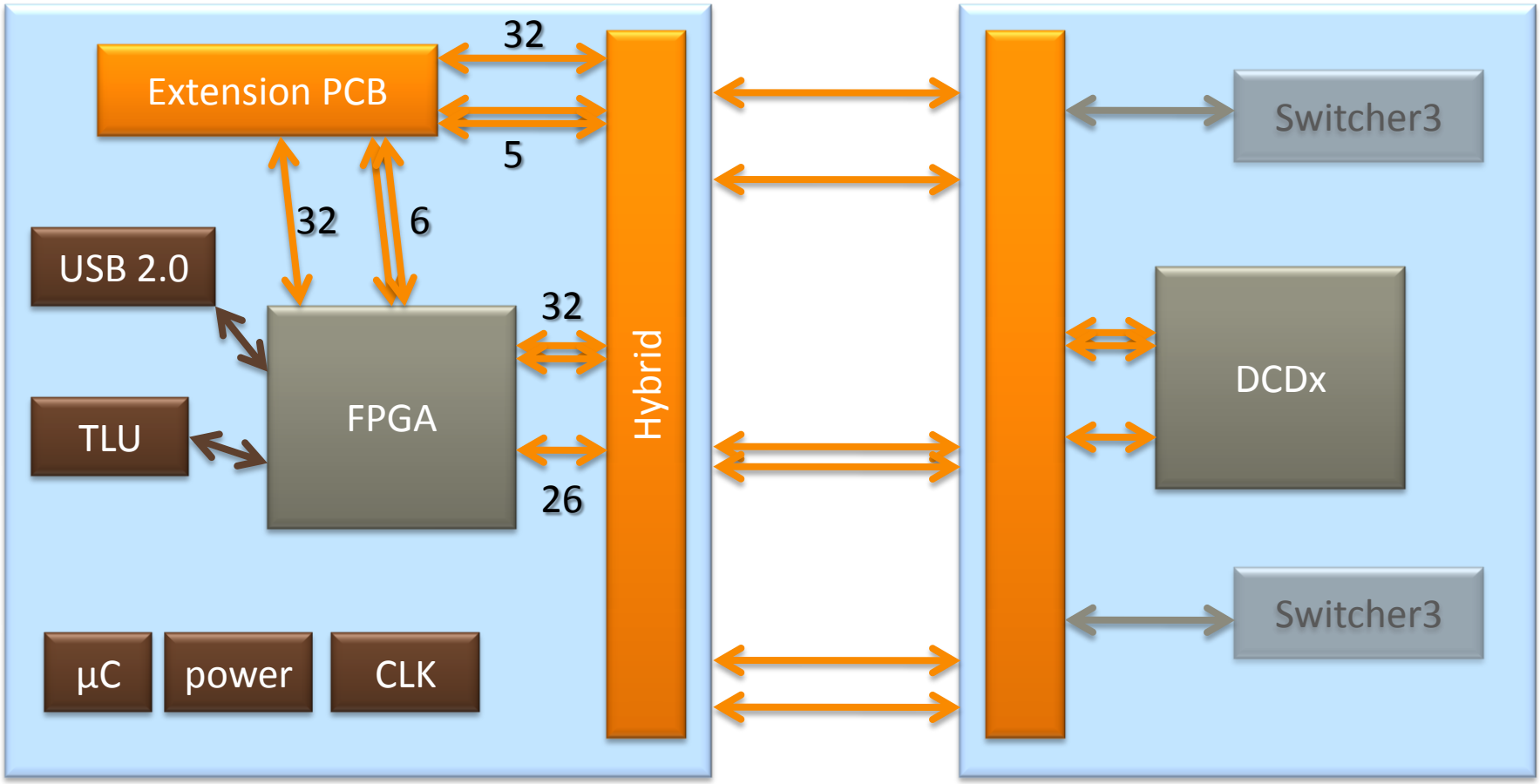
DCD1/2 Test system connectivity



connections not shown: I^2C bus, temp. diode, 4x 'power ok' (selectable threshold), 200MHz Agilent Logic Analyzer probe connector (E5385A), SMA differential CLK input, 6 "old style" LEMOs, JTAG, SPI, analog board, power,…

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