SI LAB
Silizium Labor Bonn

Development of the Data Handling Processor DHP

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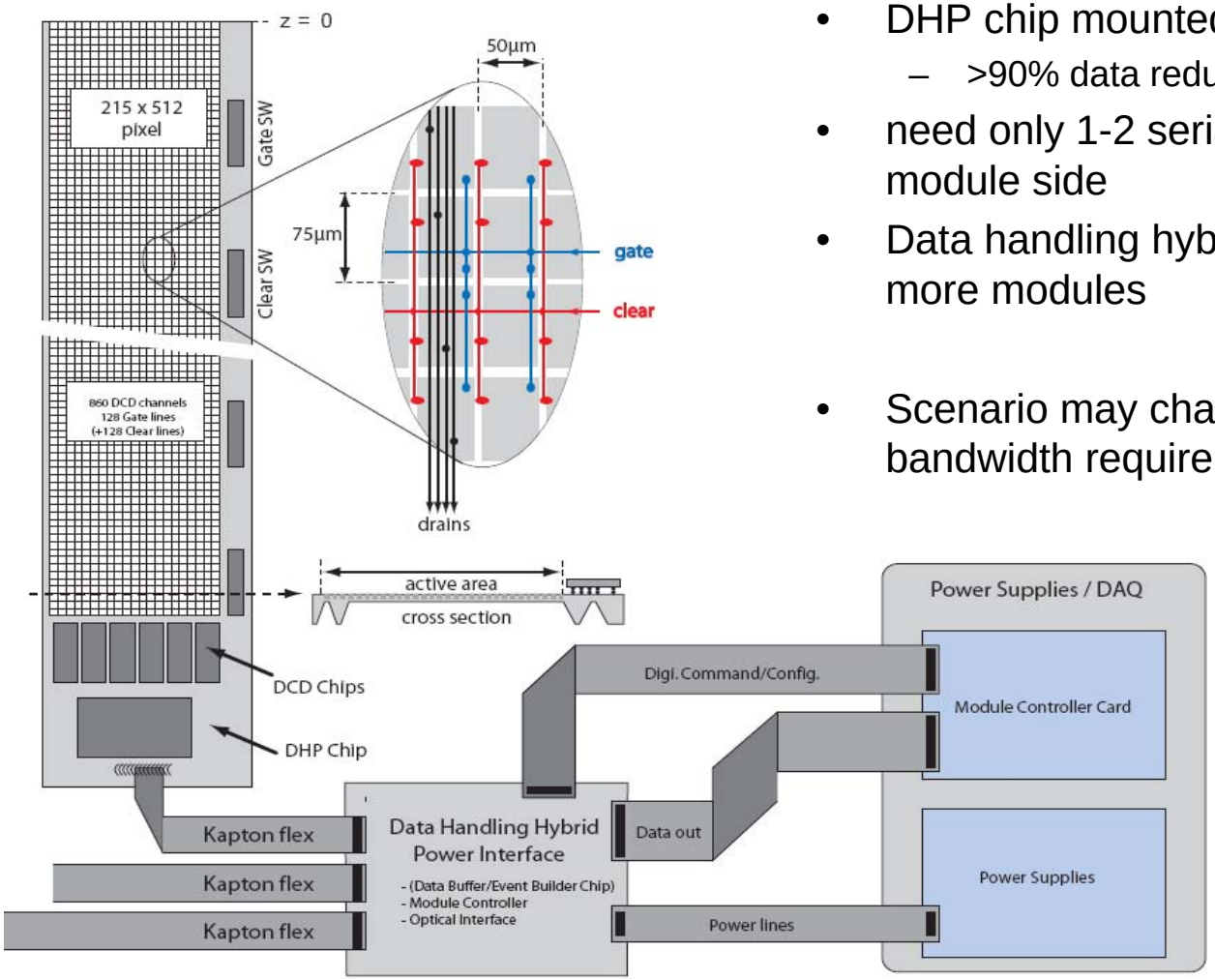
Overview

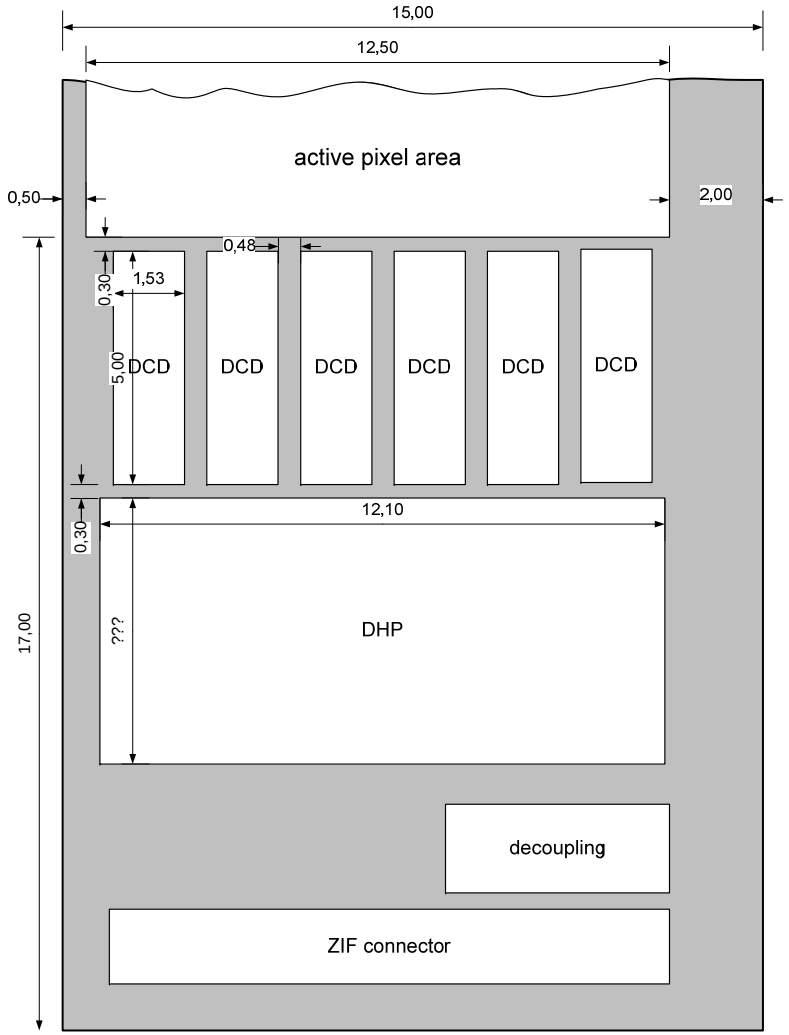
- Module layout
- Data rates
- DHP functionality
- Technology / C4 bump bonds
- Work plan

Module Layout



- DHP chip mounted on sensor module
  - >90% data reduction
- need only 1-2 serial links for data out per module side
- Data handling hybrid to support one or more modules
- Scenario may change according to bandwidth requirements

End of Module Layout



DCD

- 150 x 150 µm^2 cells
- 16 rows, 10 columns
- x4 output multiplexing
- 6 chips, 1.5 x 4.7 mm

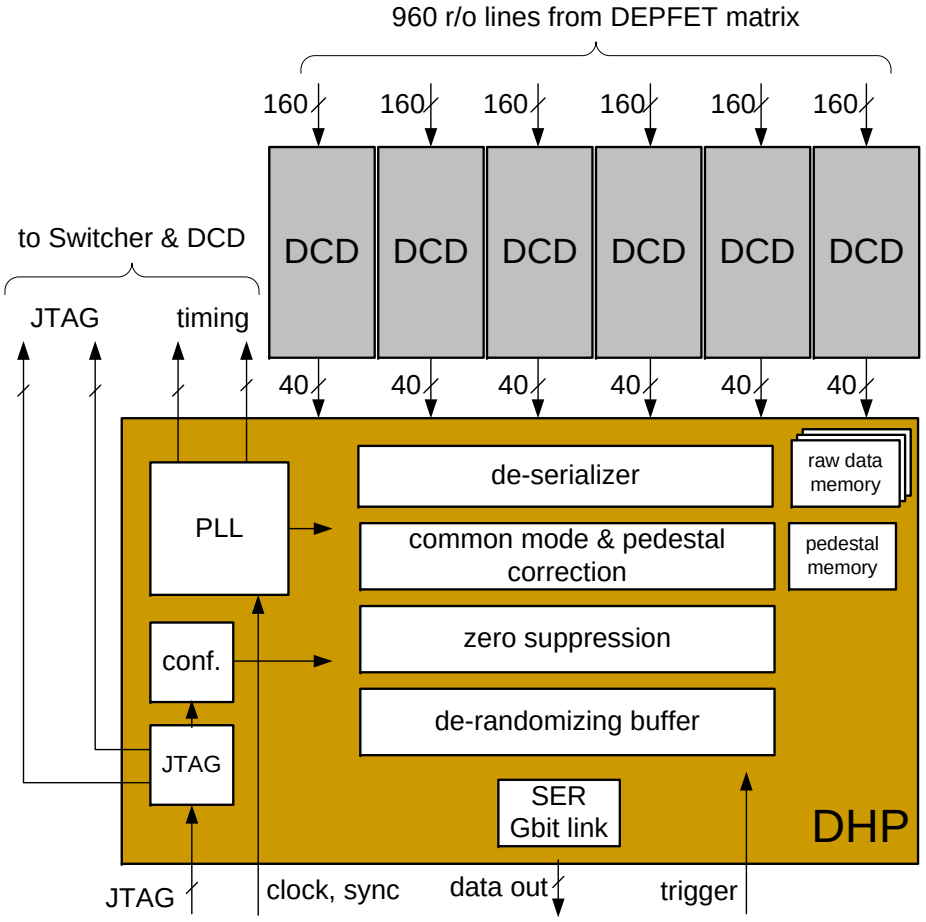
DHP

- 200 µ bump bond pitch
- 12 (6) x ??? mm
- one or two (or more) chips

Connector

Decoupling

Signal Flow and Data Rates



12.8 MHz line freq. (sample rate)

- 8 bit ADC per input channel
- 4 channels per output

410 MHz output data (x 240) = 96 Gbit/sec

zero supression → 18 Gbit/sec

trigger → 1.8 Gbit/sec

Assumptions

- 10µs r/o time
- 128 (switcher) rows
- 10 kHz trigger rate
- 5% occupancy

Function Blocks

- data processing blocks (synthesized standard cell design)
  - common mode calculation (& correction)
  - pedestal correction
  - de-randomizing buffer
- memory blocks (raw frame data, pedestal correction)
- clock & timing management (PLL, prog. delay lines)
- DACs, slow ADC for monitoring temperature etc.
- slow control interface: JTAG
- Gigabit serial transmitter (LVDS, CML…)

Participation of UB in the DEPFET collaboration tasks

ASIC Development

- Switcher
- DCD
- **Data Handling Processor (DHP)**
- Data link

- Synchronisation switcher/readout
- Beam clock synchronization
- Trigger handling
- Data control (up/download configuration data)
- ***Slow control (currents, temperatures)***
- Memory to buffer 10 frames
- Pedestal Memory needed for 0-suppression
- Eventually common mode suppression
- Readout buffer holding 4 0-suppressed frames
- ***IO modules***

+ integration

Participation of UB in the DEPFET collaboration tasks

Meeting in Barcelona, November 11th, 2008
Phone meeting, March 25th, 2009

- JTAG interface for slow control (designer Albert Comerma)
- Bandgap reference (designer Eva Vilella)
- DAC (8 bit, slow) (designer Lluis Freixes)
- ADC (10-12 bit, slow)
- Standar LVDS
- Input differential amplifier (it is still not clear->ARM IP?)

Progress

- Agreements with MOSIS/IBM/ARM signed (Nov'08-Feb'09)
- Design kit for cms9lp and libraries ready (Mar'09)
- Design of bandgap an DAC started. Scheduled for June.
- Other modules scheduled for October.

In principle the DAC will be C-based. The ADC will be probably based on the DAC (SAR). JTAG from Synopsys.

Interface to DCD

- DHP → DCD
  - BitCLK (LVDS)
  - FrameSYNC (LVDS)
  - Row2SYNC (LVDS)
  - JTAG interface for configuration and boundary scan (1.8V CMOS)

- DCD → DHP
  - 4 to1 multiplexed ADC data per output, 400MHz
  - single-ended inputs
    (differential input stage with common threshold, set by DCD)
  - no input termination
  - BitCLK, Row2SYNC return for testing and synchronization

Interface to Switcher

- Shift register based channel selection (all LVDS)
  - CLK
  - SEROUT
  - SERIN
  - GateStrb
  - ClearStrb

- JTAG slow control (1.8V CMOS)
  - TCK, TMS, TDI, TDO

Interface to DHH

- DHH → DHP (all LVDS)
  - RowCLK (12.7 MHz, f0/40)
  - FrameSYNC (abort gap clock)
  - Trigger
  - JTAG (CMOS?)

- DHP → DHH
  - DataOUT: one or two GBit links (LVDS or CML)
  - protocol ?

SuperKEKB timing

- SuperKEKB **RF frequency** f0 = **508 MHz** (508.89 MHz precisely)
- Number of slots per cycle: 5120
- Circulation time: 10.061 µs
- System clock f0/12 = 42.3 MHz (or f0/4, f0/8, f0/16, f0/256)
- Abort gap: 200 ns (~100 bunches)
- Clock for abort gap available (**frame clock**)

- DEPFET read-out **synchronous** with **beam circulation** (128 rows):
  row clock = 508 MHz / (5120/128) = **508 MHz / 40** = 12.7 MHz
- Use **f0/8 and divide by 5 (DHH?)**

Technologies

- 130 nm good for analogue performance (i.e. clock management chip DCM), many function blocks and libraries readily available
- But: 90 nm better for digital performance and size constraints (end of stave)
- Chip area function limited → same functionality in 90nm (~4k/mm^2) not more expensive than 130nm (~2k/mm^2)

Vendor (90 nm)		min. block size [mm^2]	price [$]	price [€]	price/mm^2 [€]	bump bond pitch [µm]
UMC (Europractice)	std. MPW	16		41.800	2.613	162 ?
	mini@sic	3.5		7.000	1.991	
IBM (MOSIS)	std. MPW	16	100.000	62.500	3.906	**200** ✓
	min	4	25.000	15.625	**3.906**	
TSMC (Europractice)	std. MPW	16	89.910	56.194	3.512	180
	mini@sic	4	9.850	6.156	1.539	
Chartered (own MPW runs)	???					

C4 Bump Bonding @ IBM

- C4 bump bonds option for MPW available (130mn and 90nm)
- Costs: $ 8.000 per engineering lot (for extra wavers + bumps)
- technology options:

design	bump ∅	pitch	availability
3 on 6	?	150µ	(mentioned in the design document) MPW?
4 on 6	**100µ (130µ, HTS)**	**200µ**	**MPW via MOSIS**
5 on 10	130µ (146µ, HTS)	250µ	MPW via MOSIS

solder type		reflow temp.	UBM
HTS	Pb97Sn3	345°C-375°C (215°C-255°C with mod.)	TiW/Cr/Cu/Cu (Ni barrier option)
LTS	Sn99.5Ag0.5	235°C-255°C	?

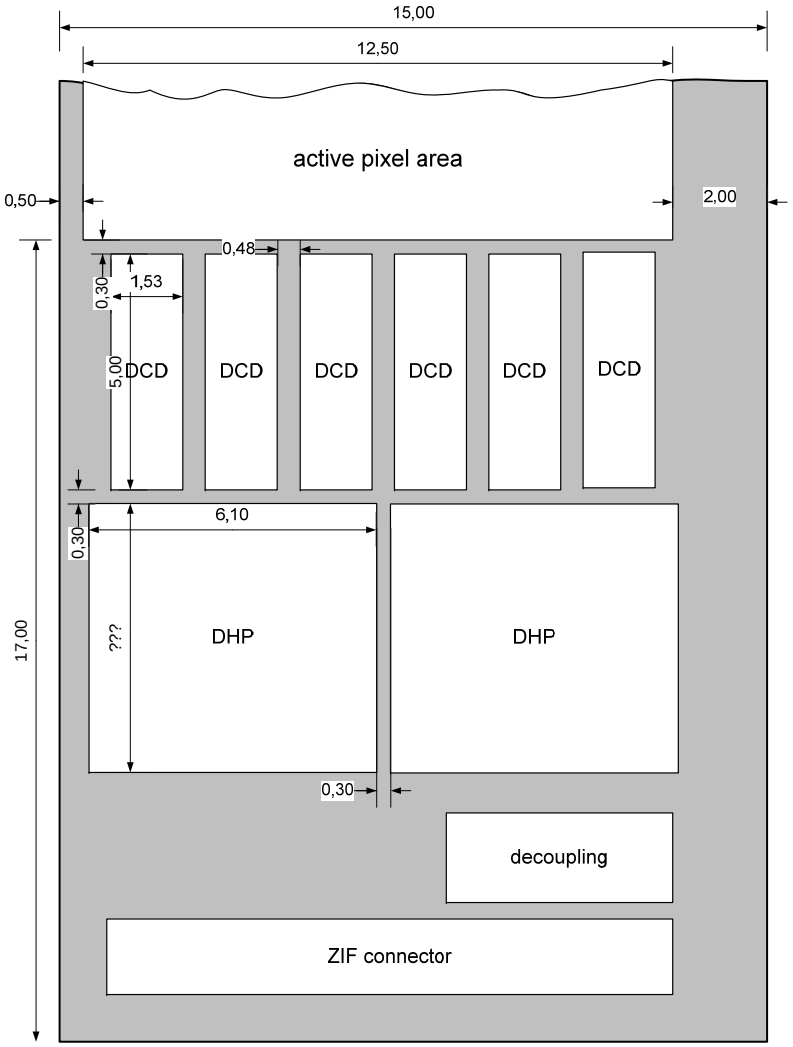
Open issues

- ADC **resolution** of the DCD (8 or 6 bit or variable)
- Frame timing: 10 or 20 µs
- **Trigger rate**
- Number of (electrical) **rows**: 128 or 256
- DCD output data format and synchronization timing
- SEU hardness?
- Interface to DHH (cable, protocol)
- …

Need to have these numbers fixed !

  - Chip size, bump bond footprint
  - Memory size
  - Data bus width
  - …

End of Module Layout – split DHP



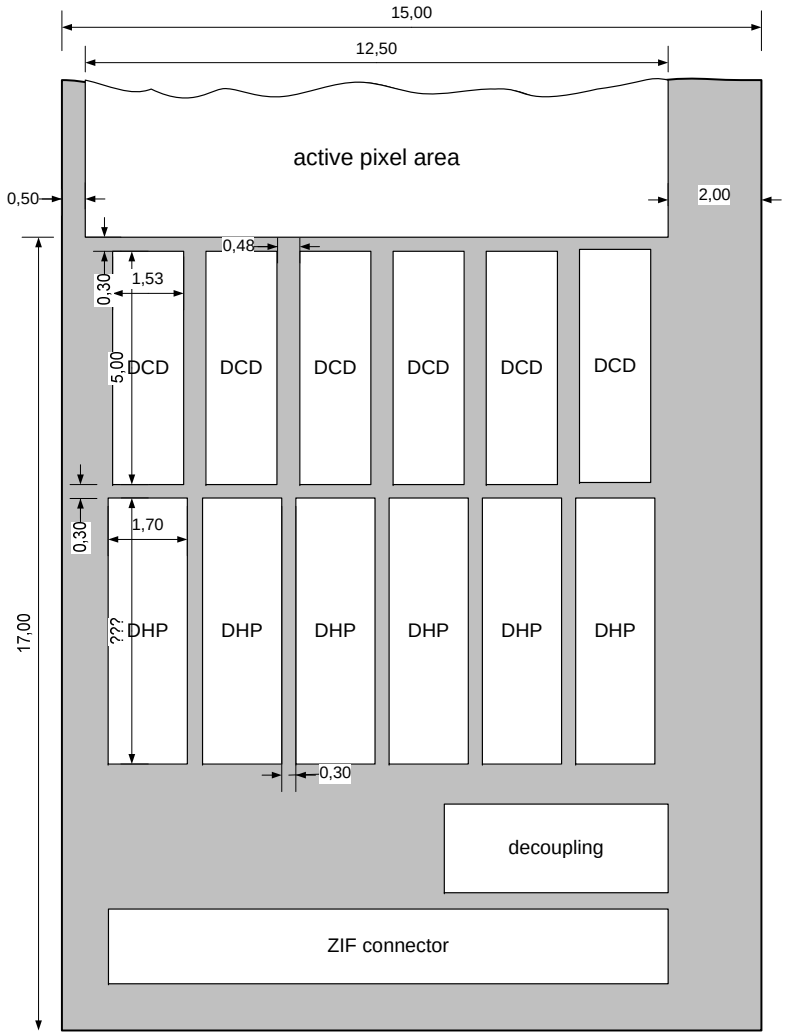
DCD

- **150 µm** x 150 µm cells
- 6 chips, 1.5 x 4.7 mm
- Input: 16 rows, 10 columns
- Output: **4 rows**, 10 columns

DHP

- **200 µm** bump bond pitch
- 2 chips
- 6.1 x ??? mm
- Input: **4 rows**, 30 columns

End of Module Layout – ‘one to one’



DCD

- **150 µm** x 150 µm cells
- 6 chips, 1.5 x 4.7 mm
- Input: 16 rows, 10 columns
- Output: **4 rows**, **10 columns**

DHP

- **200 µm** bump bond pitch
- 6 chips
- 1.7 x ??? mm
- One 1Gbit link per DHP
  → **6 Gbit per module**
- Need to change input layout:
  - **5 rows**, **8 columns**

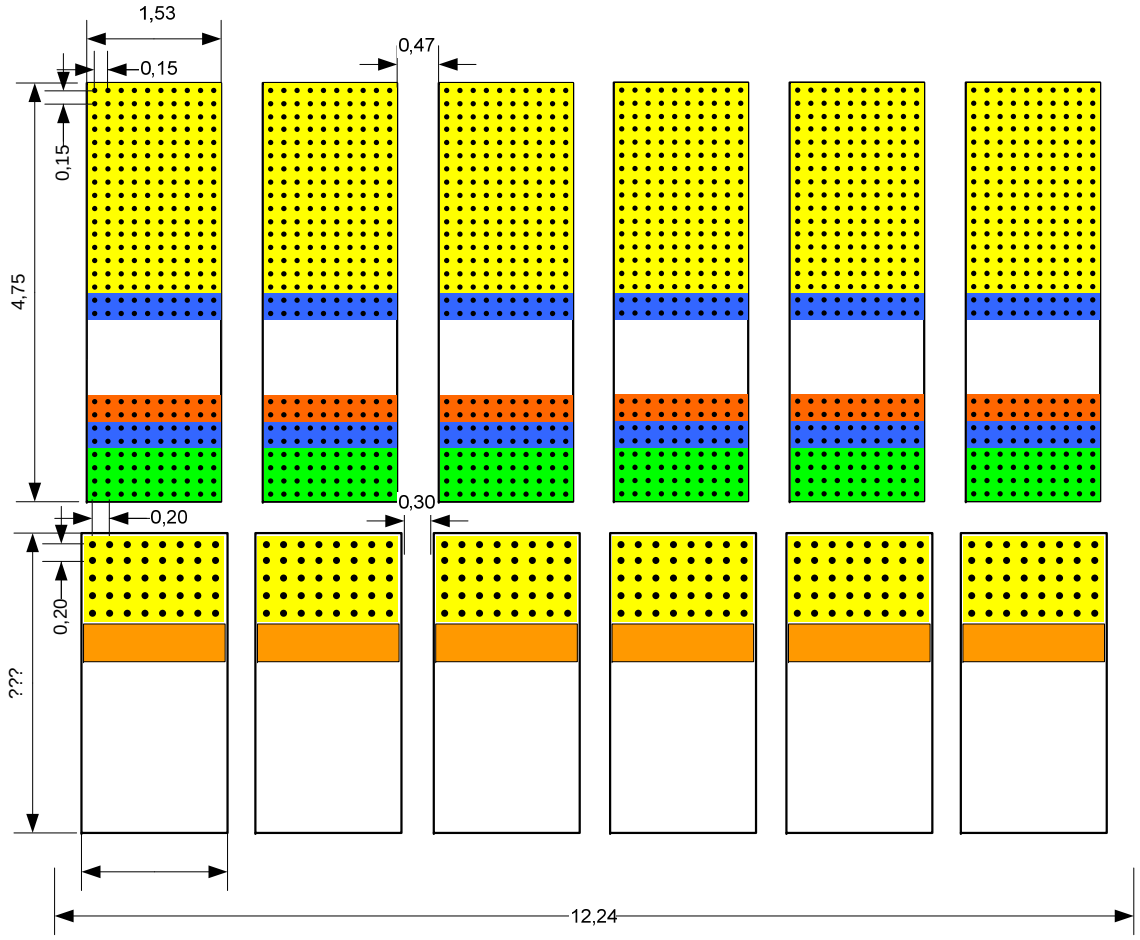
Next steps

- Test chip with full custom analog blocks (October 2009)
  - basic data processing flow (synthesized)
  - diff. input, Gbit LVDS driver
  - DAC, Iref…
- DHP 0.1 (Q2 2010)
  - full data processing
  - 40 inputs (fits to one DCD chip)
  - bump bond IOs
- DHP 1.0 (Q1 2011)
  - full chip (40, 120 or 240 inputs …)

Specs to be negotiated → synchronize with DCD development

backup

DCD + DHP footprints



6 chip DHP option

- Further reduced costs
- one Gbit link per chip @ 6 Gbit r/o per module
- but: even more redundant logic
- Need to change input pad layout
  - DCD: 4 x 10 @ 150µ
  - DHP: 5 x 8 @ 200µ

DHP Data Processing