Characterization and grading of the Pixel Vertex Detector modules for Belle II

Philipp Leitl
phleitl@mpp.mpg.de

Max Planck Institute for Physics
Semiconductor Laboratory of the MPG

DPG Frühjahrstagung - Münster
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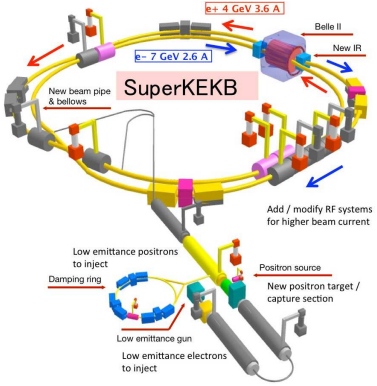
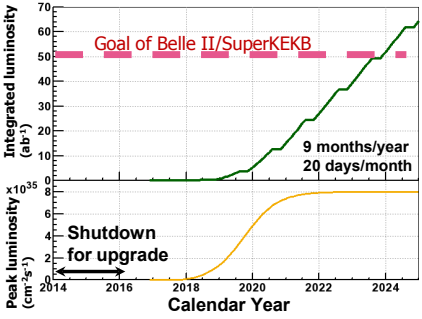
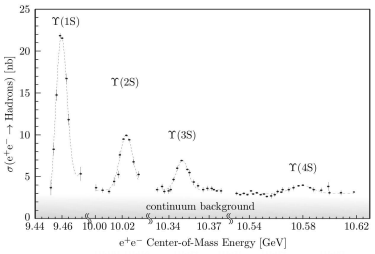
SuperKEKB and Belle II



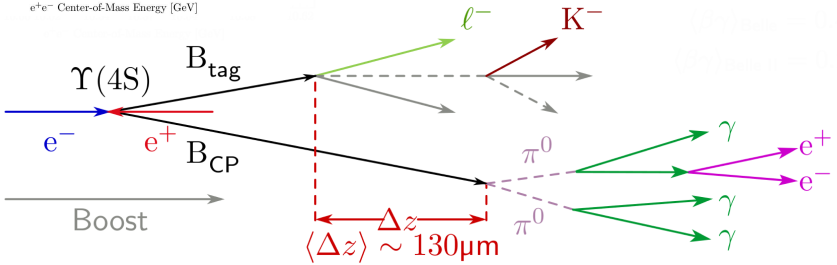


- Upgrade of the KEKB accelerator at the High Energy Accelerator Research Organization in Tsukuba, Japan
- Asymmetrical electron-positron accelerator (7 GeV e^-, 4 GeV e^+)
- Design luminosity: $8 \cdot 10^{35}$ cm^{-2} s^{-1}

CP-violation in the B meson system

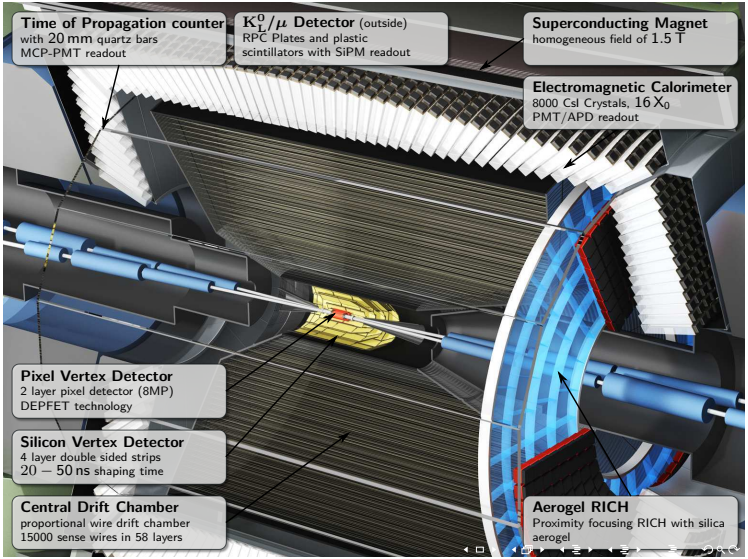


- $\Upsilon(4S)$ resonance at 10.58 GeV
- threshold for $B\bar{B}$ production

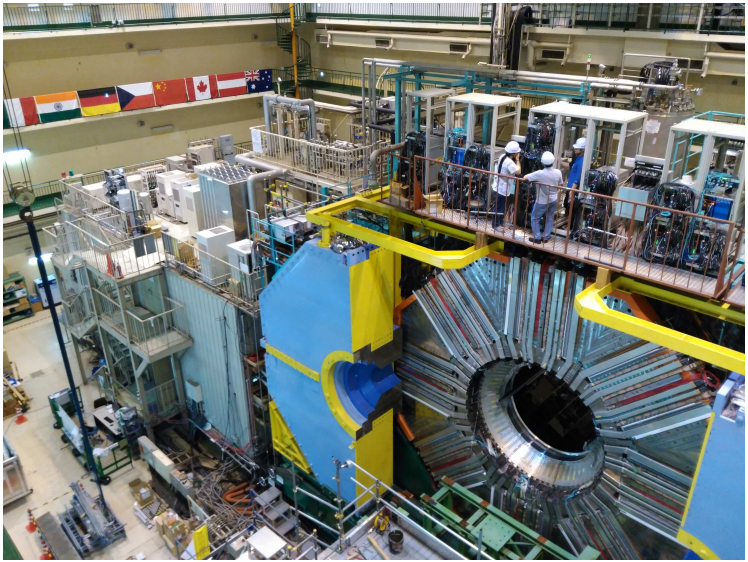


- higher statistics → higher precision and more rare decays
- lower boost as for KEKB → higher vertex resolution necessary
- higher luminosity and higher background → higher occupancy

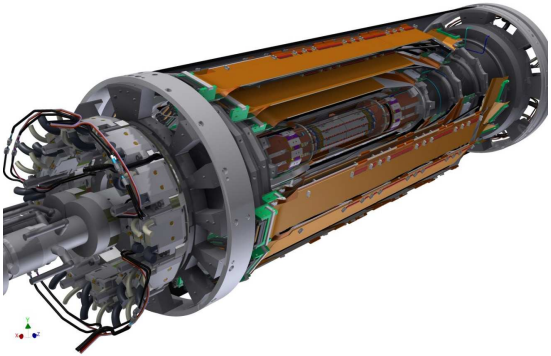
Belle II Detector

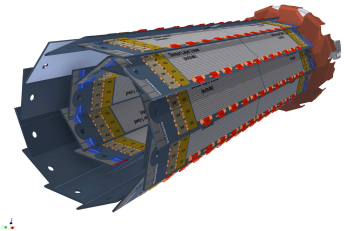


Belle II Detector



Silicon Vertex Detector

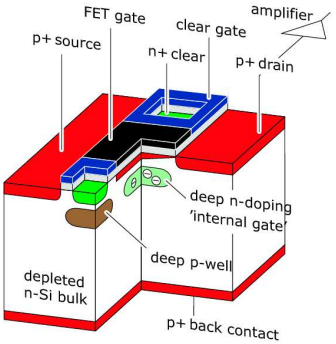


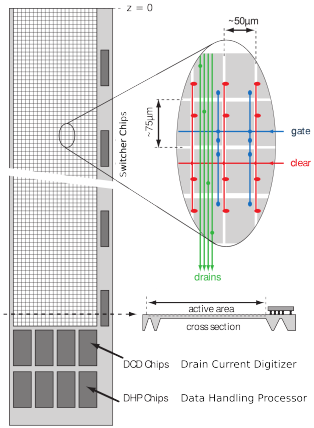


- 2 layers of DEPFET pixel sensors
- 4 layers of silicon strip sensors

- 8 ladders in layer 1 (radius 14 mm)
- 12 ladders in layer 2 (radius 22 mm)
- 40 modules with each 192 000 Pixeln
- pixel sizes: 55 μm$\times$50 μm up to 80 μm$\times$50 μm
- frame rate: 50 kHz row rate: 10 MHz

DEPFET pixel and matrix structure

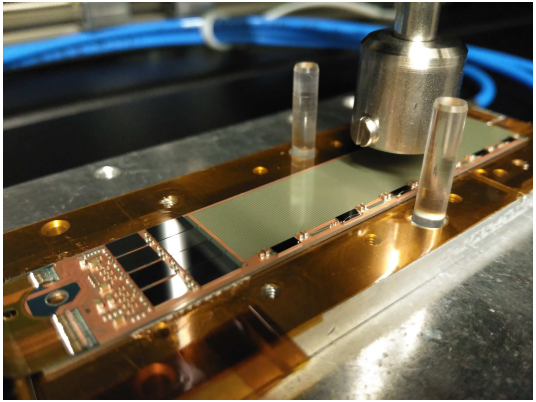




- DEpleted P-channel Field Effect Transistor
- conversion of charge into current
- internal signal amplification
- just 75 µm thick

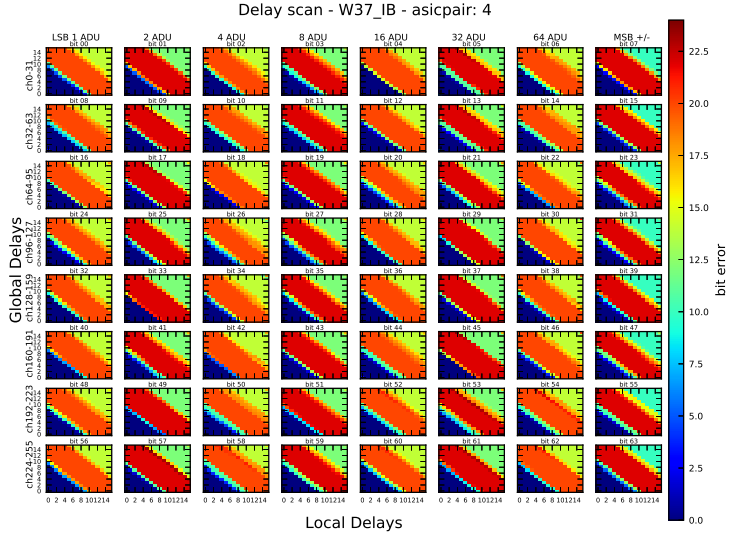
- 3 ASICs for control and readout
  Application-Specific Integrated Circuit
- readout of four lines at the same time
- (active part / total matrix size) = 100 %

Quality assurance and characterization of PXD modules



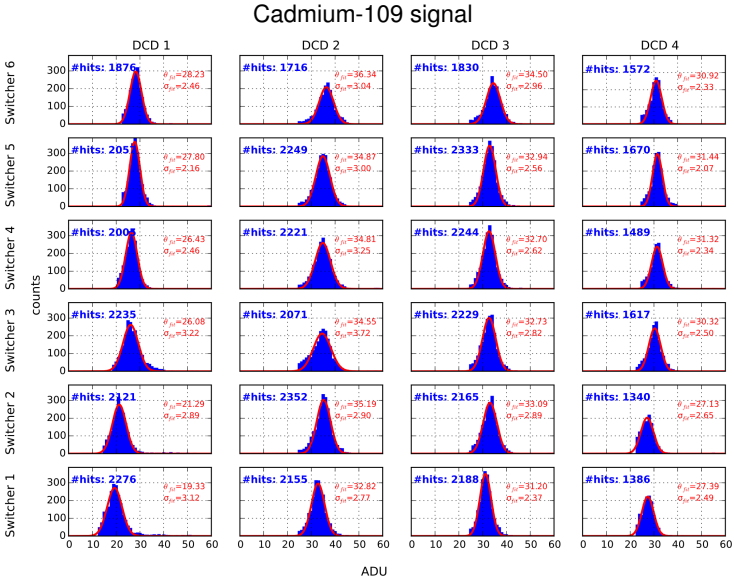
- Optimal settings will be detected in various tests and will be stored in a configuration database.
  > 10 000 process variables per module
- Analyzed data/results will be uploaded to a production database. Upon this basis the modules will be evaluated and sorted in to classes.
- The best modules will be used for the PXD.

Examples for measurements: delay elements



- 2D scan over the delay settings of the communication between Drain Current Digitizer and Data Handling Processor
- Color code indicates the number of faults during transmission of a test pattern.

Examples for measurements: Cadmium-109 source

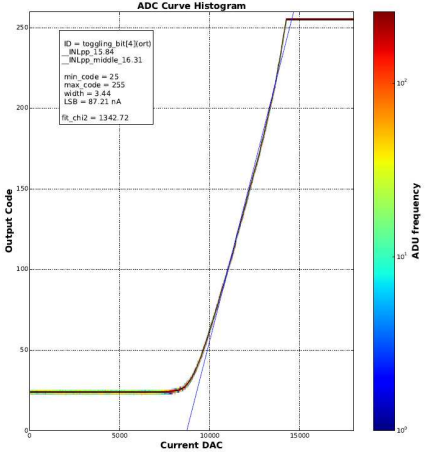


- reference signal corresponding to a MIP (minimum ionizing particle)
- optimization of the various operation voltages for matrix and ASICs

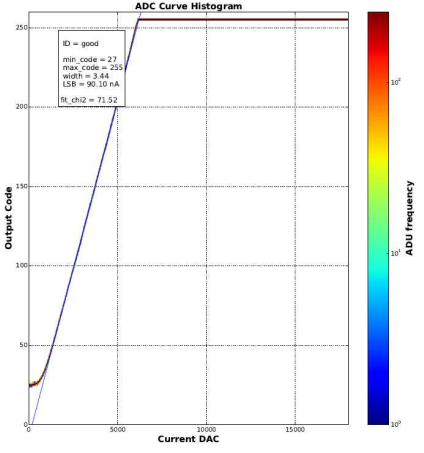
Examples for measurements: analog-digital transfer curves

Linearity of the transfer curves of the analog-to-digital converters

not linear



linear



EMC measurements at ITAinnova, Zaragoza

EMC = Electromagnetic Compatibility

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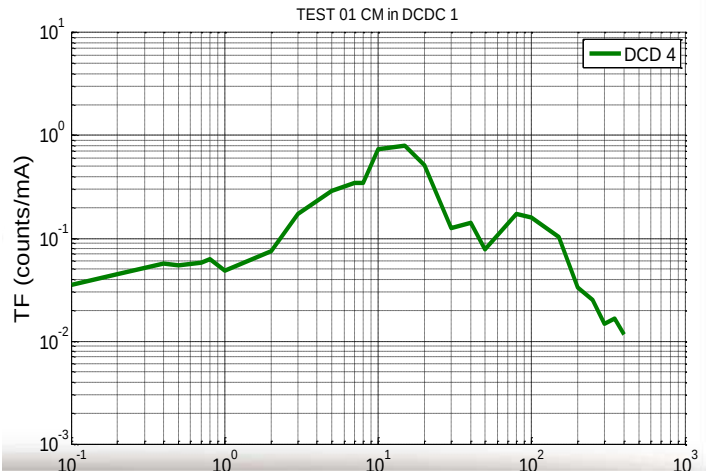
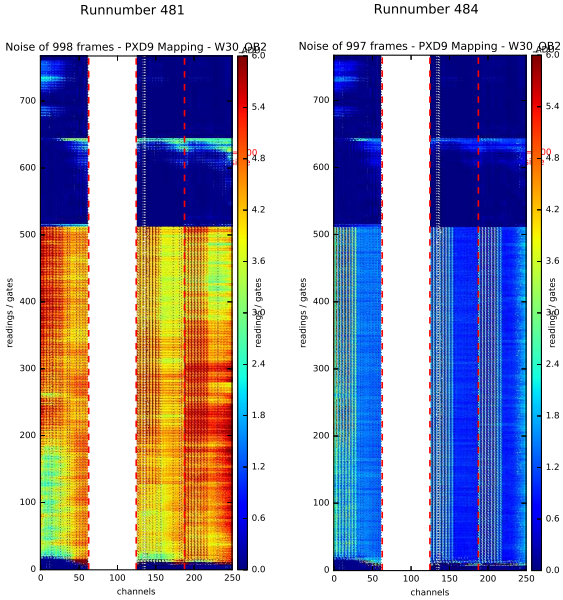


EMC measurements at ITAinnova, Zaragoza

frequency: 20 MHz
amplitude: 80 dB
current: 10 mA



frequency: 40 MHz
amplitude: 84 dB
current: 16 mA

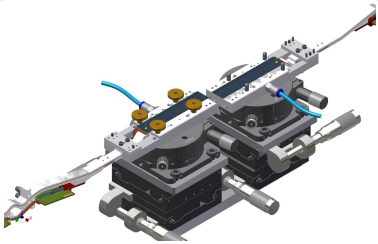
Summary and outlook

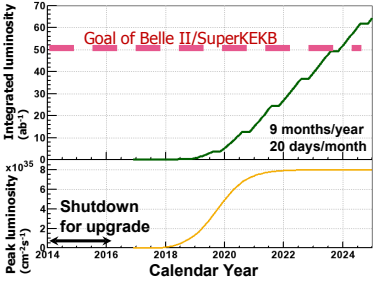
Summary:

- upgrade of SuperKEKB and Belle II
  finished soon
  first bunches: already in 2016
- promising prototypes of DEPFET modules
  have been tested
- series production of PXD modules started
- preparations for the quality assurance and
  characterization almost finished

Outlook:

- gluing of two modules to one ladder
  mounting onto support and cooling structure
- start of first part of the vertex detector:
  mid of 2017
  (all 6 layers but just one direction)
- PXD at KEK: October 2017





Backup

Quality assurance and characterization of PXD modules

measurements for each module in detail

- power up and JTAG configuration, voltage checks (digital, analog, matrix)
- JTAG Boundary-Scan
- DHPT link parameter
- DHPT - DCD communication delay-scan
- pedestals (number of working pixels)
- ADC transfer curves
- 2bit offset DACs
- sample point
- DEPFET optimization with Cd-109 source
- clear efficiency with infrared laser
- Gated Mode

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