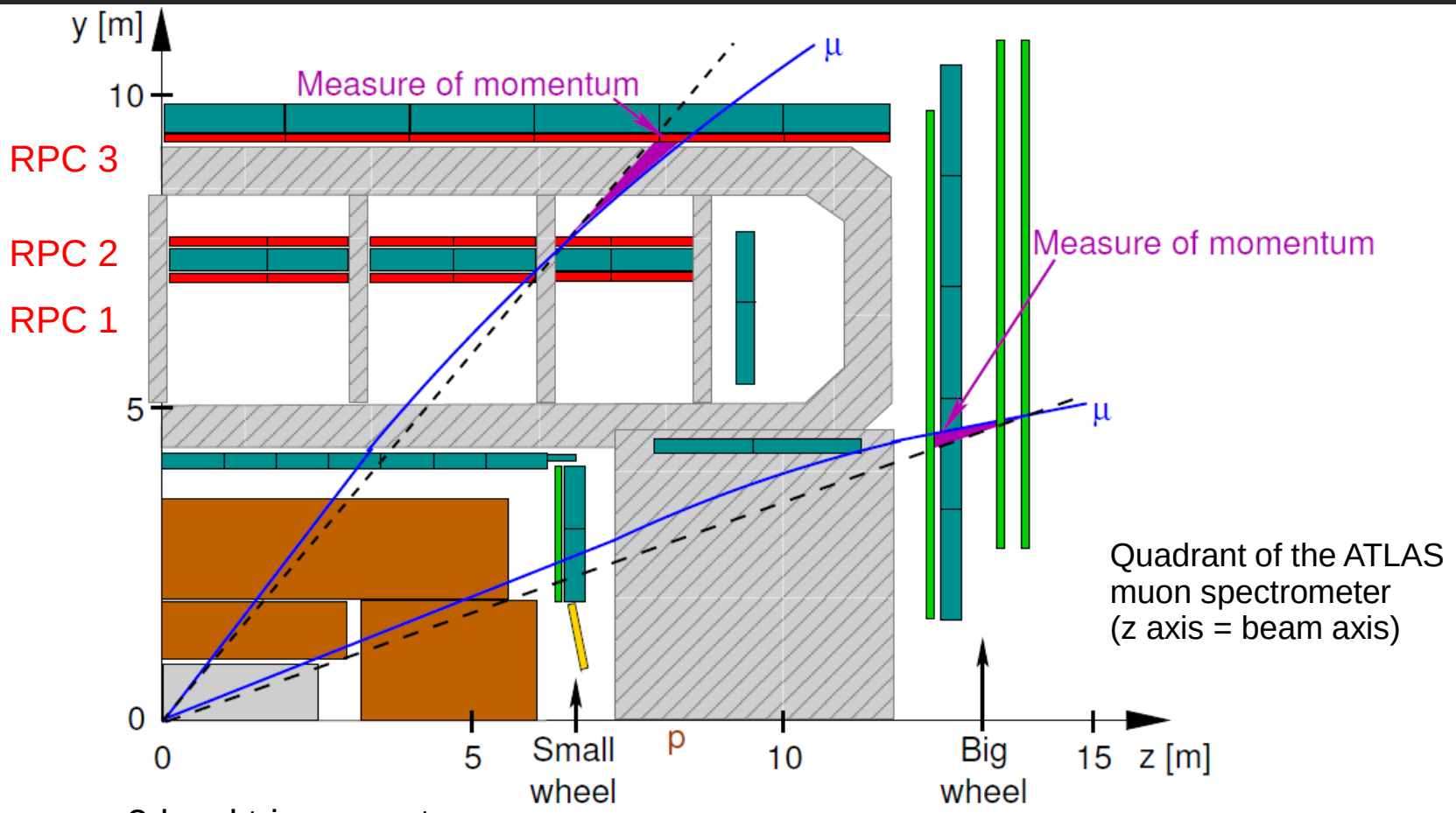
Development and Test of a Demonstrator for a First-Level Muon Trigger based on the Precision Drift Tube Chambers for ATLAS at HL-LHC

K. Schmidt-Sommerfeld

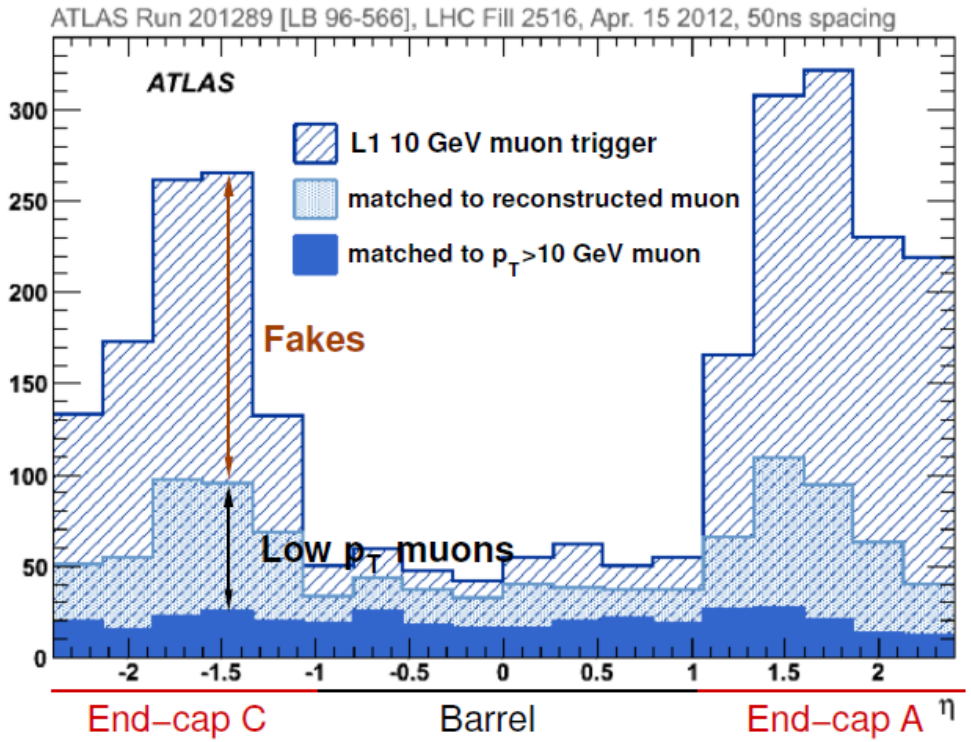
Max-Planck-Institut für Physik, München

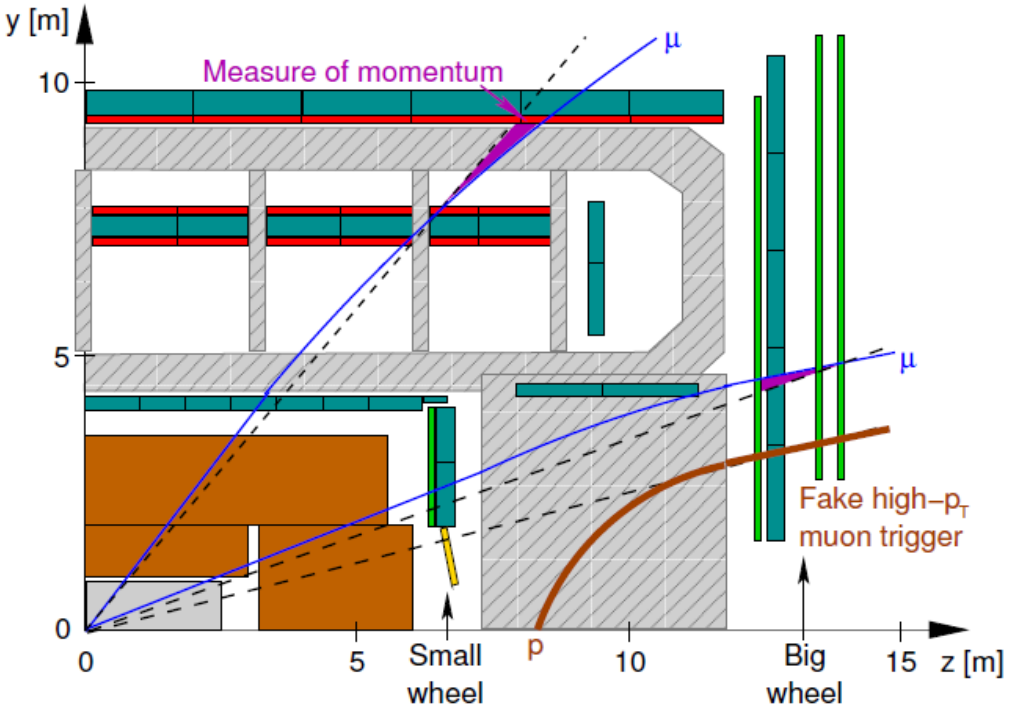
The ATLAS 1st Level Muon Trigger in LHC Run 1



- ATLAS presently uses a 3-level trigger system.
- The Level-1 high-p_T muon trigger is based on the coincindence of hits in three RPC layers in the barrel and three TGC layers in the middle endcap wheels.
- Muon momentum determination from the deviation of the hits from a straight line through the interaction point.
- High γ and neutron background rates in the ATLAS muon spectrometer.
  $\rightarrow$ ~7 x higher at HL-LHC: up to ~300 kHz/drift tube in the middle endcap layer corresponding to ~10% occupancy.

Sources of Level-1 Muon Triggers Run 1

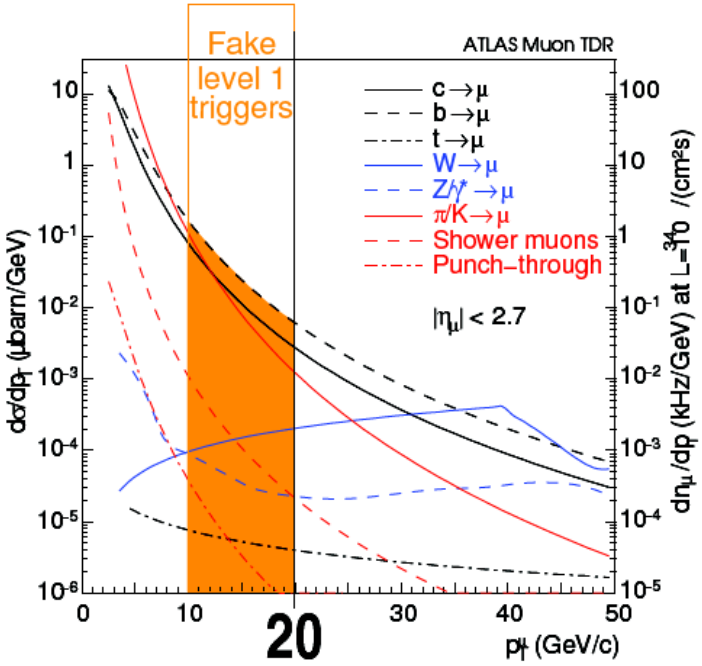




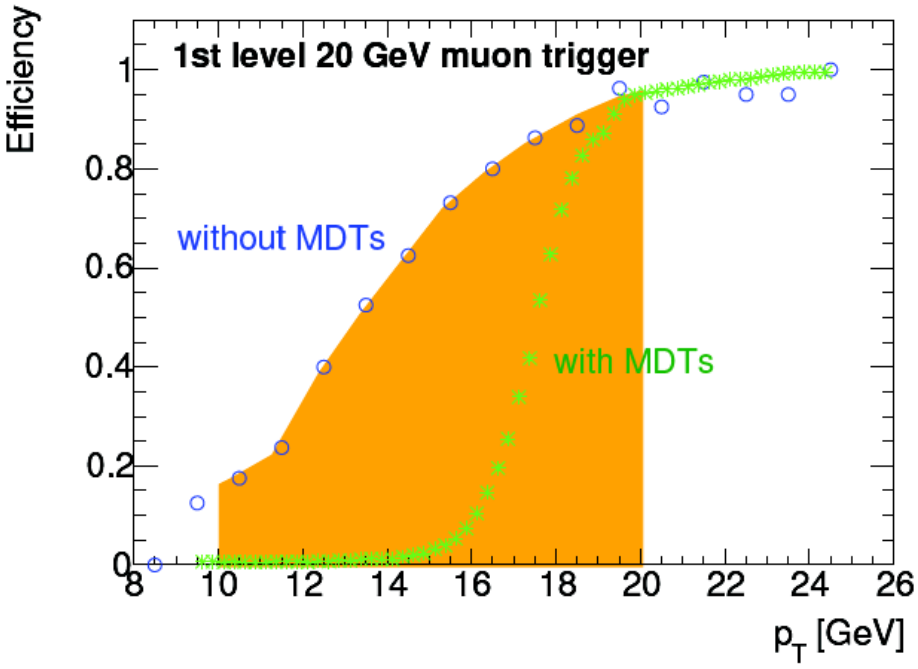
- The muon trigger rate is dominated by fake triggers in the end-caps caused by charged particles not emerging from the interaction point.
- Real muon triggers contaminated with below-threshold muons due to the limited spatial and momentum resolution of the trigger chambers.

MDT-Based 1st Level Trigger at HL-LHC

Inclusive muon cross section



Muon 1st level trigger effciency



- The interesting physics is at p_T > 20 GeV.
- The inclusive muon cross section rises very steeply at low p_T.
- The present 1st level muon trigger with 20 GeV nominal threshold accepts high rate of muons with 10 GeV <p_T<20 GeV due to the limited spatial resolution of the trigger chambers.
- Sharpening of the trigger threshold by using the precision muon drift-tube (MDT) chambers is the solution to limit the muon trigger rate
- ⇒ New MDT on- and off-chamber electronics for new read-out and trigger architecture.

New MDT Readout Architecture

- 1 MHz 1st level trigger rate with 6 µs latency for ATLAS operation at HL-LHC.

  (Present Level-1 trigger: 100 kHz rate, 2.5 µs latency).

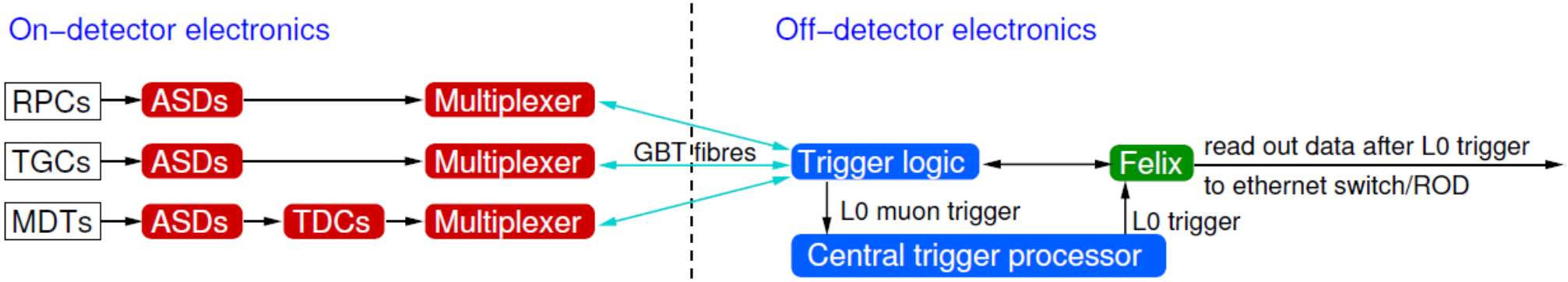
  For fast hardware-based muon track trigger algorithms with < 3 µs latency see talk by Ph. Gadow.

- For MDT-based 1st level trigger:

  MDT chambers send their data continuously to the trigger and DAQ system.
  All further processing and muon track and momentum reconstruction with full resolution performed in trigger processor off the detector.

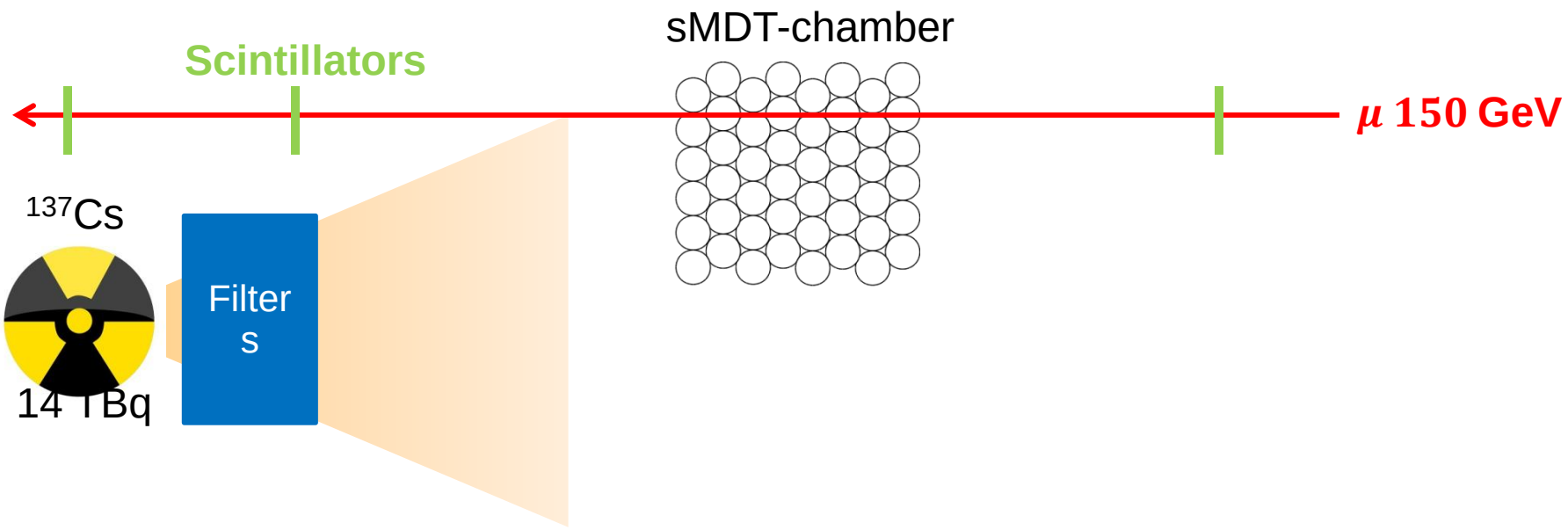
  RoIs of the RPC/TGC muon trigger chambers are used as seeds for MDT track segment finding

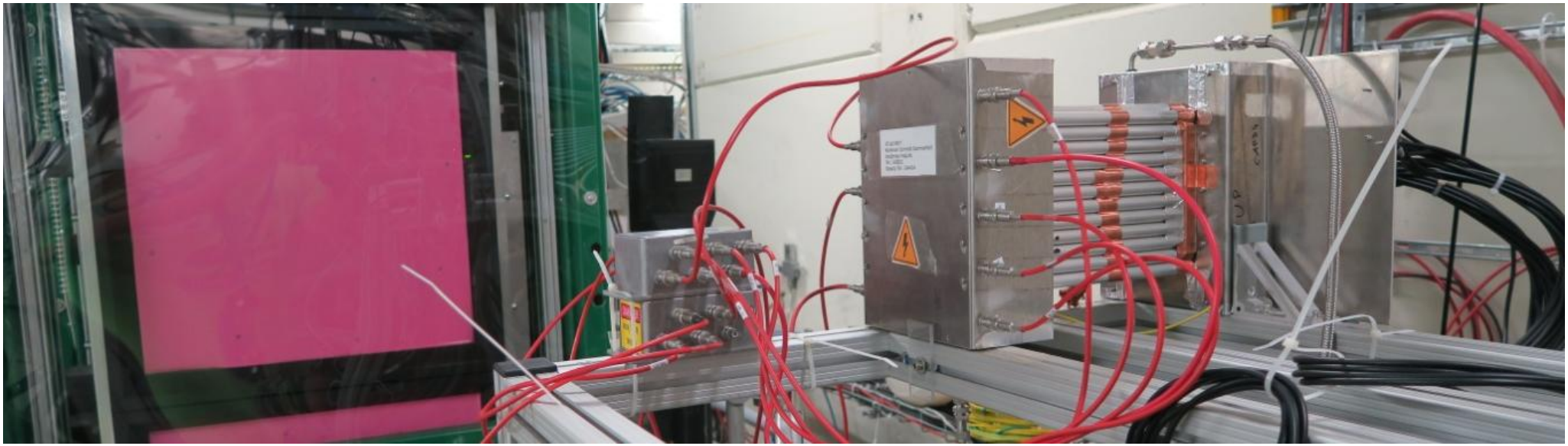
- New MDT on-chamber electronics is required,
  front-end boards with amplifier-shaper-discriminator (ASD) and TDC chips,
  As well as new off-chamber electronics, MDT trigger logic, Readout Driver ("Felix"):



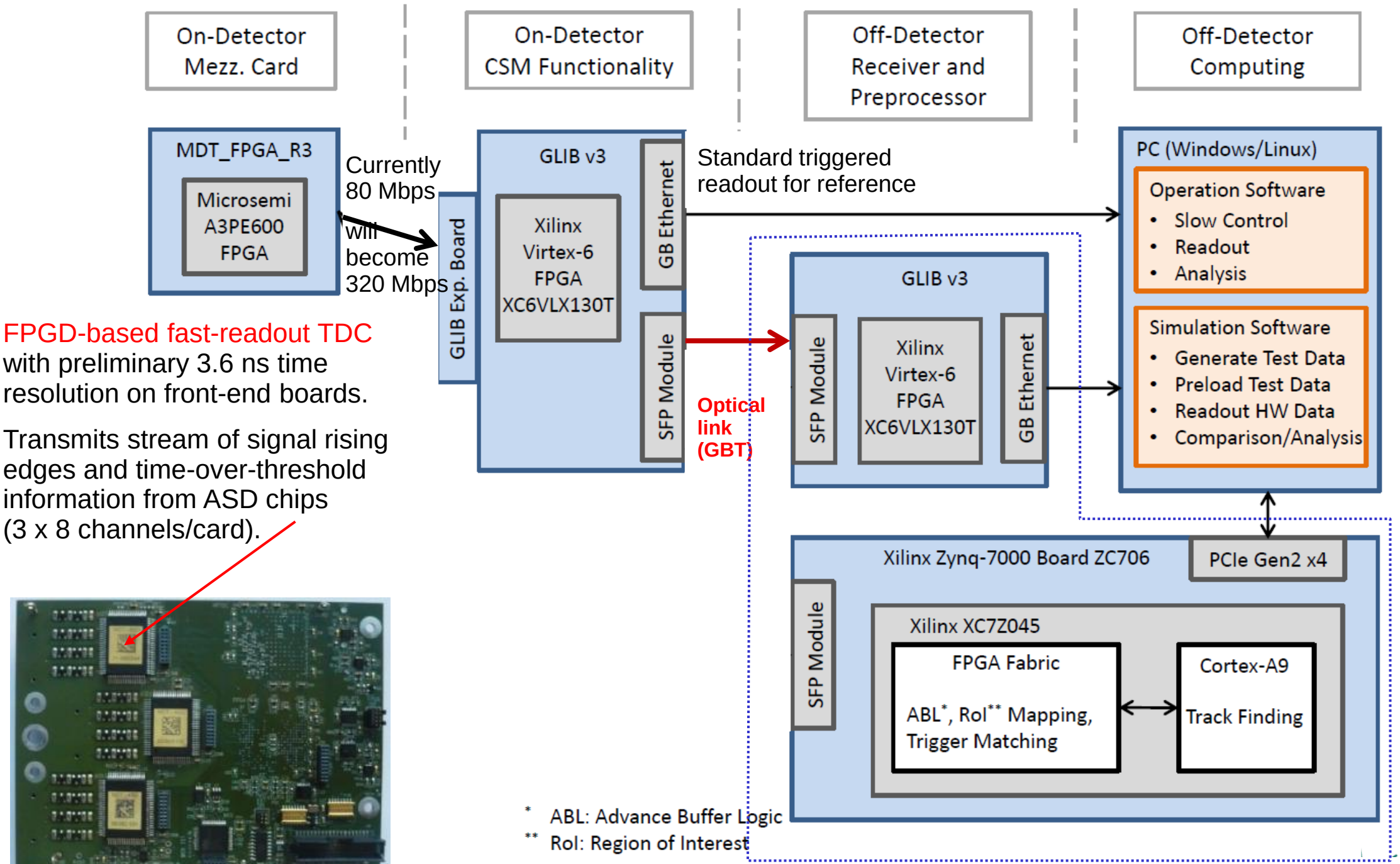
MDT Trigger Demonstrator Test

Setup in a muon beam at the γ irradiation facility (GIF++) at CERN:





MDT Trigger Demonstrator Schematics



FPGD-based fast-readout TDC with preliminary 3.6 ns time resolution on front-end boards.

Transmits stream of signal rising edges and time-over-threshold information from ASD chips (3 x 8 channels/card).

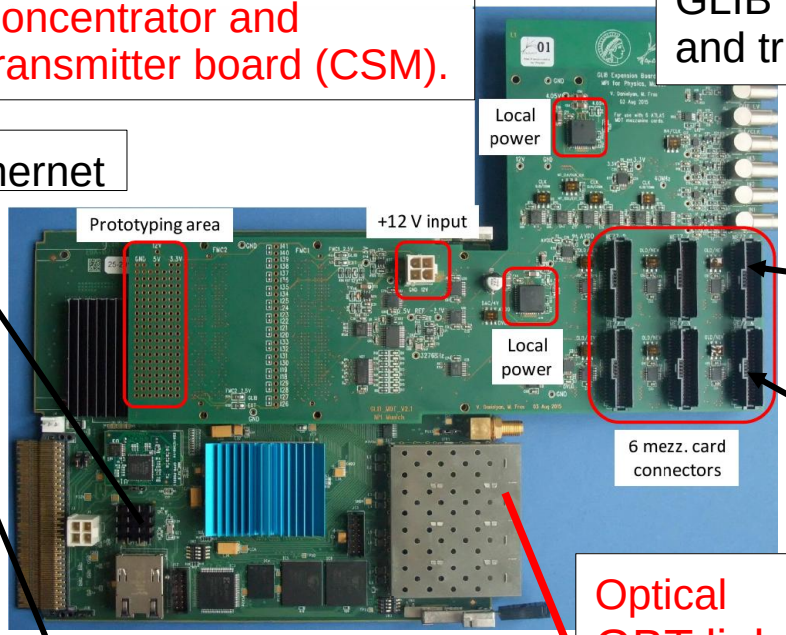
MDT Trigger Demonstrator Electronics

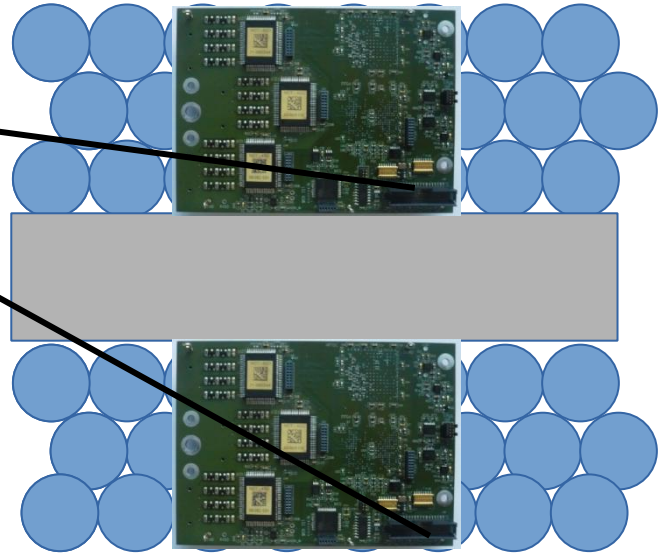
Readout and DCS PC

Gbit ethernet

On-chamber data concentrator and transmitter board (CSM).

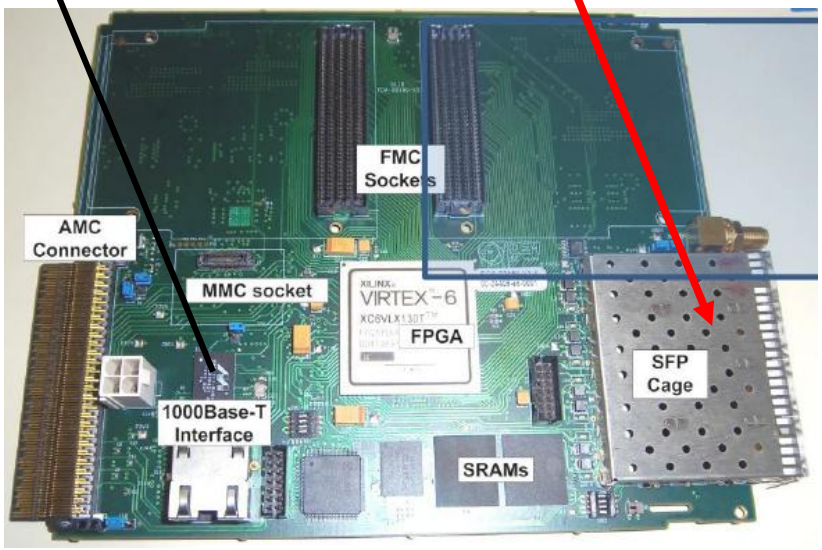
GLIB based interface to front-end cards and trigger (for standard readout as ref.)

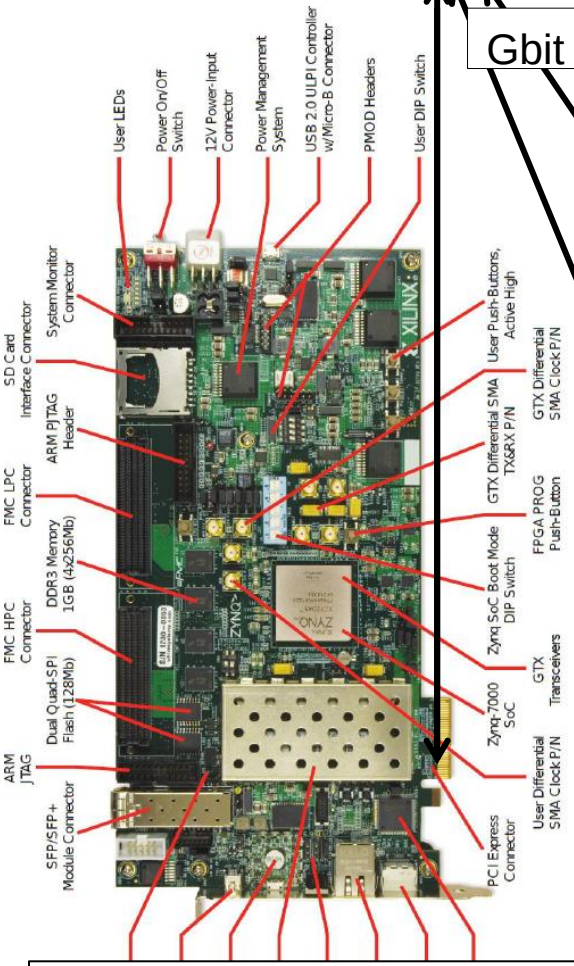




Optical GBT link

Off-chamber data receiver board



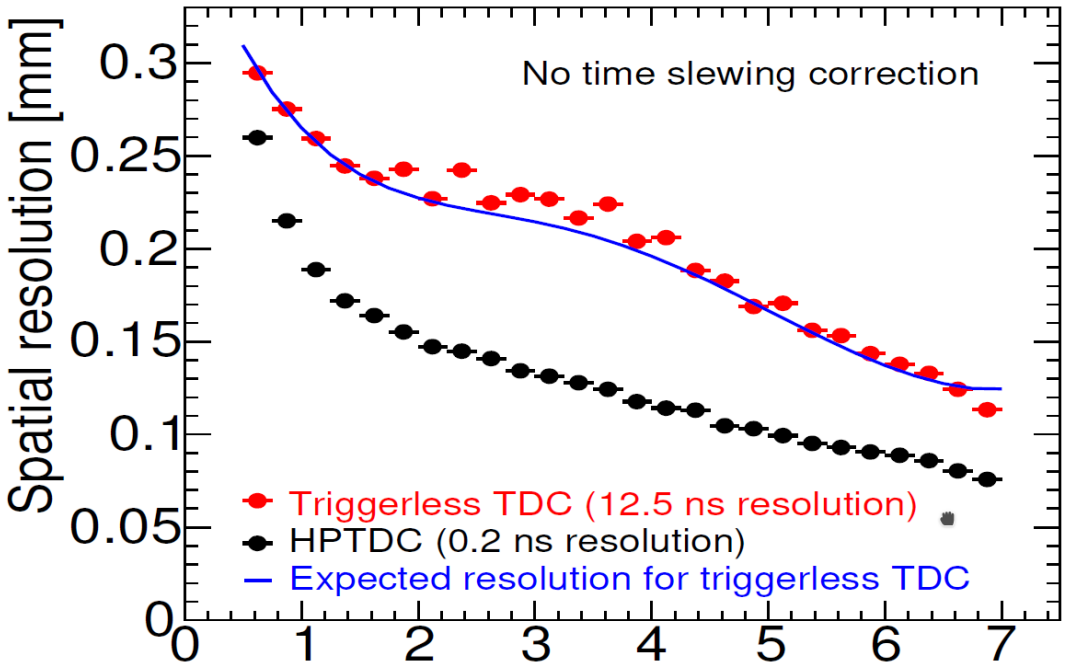


Track trigger processor:
Cortex-A9 ARM CPU (dual core) with FPGA interface on a Xilinx-Zynq-7000 board

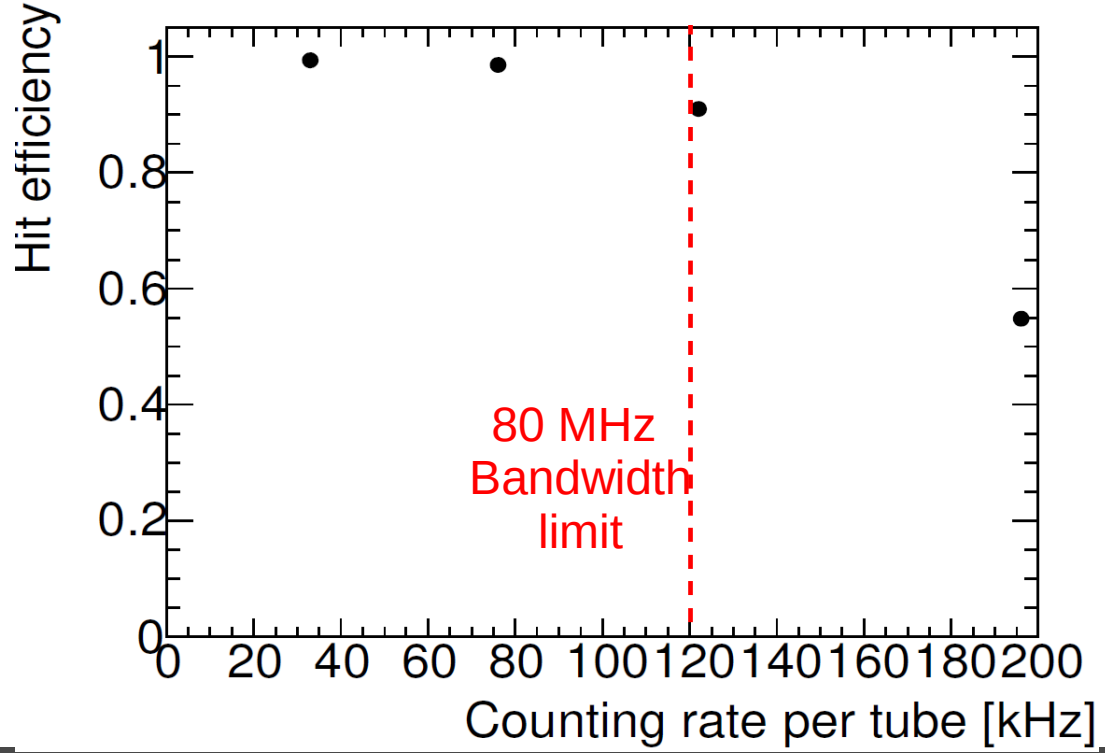
MDT front-end (mezzanine) cards with standard TDC chips (CERN HPTDC, 0.2 ns time resolution) and additional FPGA-based TDCs supporting continuous triggerless readout

Tested in muon beam at CERN under high γ irradiation (GIF) 2013-2016.

MDT Trigger Demonstrator Test



- Drift tube spatial resolution as a function of drift radius
- Expected dependence on the radius
- Difference between triggerless TDC and HPTDC due to digitization resolution
- Measured in a muon beam at the γ irradiation facility (GIF++) at CERN in 2016



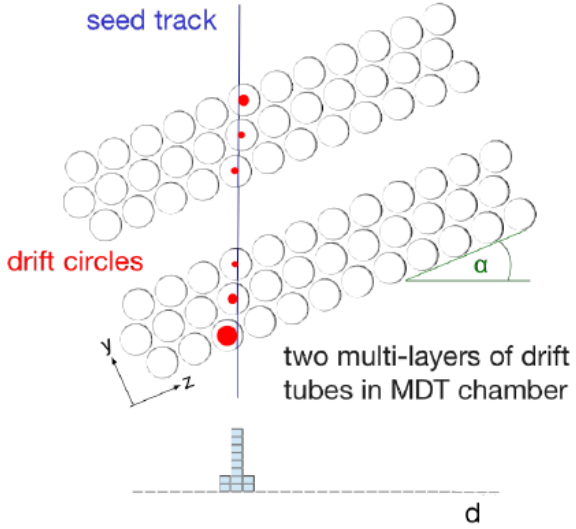
- Efficiency := fraction of HPTDC hits found in triggerless TDC read-out chain
- 100% eff. up to 80 kHz counting rate
- Eff. loss at high rates due to bandwidth limitations

First MDT Track Trigger Processor Performance Test

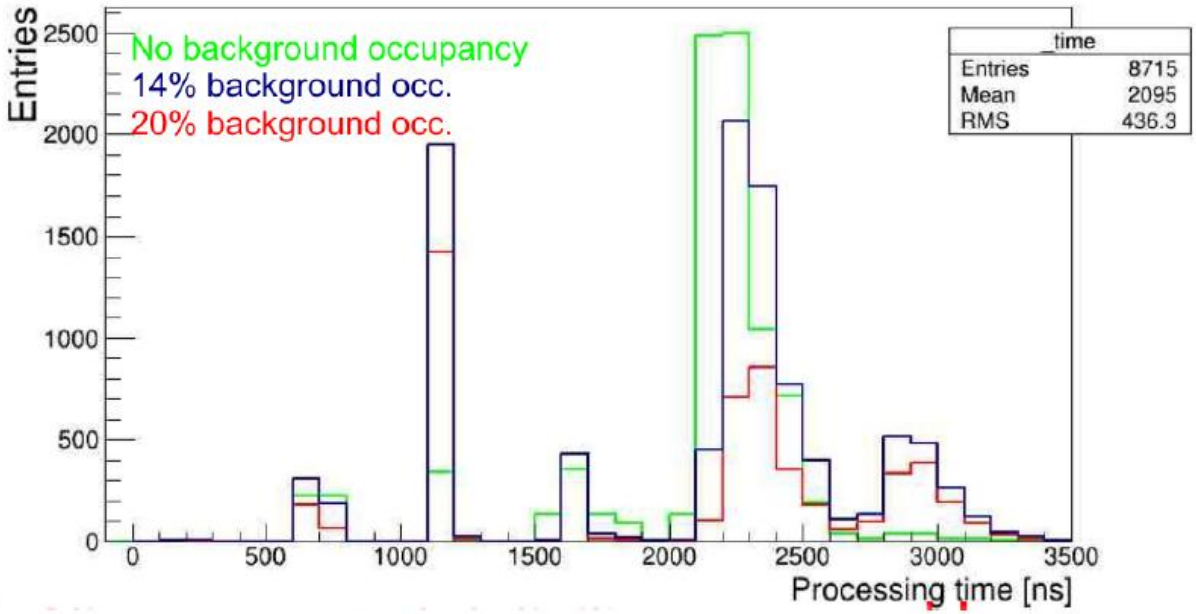
- Data recorded with a MDT chamber at the Gamma Irradiation Facility at CERN used to simulate realistic operating conditions.

- Track segment reconstruction algorithm in C and ARM assembler code (simplified, 1D Hough transform-based algorithm for first test).

  Run on the Cortex A9 ARM processor at 1 GHz (FPGA used for I/O and data mangement).



Processing time on a single ARM core:



Processing time already <3.5 µs

even at 20% occupancy which is twice the maximum occupancy in ATLAS at the HL-LHC!

Still many possibilities for optimisation.

Conclusions

- A highly selective 1st level muon trigger is required for the operation of the ATLAS muon spectrometer at HL-LHC.
- This is achieved by incorporating the data of the precision muon drift-tube (MDT) chambers in the 1st level muon trigger.
- The selectivity of an MDT-based trigger was studied with LHC run-I data and shown to give a low 20 GeV single-muon trigger rate of $\leq$ 20 kHz.
- The MDT-based trigger requires fast, triggerless (streamed) MDT read-out and new readout electronics.
  .
  TDC chip with fast streamed readout and increased bandwidth under development, replacing FPGA-based demonstrator.
- Demonstrators of all components of this fast readout have been designed and successfully tested in muon beams under realistic γ background radiation rates.