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DEPFET Active Pixel Detector

Belle II

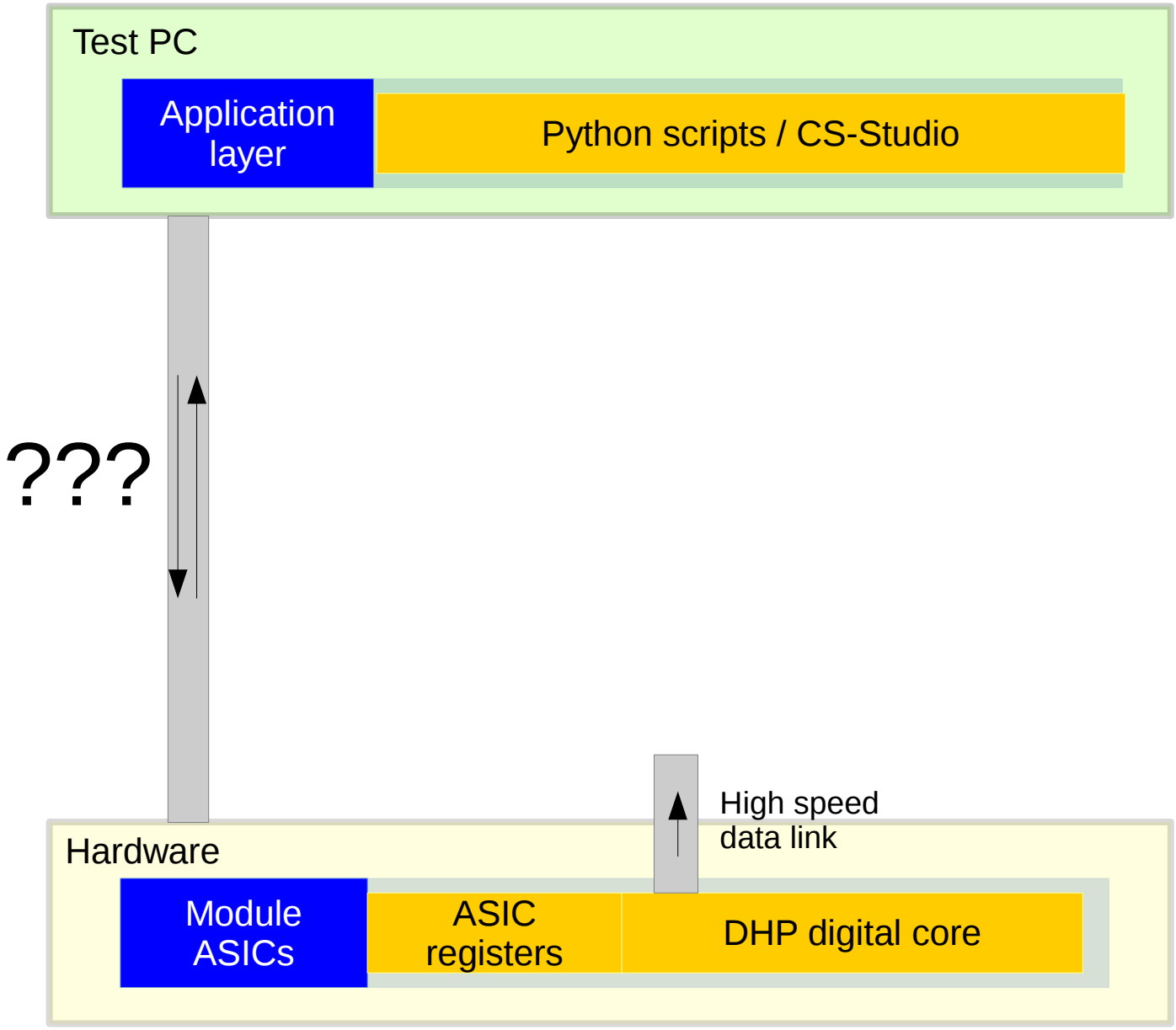
SI LAB Silizium Labor Bonn

Test System Timing Pitfall

Botho

SiLab DEPFET Meeting
15th February 2017

How does the Test System work?



CS-Studio and Python

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Test PC

Application layer

Python scripts / CS-Studio

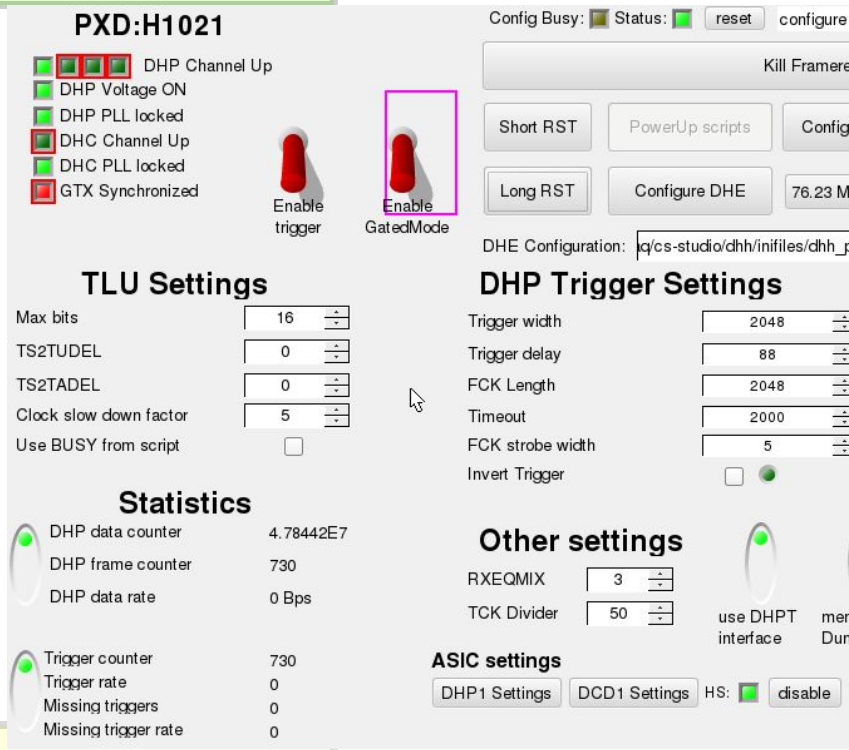
???

```
# enable triggering
trigger_enable = \
  get_pv("PXD:H1021:trg_en:S:set")
trigger_enable.put(1)

# check link status
link_status_pv = \
  get_pv("PXD:H1021:dhp1_channel_up:S:cur")
link_ok = link_status_pv.get()

if not link_ok:
      print("DHP link 1 is down")

# set DHP CML bias value
# and write to DHP JTAG register
get_pv(DHP, "idac_tx_bias:VALUE:set").put(200)
get_pv(DHP, "globalrs:trg:set").put(1)
```



High speed data link

Hardware

Module ASICs

ASIC registers

DHP digital core

Process Variables (PVs)

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Test PC

Application layer

Python scripts / CS-Studio

Read/write

EPICS IOC server

Process Variables (PVs)

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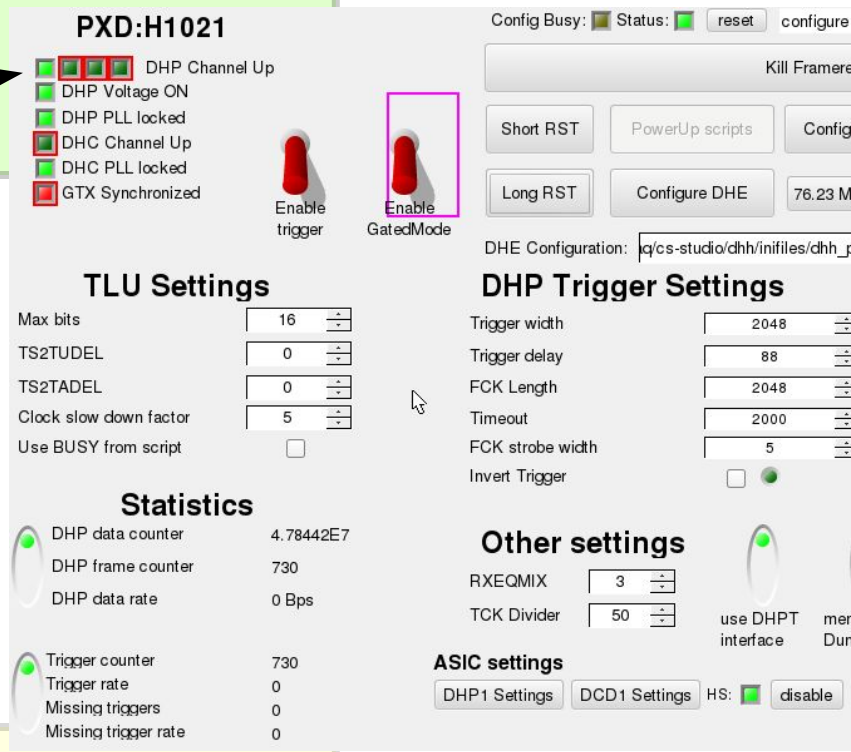


High speed data link

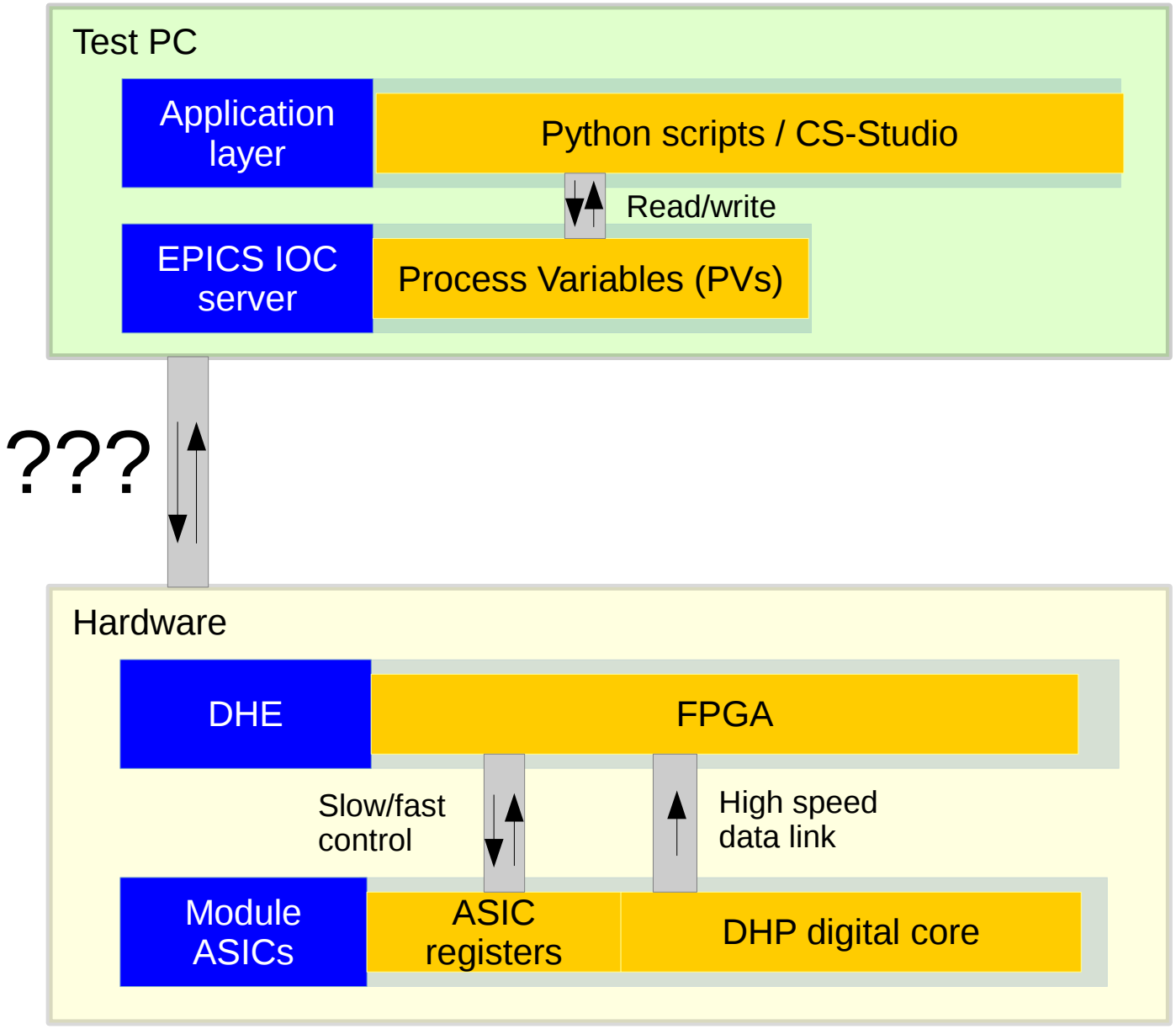
Hardware

Module ASICs

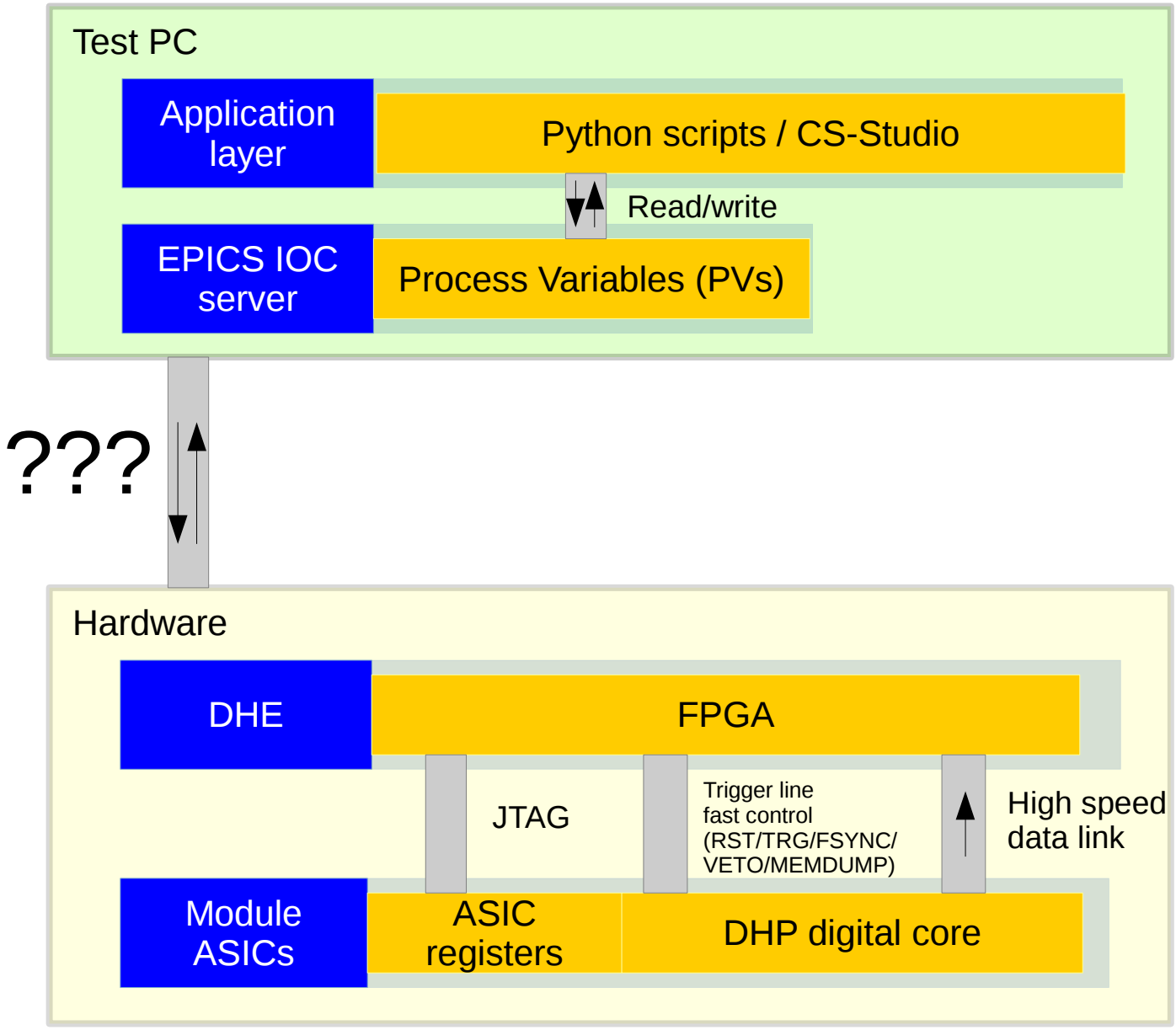
ASIC registers

DHP digital core

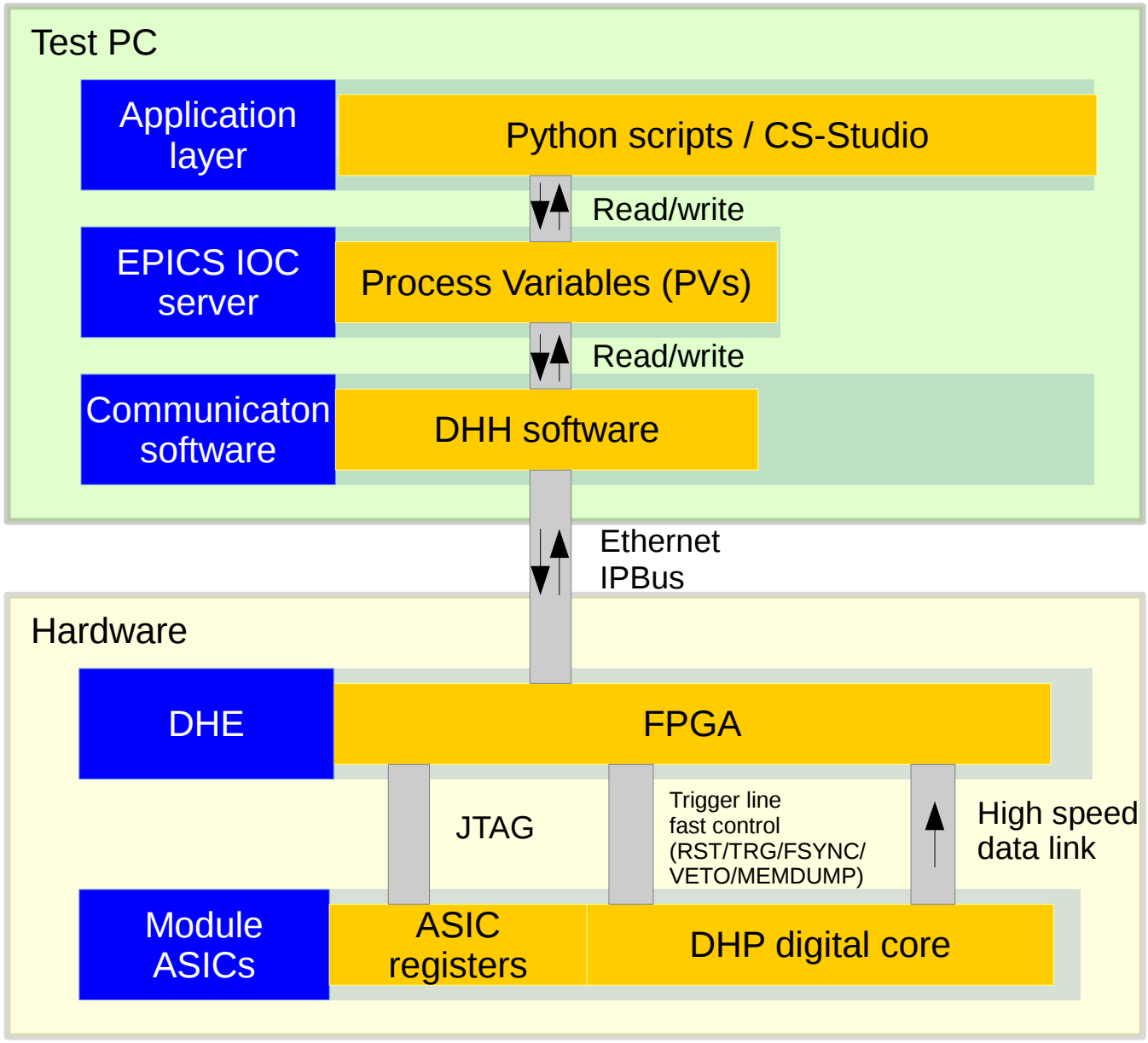
The Data Handling Enginge (DHE)



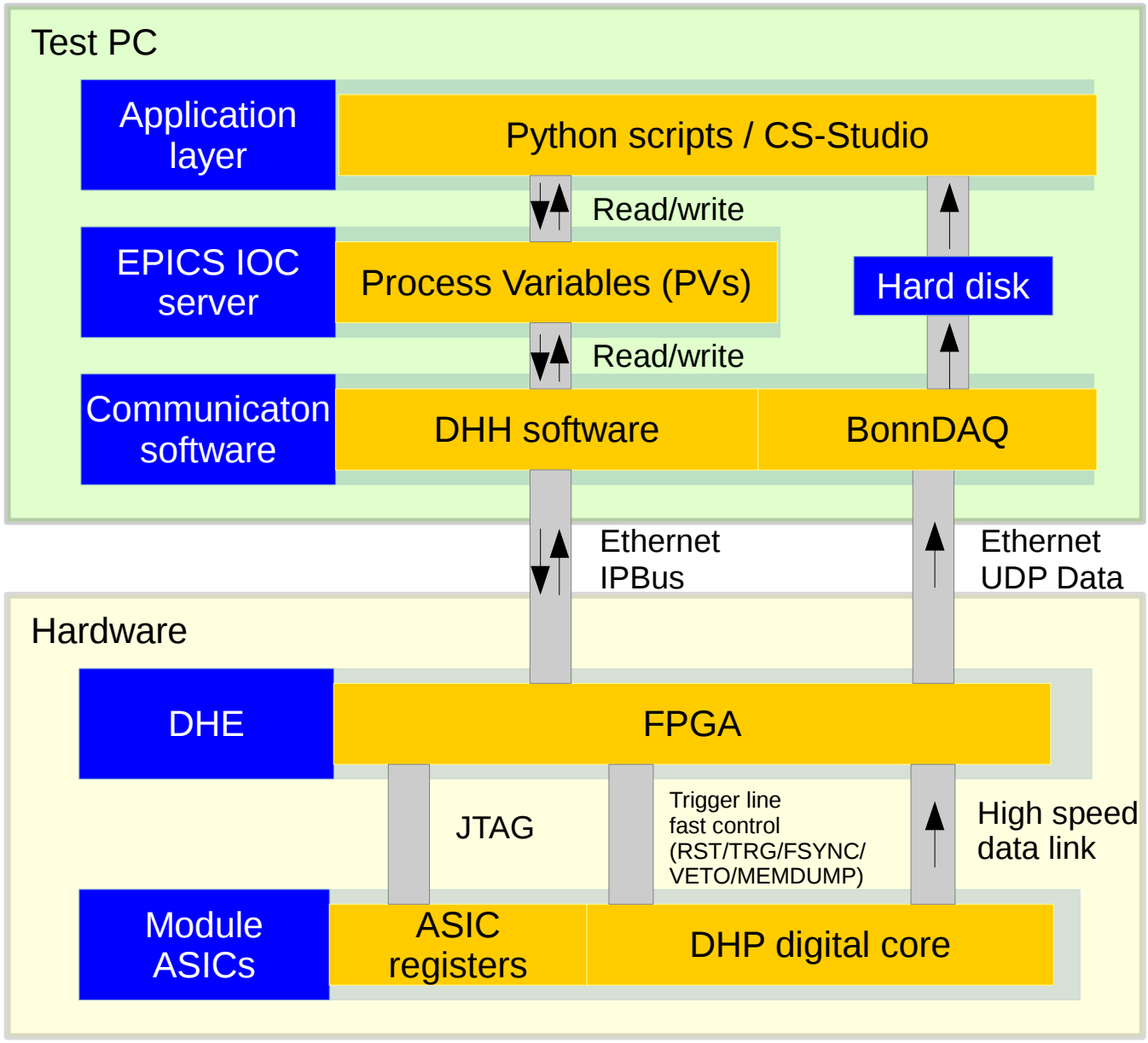
DHE ↔ Module ASIC communication



PC ↔ DHE communication

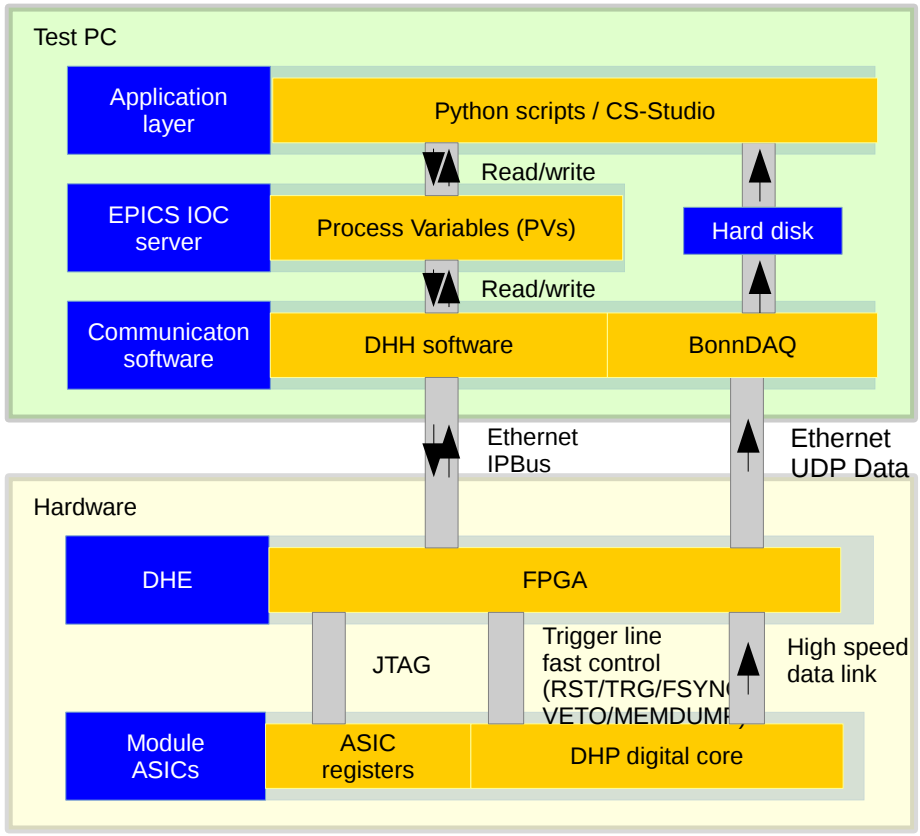


Data Aquisition



Why is it so complicated/ugly?

Laboratory Test System



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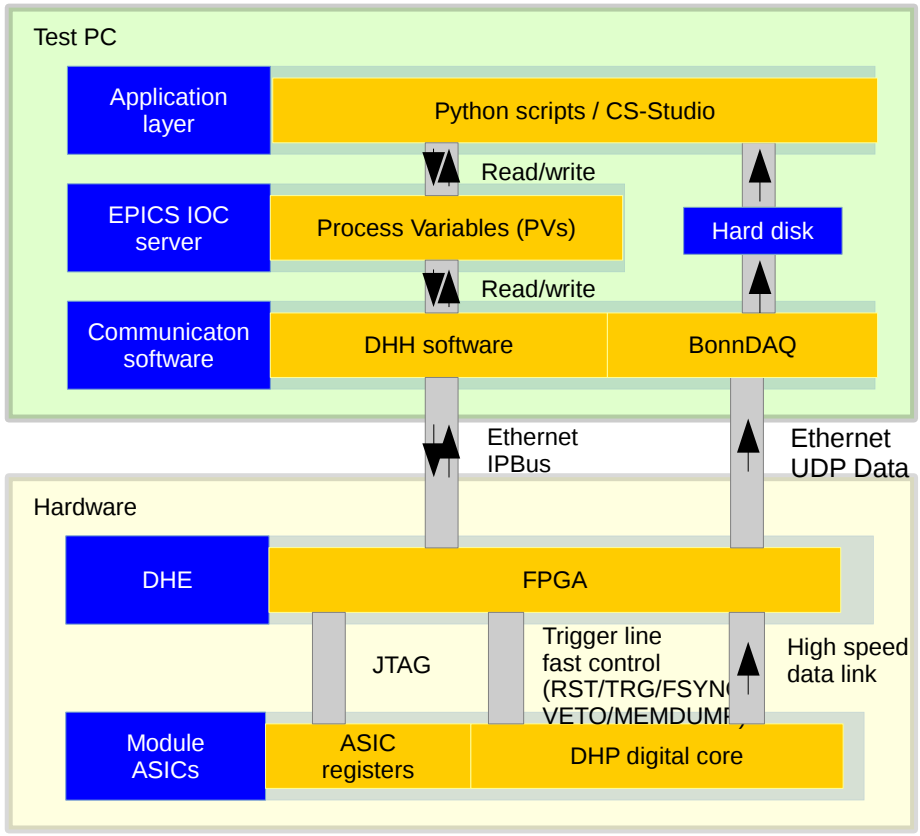
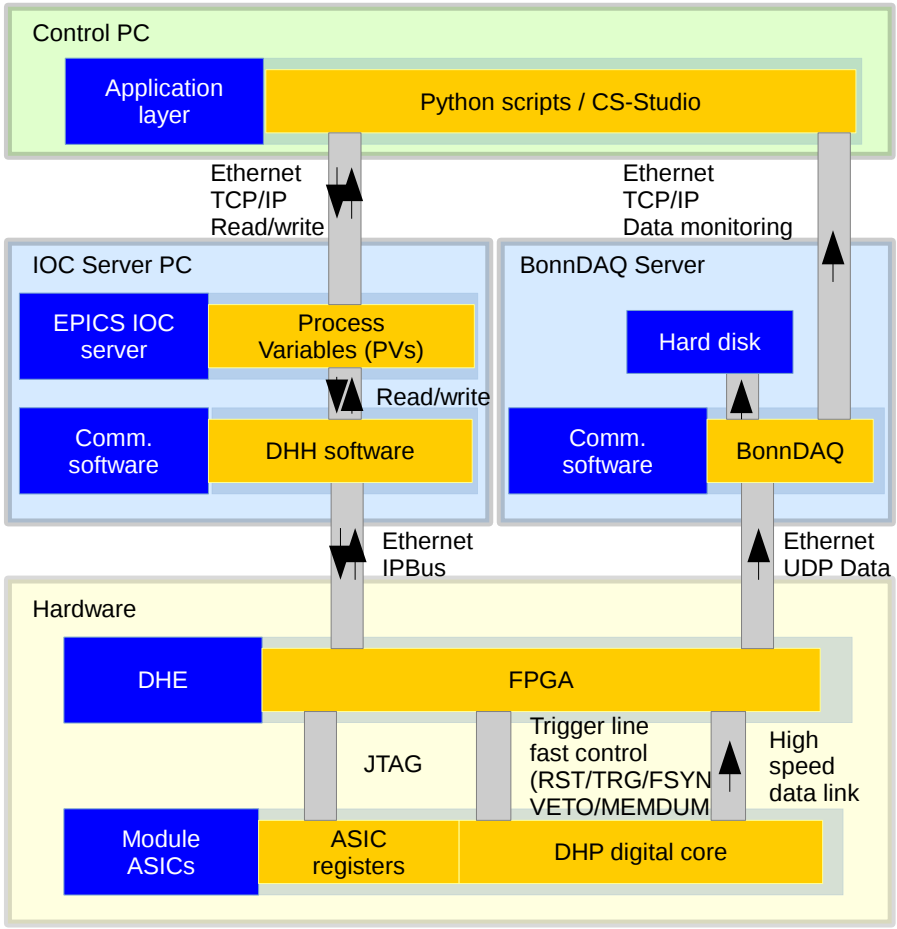
Laboratory Test System

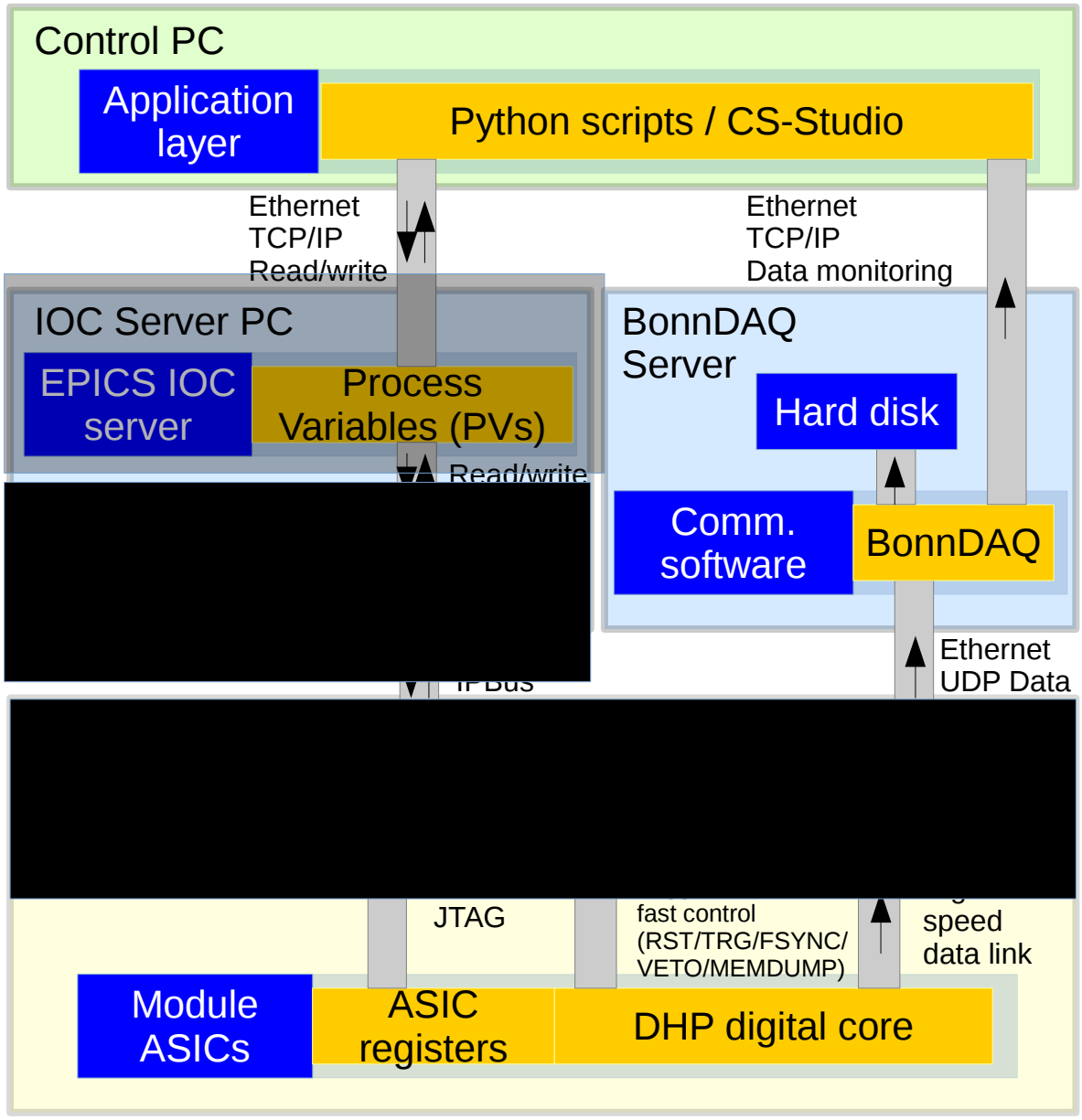


Belle II Experiment



→ The system is not optimized for laboratory testing!

Why does it give us a hard time



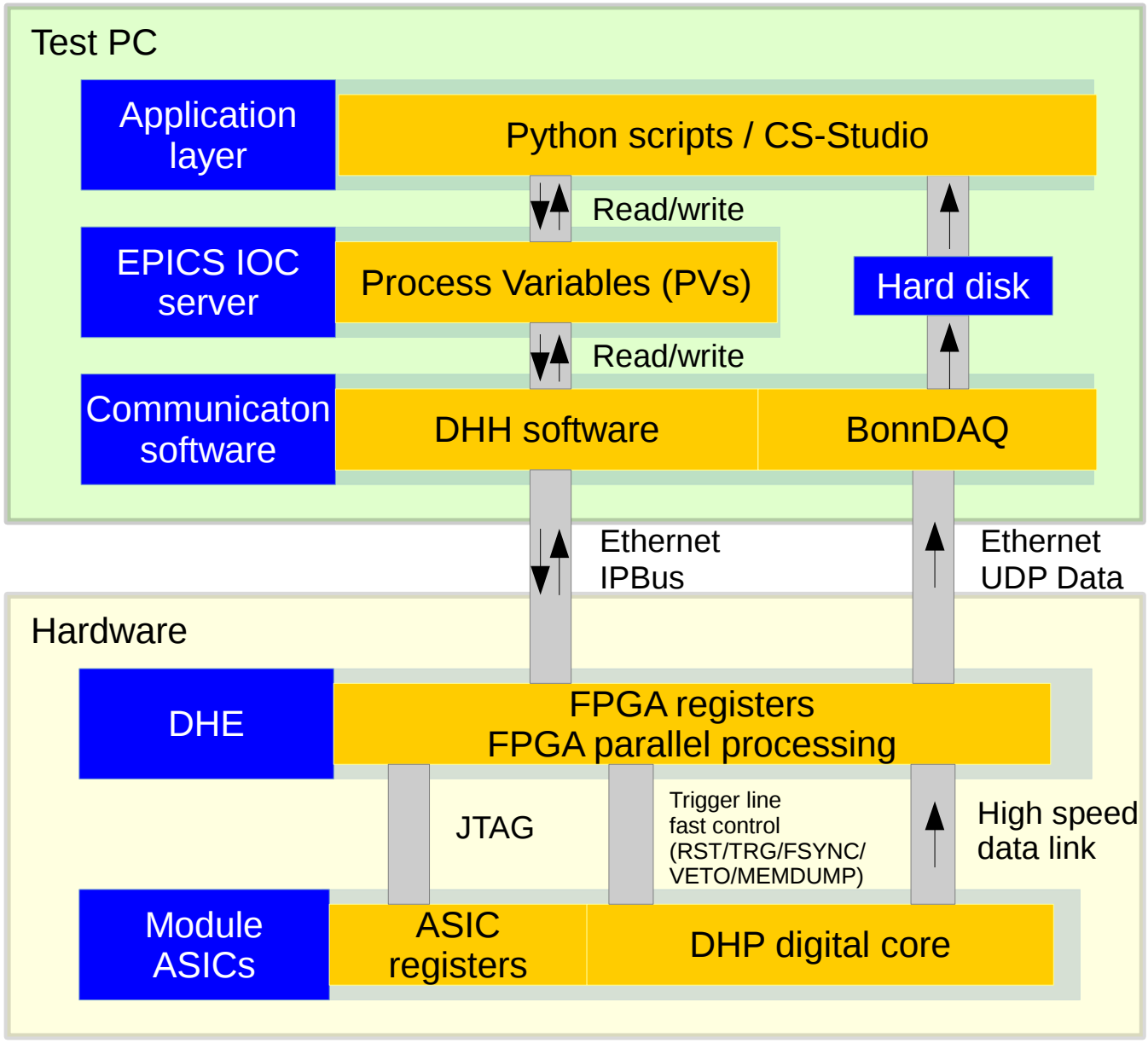
Insufficient knowledge

Black boxes!!!

Black boxes!!!

Black boxes!!!

Timing


Test PC
Application layer
Python scripts / CS-Studio
Read/write
EPICS IOC server
Process Variables (PVs)
Hard disk
Read/write
Communicaton software
DHH software
BonnDAQ
Ethernet IPBus
Ethernet UDP Data
Hardware
DHE
FPGA registers
FPGA parallel processing
JTAG
Trigger line fast control (RST/TRG/FSYNC/ VETO/MEMDUMP)
High speed data link
Module ASICs
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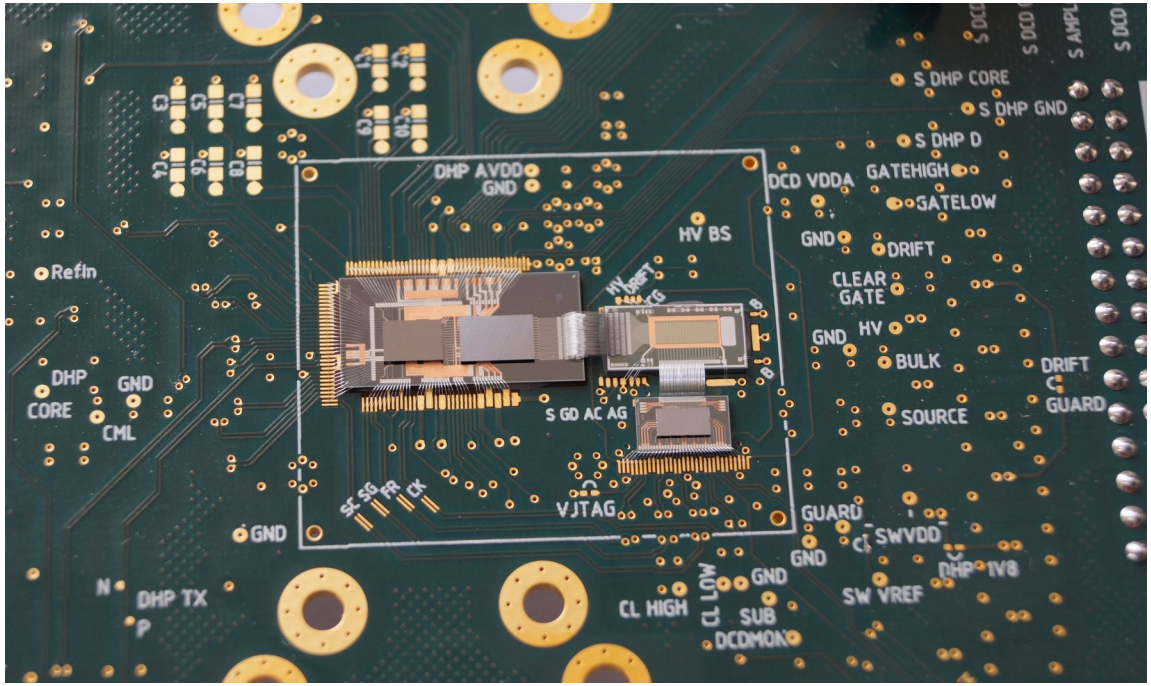
DHP digital core

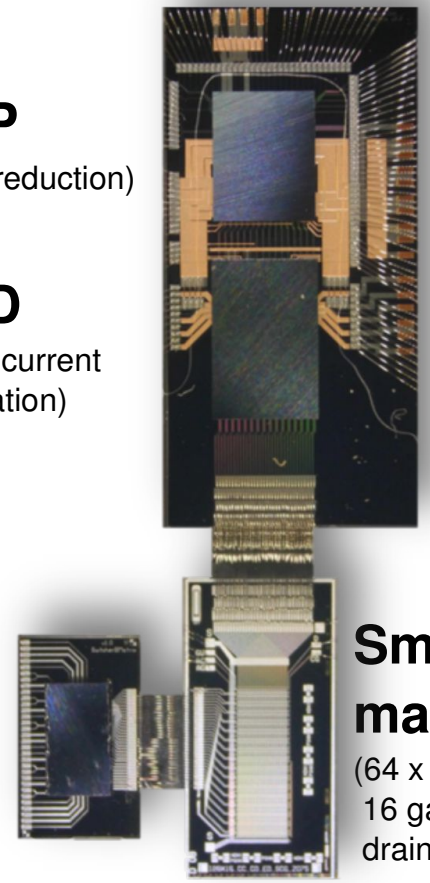
Hybrid 5 Systems

- Dedicated small system for laboratory tests



DHP
(Data reduction)

DCD
(Drain current digitization)



Switcher
(Matrix steering)

Small matrix
(64 x 32 pixels / 16 gates, 128 drain lines)

- PCB with minimal number of ASICs for a full test system
- Latest iteration of ASICs is tested as well as matrix prototypes