



Status of FANGS towards Phase 2

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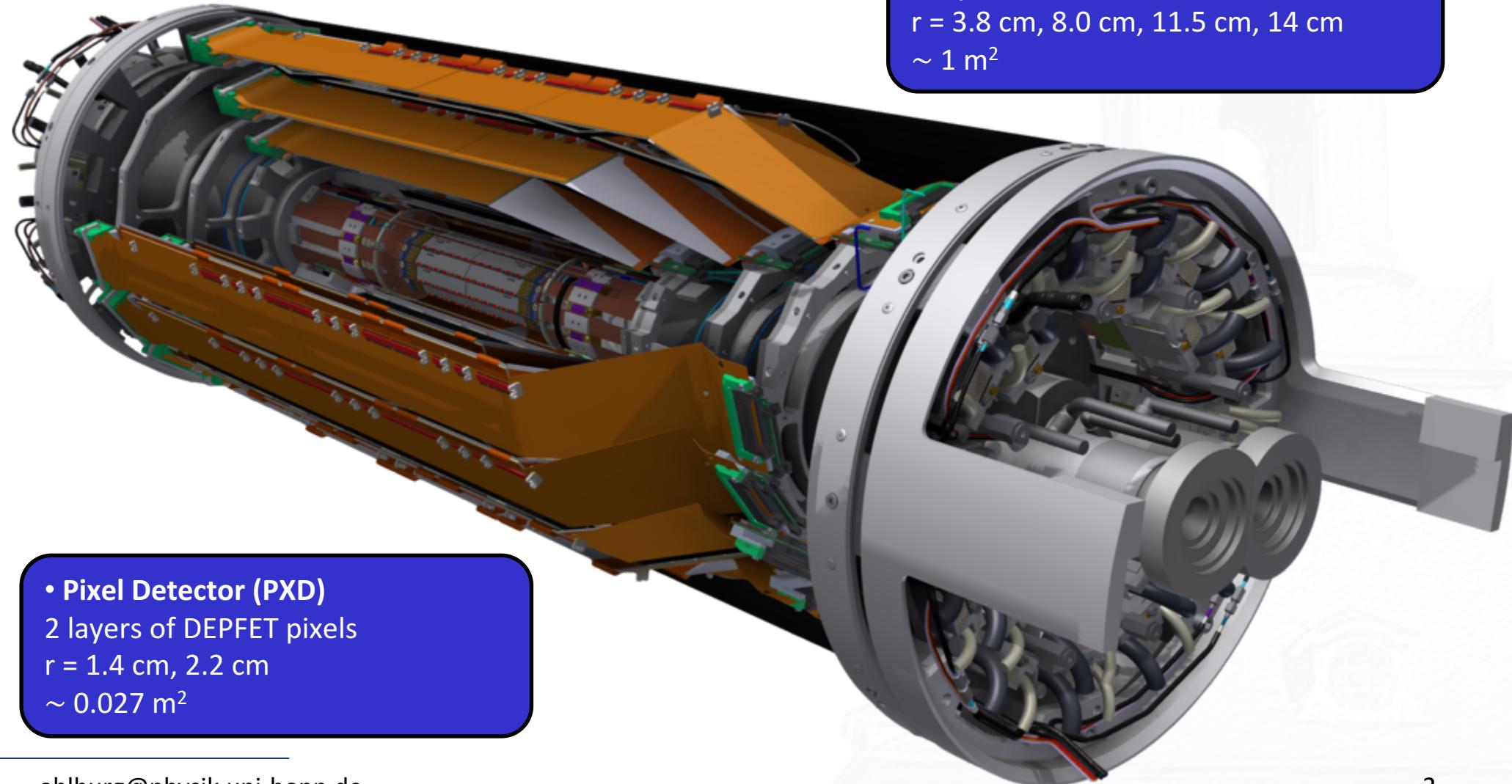
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on DEPFET Detectors and
Applications

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The Belle II Vertex Detector VXD (Phase 3)



- **Silicon Vertex Detector (SVD)**

- 4 layers of DSSD

- $r = 3.8 \text{ cm}, 8.0 \text{ cm}, 11.5 \text{ cm}, 14 \text{ cm}$

- $\sim 1 \text{ m}^2$

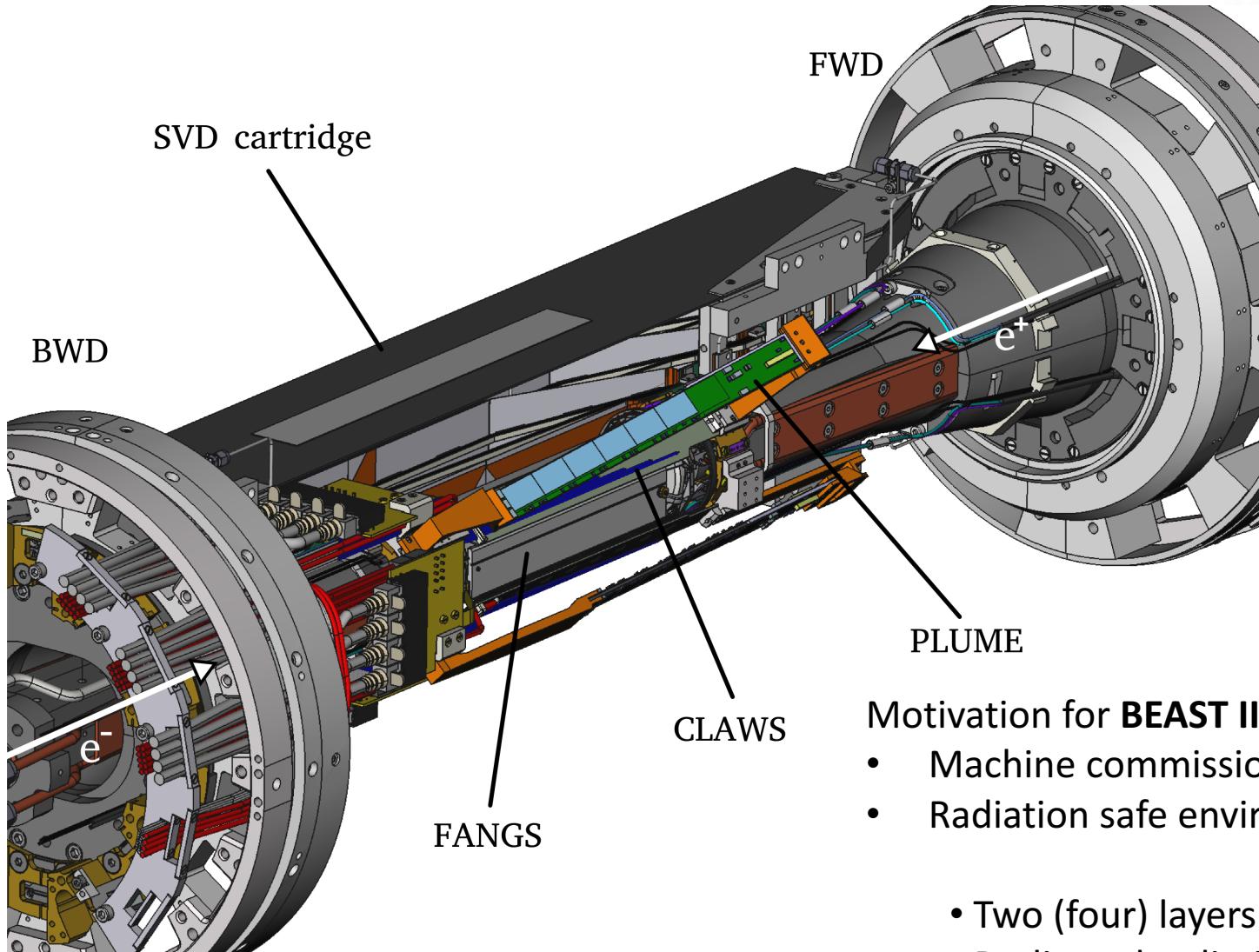
- **Pixel Detector (PXD)**

- 2 layers of DEPFET pixels

- $r = 1.4 \text{ cm}, 2.2 \text{ cm}$

- $\sim 0.027 \text{ m}^2$

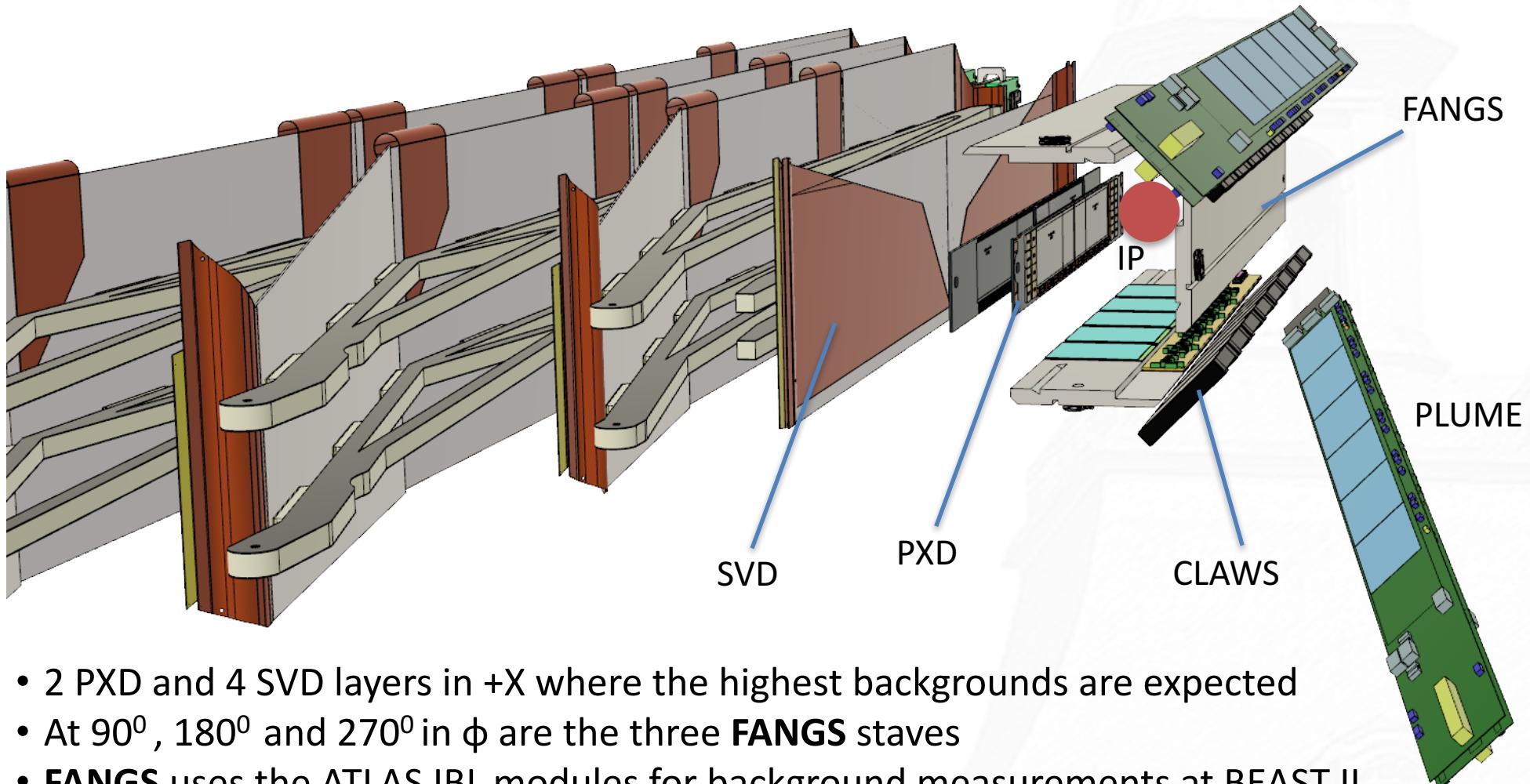
The BEAST II experiment (Phase 2)



Motivation for BEAST II:

- Machine commissioning
- Radiation safe environment for the VXD:
 - Two (four) layers PXD (SVD)
 - Dedicated radiation monitors
FANGS, CLAWS (Hendrik), PLUME

The BEAST II experiment (Phase 2)



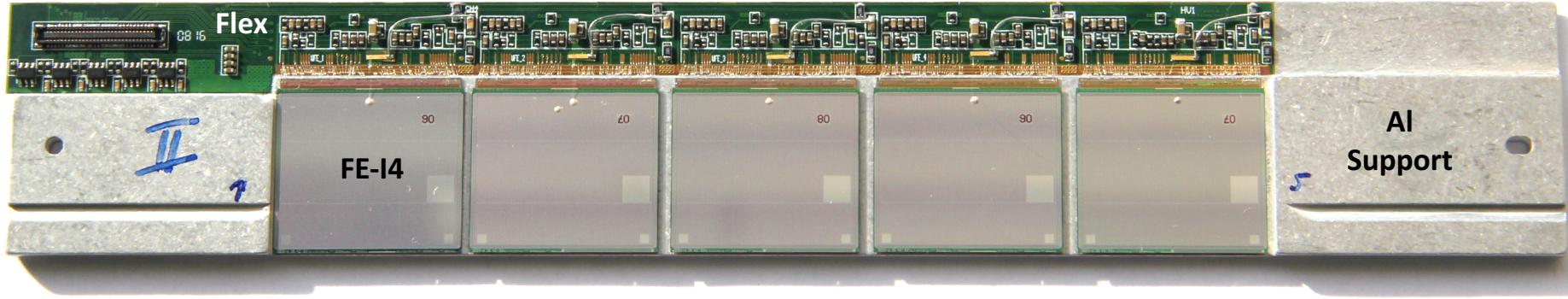
- 2 PXD and 4 SVD layers in +X where the highest backgrounds are expected
- At 90° , 180° and 270° in ϕ are the three **FANGS** staves
- **FANGS** uses the ATLAS IBL modules for background measurements at BEAST II



FANGS detector system

FANGS in the PERSY setup



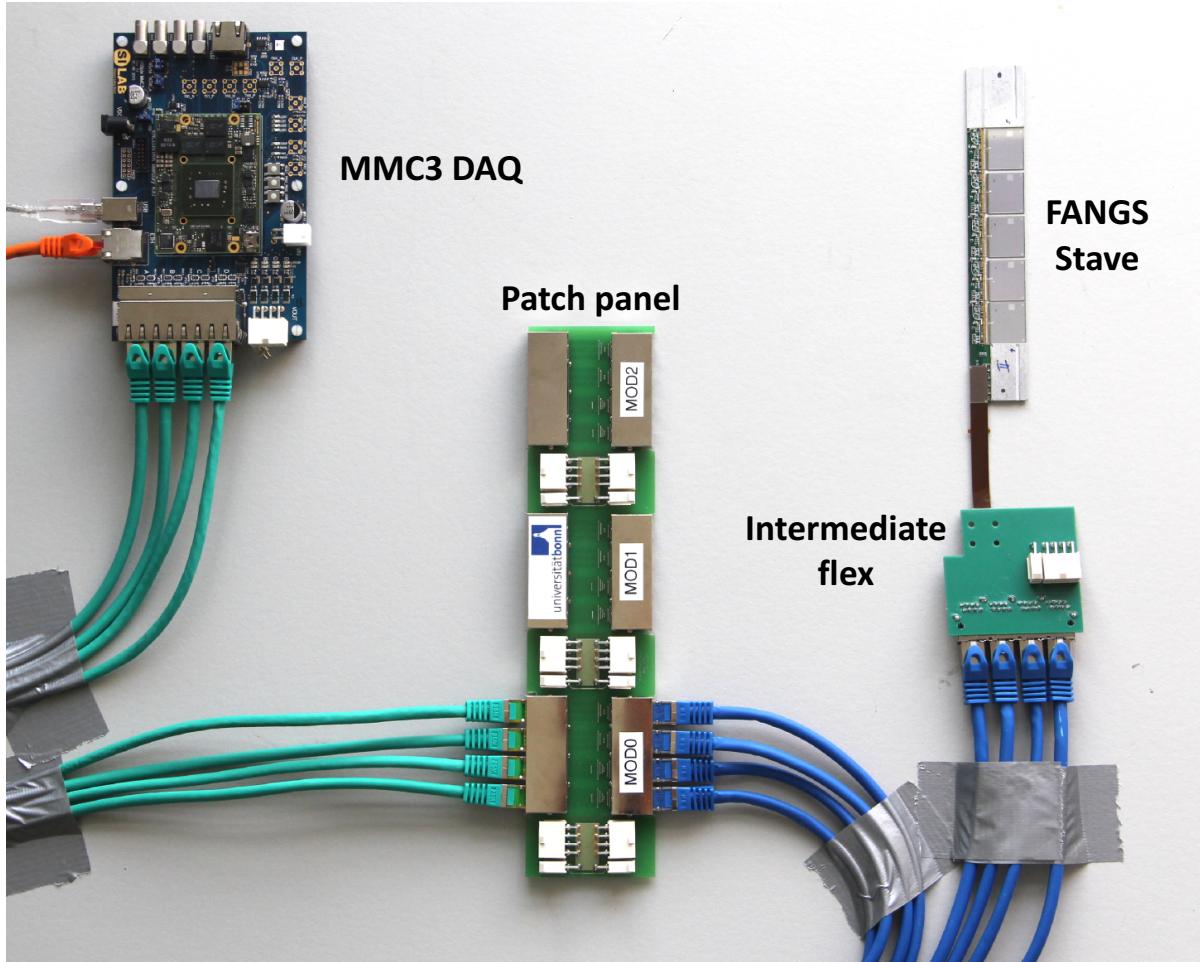


The stave is the basic unit of the FANGS detector

- ATLAS IBL pixel detector modules (FE-I4)
- Flexible circuit board (flex)
- Aluminium support structure

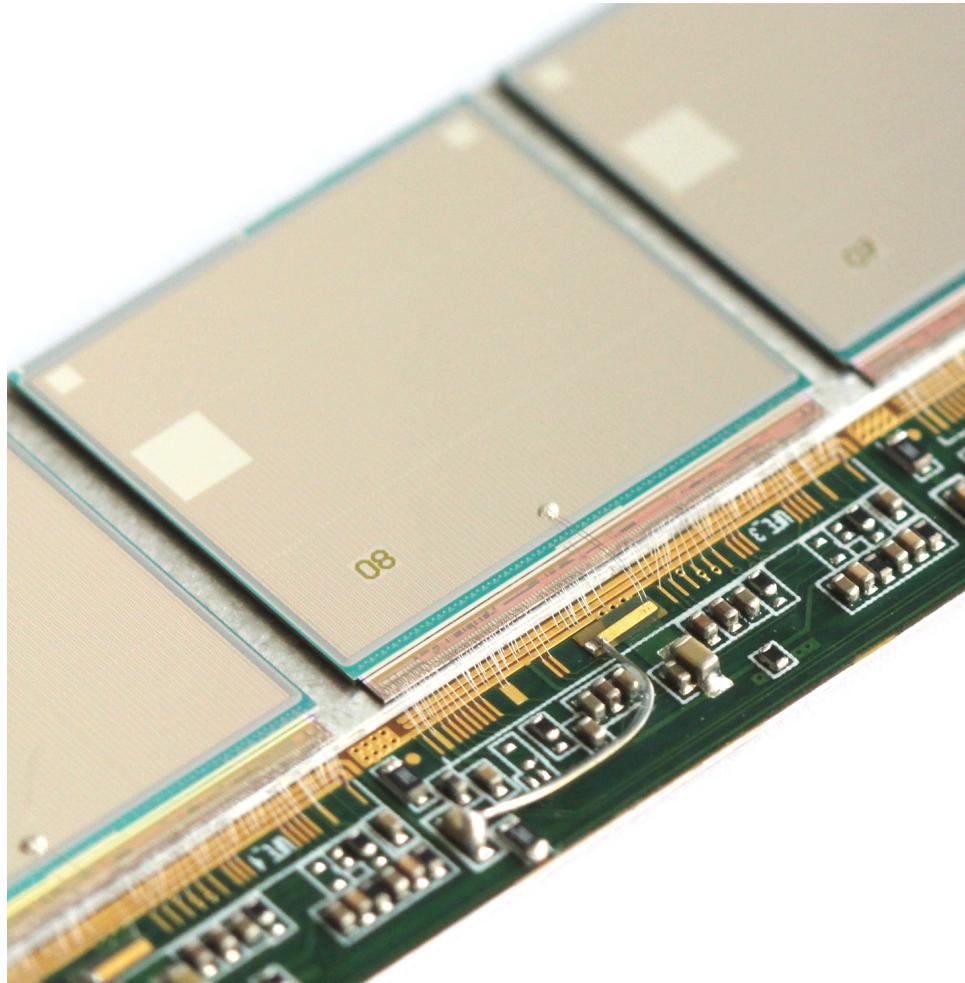
80

Lab test set-up: Final services configuration



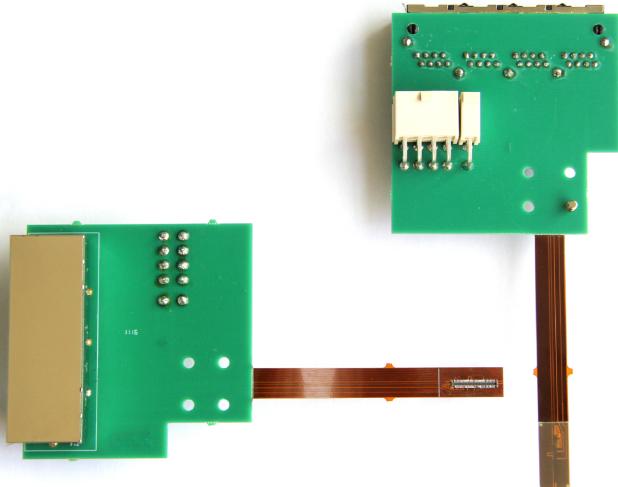
- Intermediate flex serves as interface between the stave and back-end electronics
- Signals routed to a patch panel (3m)
- Routed to MMC3 board (25m):
 - Houses the FPGA
 - Configuration and data acquisition for multiple FE-I4 in parallel
- Connection to the PC via ethernet

Production of the staves



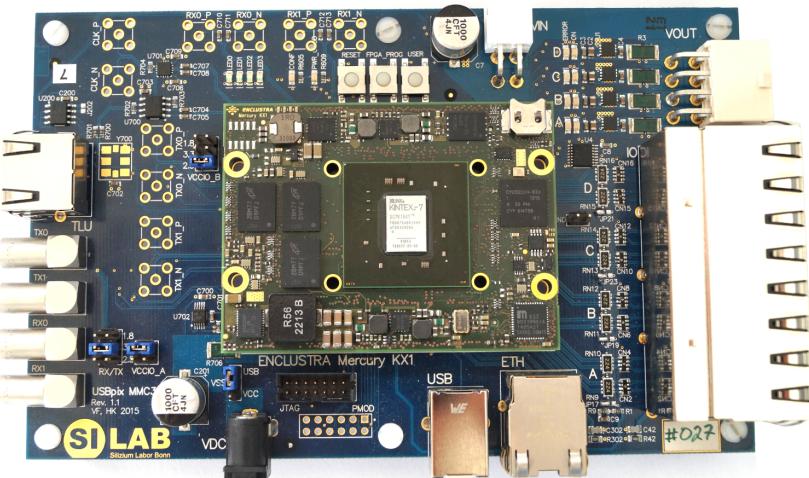
- Two staves are fully tested and characterized
- One stave is tested at the moment
- Two additional staves will be produced

Intermediate and MMC3 board



- Intermediate flex:

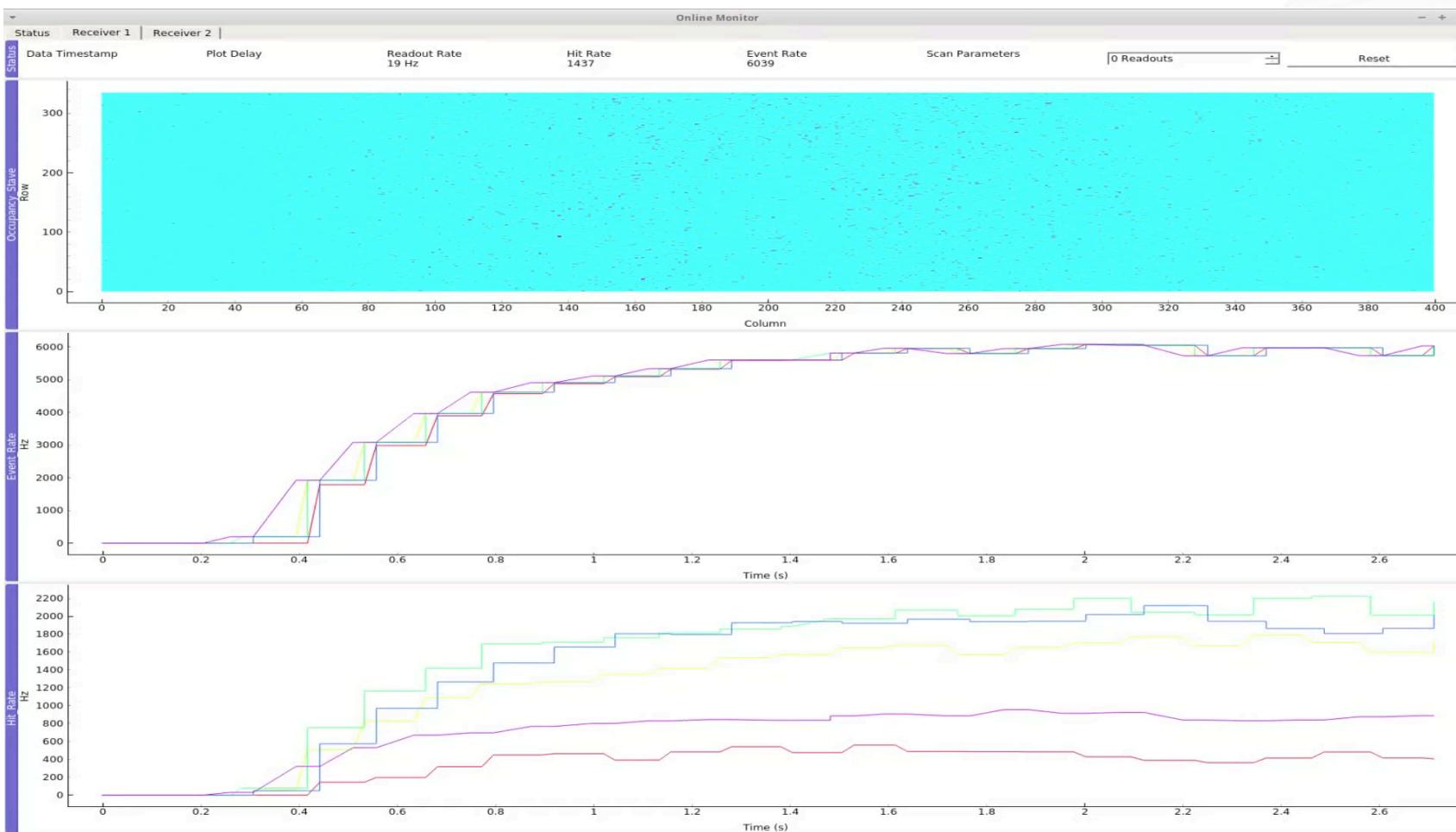
- One Intermediate per stave
- 3 produced and tested (2 more in production)



- Data acquisition - MMC3 board

- One MMC3 board per stave
- 2 produced and tested (FPGA boards are ordered)

Online monitor (receiver 1)



Hit maps

Event rate

Hit rate

Online monitor (receiver 2)

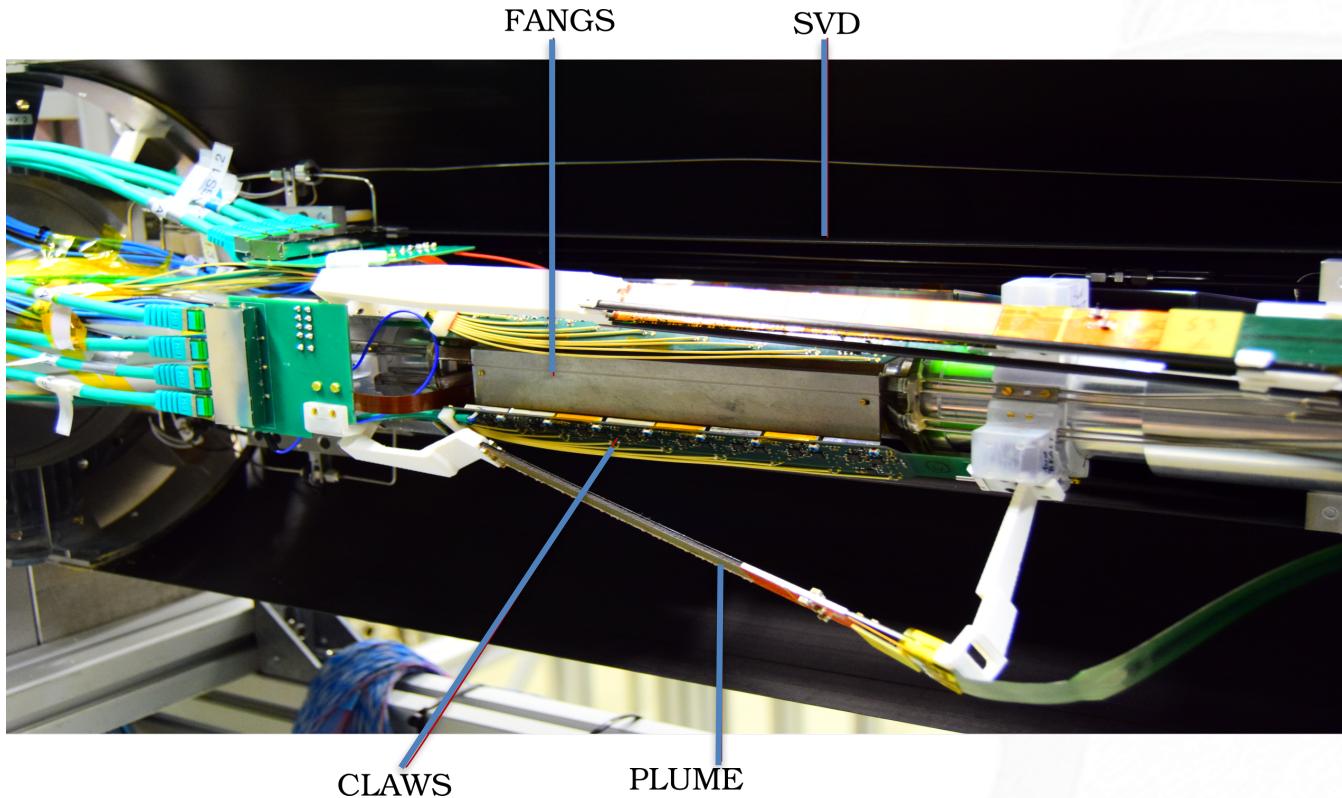
TDC

ToT



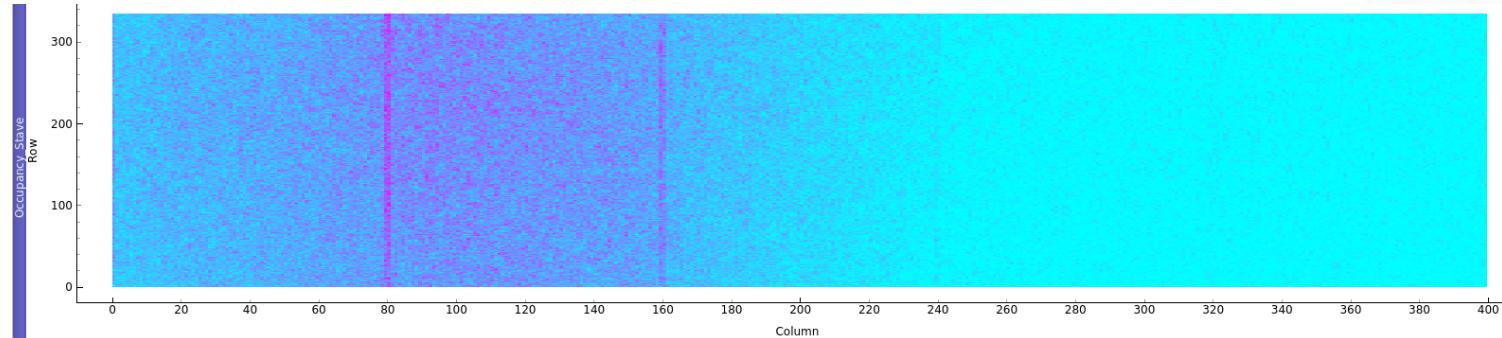
FANGS detector system FANGS in the PERSY setup



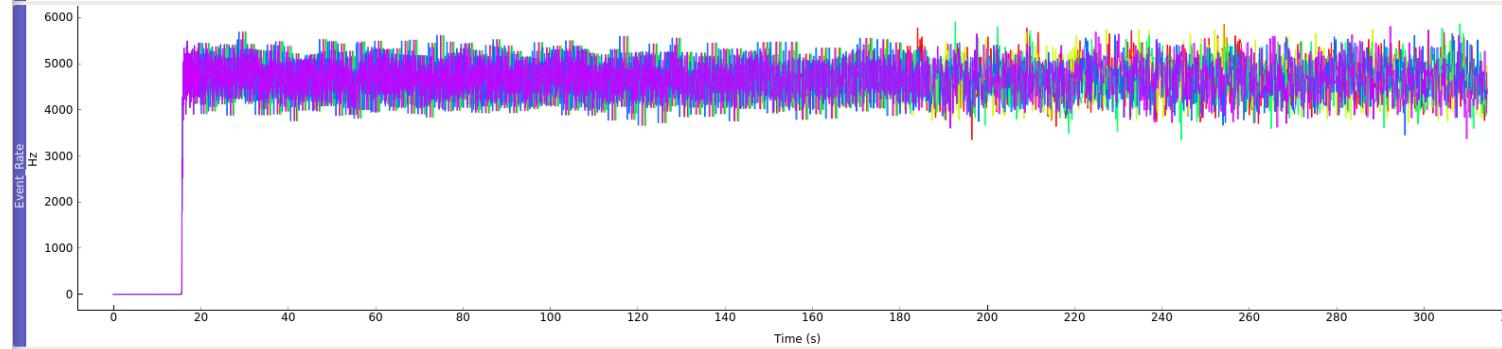


- System integration campaign carried out in December 2016 with all the five sub-detector systems and final configurations
- Integration and combined operation of all sub-detectors for the first time
Works!

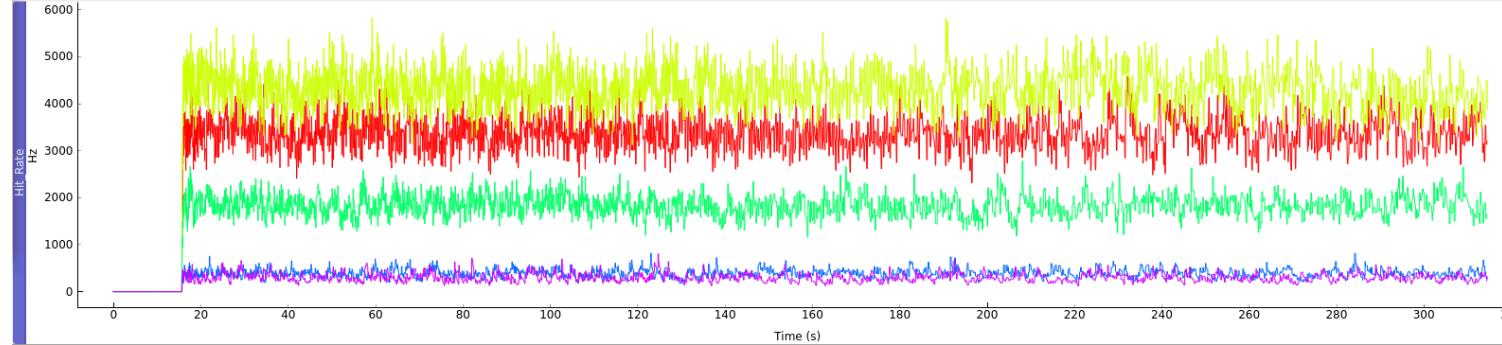
Online monitor (receiver 1)



Hit maps

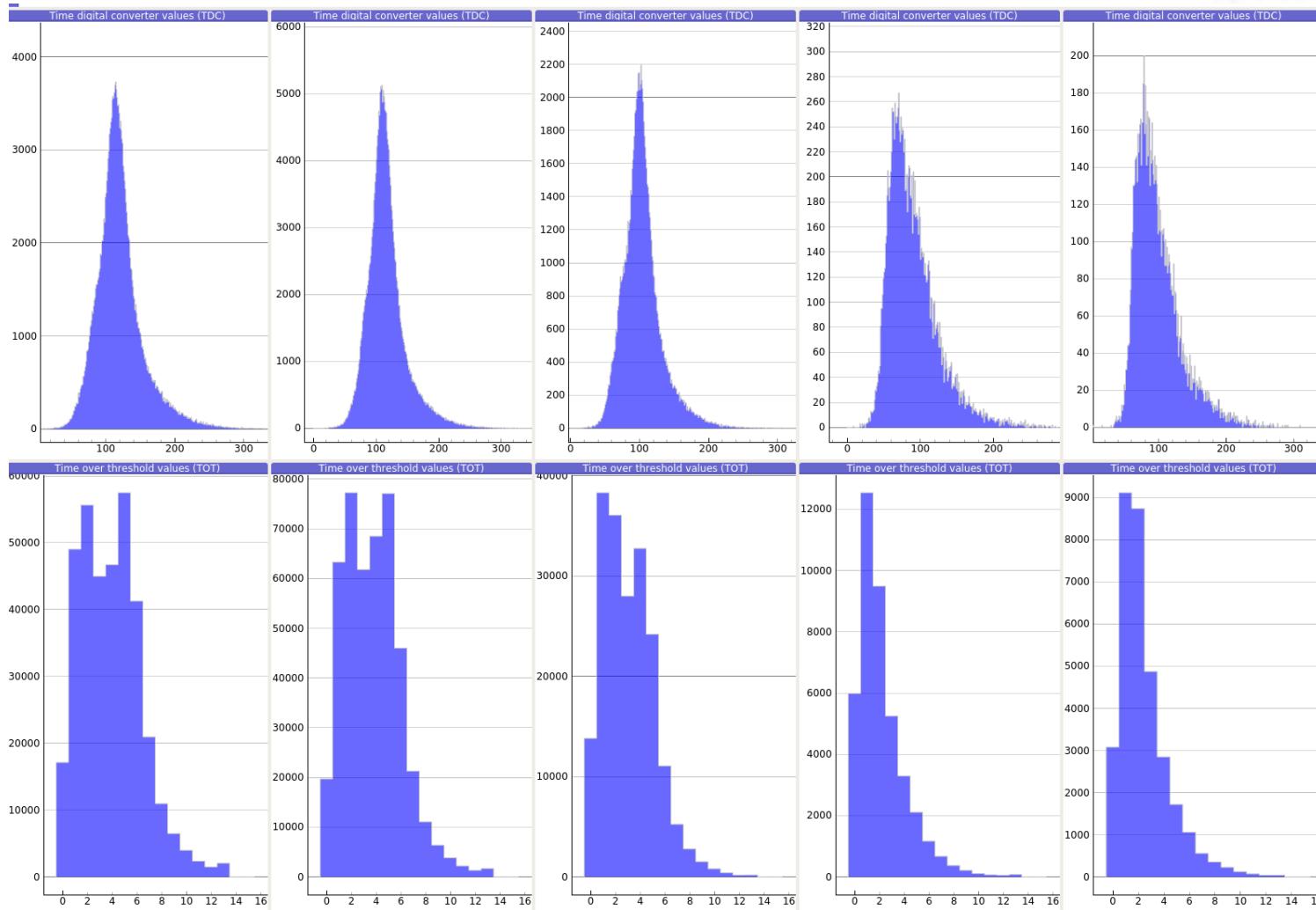


Event rate

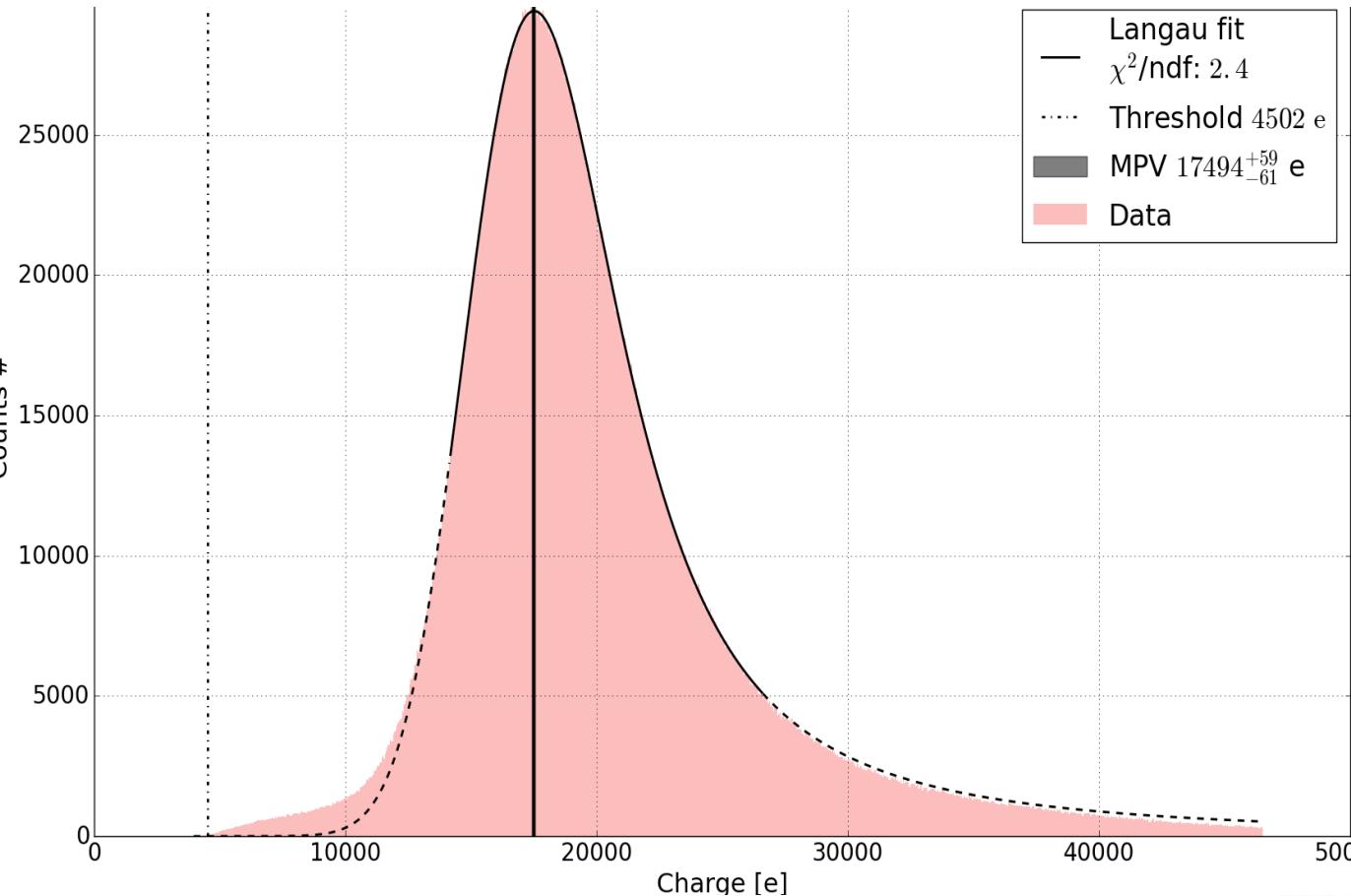


Hit rate

Online monitor (receiver 2)



Test beam analysis



- Beam energy: 2.2 GeV
- Expected MPV for 250 μm silicon sensor: **18 ke**
- Measured MPV: **17.5 ke**

- BEAST II experiment to help in SuperKEKB machine commissioning and ensure background safe conditions for VXD installation

FANGS

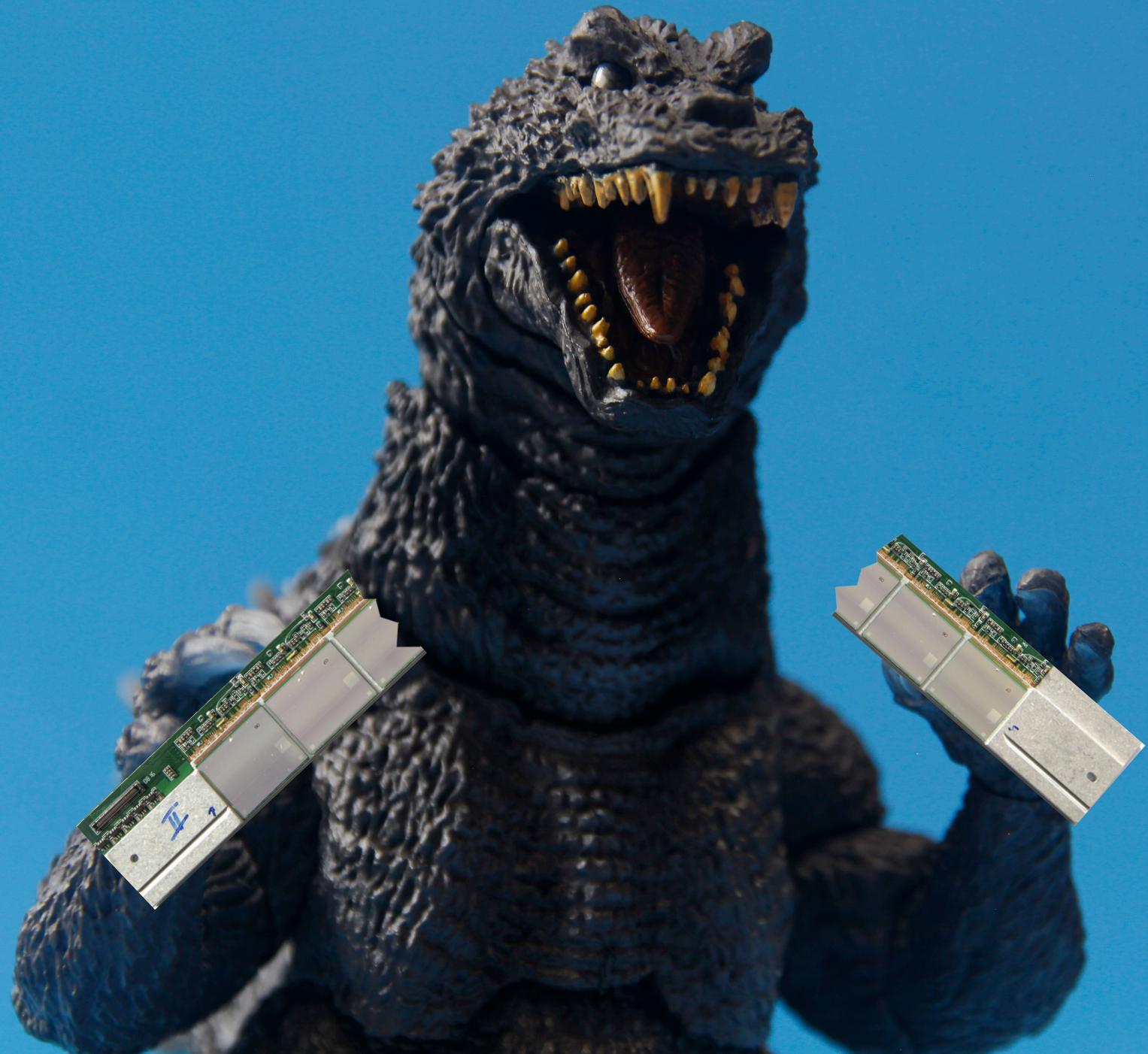
- Design prove of principle demonstrated
- 2 FANGS staves fully tested with final components. Production ready (5 staves)
- Radiation hardness of the flex components (LVDS driver) was tested
- Pre-integration campaign with CO₂ and PXD SCBs

Outlook

- Simultaneous use of 3 staves
- Trigger? Grounding?.. Some things still to do
- Final integration of the detector in the BEAST II experiment (Installation ~3 days)



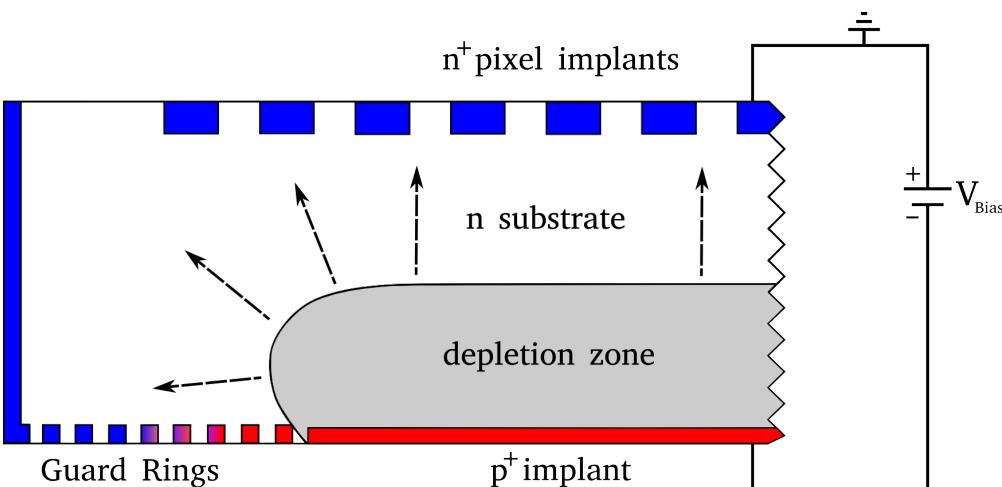
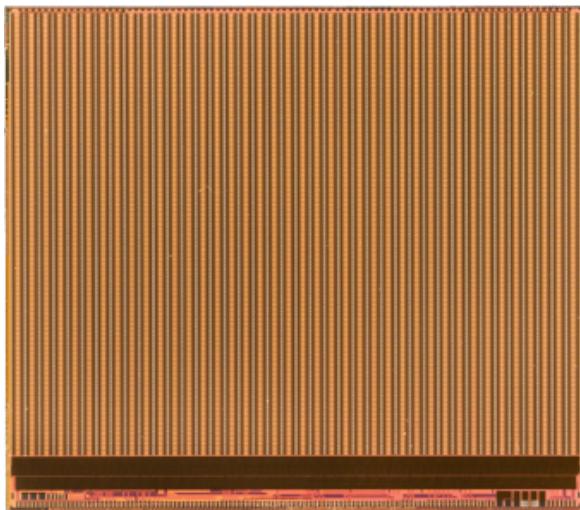
Thank you





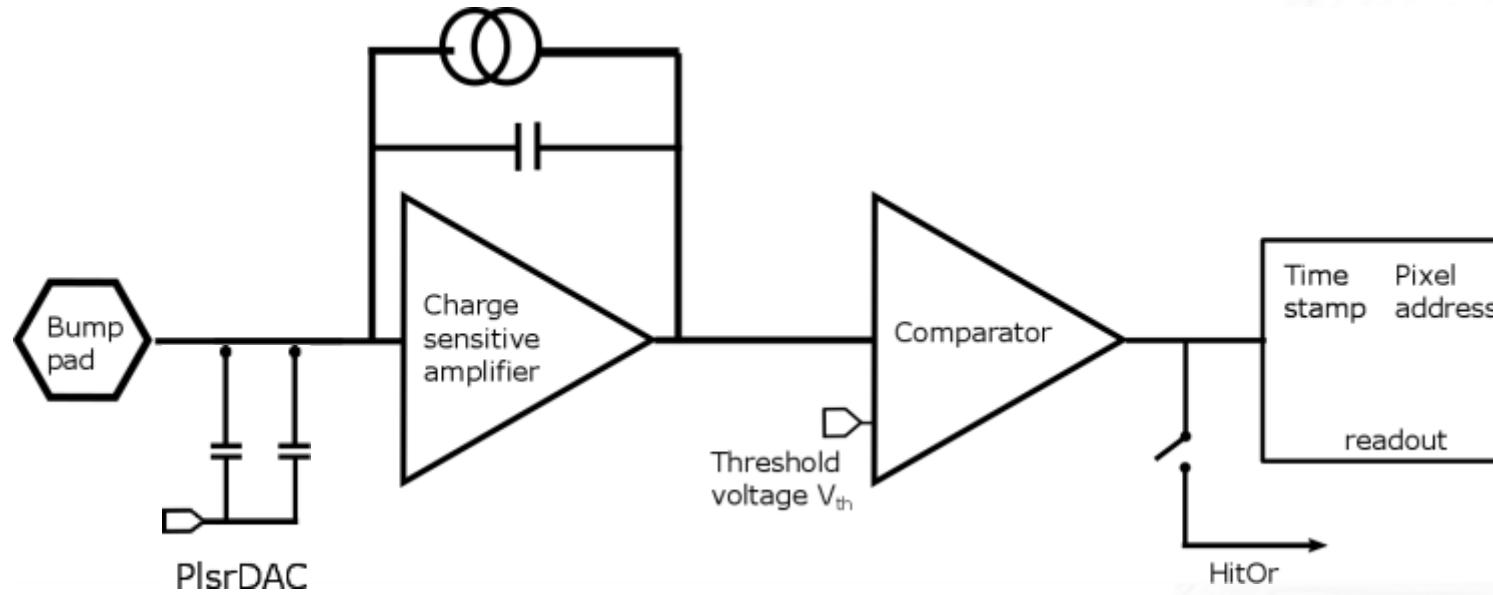
Backup



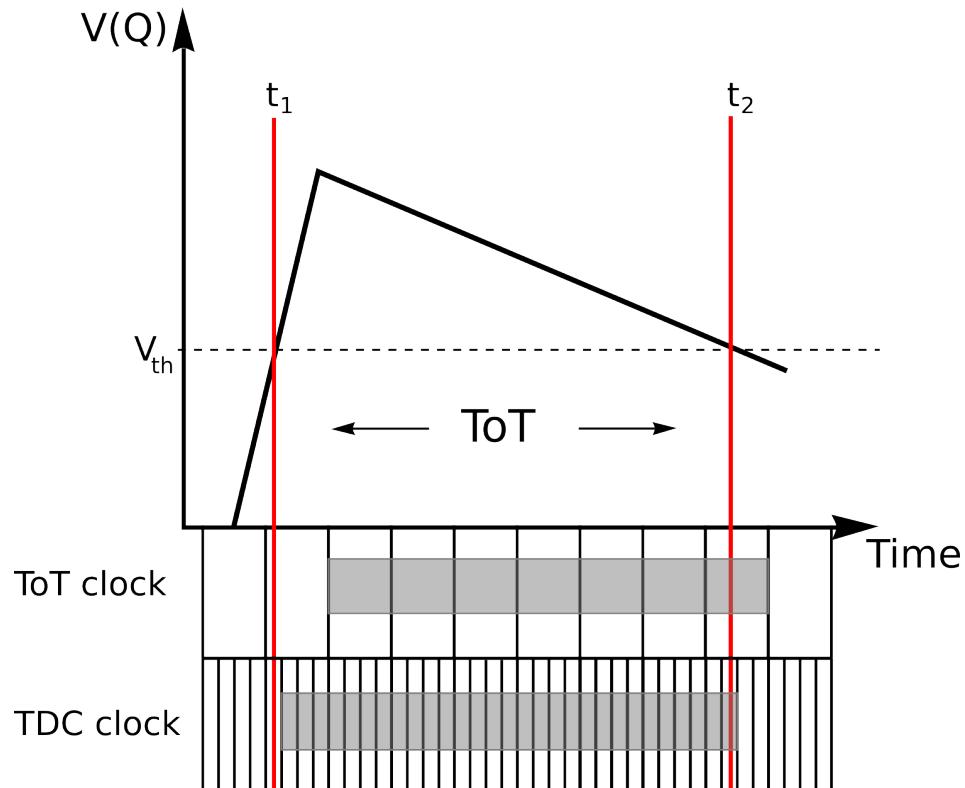


Hybrid pixel detector:

- FE-I4 read out chip:
Up to a hit rate of **400 MHz/cm²**
Radiation tolerance of **300 Mrad**
Read out for 80x336 pixels
Thickness = 150 μm
Physical size = 21x19 mm²
- Silicon sensor:
n-in-n planar
Thickness = 250 μm
Bias voltage V = 100V
Power = 1.2 W
- Solder balls for interconnection



- Charge sensitive amplifier → Discriminator with adjustable threshold.
- Time over threshold (**ToT**) with 40 MHz clock.
- Output of each pixel is Ored: HitOr
 - Time stamped with external FPGA 640 MHz clock (**TDC**)
- Internal charge injection for tuning and calibration in units of PlsrDAC

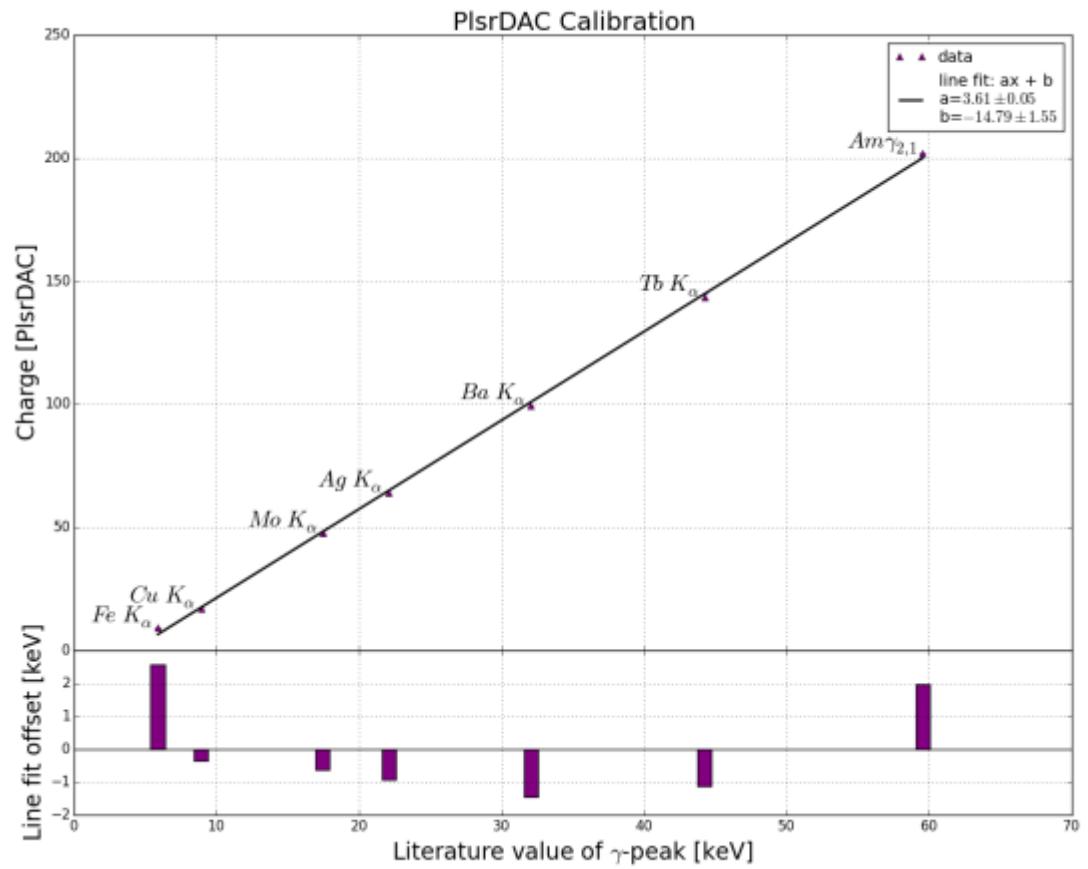
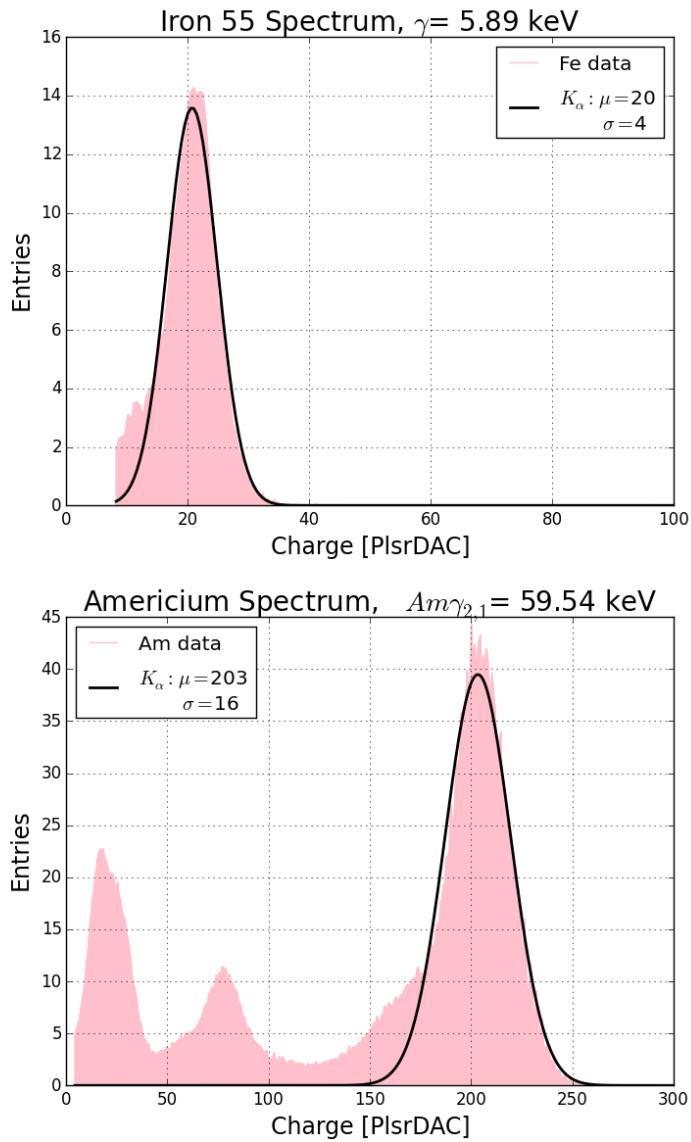


Two independent measurements simultaneously:

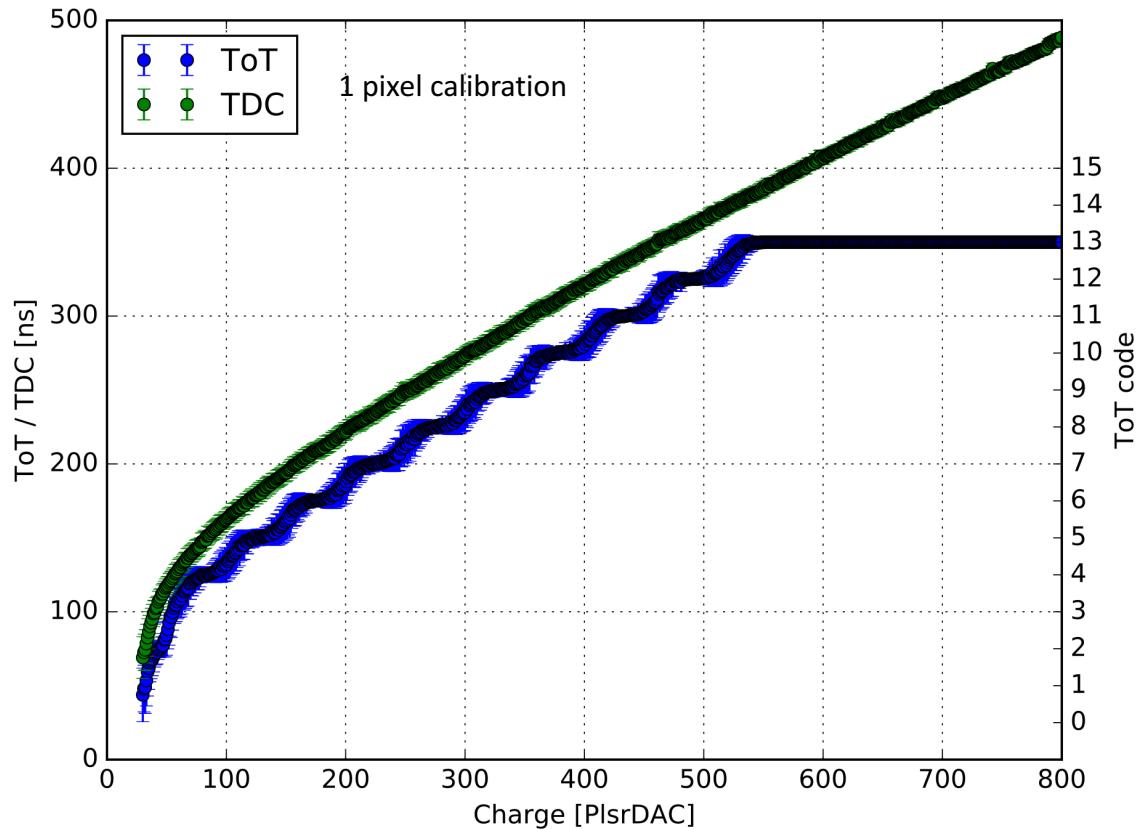
- A. **ToT** 40 MHz clock: 4 bit resolution
 - Contains pixel and timing information

 - B. **TDC** with external FPGA's 640 MHz clock: 12 bit resolution
 - Voltage signal of comparator output with the highest charge
- TDC improves energy resolution
➤ ToT needed for position information

Calibration and Dynamic Range

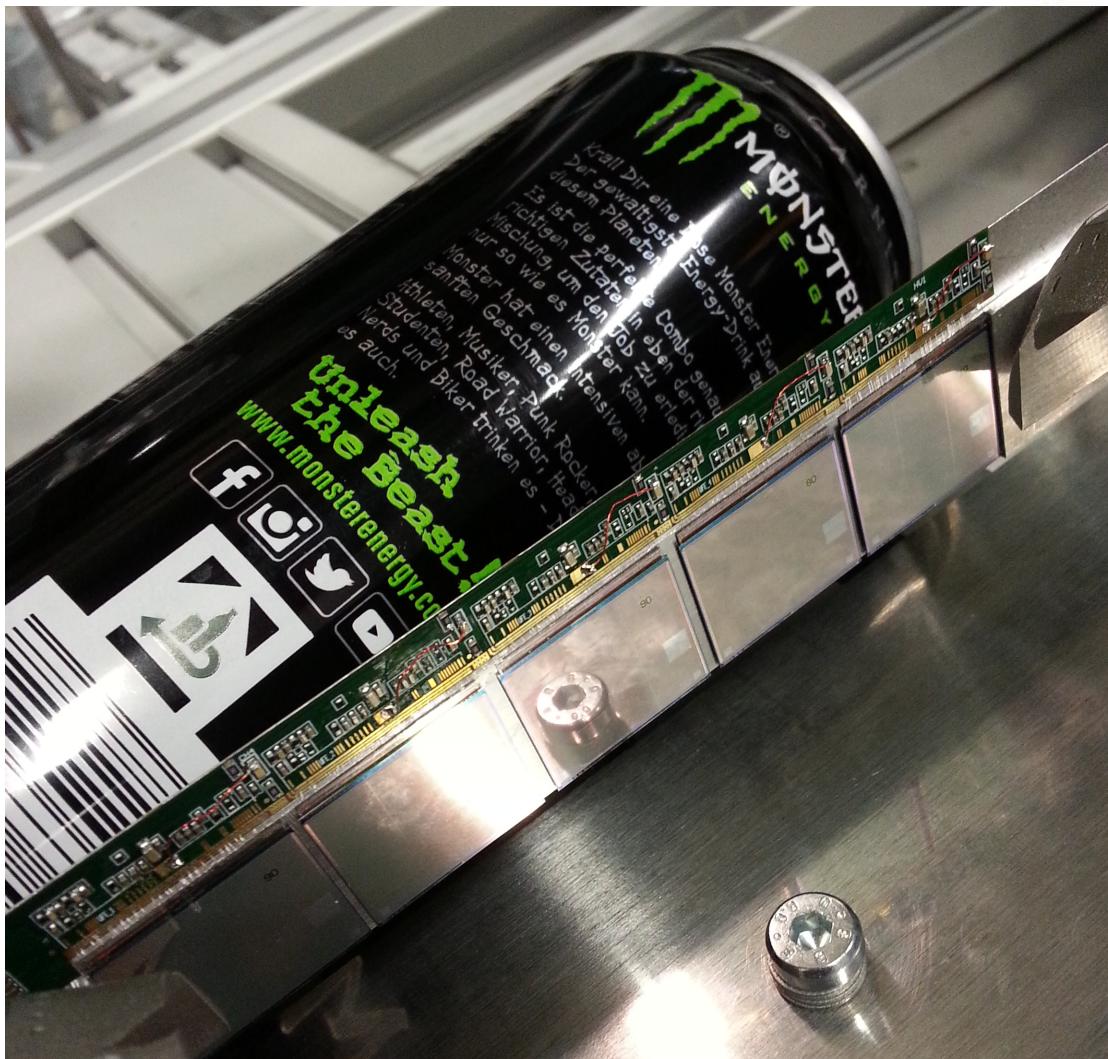


- Dynamic range 10-60 keV

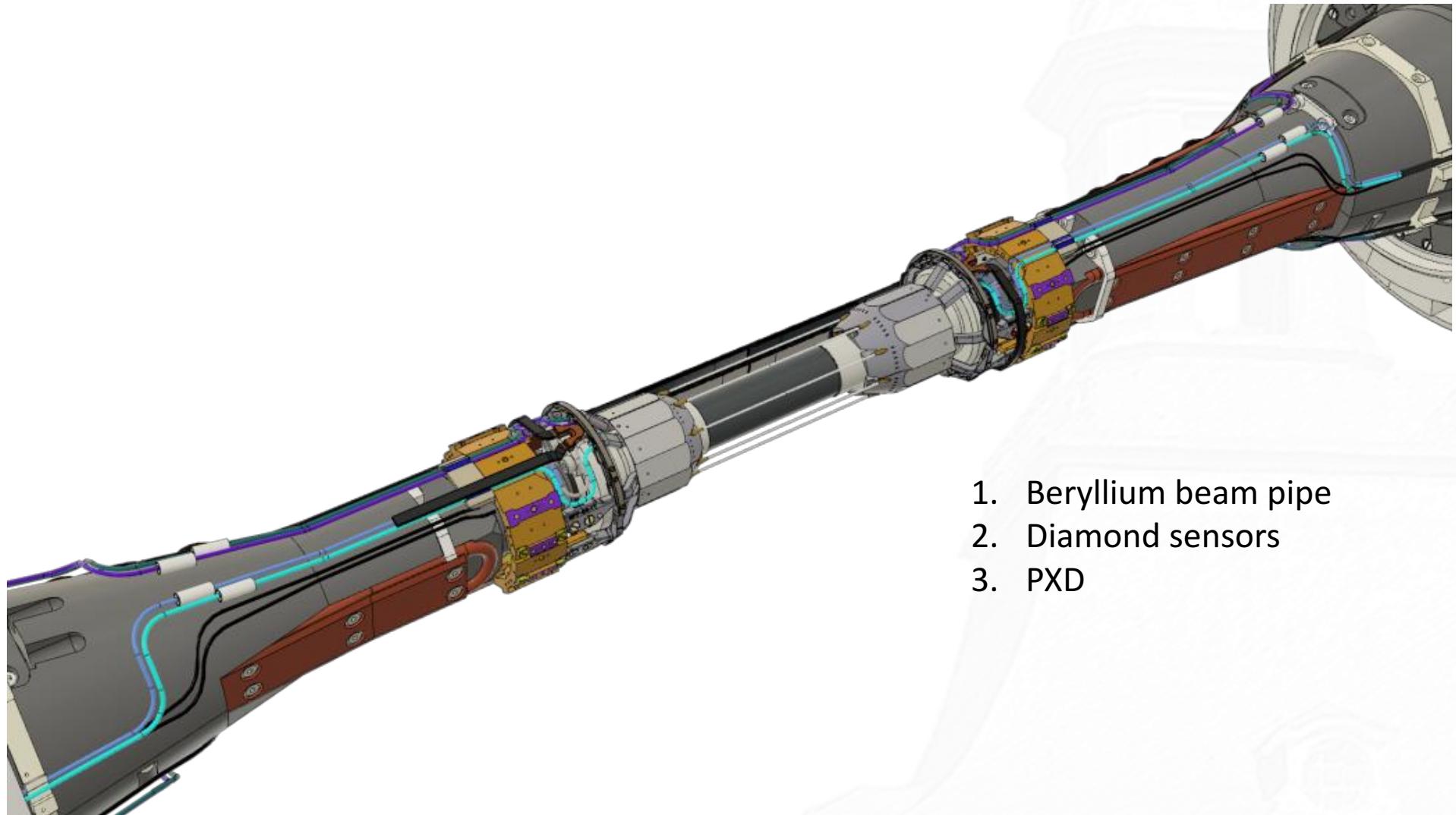


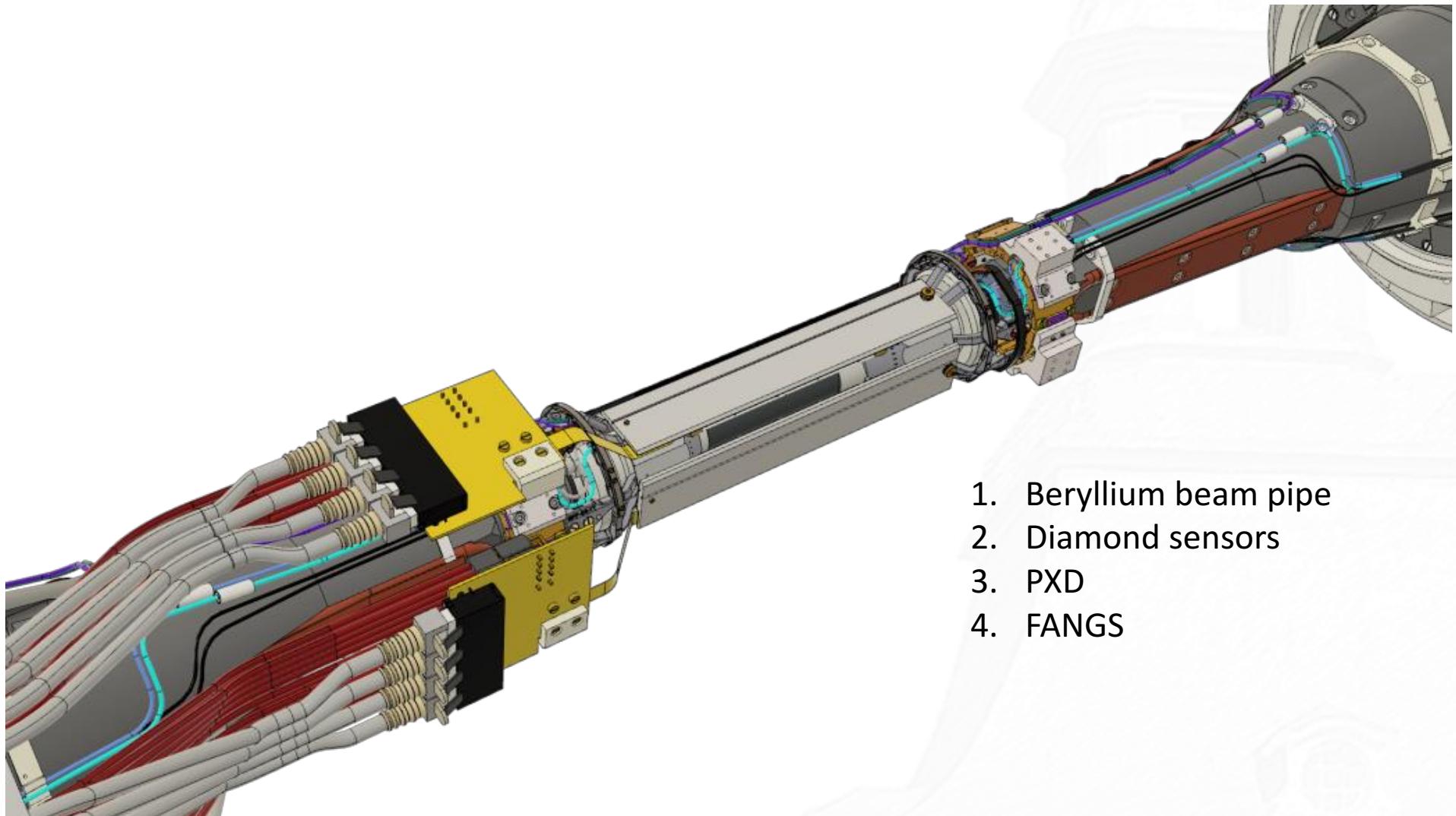
- ToT and TDC values response to increased injection charges
- Per pixel charge calibration to increase charge resolution
- Reference table for each pixel converting charge to ToT and TDC
- TDC method expands the measureable energy range

Integration of the stave



Mounting sequences





1. Beryllium beam pipe
2. Diamond sensors
3. PXD
4. FANGS