ONSEN Lab Tests and Development

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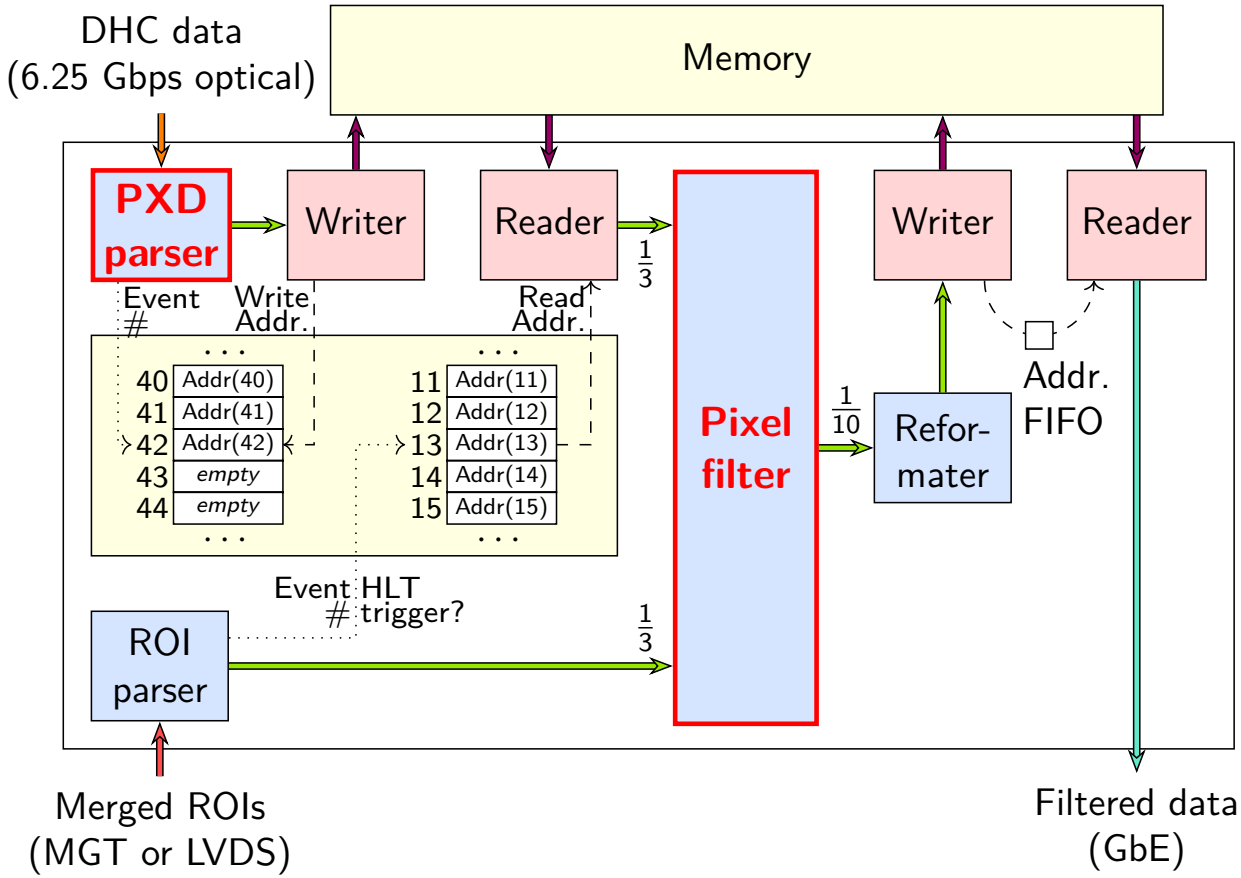
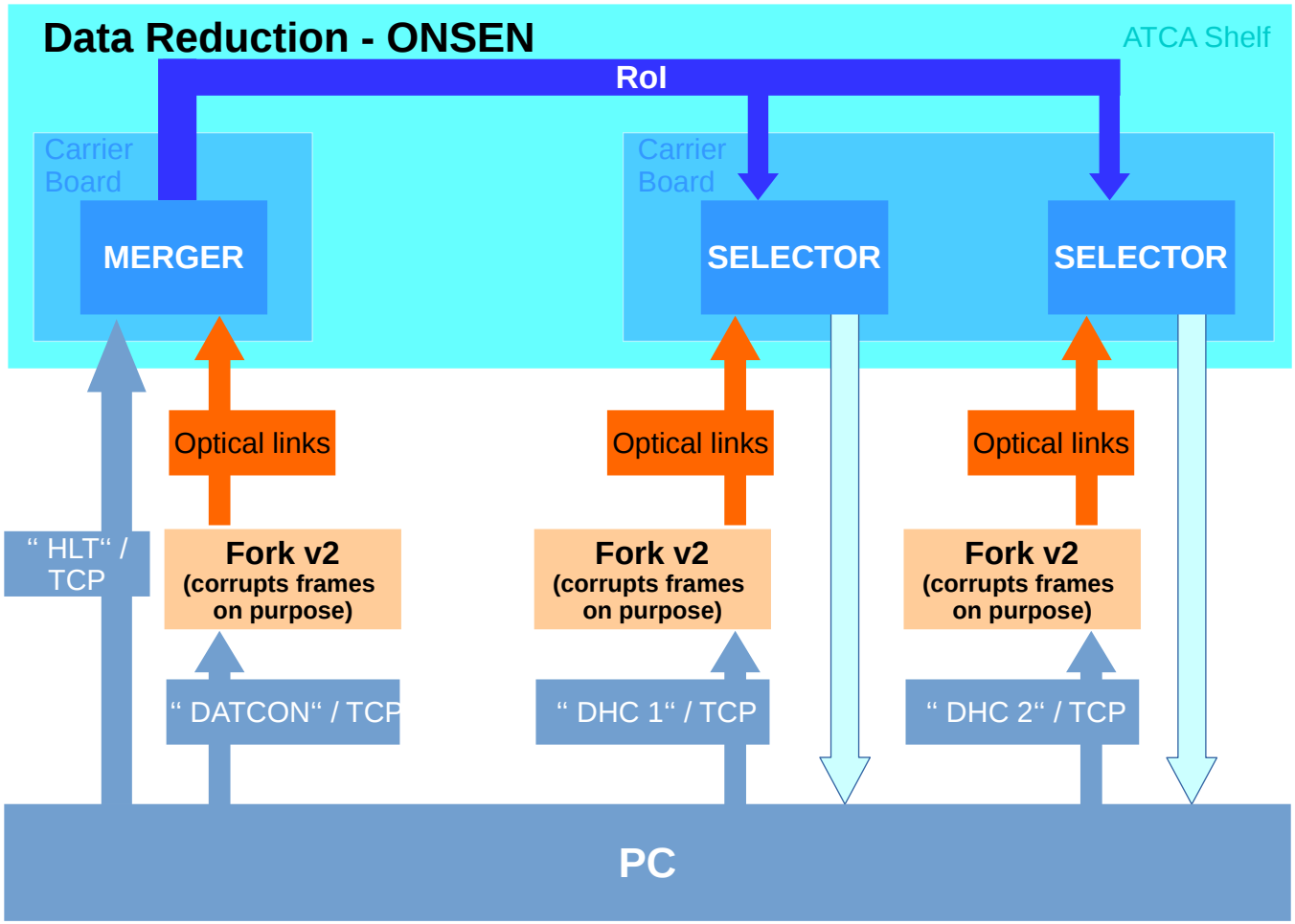
Debugging of Data Corruption

Selector Data Flow: "ONSEN Trigger Mismatch" Sources



- **PXD parser:** Sensitive to event/framing errors in PXD data → Internal event synchronization goes out of sync
- **Pixel filter:** Produces framing errors if inputs out of sync; state machine reset not properly implemented → **Cold start** necessary

Test Setup in Gießen



Problematic Conditions

Invalid CRC in HLT frame	Fragmented first DHH data (cut in middle of ZSD)	Double DHC Start frame at the beginning of run
ONSEN Merger discarded this data but also the beginning of the next (valid) HLT frame	Internal buffer management did not end the event properly	Additional / faulty DHC Start was not discarded properly in ONSEN
ONSEN Merger blocked any incoming HLT data after invalid CRC	Resulted in "**event fusion**" of the first DHH data (DHE data of second event started in ZSD of first event)	Lead to **event mismatch** but also to internal backpressure (Selector AMC)
	Corrupted "only" two events	Softreset needed for getting rid of backpressure but event mismatch was still occuring
Coldstart needed	No coldstart needed	Coldstart needed

ONSEN firmware update: these three conditions don't cause trouble anymore

ONSEN Emulator

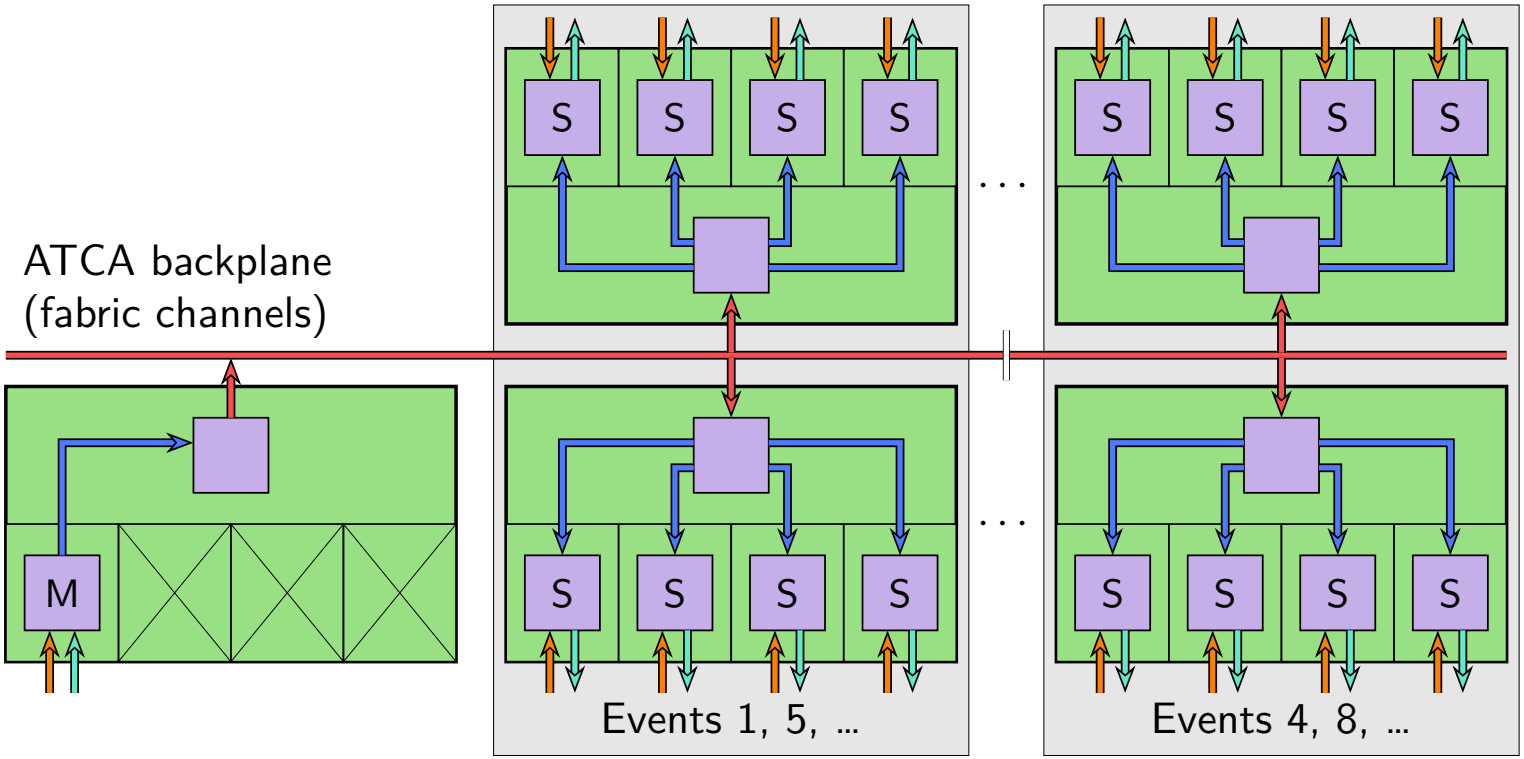
- C++-Program by S. Reiter, **PXD data reduction in software**
- Loads **test data from file** (PXD/HLT/DATCON) (requires 0xBE12DA7A header)
- Similar **memory management** as ONSEN
- **Processing time** example
  1000 events, 40 % PXD occupancy = 780 MB pixel data:
  - **ONSEN:** $<$ 2 seconds after sending HLT (1 Selector node)
  - **Emulator:** (Intel i7 @ 3.4 GHz, 16 GB RAM):
    - 11 min, 50 sec with 1 thread
    - 2 min, 40 sec with 8 threads

Test Results and Progress

- Several **framing and event error** cases were reproduced with test data, identified, and **fixed**
- Verified by testing with corrupt test data
  $\rightarrow$ patched PXD parser correctly **sanitizes PXD input**
- Correct ONSEN data processing verified with software emulator
- Next steps:
  - Replace with **rewritten PXD parser**
    $\rightarrow$ increases robustness and adds better error analysis
  - Do the same thing for **DATCON parser**
  - Revise **Pixel filter** input state-machine, fix reset

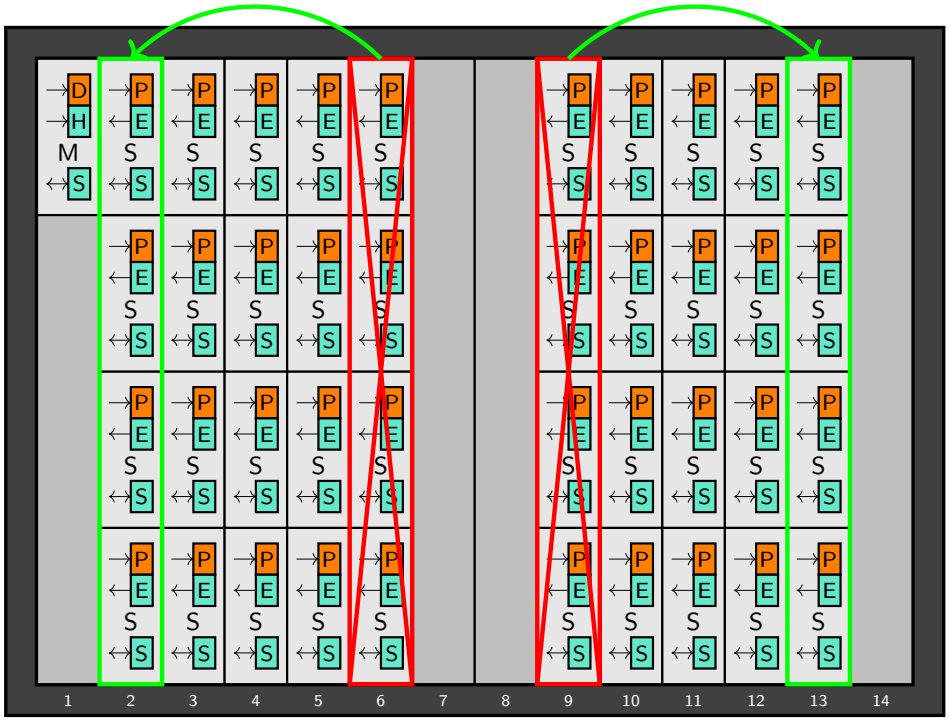
Debugging of ONSEN Internal Links

ONSEN Internal Links (for ROI Forwarding)



- ⟶ 4×600 Mbps LVDS Carrier-AMC links
- ⟶ 3.125 Gbps MGT ATCA Backplane links

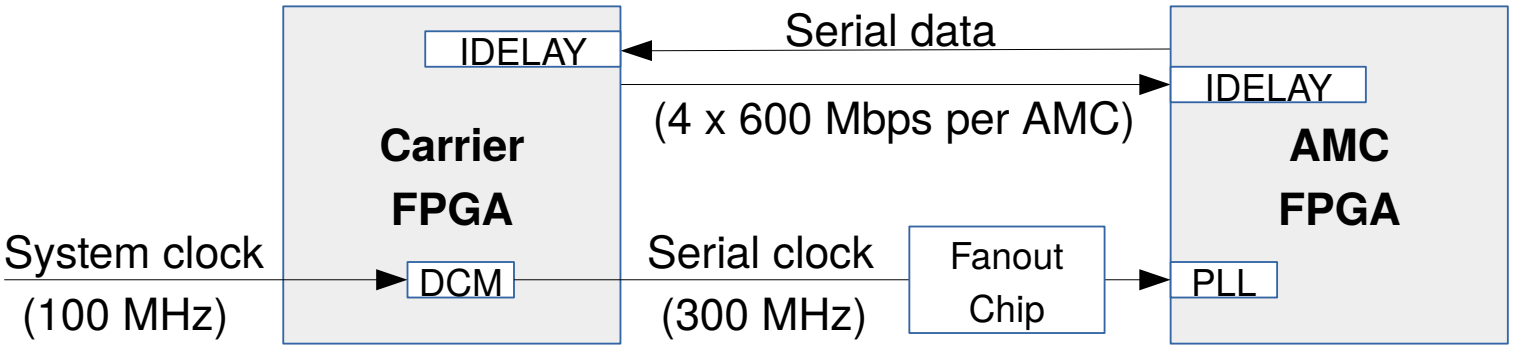
MGT-Links on ATCA Backplane



- For Belle II, ONSEN will be scaled **from 2 to 9** ATCA boards
- First scaling tests showed troubling results: With "Merger" firmware sending **to multiple boards**, *all* backplane links become **unstable**
- Debugged in detail by S. Reiter in Gießen

- Problem: **Crosstalk** between Ethernet IO and one MGT power supply
- Solved by avoiding that link $\rightarrow$ **use different ATCA slots**
- Additionally, **Aurora reset logic** had to be revised

LVDS-Links Between Carrier and AMCs



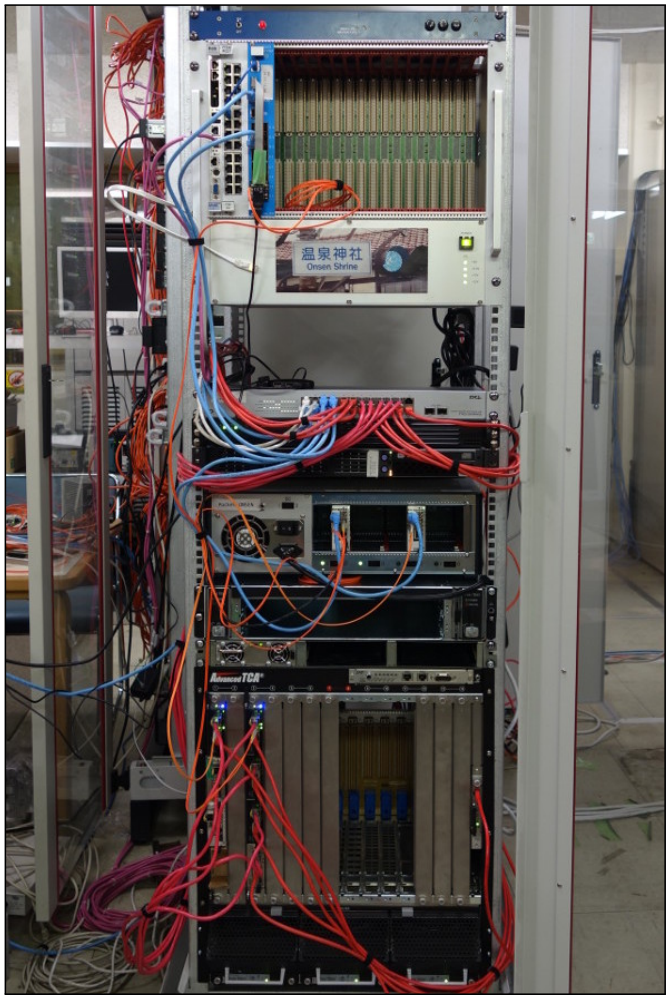
- Connection Carrier FPGA AMC FPGA uses serial (LVDS) links
- Serial clock is distributed from Carrier to AMCs
- Clock/data phase shift is compensated by **delay**, determined by **tuning**
- Problem 1: Strong delay difference **between Carrier/AMC combinations**
- Problem 2: Small **temperature drift** of the delay
- **Solved** by implementation of online self-calibration mechanism

Link Tests After Fixes

- Forward HLT packets from
  - 1 Merger in
  - 1 Merger-Carrier to
  - 4 Selector-Carriers with
  - 2 Selectors each
- Selector output **recorded and verified** (i.e., compared to expected output from emulator)
- 60-hour test with low rate ($\sim$10 Hz): **no link or data errors**
- 30-minute test 2 kHz: **no link or data errors**
- Short test with 30 kHz and DATCON data: **no link or data errors**
- Next: **Full-scale test** (8 Selector-Carriers) when all boards return from PERSY and repair at IHEP

Phase 2 Readiness

ONSEN (Phase 2) Shelf in Tsukuba B3: Damage



- Chassis of the ONSEN Prototype ATCA Shelf (planned for Phase 2 ONSEN) was damaged/warped during shipment to KEK

ONSEN 19-Inch Rack in E-Hut

- The 19-inch racks foreseen for ONSEN in the E-hut don't have enough clearance to accept the deformed shelf

ONSEN Phase 2 Preparation: Outlook

- KEK ONSEN shelf **must be replaced**
  - Buy a new shelf or
  - Send replacement from Gießen (2-slot shelf with RTM-slots sufficient)
- DAQ group offered to buy a shelf for R&D and lend it to ONSEN during Phase 2 $\rightarrow$ will be discussed at B2GM
- Two ONSEN experts will be at KEK for one month from September, more from January 2018
- Support for Onsen team at KEK during phase 2 and VXD vosmic data taking provided by JENNIFER

Compute Node Upgrade for PANDA (Design and Production by the IHEP Beijing Trig Lab)

Compute Node Upgrade: Carrier Board

- **First stage:** upgrade CNCB (but remain compatible with current xFP)
- **FPGA:** Change to Xilinx UltraScale architecture

	Virtex-4 FX60 (CNCB)	Virtex-5 FX70T (xFP)	Kintex UltraScale 060 (Upgrade)
Registers	50k	44k	663k
LUTs	50k × 4-input	44k × 6-input	332k × 6-input
DSP Slices	128	128	2760
BRAM	4 Mb	5 Mb	38 Mb
MGT	16 × 6.5 Gbps	16 × 6.5 Gbps	32 × 16.3 Gbps
CPU	PPC405	PPC440	-

- **No more hard-core CPU** → Slow control on MicroBlaze or light-weight option like IPbus

Compute Node Upgrade: Carrier Board

- **RAM:** 2 GiB DDR2 SODIMM $\rightarrow$ 16 GiB DDR4 (8 chips)
- **Configuration:** Flash/CPLD (slave serial) $\rightarrow$ automatic from NOR Flash (master BPI)
- **GbE switch:** 4 AMCs, 1 switch FPGA, 1 uplink to ATCA Base Interface
- **16.3 Gbps MGTs**
  - 4 links to each AMC card (currently: 4 $\times$ 600 Mbps LVDS)
  - 14 links to ATCA backplane
  - 1 link to RTM (10G Ethernet)
- **Programmable MGT clock**
- **Keep:**
  - JTAG chain/AMC decoupling
  - I2C buses, sensors
  - IPMC connector

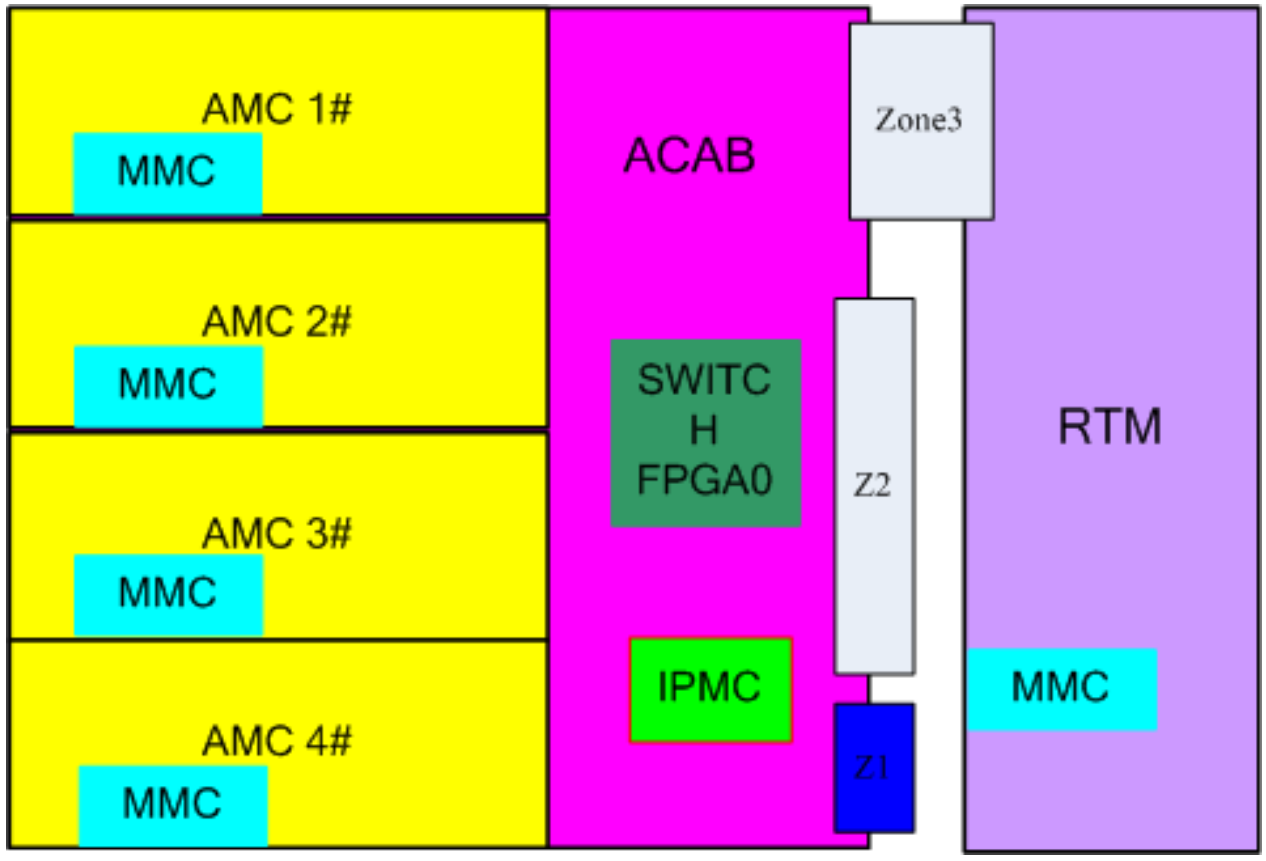
Compute Node Upgrade: Rear-Transition Module (RTM)

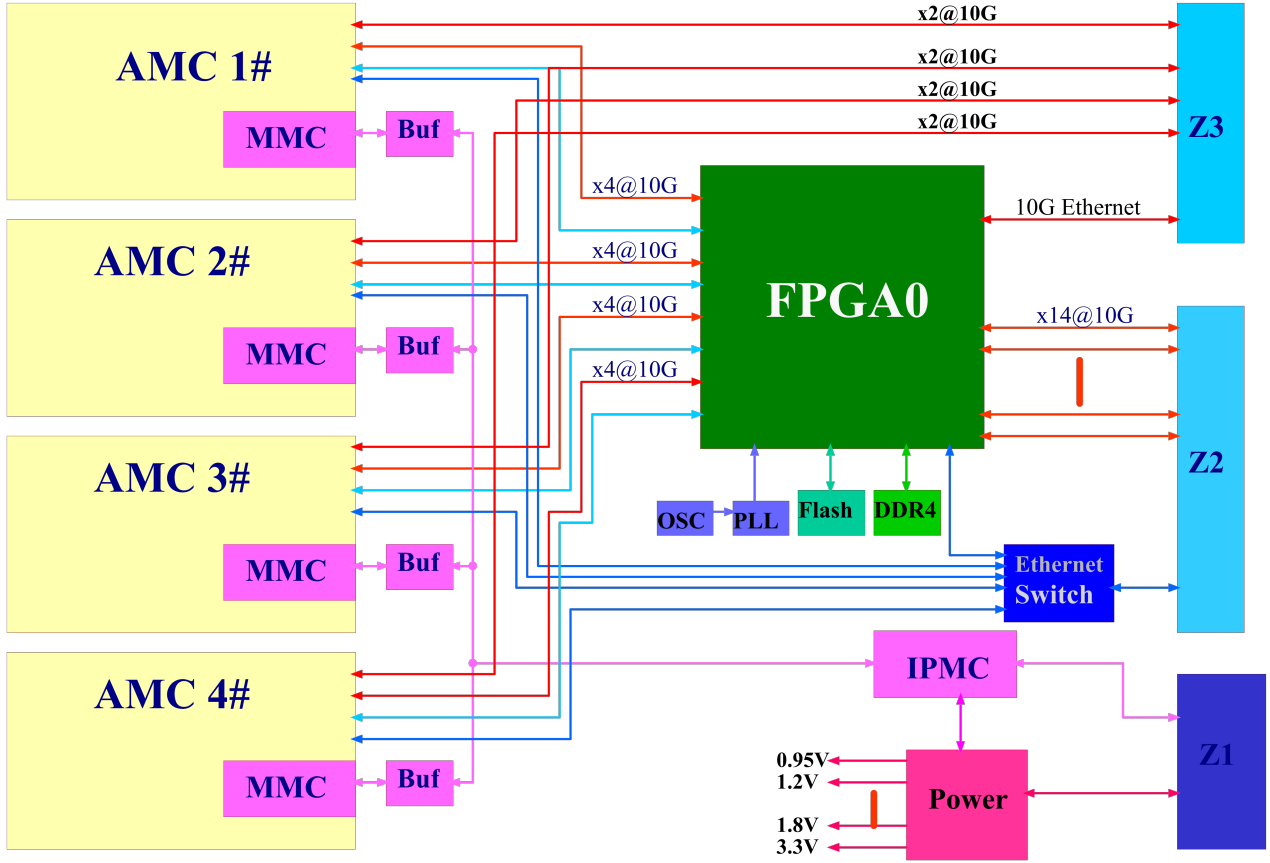
- On-board **USB-JTAG programmer** (Digilent)
- **UART-USB interface** for 4 AMC cards + switch FPGA
- **USB hub** for UART interfaces, IPMC
- **SFP+ cage** for switch-FPGA 10G Ethernet

CN_V4 Design Status

Jingzhou ZHAO, Zhen-An LIU, Wenxuan GONG
Trigger Lab, IHEP, Beijing

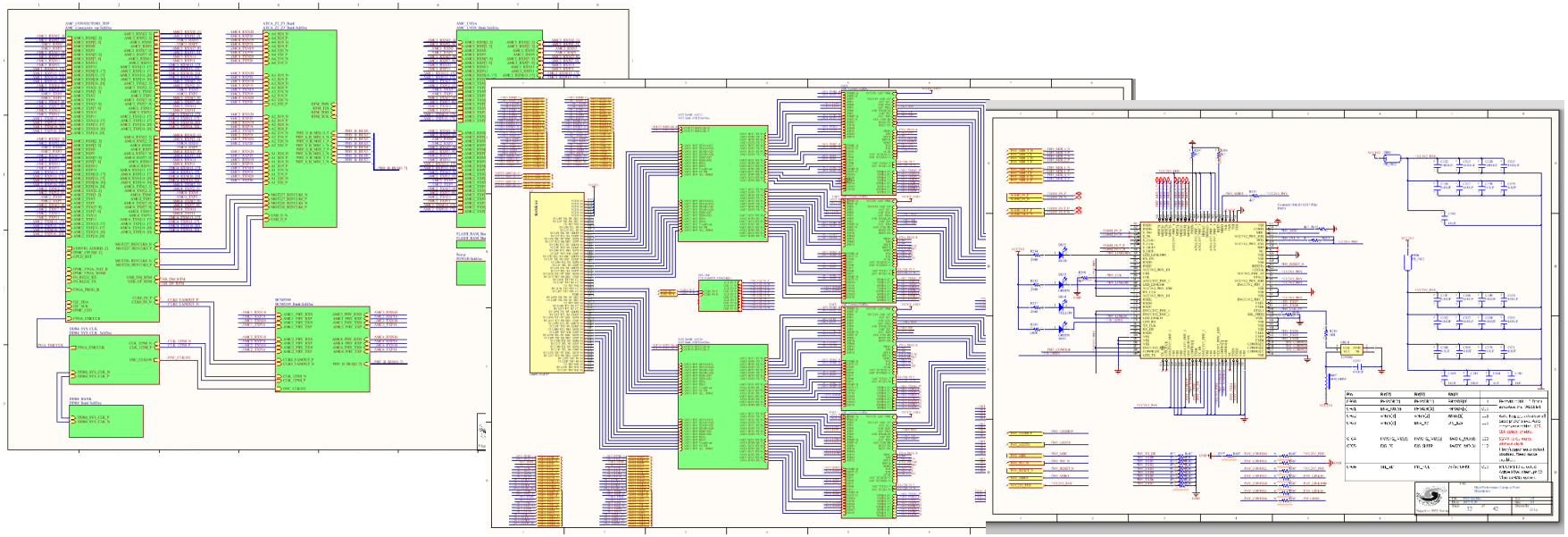
CN_V4 Block diagram




AMC 1#
MMC
Buf
AMC 2#
MMC
Buf
AMC 3#
MMC
Buf
AMC 4#
MMC
Buf
x2@10G
x2@10G
x2@10G
x2@10G
Z3
x4@10G
x4@10G
x4@10G
x4@10G
FPGA0
10G Ethernet
x14@10G
Z2
OSC
PLL
Flash
DDR4
Ethernet
Switch
IPMC
Z1
0.95V
1.2V
1.8V
3.3V
Power

CN_V4 design status

- Schematic of Carrier board is under designning.



Compute Node Upgrade: Current Status and Belle II Application

- **Update:** Schematics finished, PCB design ready in about two months
- First prototypes expected later this year
- Possible **replacement** for ONSEN carrier boards (only 2 spares)
  $\rightarrow$ requires significant firmware changes
- Possible **upgrade** path for ONSEN hardware

Firmware-Version Management

Firmware-Version Management

- Problem: **FPGA Firmware version** (e.g., DHH, DATCON, ONSEN) should be identifiable online and in data files
- Idea: Store the first 32 bits of the **git commit hash** in the FPGA's USERCODE or USR_ACCESS ($\geq$ Virtex-5) register
  `bitgen -g UserID:0x$(git rev-parse --short=8 HEAD)`
- Make it accessible to EPICS through a **PV**, and log it
- Maybe put look-up table in EPICS to pretty-print tagged versions

```
git tag | while read t; do echo $(git rev-parse
--short=8 $t) $t; done
d5cb6ce8 v1.00.a
10eb7c50 v1.01.a
...
```

- According to Dima, DHH already implemented a similar mechanism:
  - Store a time stamp and board number in USR_ACCESS
  - Write the time stamp to a git tag to identify the commit