

DCD and Switcher4.2B Tests

21st International Workshop on DEPFET Detectors and Applications, 28.05.-31.05.17
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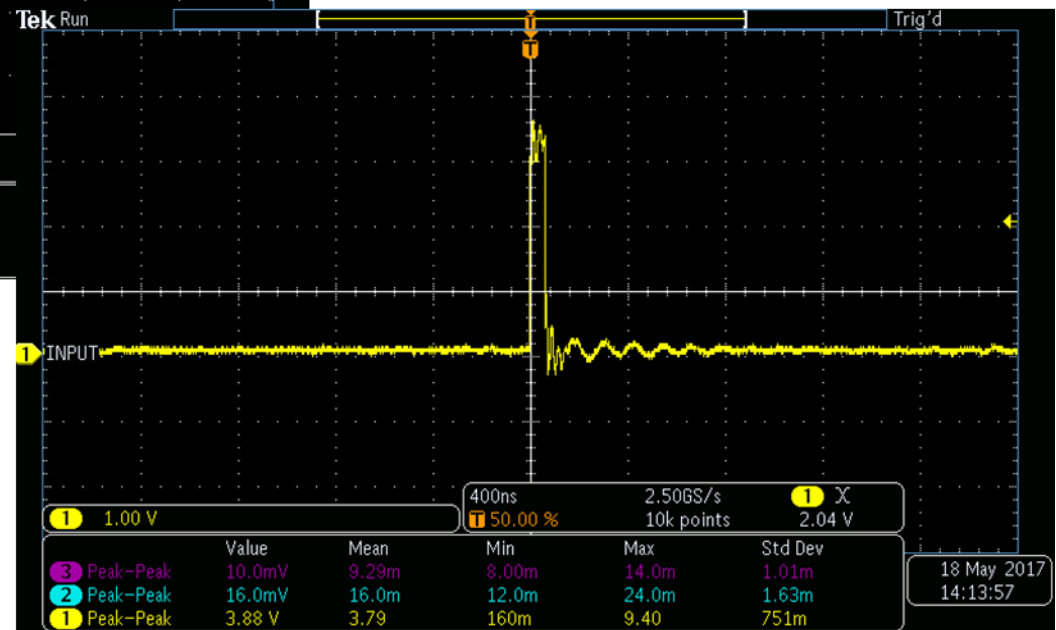
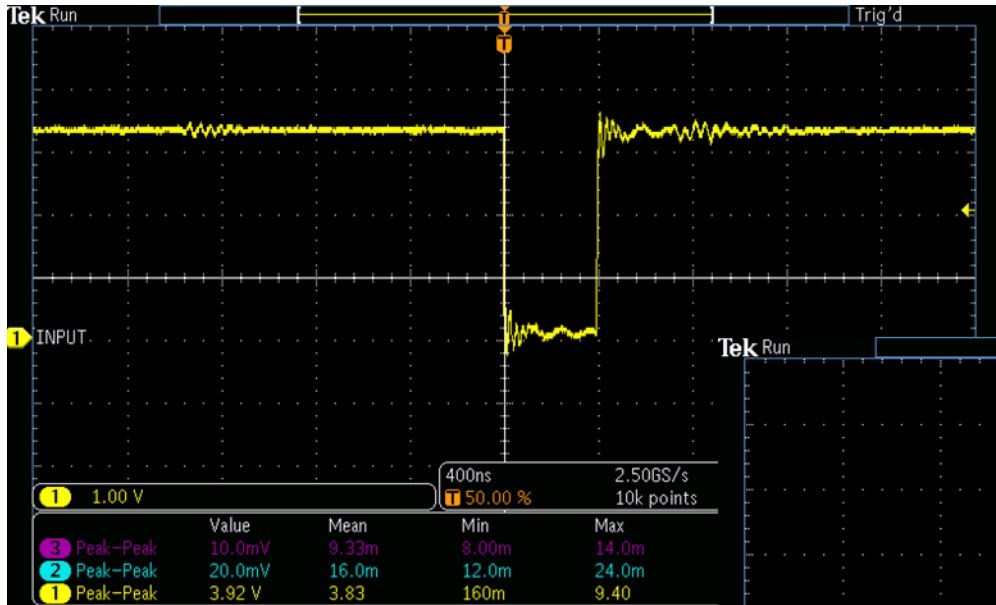
KIT-ADL (ASIC and Detector Laboratory), IPE (Institute of Data Processing and Electronics)



- Switcher4.2B Test Procedure
 - JTAG
 - Test of all gate and clear signals
- DCDIII Test Procedure
 - JTAG
 - Test of ADCs (single, one column, 256 ADCs)
 - Measurement of ADC linearity and noise
- Chip Probe Station
 - Mechanical construction
 - Software control and readout
 - Probe cards for Switcher and DCD
- Test Status and future tests

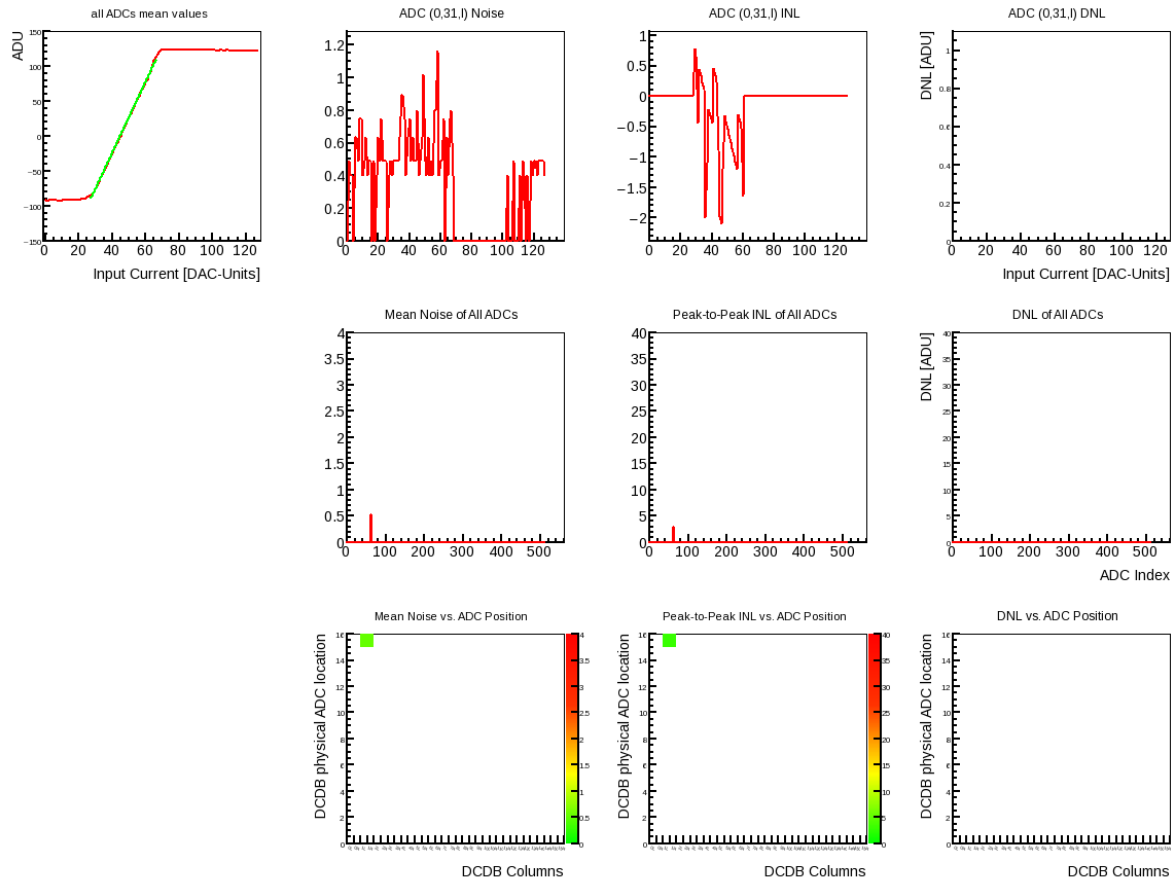
- 1) The chip is contacted
 - 2) Following voltages are used: $V_{DD} = 1.8V$, $V_{gate\ High} = 3.3V$, $V_{clear\ High} = 3.3V$, other voltages are zero
 - 3) The probe card can contact all Clear and all Gate outputs – in total 64
 - 4) The outputs are connected to one 64→1 “high voltage” MUX
 - 5) The output of the multiplexer is connected to a voltage divider (5→1) and to a comparator, it has variable threshold. The threshold is connected to 300 – 400mV
 - 6) The output of the comparator is measured by a scope probe
 - 7) JTAG ID test
 - 8) The current V_{DD} current consumption versus the DAC value, concerning Clear and Gate current consumption was checked
 - 9) Scope measurements of all 64 outputs. A counter is used to increment the channel number, all waveforms are checked
- ** If there is a short between Clear and Gate then would fail and current consumption (Power supply Hameg) would go on

Switcher4.2B: Gate and Clear Signal

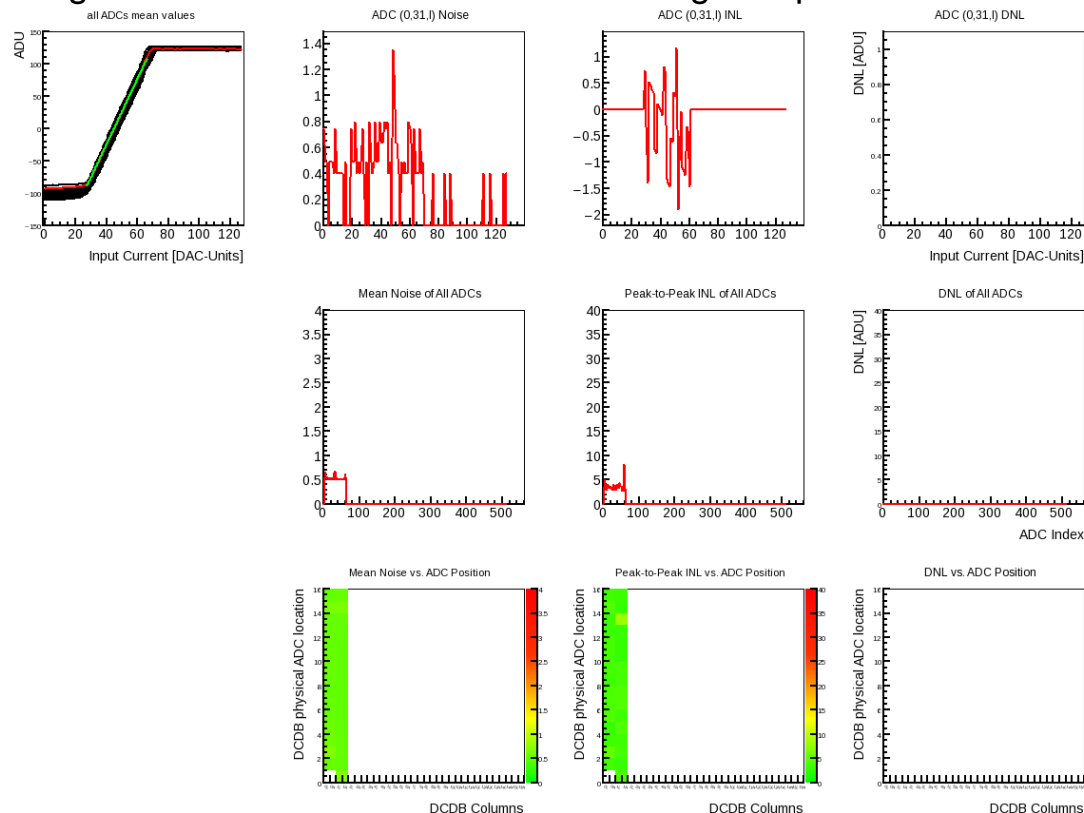


- 1) The chip is contacted
- 2) Following voltages are used $V_{DDD} = 1.8V$, $V_{DDA} = 1.8V$, $RefIn = 1.1V$, $AmpLow = 300mV$
- 3) In order to check the contact JTAG ID readout, when there is ID then the chuck raising is stopped
- 4) Second test is tests patter readout
- 5) Third test is analog power consumption after DAC configuring
- 6) It happens often that $RefIn$ current is not in the correct range (300mA) after DAC enable
- 7) In this case the chuck is additionally lifted by less then 100um. (Probe station shows the overdrive)
- 8) After this, ADC readout is started
- 9) ADCs are readout via JTAG, 256 are readout is parallel, the test time is so quite short
- 10) For the test, the current source IP_Signal (internal source) is used
- 11) Very often there is a contact problem, the ADC lines does not look nice, in this case usually can be observed that $RefIn$ current oscillates. The chuck is lowered slowly until $RefIn$ current gets stable. Almost always the ADC lines are nice then.
- 12) Our software can measure noise in principle, however for this many points have to be measured per one input. To speed up tests no noise was measured. We observed that noise is very good

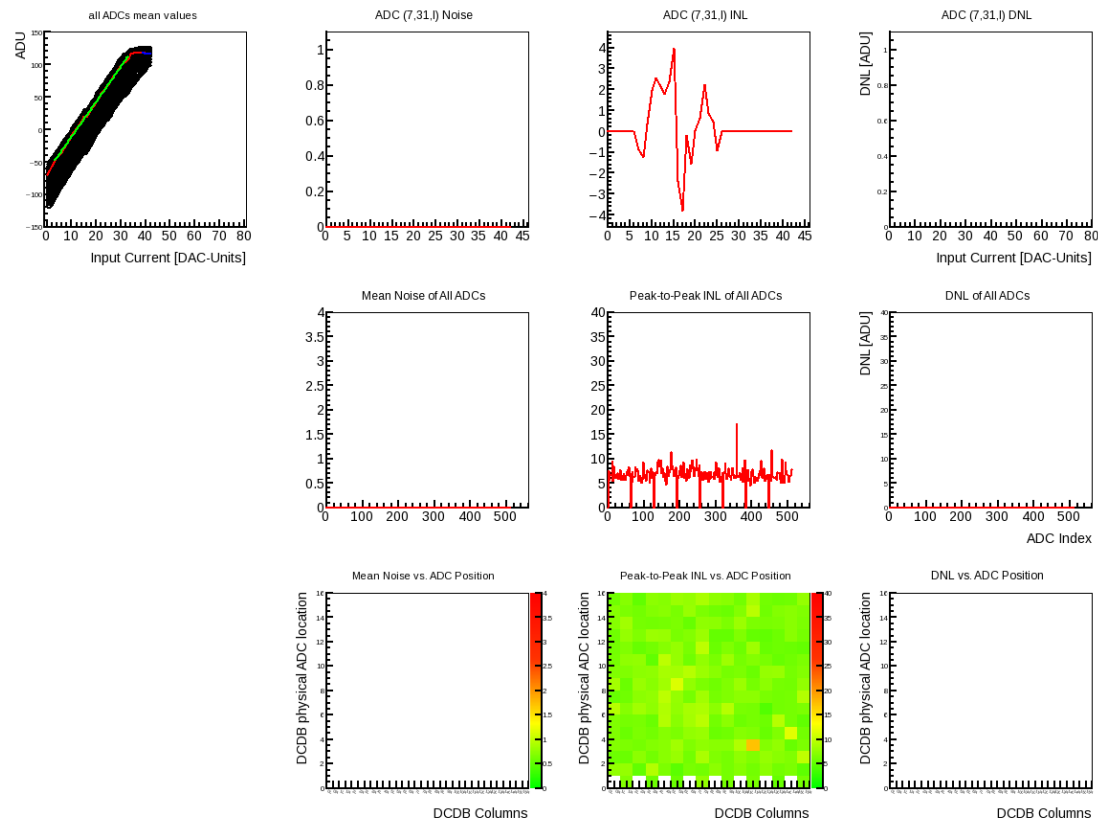
- The figure shows the test of only one ADC. We see also the noise
- The noise is 0.5 and the INL about 2 LSBs



- Figure show the test of all ADCs in one double column, similar results are obtained
- Here all ADCs in one column are measured at the same time
- We have observed that the results are slightly worse when all ADCs (all 8 double-columns)
- The reason is that all VPSignal currents are swept at the same time, therefore the current consumption changes a low and there is a variable voltage drop. This leads to instabilities



- In order to speed up the tests, we didn't measure the noise
- We think this is not a problem
- Noise can be seen in the INL plot – it shows the superposition of noise and INL



- We have measured ADCs with JTAG
- However we didn't use as we wanted initially the test pads
- The test pads do not have bumps and are places on the top and on the bottom of the chip
- We were able to measure several chips via test pads (see measurement with DCDC), however the time needed to establish contact was too long
- For the measurement with test pads we develop special probe card (PC22)
- Concerning measurements with bumps, we used finally the PC from Heidelberg with a new needle ring
- It showed to be easier to establish contact with this PC than with the PC135
- (JTAG tests work always with all PCs however ADC tests are more difficult)

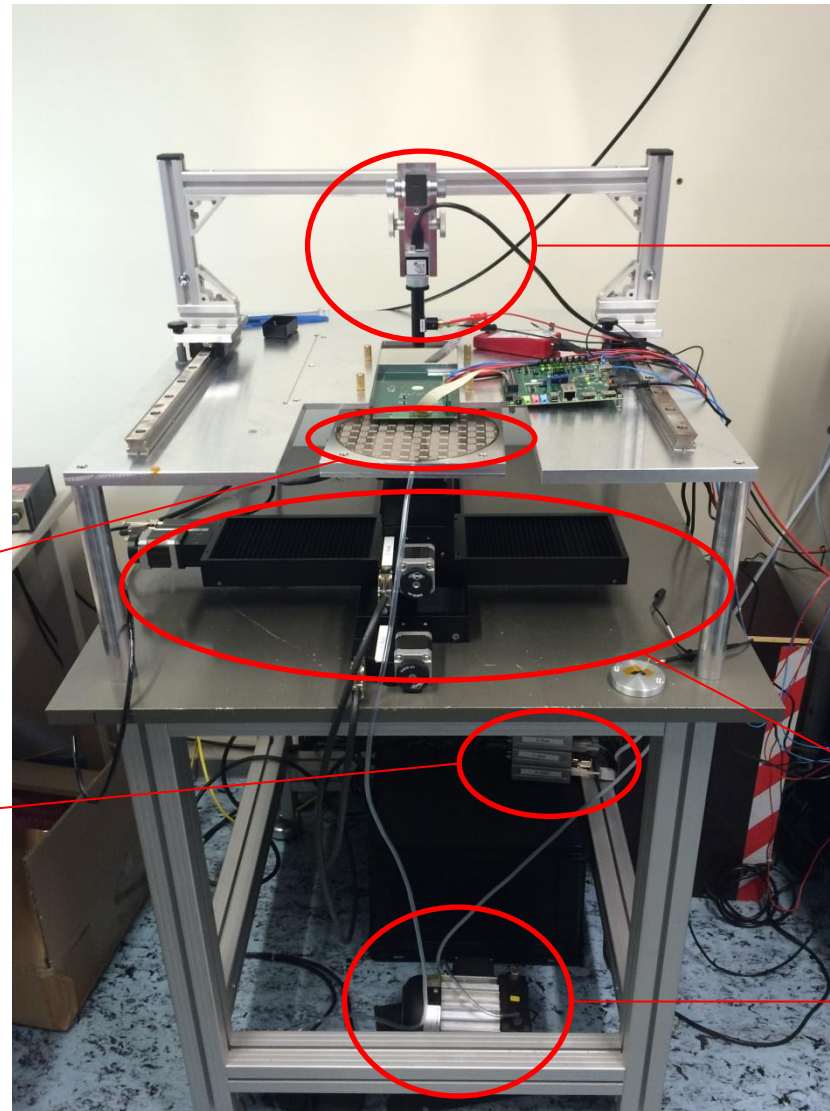
Wafer Chuck

PS-10 Motor
Controller
(CAN-Bus)

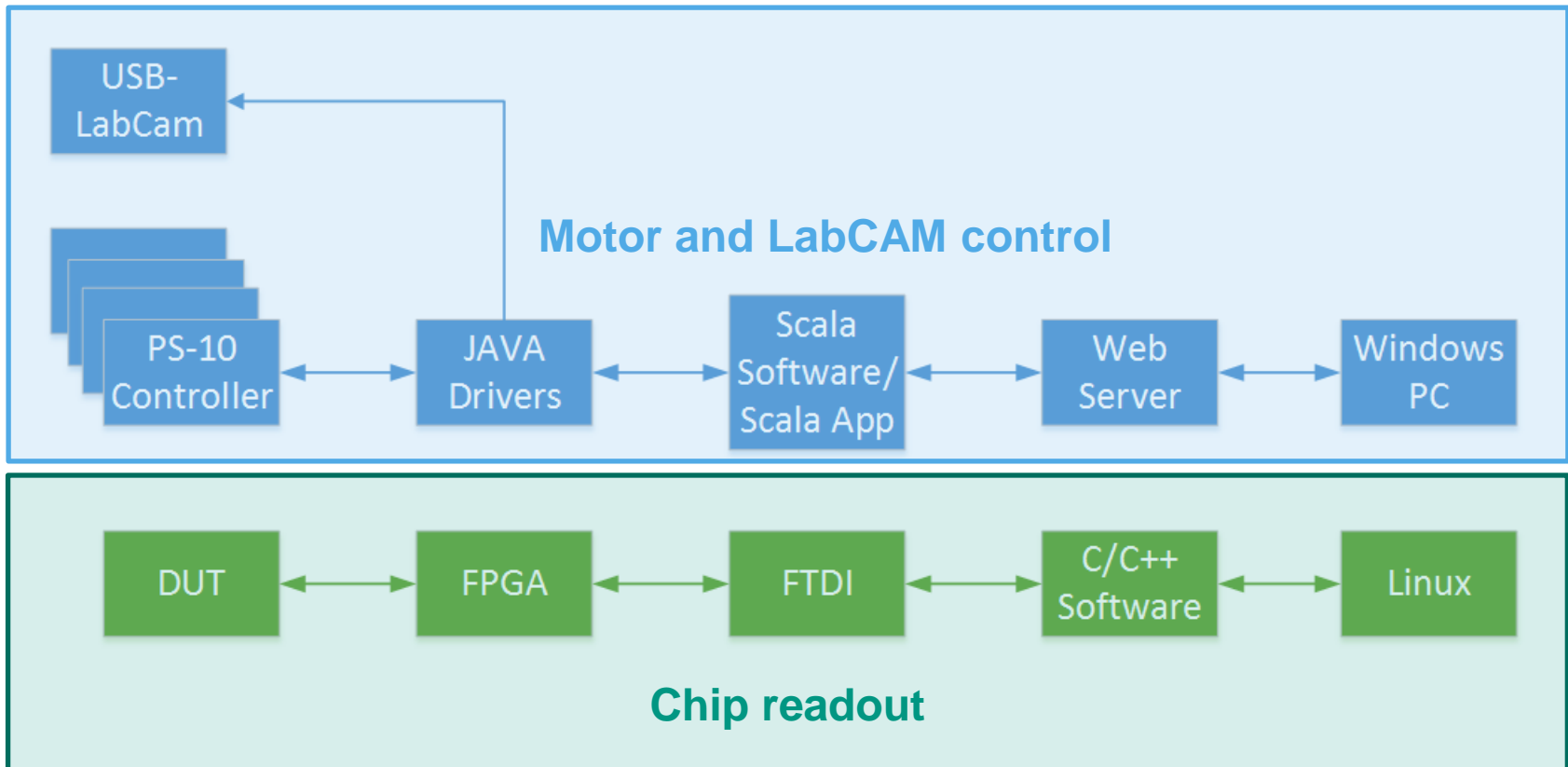
USB-LabCam +
fine drive for focal
length adjustment

Step Motors

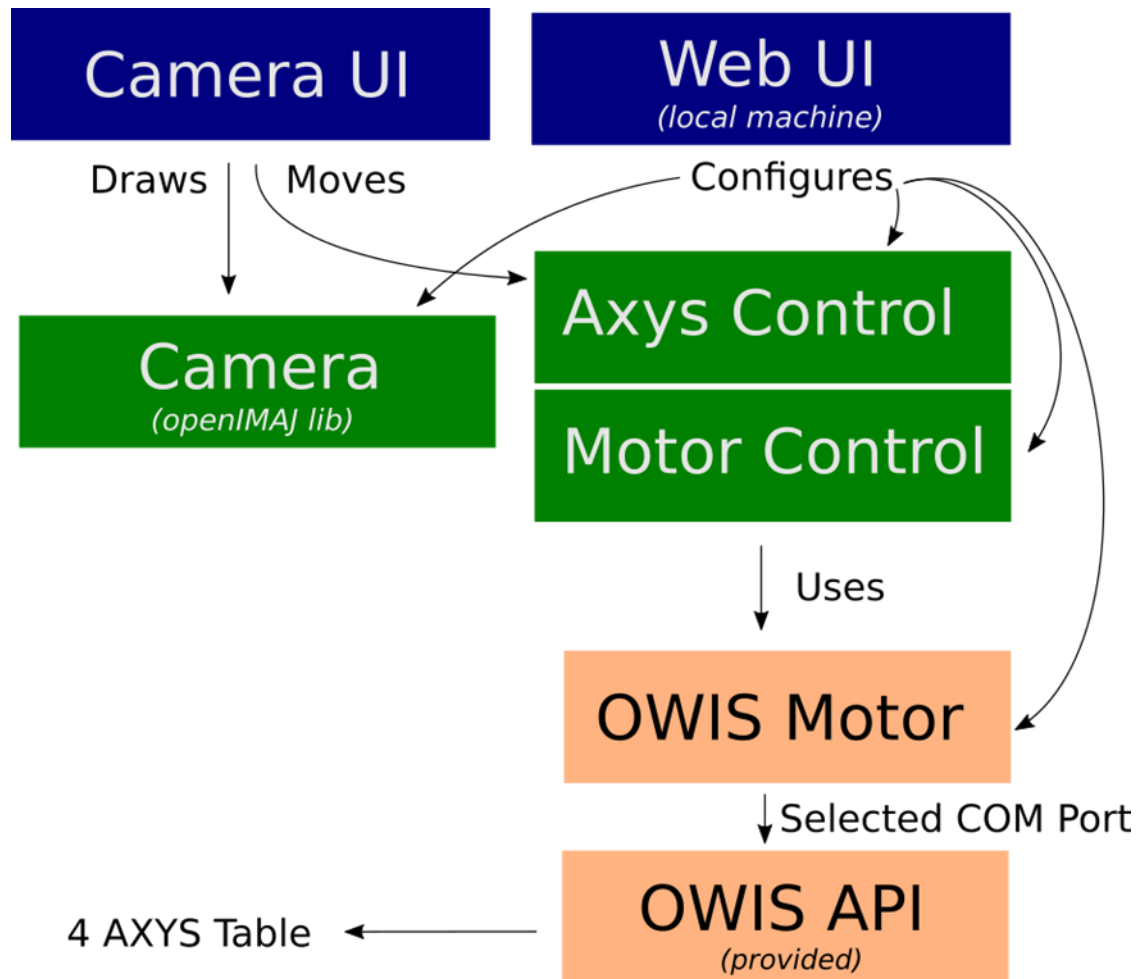
Vacuum pump



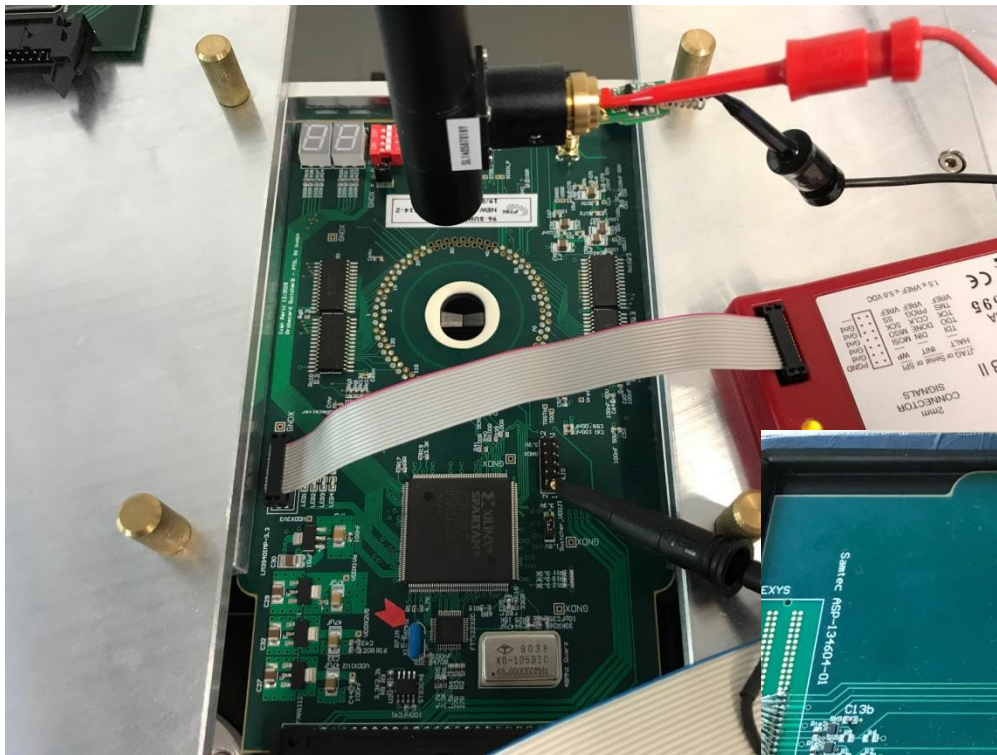
Simplified Block Diagram



Simplified Block Diagram of the Test Setup

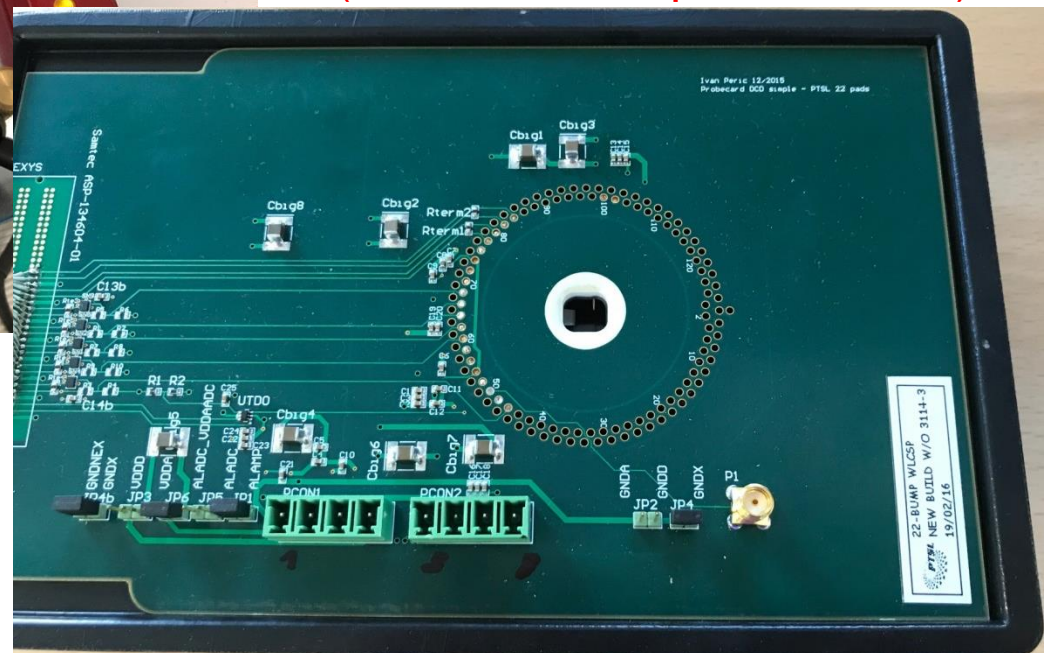


Switcher4.2B and DCD Probecards



Switcher4.2B Probecard
with Spartan 3 Readout (16:1
MUX for HV tests)

DCDIII Probecard
Via Nexys Video Board Readout
(DCD readout up to 150 MHz)



■ Webserver Application (Axy's control)

← → ↻ localhost:8586/probestation/config/axys ☆

Probestation ::

Switcher4.2B ▾ × +

Axy's -> Ref
Stop All

Dashboard
Motor Configuration
Axy's Configuration
Camera Configuration
GUI: Motor Control Window
Documentation Config
Documentation

Page Content:
Axy's Configuration
Saved Positions
Auto Move Scripts

Axy's Configuration

Move All to Reference

Name	Motor ID	Motor Detected	Exclude from Back to Reference	Back to Zero	Max (mm)	Speed (mm/s)
Phi	4 ▾	Yes	<input checked="" type="checkbox"/>	<input type="checkbox"/>	9999,0	0,5
X	1 ▾	Yes	<input type="checkbox"/>	<input type="checkbox"/>	10000,0	0,5
Y	2 ▾	Yes	<input type="checkbox"/>	<input type="checkbox"/>	10000,0	0,5
Z	3 ▾	Yes	<input type="checkbox"/>	<input checked="" type="checkbox"/>	10000,0	0,5

Axy's Name: Add

Saved Positions

	Name	Phi	X	Y	Z	Actions
×	Switcher4.2B	179,9247	131,703	134,9515	20,0	Go To Update with Actual
×	Switcher4.2B Load	179,9247	46,8009	-0,6204	4,6790666666666666	Go To Update with Actual

Add Position: Add

Auto Move Scripts

Add

■ Webserver Application (LabCam control)

Absolute:	X=	131,745	Y=	135,166	Z=	28,694
Relative:	X=	7,012	Y=	80,674	Z=	25,868
Saved:	X=	124,732	Y=	54,492	Z=	2,826

WebcamPictureSource

☒ Visible

☒ bool.reverseX : ☒

☒ bool.reverseY : ☒

GridOverlayStep

☒ Visible

int.xPitch :

int.yPitch :

int.xOffset :

int.yOffset :

int.thickness :

MotorControlOverlay

☒ Visible

☐ Motor On/Off

Speed:

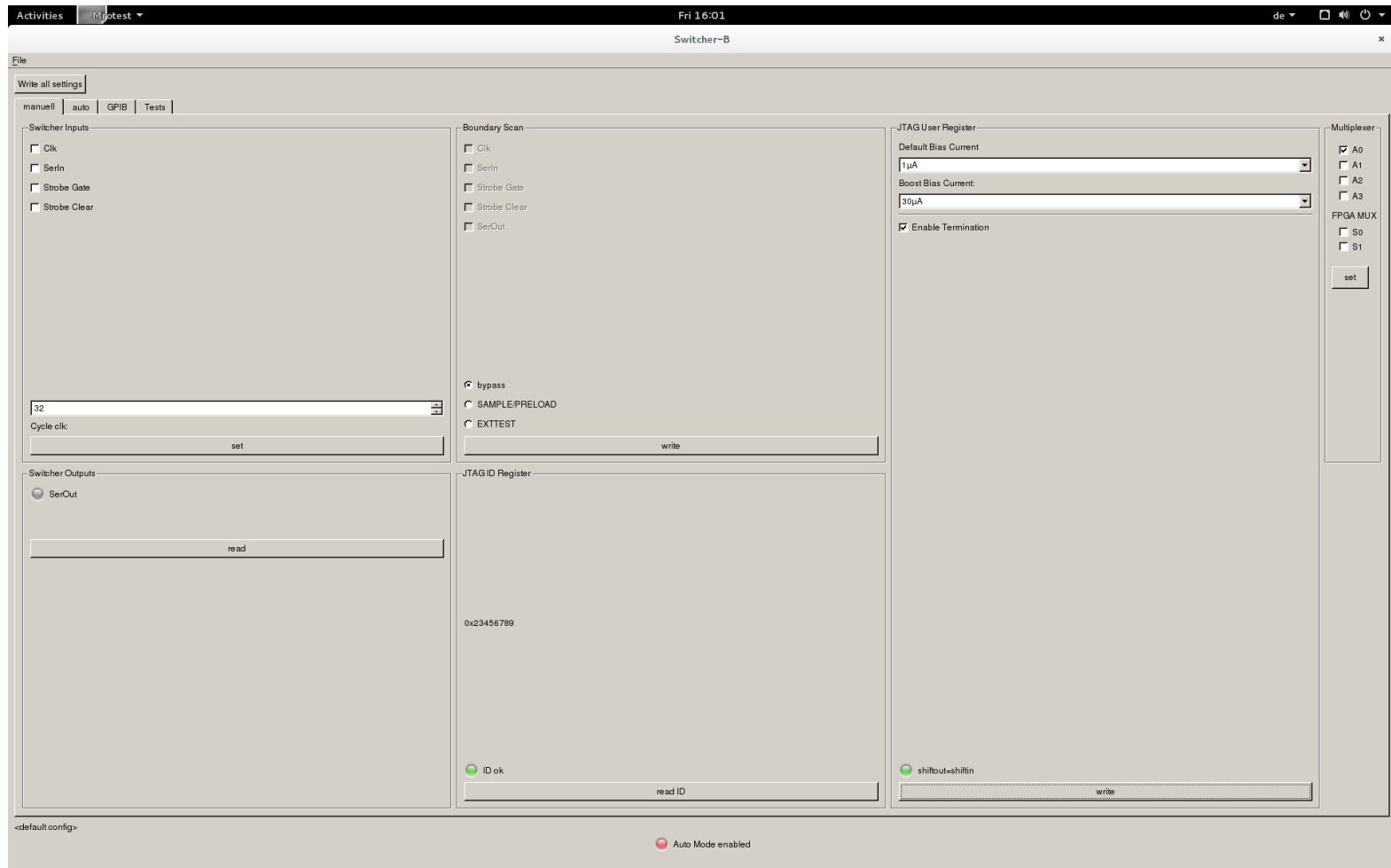
X:

Y:

Z:

Phi:

■ Chip Readout Software (C/C++)



TEST STATUS

Results of Switcher4.2B tests

Switcher Chips	Read JTAG ID	Current Consumption (1.8V/HV)	64 HV-Signals	Bias Current	Boost Current
89	✓	✓	✓	✓	✓
10	✓	✓	✗ *)	✓	✓
1	✓	✗	✗	✓	✓

*) It seems a contact problem between needles and switcher. Half of the channels are working!

DCD Chips	Read JTAG ID	Current Consumption (VDDA, VDDD)	Digital Test Pattern	Bias Current	Input/Output characteristic
197 (DCDB4.2)	✓	✓	✓	✓	✓
10 (DCDE-II)					
10 (DCDC)					
10 (DCDEC)					

- May 2017
 - 100 Switchers (already done!)
 - 200 DCDs (already done!)

- July 2017
 - 200 Switchers (to do..)
 - 130 DCD (to do..)



Thank you for your attention!