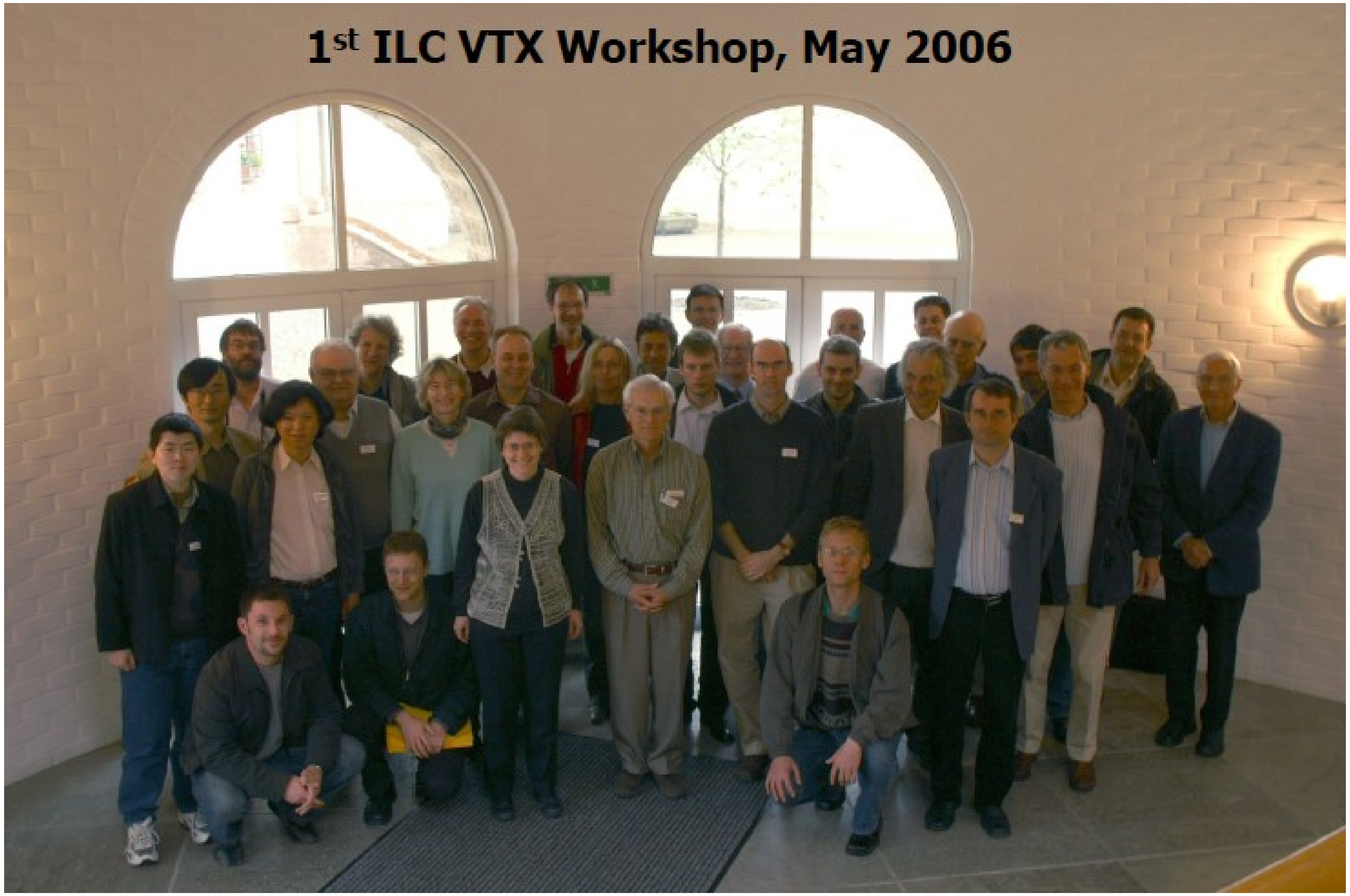
ILC & CLIC, established technologies and promising R&D paths, requirements, simulation and performance, cooling, supports & services

Marcel Vos IFIC (U. Valencia/CSIC), Spain

Back together after 10 years



1st ILC VTX workshop 2006

2nd ILC VTX workshop 2008

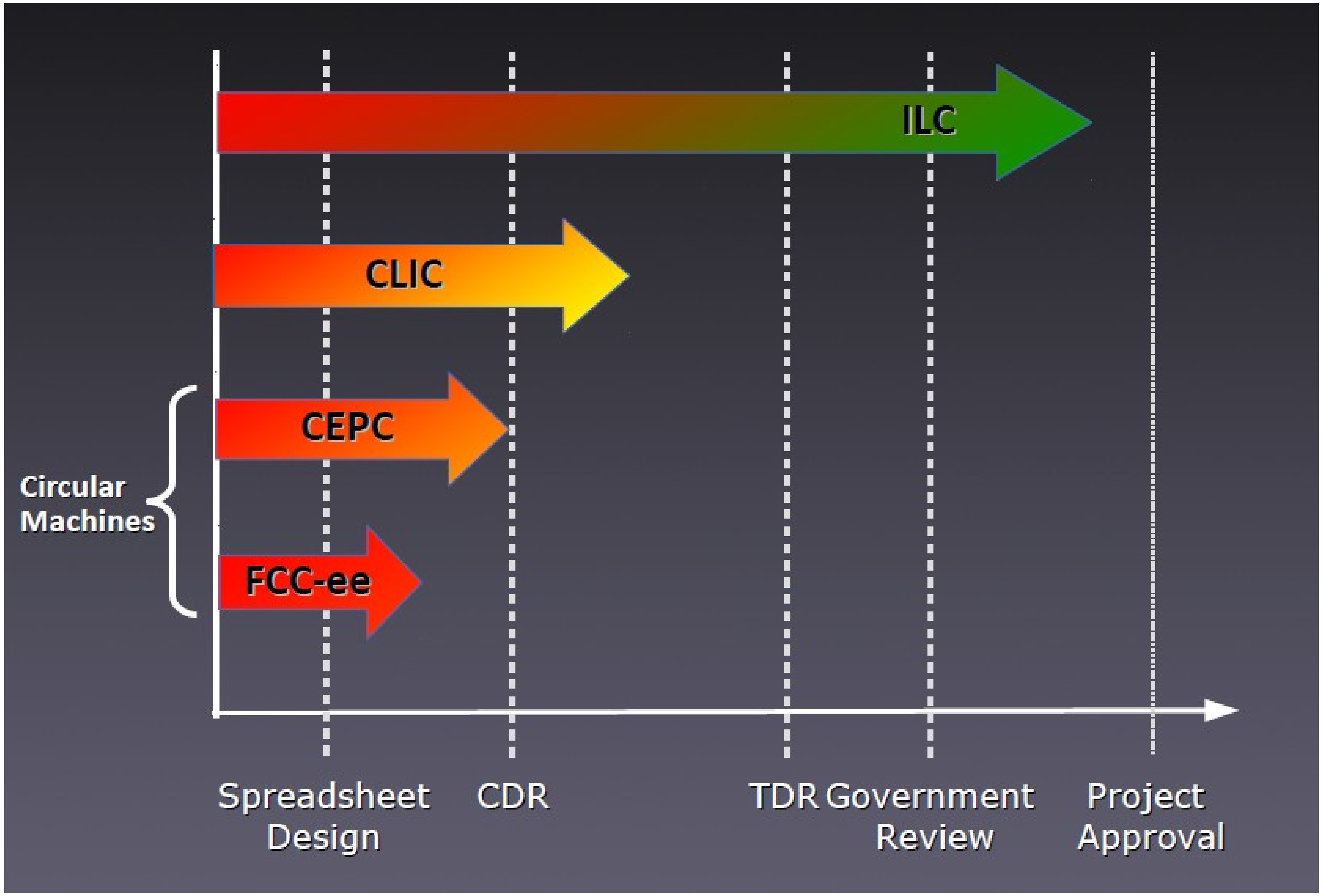
3rd LC VTX workshop 2017

….

Laci Andricek

LC vertex 2017

Readiness



Marcel Stanitzki

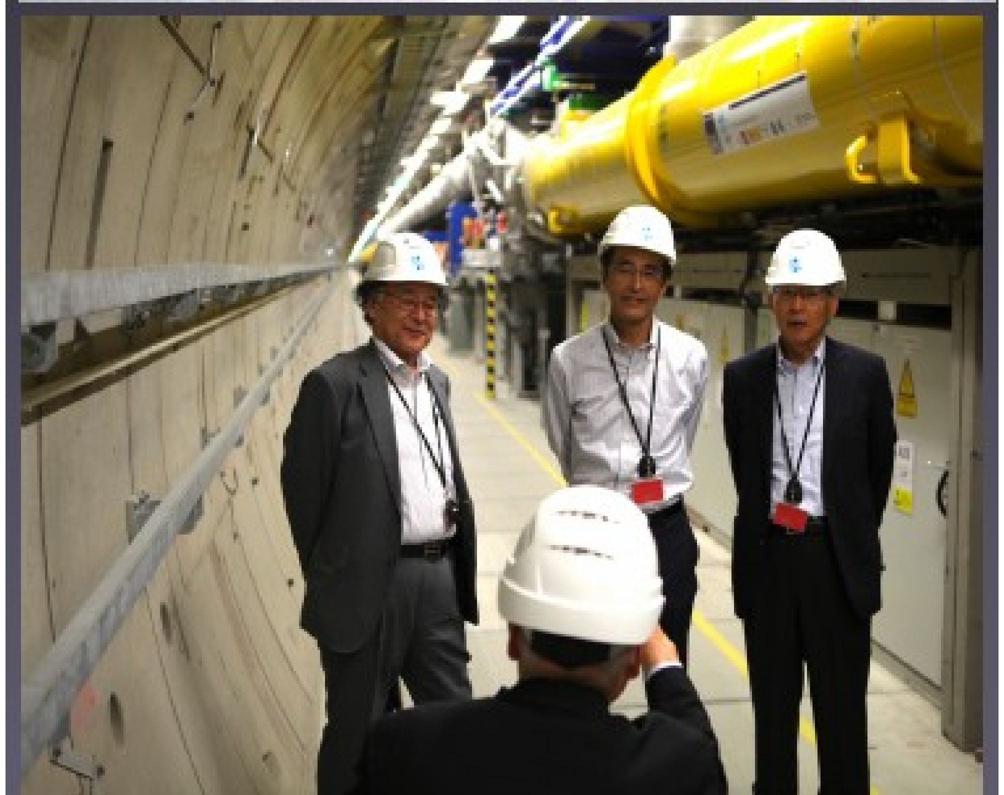
European strategy update due in 2019/20

ILC TDR in 2013 → government decision before 2019

CLIC CDR in 2012 → CERN decision by 2020

FCCee/hh and CEPC CDR before 2019 (design, cost, time)

ILC news



Marcel Stanitzki

Proposal for ILC in Kitakami area is in government review in Japan

Looking for international contributions
- high-level US-Japan meetings
- exploratory visits to larger European countries

Japanese decision is “an input to the European strategy update” (KEK management)

Stage the programme to reduce cost
- start/limit operation at 250 GeV?

ILC is in the hands of the politicians

CLIC status

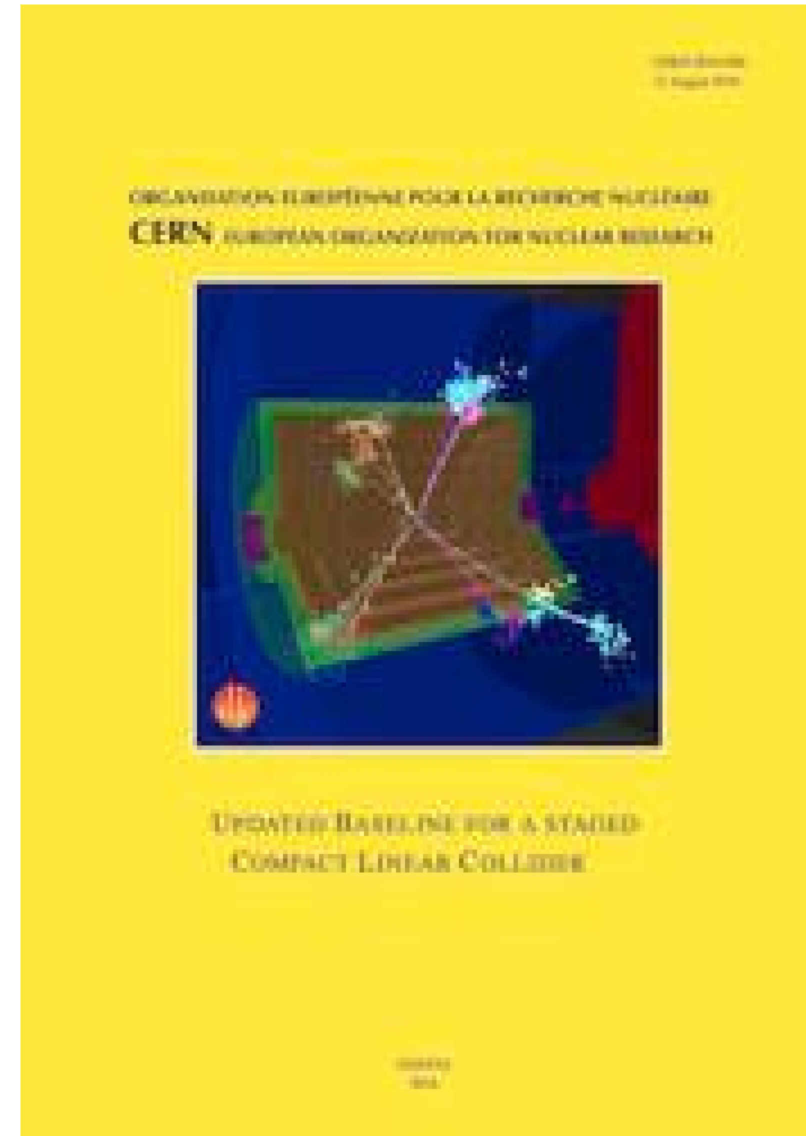
CLIC staging

- start with “low” energy: 380 GeV

  precision Higgs and top physics in an “affordable” machine

- move to 1.5-3 TeV (as required by new physics reach)

Challenging combination of small beams (→ significant background) and short (0.5 ns) bunch spacing requires fast read-out (slim hybrid pixels, monolithic CMOS)



CERN-2016-004

Dominik Dannheim

Circular colliders

Circular e^+e^- colliders

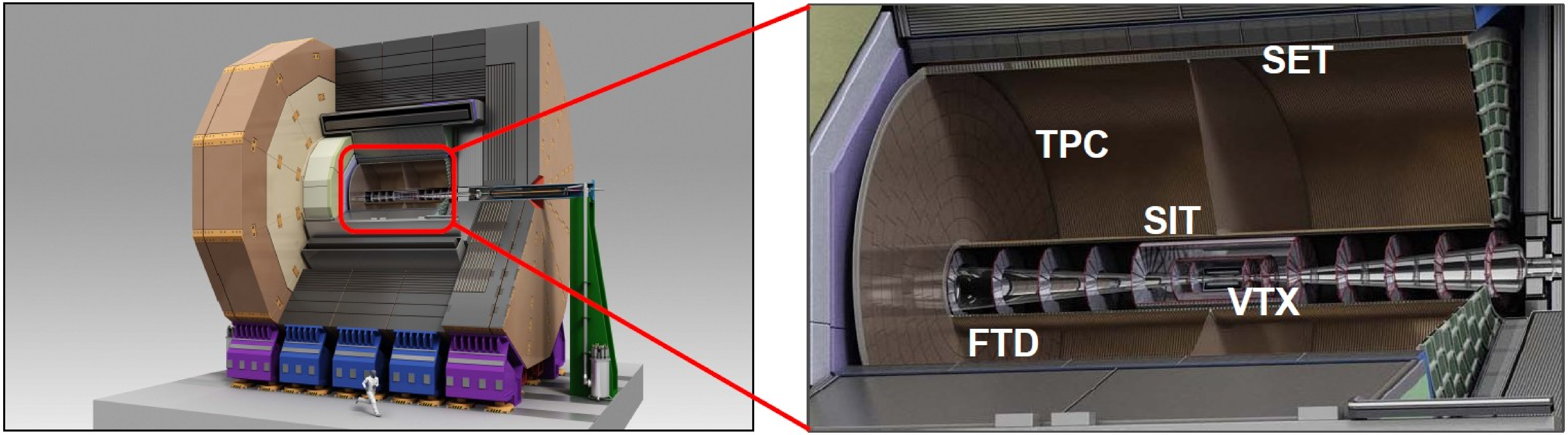
Chinese project looking to internationalize

FCCee detector work starting?

DEPFET is a good candidate

Talk by Hongbo Zhu

Detector concepts



ILD → CMOS MAPS, DEPFET, FPCCD

Adequate presence: VXD convener (M.V.) + Forward Tracker Disks (I. Vila)

SiD → single BX time stamping with 3D-integrated devices or Chronopixels)

Vertex detector

The vertex detector is key to several measurements:

– Higgs couplings to bottom and charm

→ charm tagging (= impact parameter resolution)

– A_{FB} in $b\bar{b}$ production

→ vertex charge (= coverage: down to 100 MeV and 6^o)

Benchmarking & optimization requires detailed studies of tracking/vertexing performance (efficiency, parameter resolution) with realistic background overlay and studies to relate

Precision vertexing

Mainstream R&D for silicon pixel detectors for HL-LHC is primarily about robustness:

– detect O(1000) tracks every 25 ns, survive a fluence of 10^{16} n/cm^2

The ILC* offers a motivation to build the next generation of precision devices:

– Inner radius: 30 mm → 15 mm

– Spatial resolution: 10 μm → 3-5 μm

– Material budget: 1% X_0 → 0.1% X_0

– Timing precision: 25 ns → 300 ns/1 μs/100 μs**

*CLIC is somewhere between the two extremes. It requires 10 ns time stamping to deal with backgrounds and relaxes some of the other specifications

**The timing requirement remains object of debate: SiD requires 300 ns (single BX), ILD envisages a combination of very precise, relatively slow layers mixed and fast, coarser-grained layers.

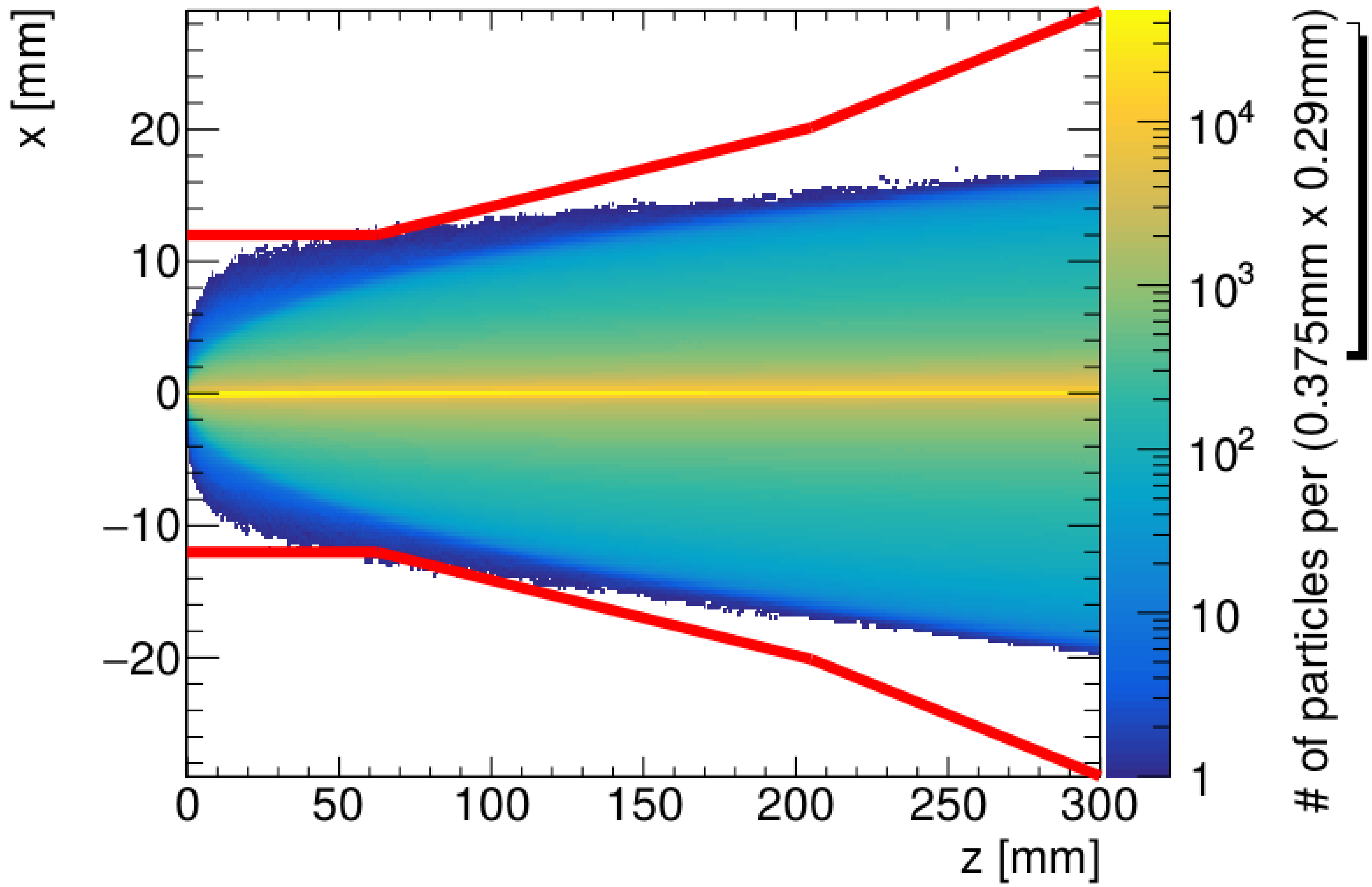
Background levels

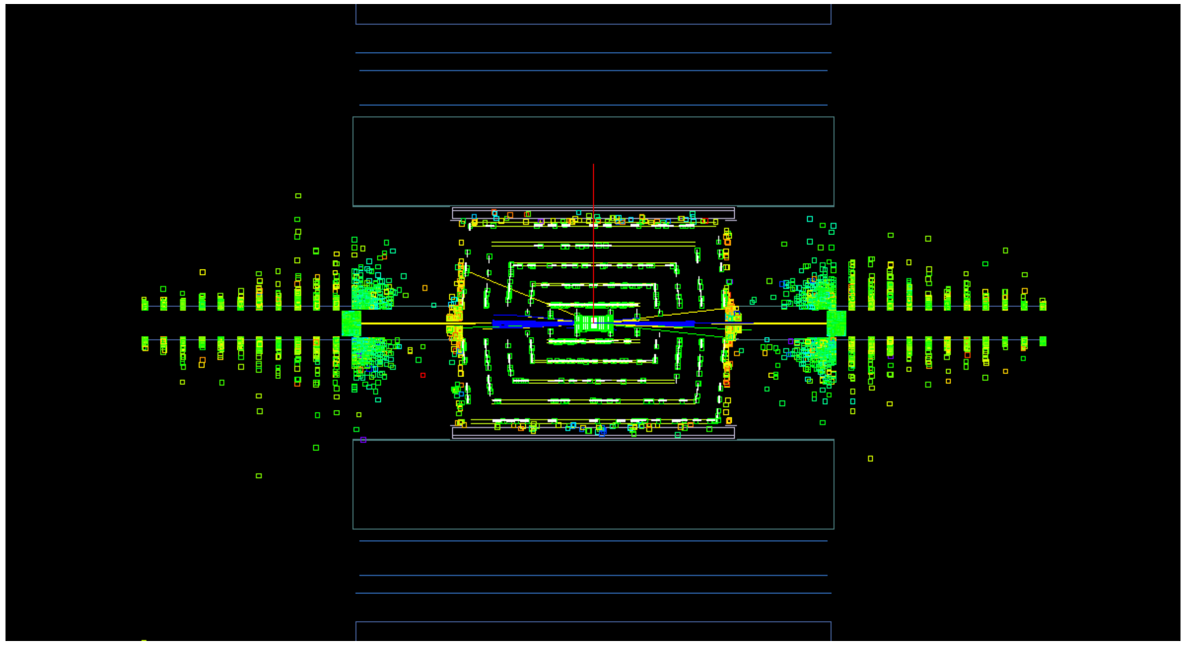
Incoherent pair production off very intense beams produces a spray of low-momentum, low-angle electrons and positrons

Hit rates depend on:

- inner radius & magnetic field
- Center-of-mass energy
- Machine parameters

O(1) hit/mm²/ns in innermost layer

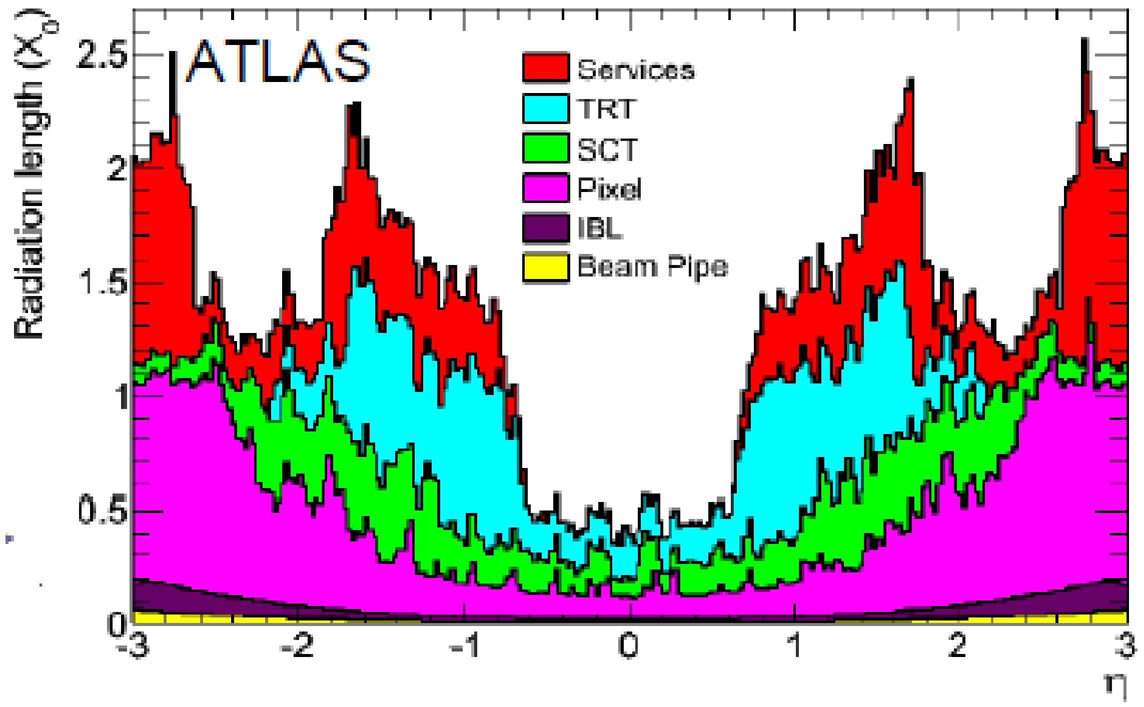




DEPFET

Active Pixel Detector

Material budget



That's too much material!

20%-100% X_0 in pixel detector

50%-200% X_0 in complete tracker

Limits tracking&vertexing and global performance (photons)

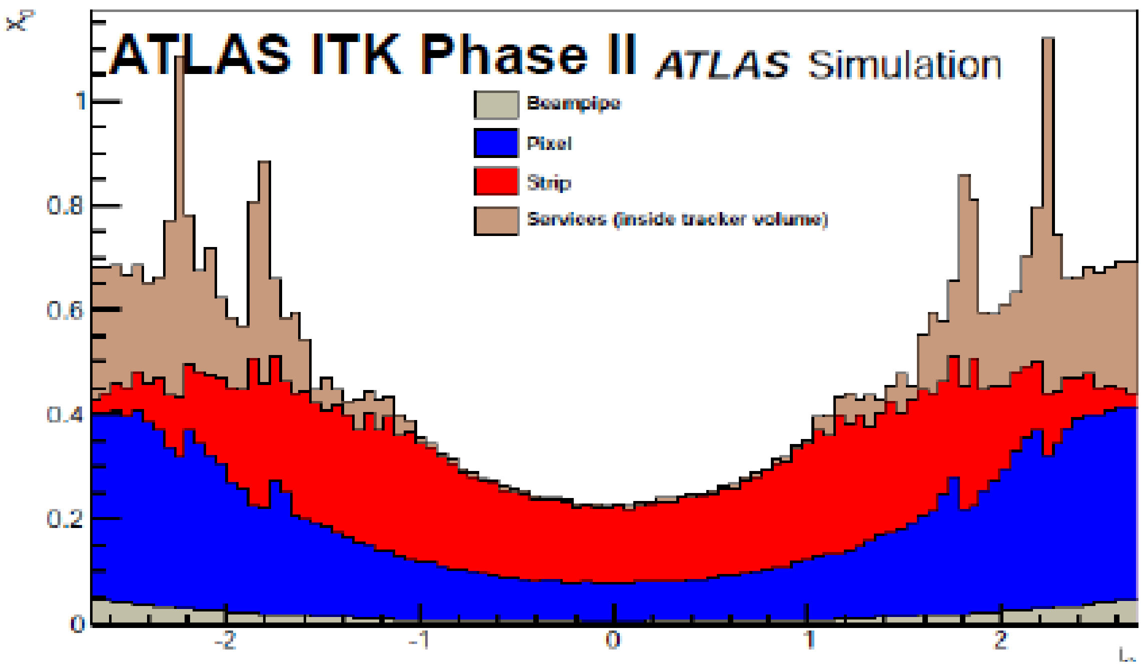
Can we do better?

Material budget

Can we do better? YES!

10%-40% X_0 in pixels

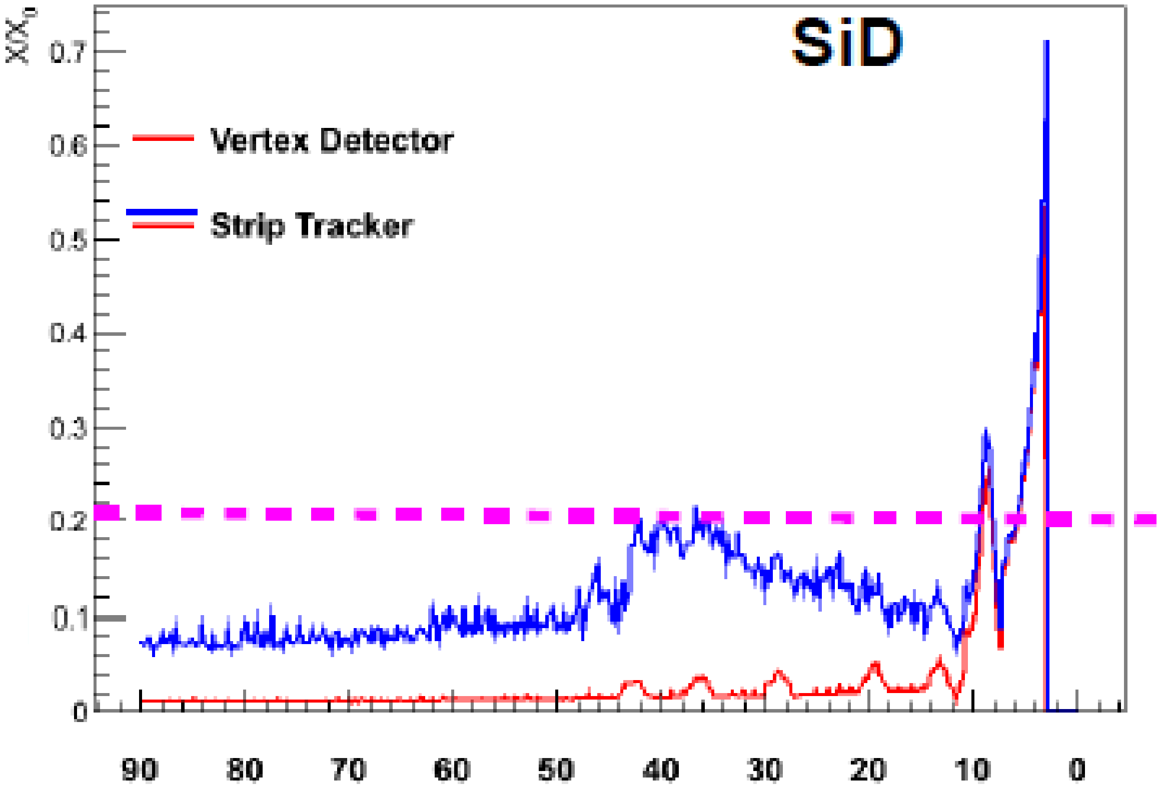
30%-70% X_0 in complete tracker



Material budget

Can we do better still? YES!
< 1% in vertex detector
10%-20% in entire tracker

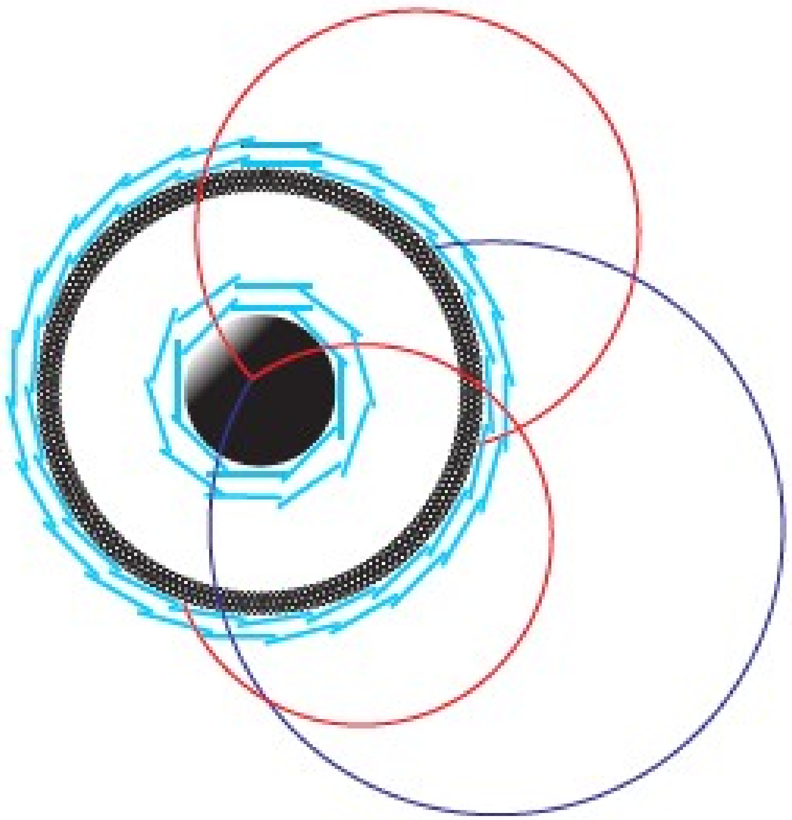
Definitely, life is easier if hit rates and radiation levels are several orders of magnitude smaller



Material budget

Mu3e: track and vertex reconstruction for 50 MeV electrons

Are we too optimistic?

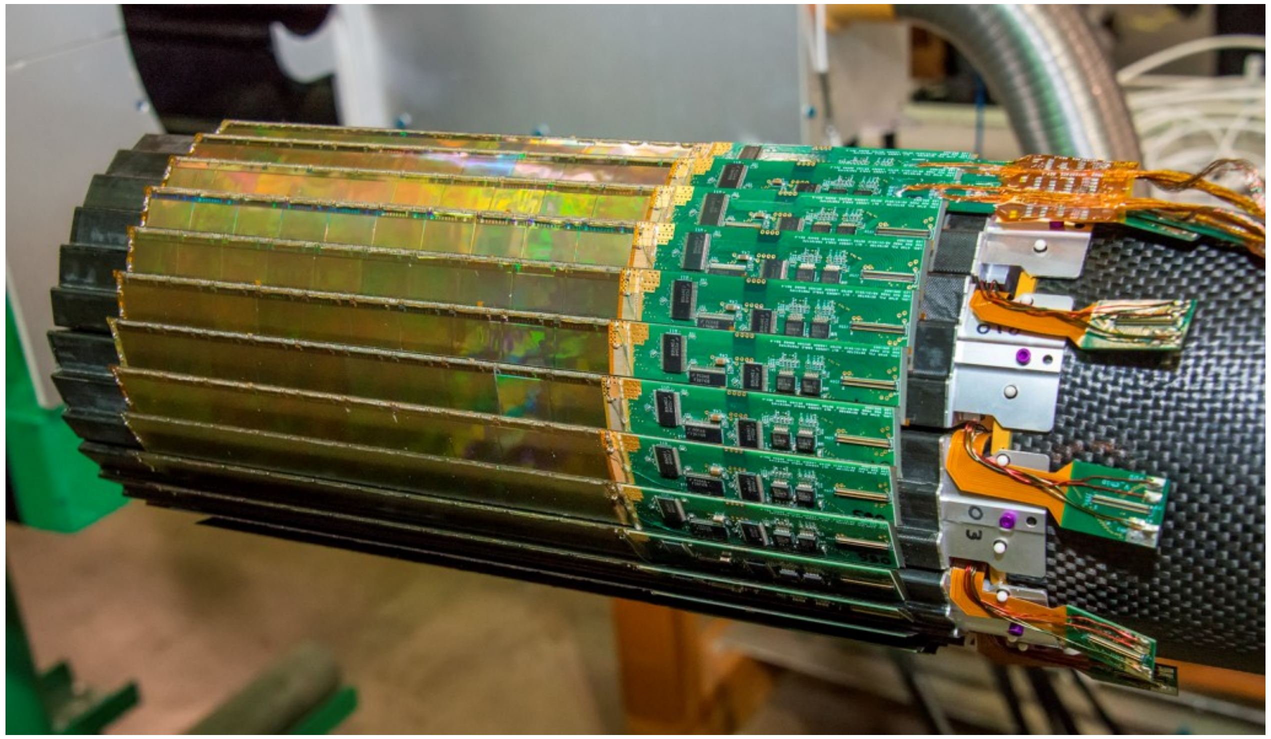


Experiment	Ref.	x/X_0 per layer [%]
ATLAS IBL	[1]	1.9
CMS Phase I	[2]	1.1
STAR	[3]	0.4
ALICE upgrade	[4]	0.3
Belle-II IBL	[5]	0.2
Mu3e		**0.1**

Table: Frank Meier

CMOS MAPs

Leo Greiner (LBL)



STAR Heavy Flavour Tagger →
1st generation MAPS-based vertex detector

Based on Strasbourg sensors:
- S/N ratio ~ 30,
- resolution ~ 4 μm
- ro time 186 μs

Air cooled, 50 μm thin sensors
Material 0.4% X_0

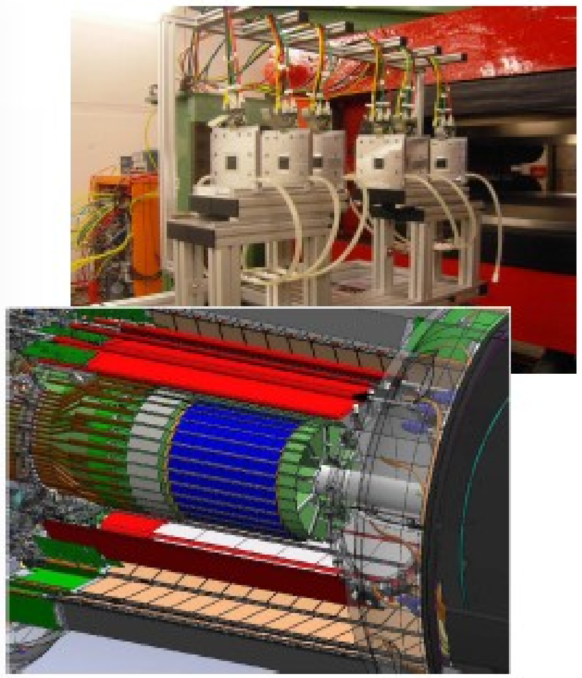
CMOS MAPs - future

Improving Speed and Radiation Tolerance

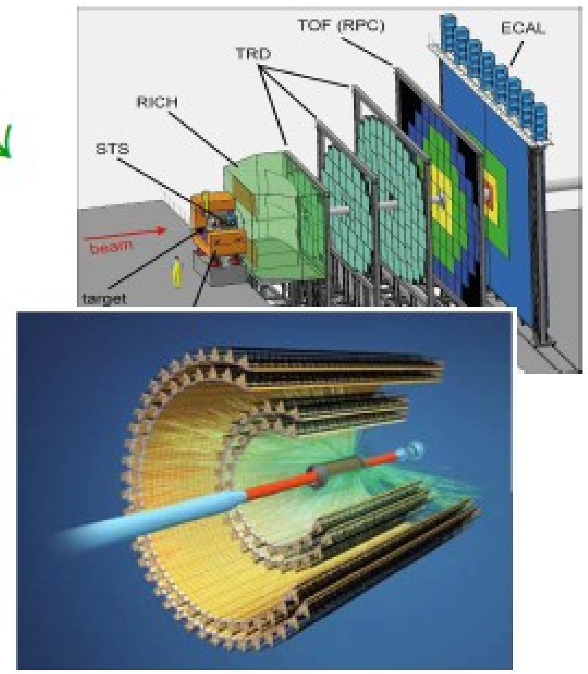
Marc Winter

O(10^2) μs

How to improve speed & radiation tolerance while preserving 3-5 μm precision & $< 0.1\%$ X_0 ?

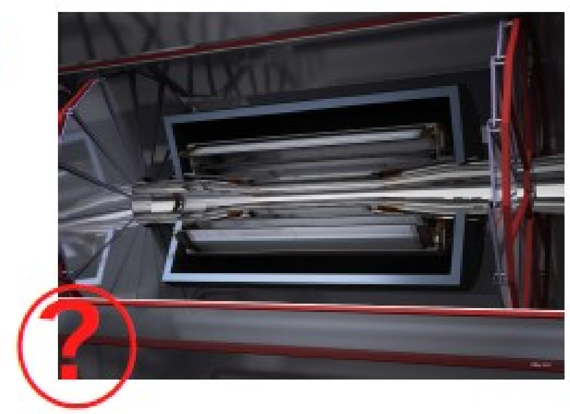


O(10) μs



ALPIDE/MISTRAL in quadruple-well 0.18 um TowerJazz technology

O(1) μs



EUDET/STAR	$\rightarrowtail$	**ALICE/CBM**	$\rightarrowtail$	**?X?/ILC**
2010/14	$\rightarrowtail$	2015/2019	$\rightarrowtail$	$\gtrsim$ 2020

9

	σ_{sp}	$t_{r.o.}$	Dose	Fluency	T_{op}	Power	Active area
STAR-PXL	$< 4\ \mu m$	$< 200\ \mu s$	150 kRad	$3{\cdot}10^{12}$ n_{eq}/cm^2	30-35°C	160 mW/cm^2	0.15 m^2
ITS-in	$\lesssim 5\ \mu m$	$\lesssim 30\ \mu s$	2.7 MRad	$1.7{\cdot}10^{13}$ n_{eq}/cm^2	30°C	$<$ 300 mW/cm^2	0.17 m^2
ITS-out	$\lesssim 10\ \mu m$	$\lesssim 30\ \mu s$	15 kRad	$4{\cdot}10^{11}$ n_{eq}/cm^2	30°C	$<$ 100 mW/cm^2	$\sim$ 10 m^2

DEPFET

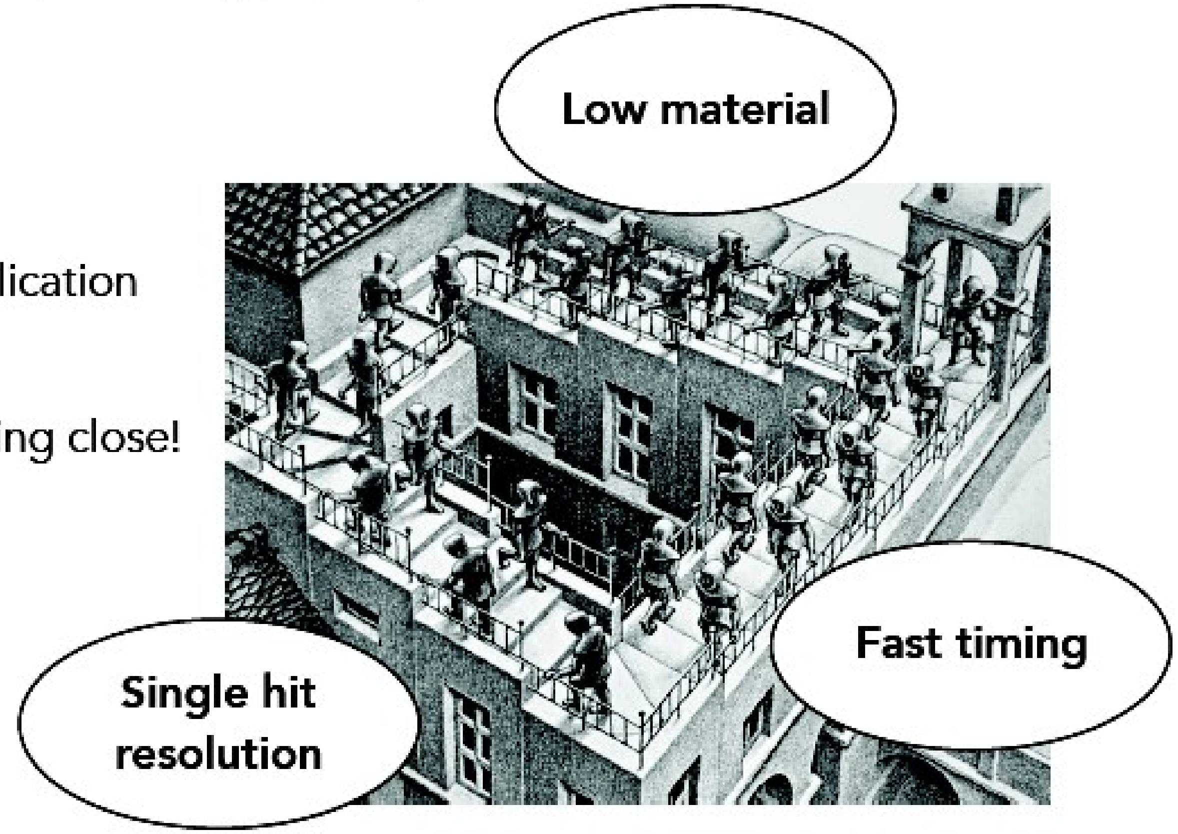
Active Pixel Detector

CMOS MAPs

CMOS adopted by large number of groups, including CLIC pixel group

Thank you for your attention!

- For CLIC, current focus is on pixel R&D
  - Highly granular, low mass pixel tracker using monolithic sensors (~ 30 µm x 300 µm pixels)
  - Hybrid pixel detector for the vertex still the most likely option (~ 25 µm x 25 µm pixels)
- Keep a close eye on CMOS processing developments
  - Huge proliferation of CMOS technologies
  - All heading in the same direction, but different focus for each application
  - Take advantage of work by many collaborations
  - Exact requirements still not met with current assemblies - but getting close!
- Next R&D steps:
  - Production of a prototype monolithic chip for the CLIC tracker
  - Testing of 2nd generation capacitively coupled assemblies



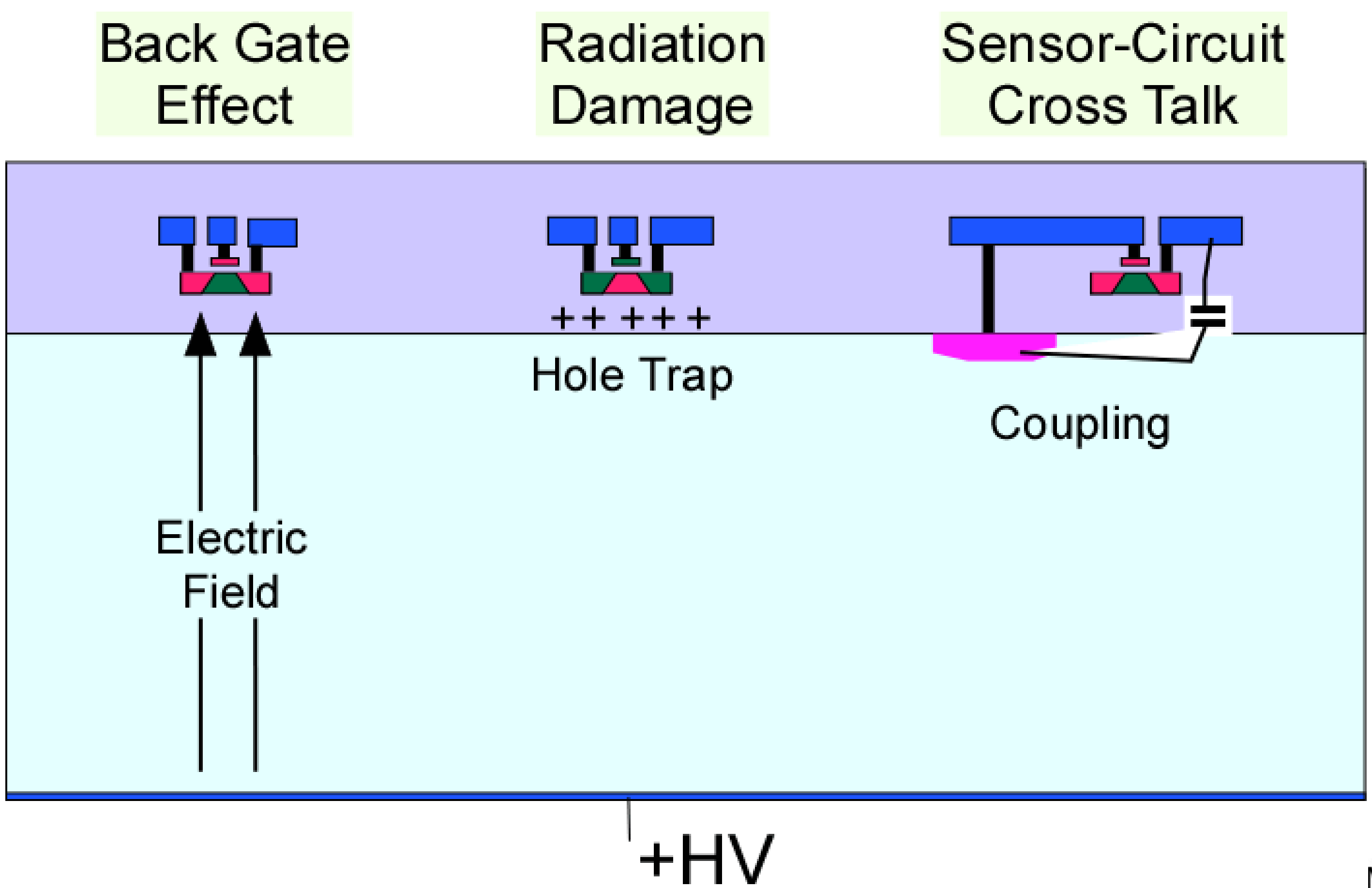
Daniel Hynds

Marcel.Vos@ific.uv.es

Contributions by Marek Idzik, Manabu Togawa, Hongbo Zhu

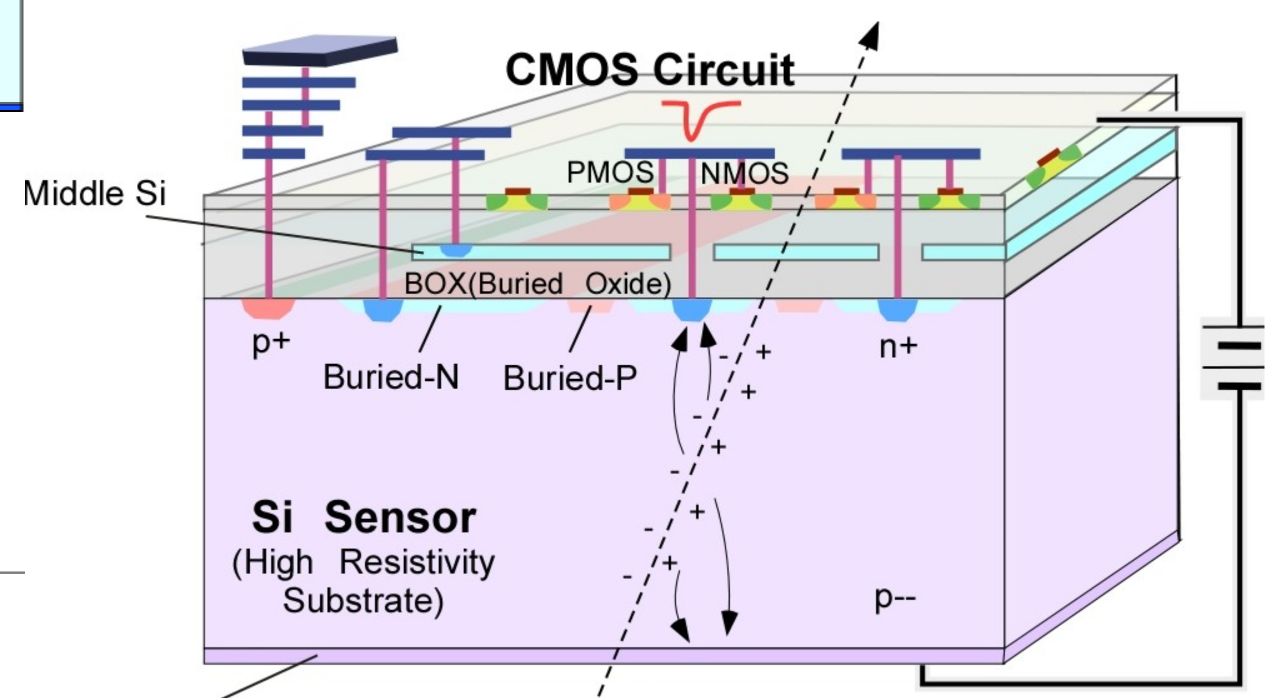
SOI

SOI renaissance. Japanese, Chinese and European groups very actively pursuing this technology for future e^+e^- colliders.



Problems: transistor operation affected by back-gate effect, signal cross-talk and charge trapped in Oxide.
All these issues are solved by introducing additional conductive layer under the transistors (Double SOI), Arai, LCWS16

Lapis (formerly OKI) 0.2 µm double-CMOS process

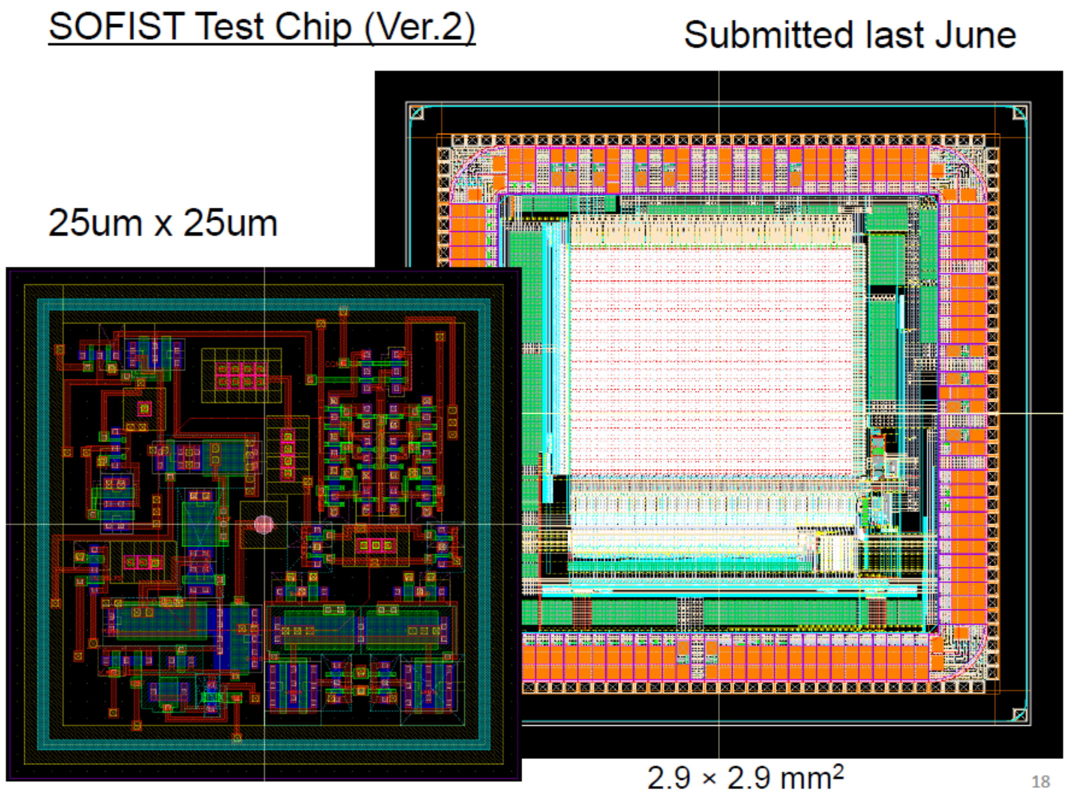


SOI

SOFIST (KEK), fully depleted sensor with full functionality in 25 x 25 μm^2 pixel (including time stamp)

2.9 x 2.9 mm^2 chip, 1 mm^2 pixel matrix

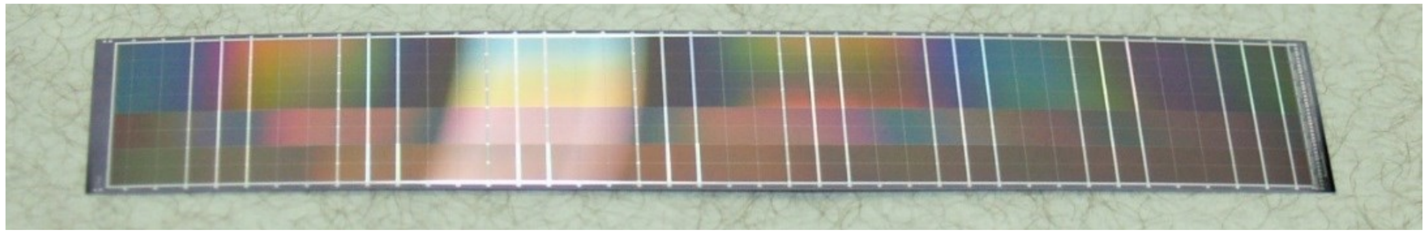
S/N ratio ~ 370 for 500 μm sensor



FPCCD

CCDs with extremely small pixels (5 x 5 μm^2):

– granularity makes up for relatively slow read-out

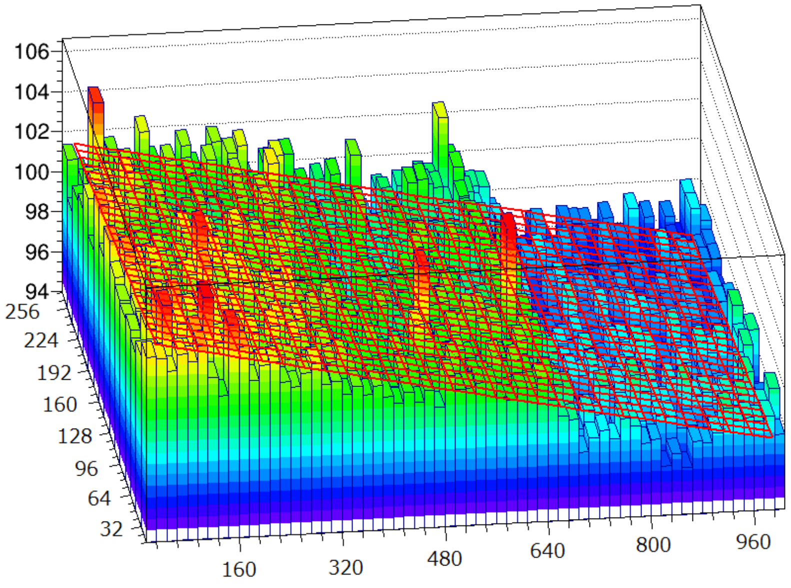


Fabricated by Hamamatsu Photonics, tested at KEK/Tohoku

Cryogenic operation (-40^o C) required to reduce dark current → active (CO_2) cooling system

Non-ionizing radiation affects Charge Transfer Inefficiency → neutron irradiation to 2 x 10^{10} n_{eq}/cm^2 yields CTI ~ 6 x 10^{-5}

Can be improved by factor 9 by filling traps (LED illumination) → enough for 3-years at 250 GeV



R&D time line

It's still a long time before the ILC experiments install their vertex detector

Technology choice around 2025

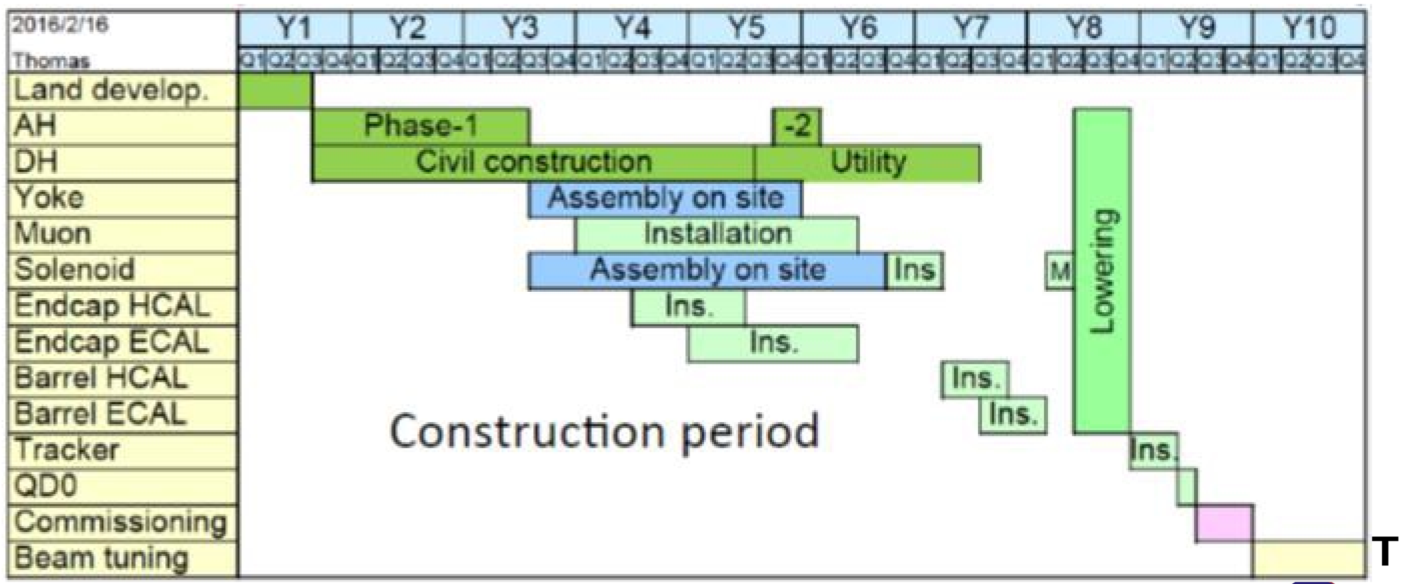
(shoot-out or combination of different technologies)

Emerging technologies have plenty of time to mature

Auguste Besson

–Reverse Calendar:

- Data taking: ~2030-32
- Commissionning / beam tuning ~ 1 year ?
- Integration and vertex detector construction ~ 1- 2 years ?
- chip prototyping/validation/production ~ 2 years
- Technology choice : ~ 2025 ?
- Define the procedure/criteria to chose the technology: several years before ? ~ 2023 ?

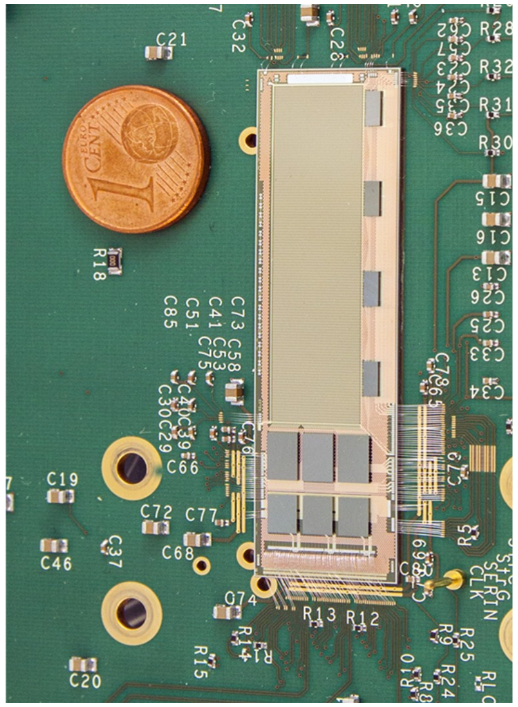


DEPFET time-line

"Early days"

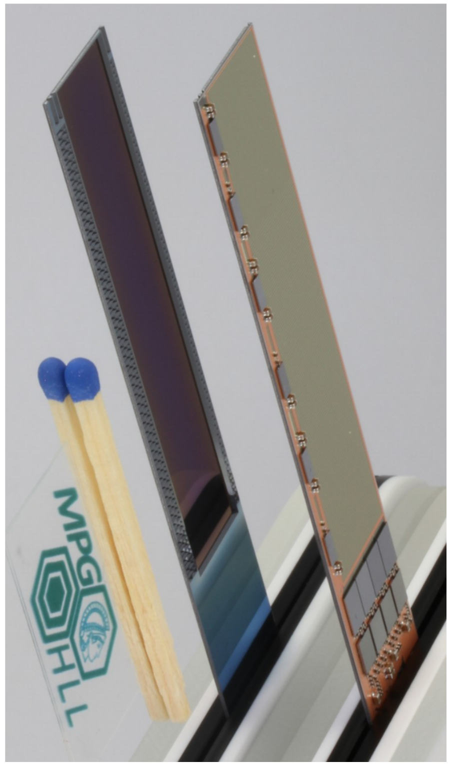
2007-2011 prototypes with O(10^3-10^4) pixels

"The most complex piece of silicon in the world", ECFA review



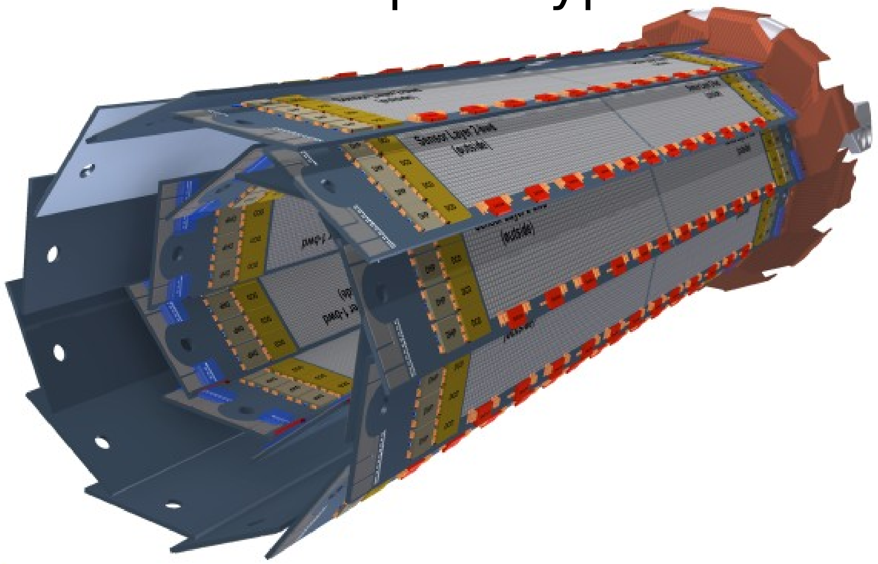
January 2014, first large-scale, multi-ASIC ladder at DESY TB

"The real thing!"



October 2015, first complete & operational Belle II ladder

The Belle II VXD
"a 30% ILC prototype"



Assembly Belle II VXD

DEPFET
Active Pixel Detector

Belle II upgrade

Proof-of-principle | Complete demonstrator | A real detector | Physics

2002.... | 2007.... | 2013 | 2014 | 2015 | 2016 | 2018 | ????

LC-specific detector

a vertex detector for TESLA

Small-pixel prototype with 1.5 µm resolution

DEPFET for ILC, IEEE TNS 60, 2, 2

ECFA review: http://ific.uv.es/~vos/ECFA_DEPFET.pdf

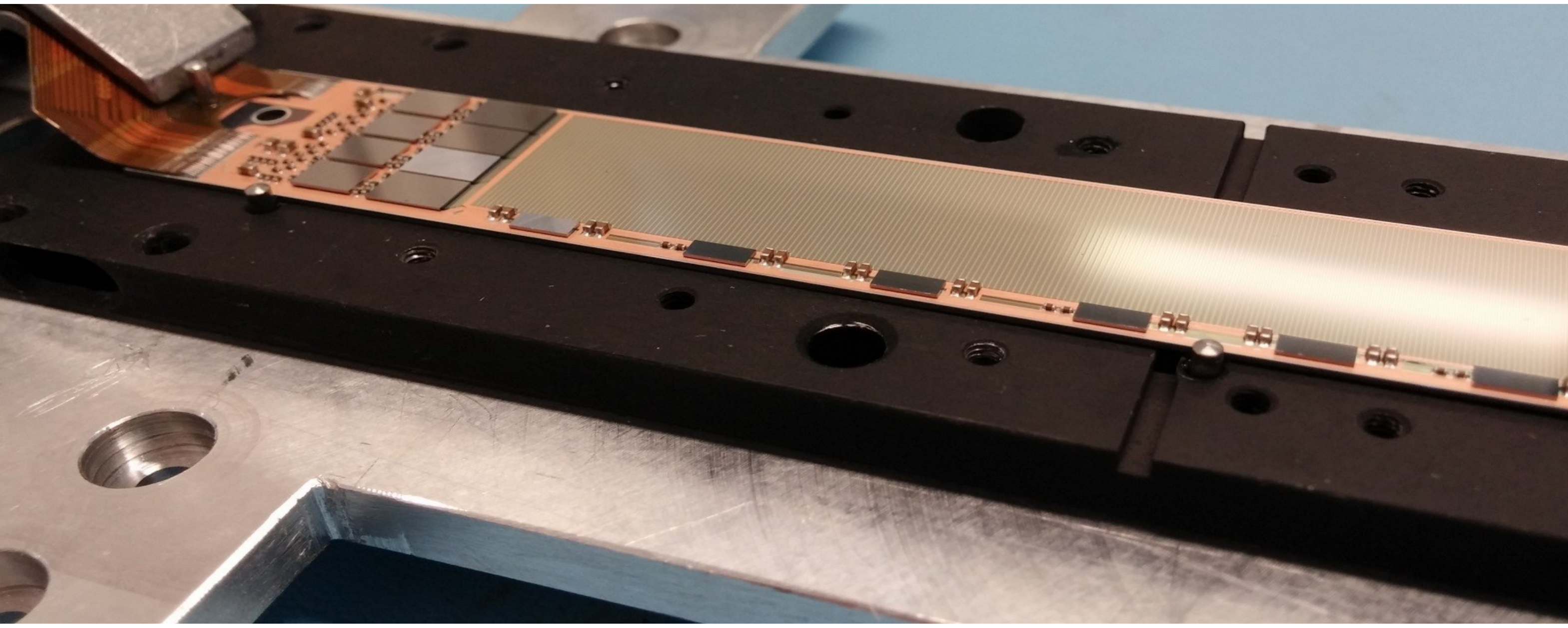
ILC candidacy benefits from developments for Belle-II

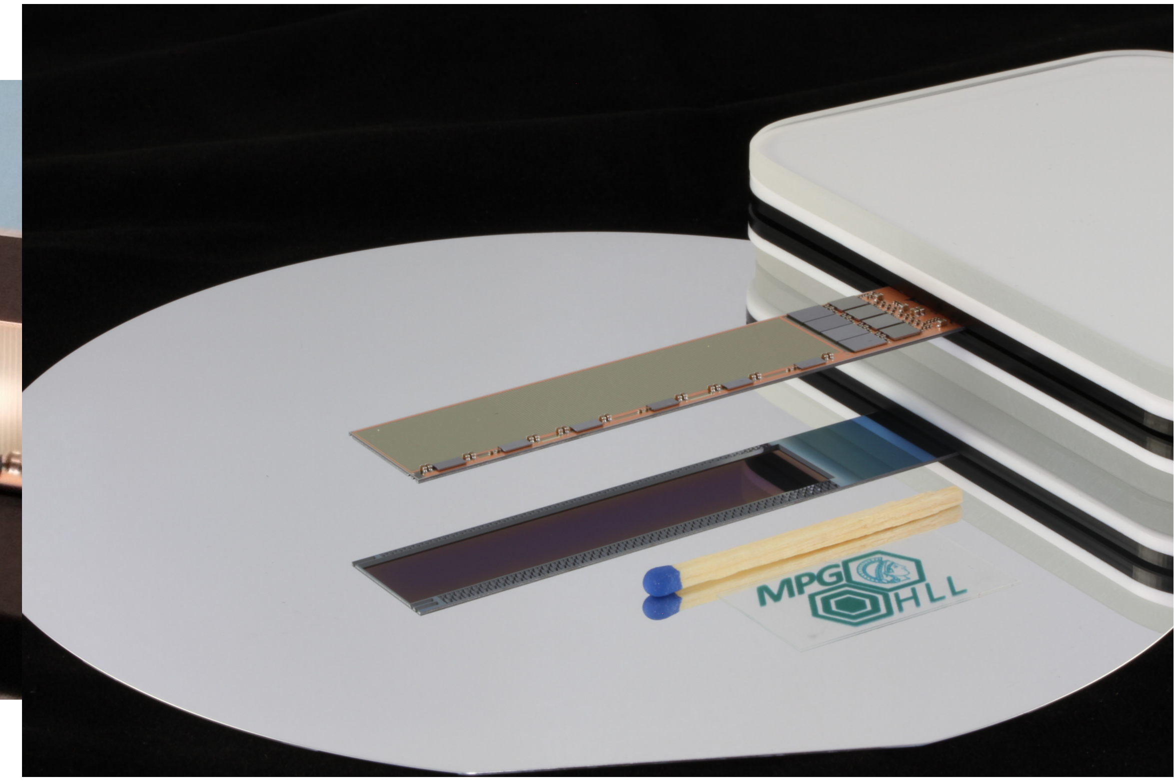
DEPFET
Active Pixel Detector

DEPFET beyond Belle II

Belle II PXD meets most requirements. And we know we can meet the others...

DEPFET for ILC, IEEE TNS 60, 2, 2





Can DEPFET improve further?

- smaller gate length (upgrade lithography) ---> higher g_q, less DCD power
- read-out speed (+//, +metal, faster sampling) ---> crucial
- forward coverage ---> adapt ladder to disk geometry
  ---> reduce end-of-ladder area/material
- advanced cooling (MCC) ---> especially in DC machines

Mechanics - PLUME

Joel Goldstein (Bristol)

PLUME approach

Double-sided ladder

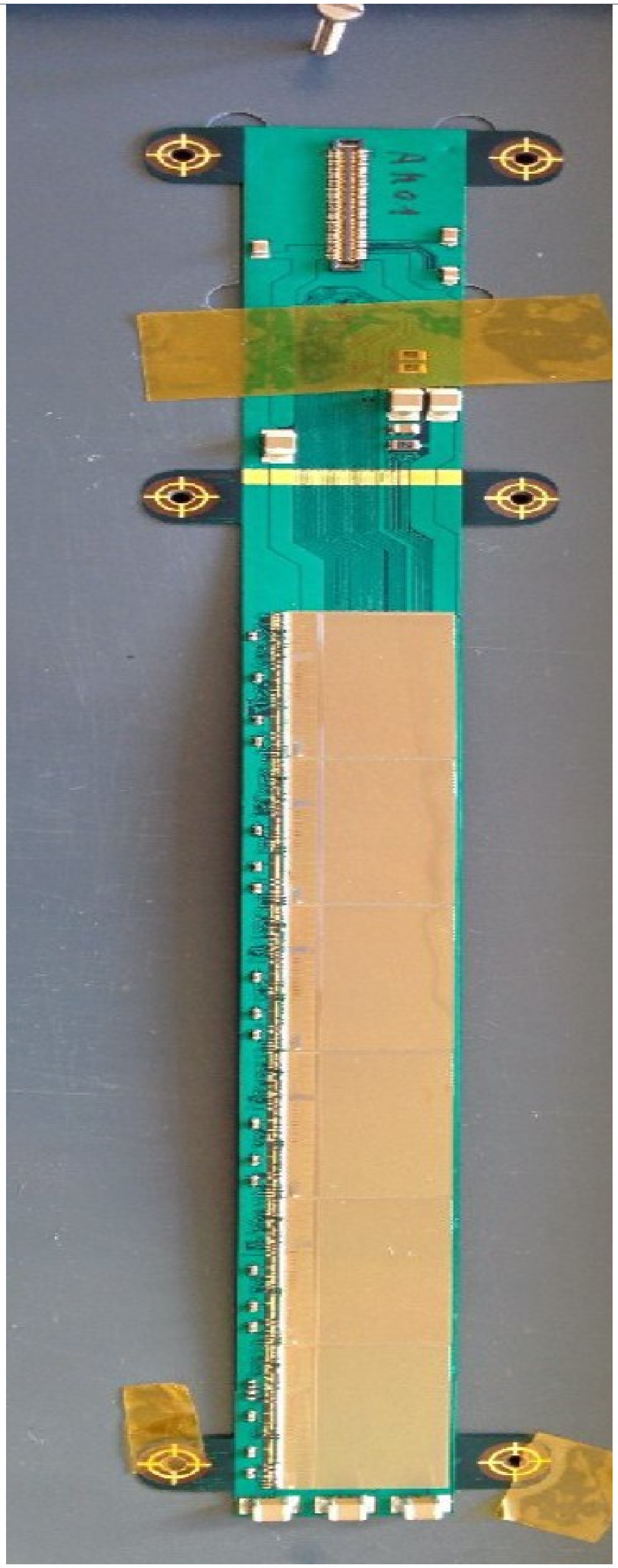
Aim for double ladders with very low material budget: 0.35 % X_0

4% SiC foam

– brittle...

Low-mass kapton

– delicate Al traces



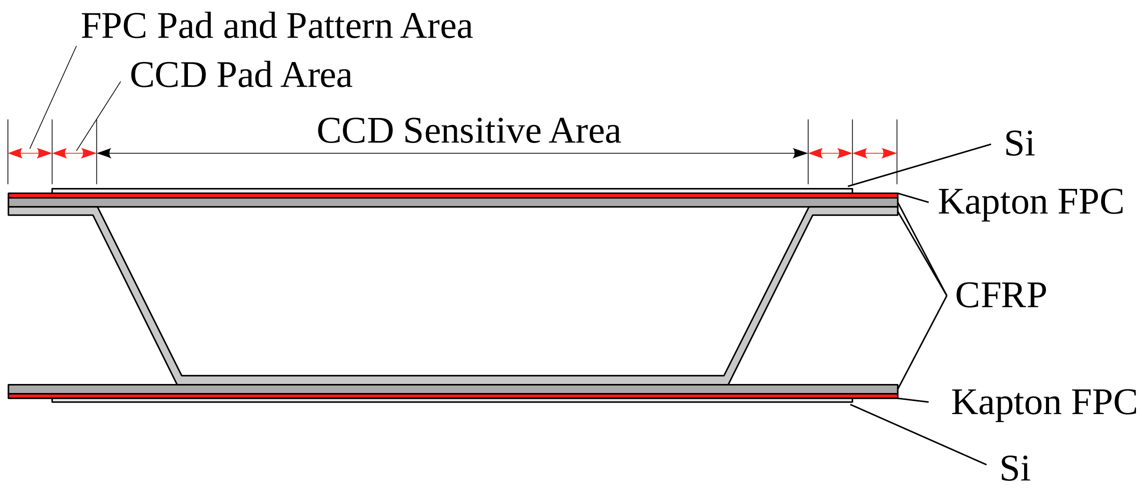
AIDA 2020

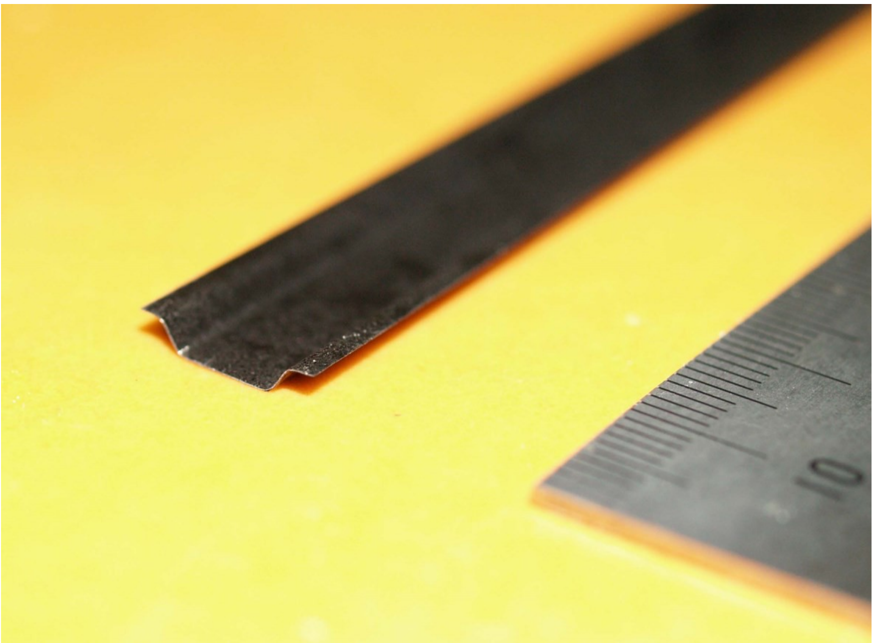
Preparing performance studies of mechanical samples at Oxford AIDA2020-Deliverable D9.6

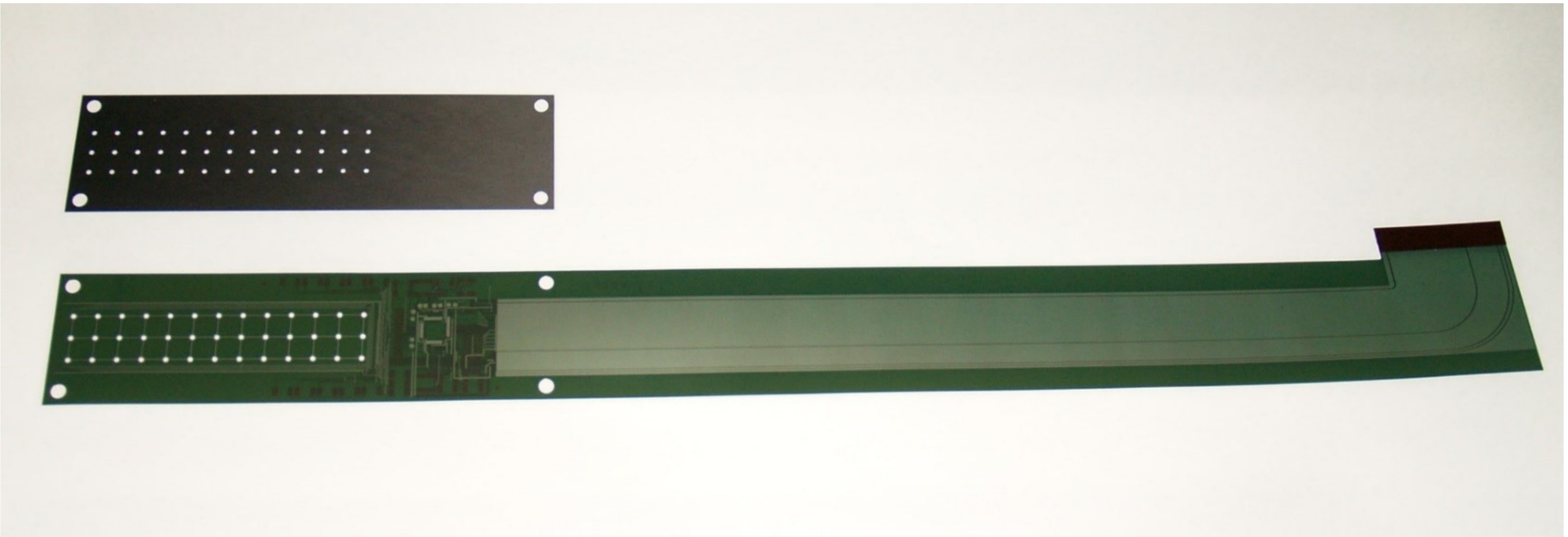
Beam tests @ DESY 2017/18
Test in a collider in 2018
(BEAST2 at SuperKEKB)

DEPFET

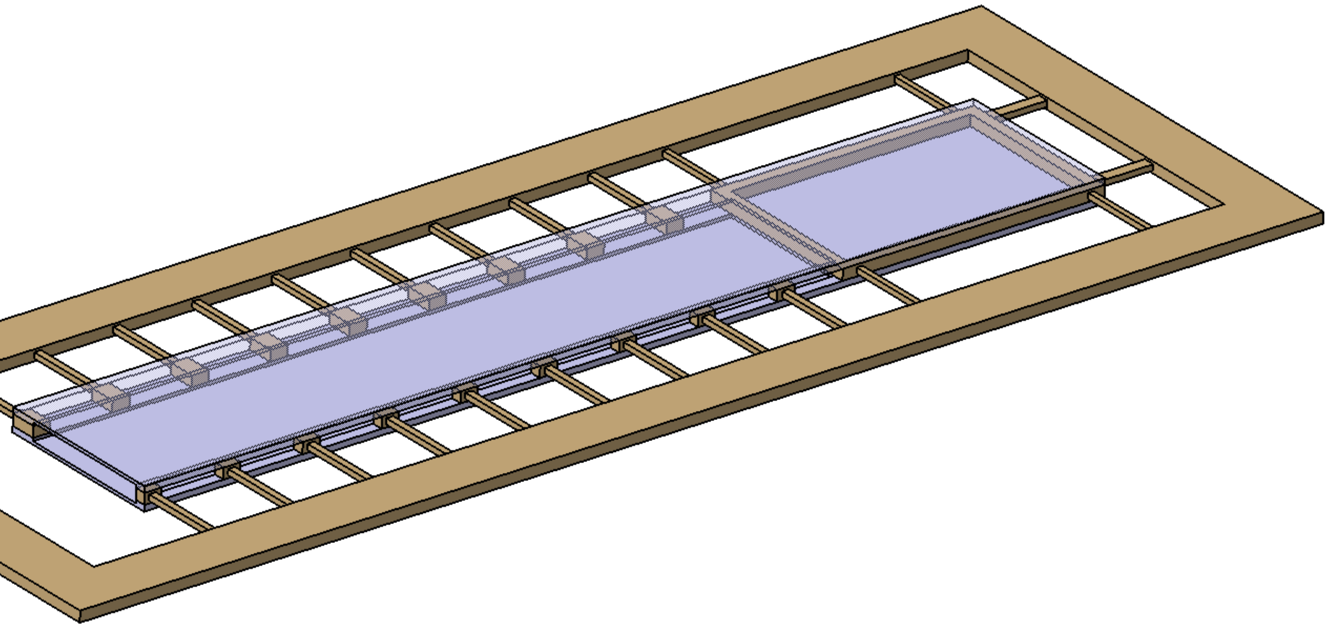
Mechanics - FPCCD





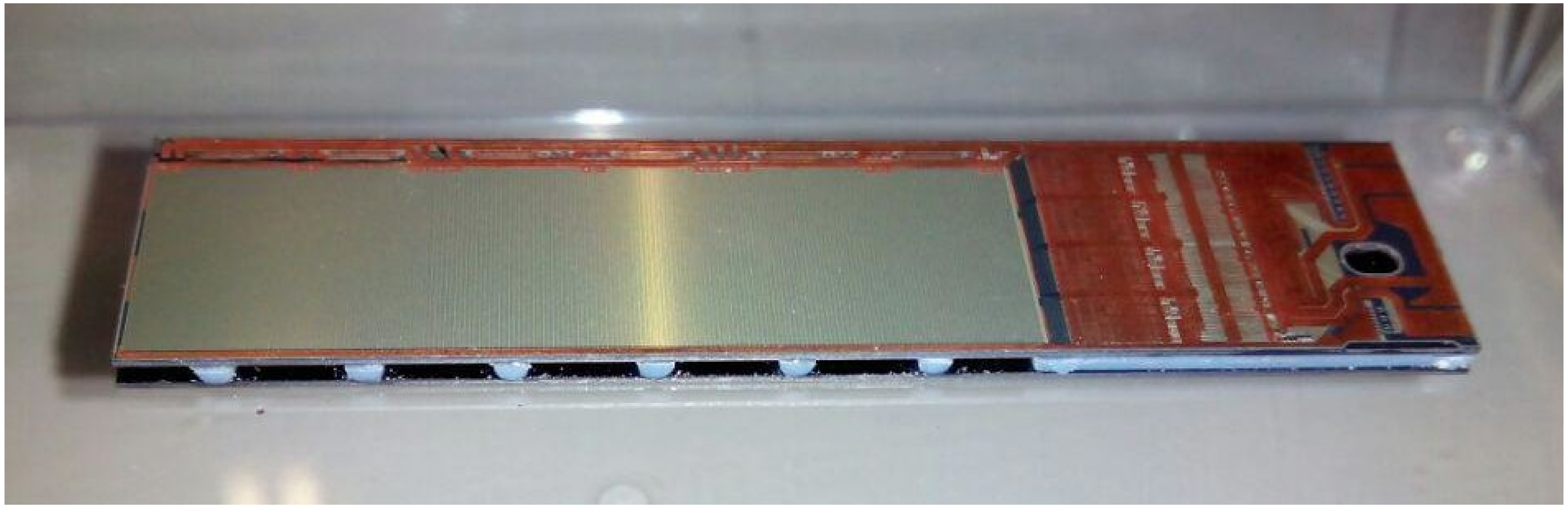


Mechanics - DEPFET

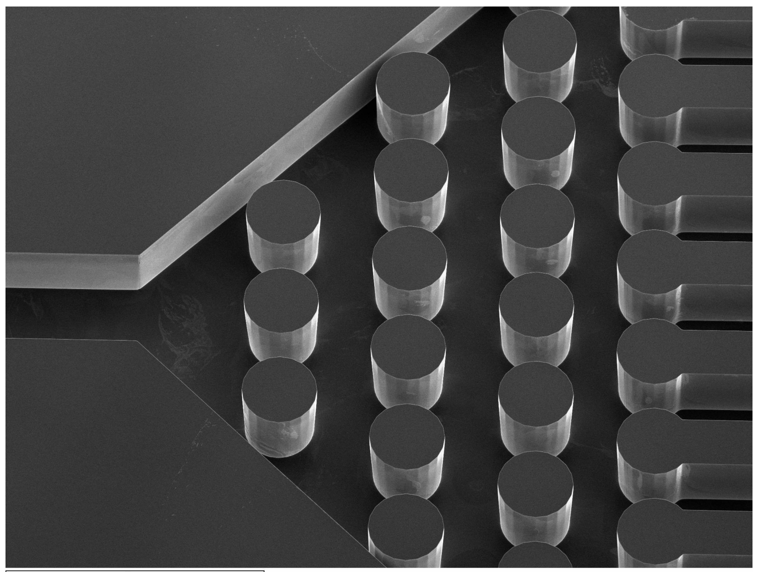


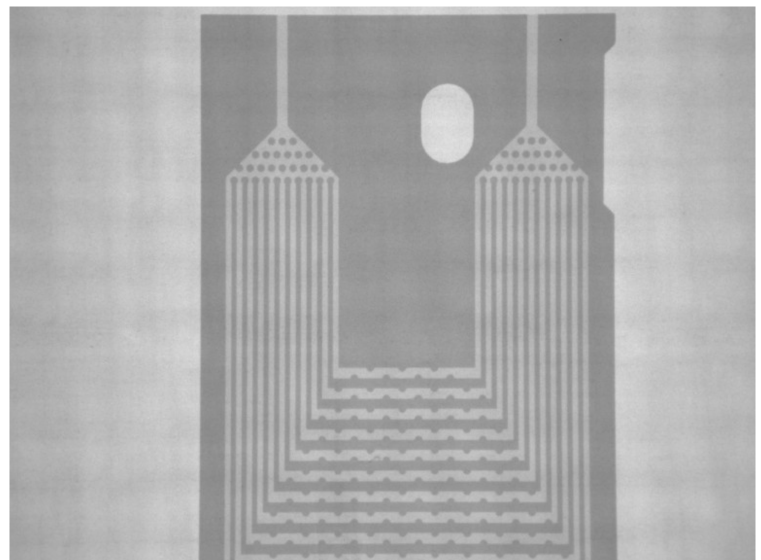
Measure mechanical performance of all-Silicon ladders in realistic environment

Double-sided ladder separated by plastic (3D printed polymer) spacer
→ negligible material (0.01% X_0)
→ increased stiffness

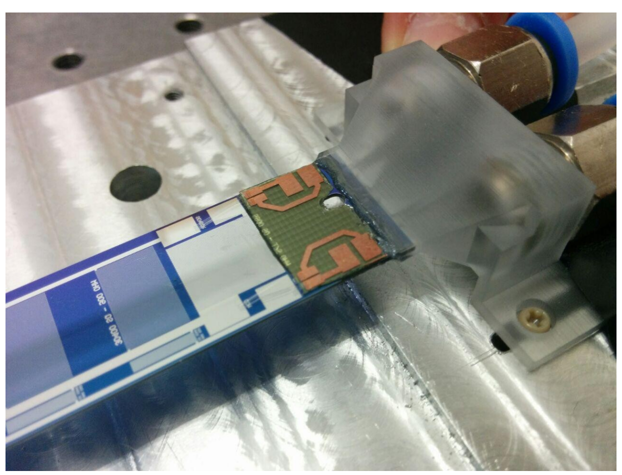


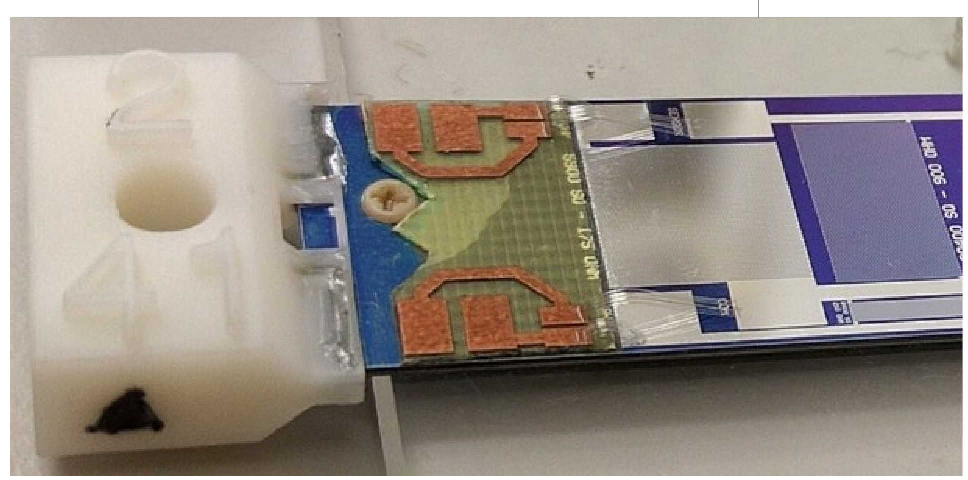
Micro-channel cooling

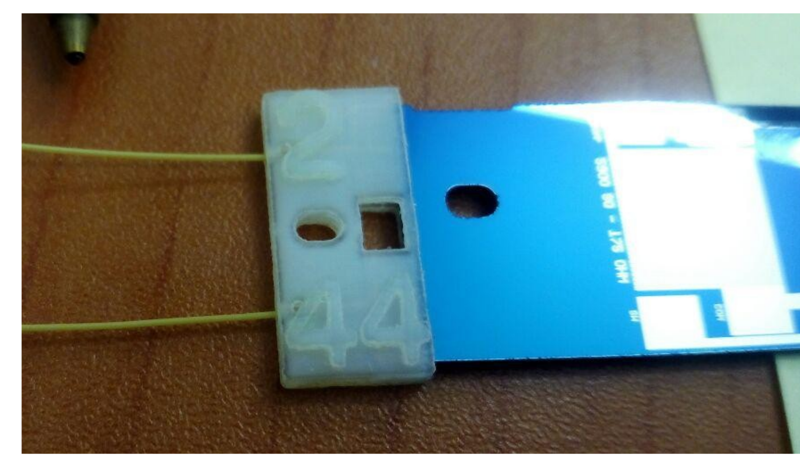




Micro-manifold before (photograph) and After wafer bonding (X-ray image) Samples produced at HLL.





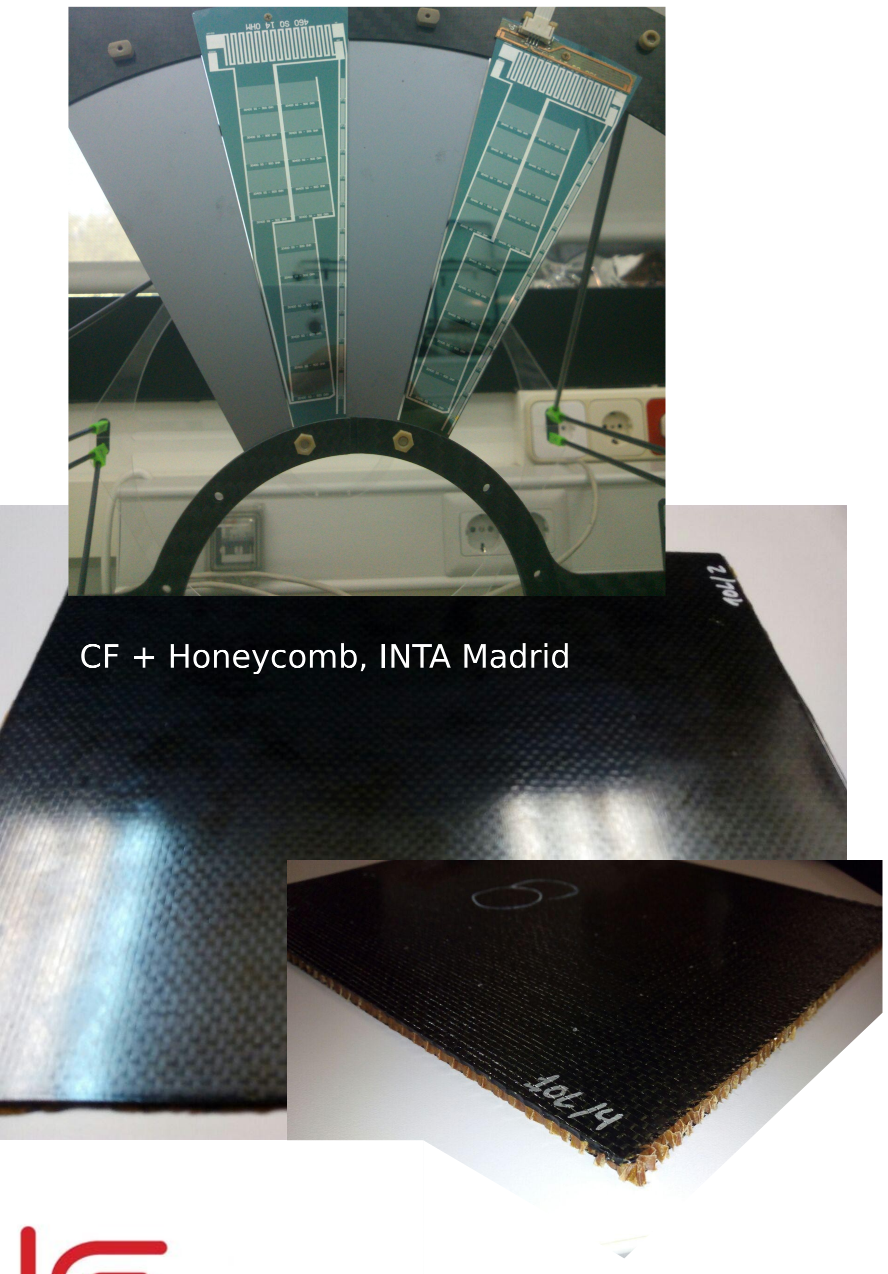


High-tech plumbing: custom, 3D-printed interfaces to commercial piping

First encouraging results: “cool 40 W with 3 l/h and ΔT = 10 K”
Published in JINST (arXiv:1604.0877)

Disk design and mock-up

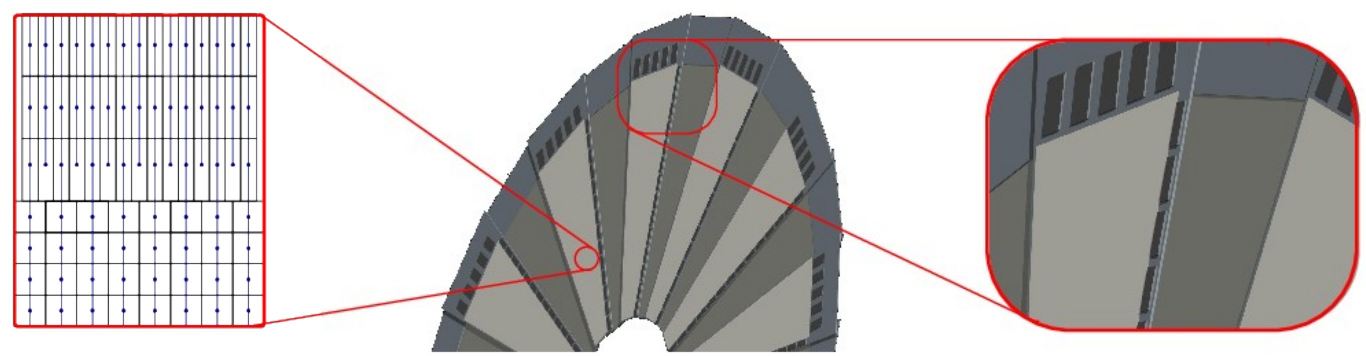
ECFA review panel: "For the ILC the main challenge is to engineer the forward tracking disk region. We recommend that the work on forward petal continues to demonstrate that petals that meet ILC requirements can be made... that more effort is made on the transition and forward regions to find a credible engineering solution , cooling and services."



CF + Honeycomb, INTA Madrid

ILC detectors extend coverage to 6 degrees

- need end-cap for vertex detector



Subject thin DEPFET petals to ILC environment:

- ILD/FTD geometry
- low-mass CF support structure
- pulsed power in heater circuits
- forced air flow for cooling (no liquid!)

And monitor thermo-mechanical properties:

- power pulsing + air flow yield adequate cooling
- deformations and vibrations under control

Up for discussion

Community is setting up an R&D "consortium" with the aim of developing the next generation of precision vertex detectors (open to linear/circular colliders, ILC/CLIC, ILD/SiD, all technologies)

PRE

14
Si
28.0855
Silicon

CE*

*Not yet agreed

DEPFET candidacy for future high-E e^+e^- collider will be strengthened by successful installation of Belle II PXD

After PXD installation + approval of proyect XXX prepare to relaunch specific R&D