

Interplay of Python Scripts, EPICS, BonnDAQ, DHH and JTAG + Examples of Application

Jochen Dingfelder, Leonard Germic, Tomasz Hemperek,
Hans Krüger, Barbara Leibrock, Florian Lütticke, Carlos Marinas,
Botho Paschen and Norbert Wermes

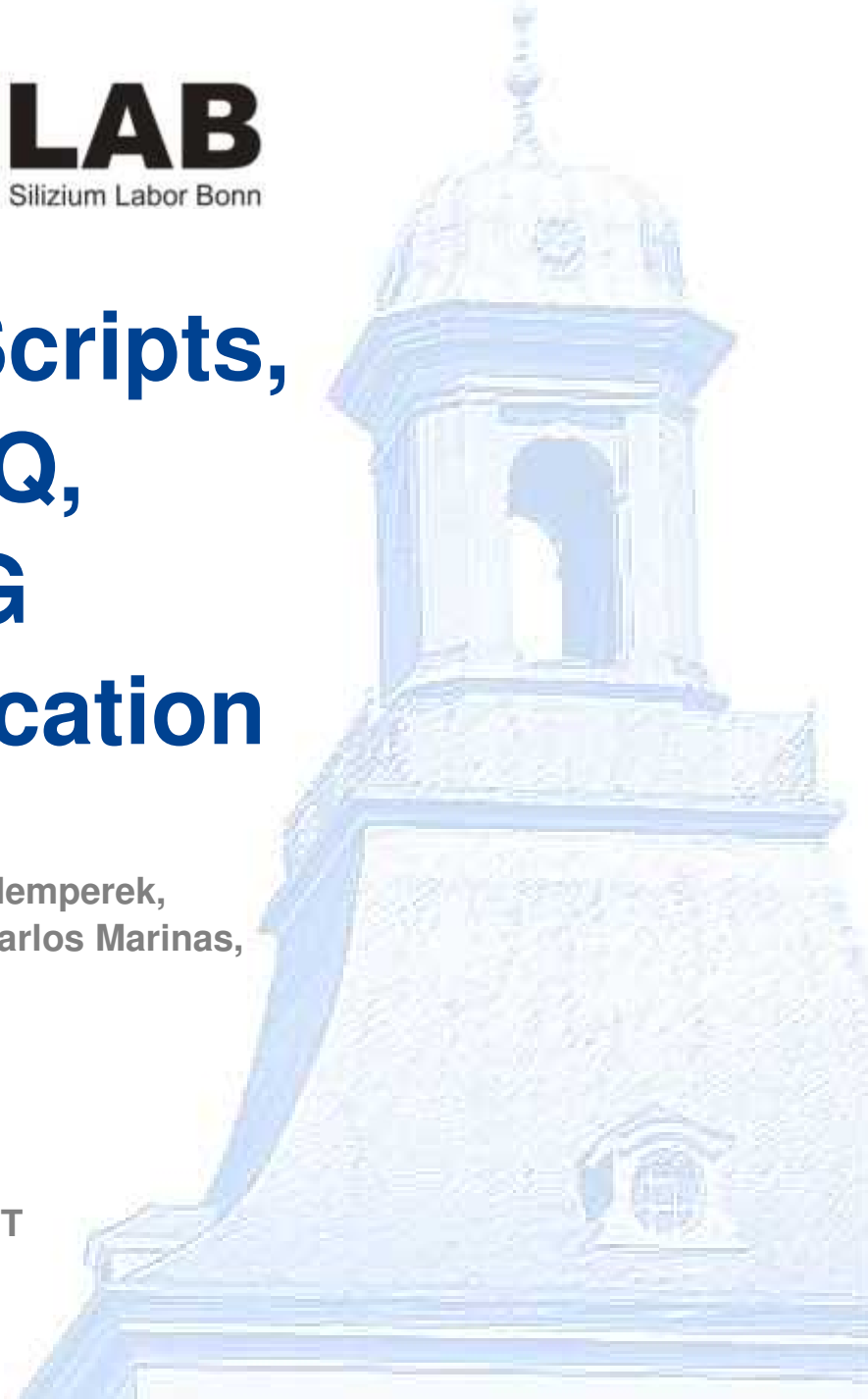
University of Bonn

DEPFET



21st International Workshop on DEPFET
Detectors and Applications

29th May 2017



Overview of the Laboratory Slow Control and two Measurements

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How does the test system work?

Test PC

???

High speed
data link

Hardware

Module
ASICs

ASIC
registers

DHP digital core

Test PC

Application
layer

Python scripts / CS-Studio

```
# enable triggering
trigger_enable = \
    get_pv("PXD:H1021:trg_en:S:set")
trigger_enable.put(1)

# check link status
link_status_pv = \
    get_pv("PXD:H1021:dhp1_channel_up:S:cur")
link_ok = link_status_pv.get()

if not link_ok:
    print("DHP link 1 is down")

# set DHP CML bias value
# and write to DHP JTAG register
get_pv(DHP, "idac_tx_bias:VALUE:set").put(200)
get_pv(DHP, "globalrs:trg:set").put(1)
```

???

Hardware

Module
ASICs

ASIC
registers

DHP digital core

High speed
data link

PXD:H1021

☒ DHP Channel Up
☒ DHP Voltage ON
☒ DHP PLL locked
☒ DHC Channel Up
☒ DHC PLL locked
☒ GTX Synchronized

☐ Enable trigger
☒ Enable GatedMode

TLU Settings

Max bits	16
TS2TUDEL	0
TS2TADEL	0
Clock slow down factor	5
Use BUSY from script	<input type="checkbox"/>

Statistics

DHP data counter	4.78442E7
DHP frame counter	730
DHP data rate	0 Bps
Trigger counter	730
Trigger rate	0
Missing triggers	0
Missing trigger rate	0

DHE Configuration: /cs-studio/dhh/inifiles/dhh_

DHP Trigger Settings

Trigger width	2048
Trigger delay	88
FCK Length	2048
Timeout	2000
FCK strobe width	5
Invert Trigger	<input type="checkbox"/>

Other settings

RXEQMIX
 TCK Divider
 use DHPT interface ☐

ASIC settings

DHP1 Settings
 DCD1 Settings
 HS: ☒ disable

Process Variables (PVs)

Test PC

Application layer

Python scripts / CS-Studio

Read/write

EPICS IOC server

Process Variables (PVs)

```
# check link status
link_status_pv = \
    get_pv("PXD:H1021:dhp1_channel_up:S:cur")
link_ok = link_status_pv.get()

if not link_ok:
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# set DHP CML bias value
# and write to DHP JTAG register
get_pv(DHP, "idac_tx_bias:VALUE:set").put(200)
get_pv(DHP, "globalrs:trg:set").put(1)
```

???

High speed data link

Hardware

Module ASICs

ASIC registers

DHP digital core

PXD:H1021

Config Busy: ☐ Status: ☒ reset configure

Kill Framers

Short RST PowerUp scripts Config

Long RST Configure DHE 76.23 M

DHE Configuration: /cs-studio/dhh/inifiles/dhh_

DHP Trigger Settings

Trigger width 2048

Trigger delay 88

FCK Length 2048

Timeout 2000

FCK strobe width 5

Invert Trigger ☐

Other settings

RXEQMIX 3

TCK Divider 50

use DHPT interface ☒ mer Dur

ASIC settings

DHP1 Settings DCD1 Settings HS: ☒ disable

TLU Settings

Max bits 16

TS2TUDEL 0

TS2TADEL 0

Clock slow down factor 5

Use BUSY from script ☐

Statistics

DHP data counter 4.78442E7

DHP frame counter 730

DHP data rate 0 Bps

Trigger counter 730

Trigger rate 0

Missing triggers 0

Missing trigger rate 0

Enable trigger **Enable GatedMode**

DHP Channel Up

DHP Voltage ON

DHP PLL locked

DHC Channel Up

DHC PLL locked

GTX Synchronized

The Data Handling Engine (DHE)

Test PC

Application
layer

Python scripts / CS-Studio

Read/write

EPICS IOC
server

Process Variables (PVs)

???

Hardware

DHE

FPGA

Slow/fast
control

High speed
data link

Module
ASICs

ASIC
registers

DHP digital core

DHE ↔ module ASIC communication

Test PC

Application
layer

Python scripts / CS-Studio

Read/write

EPICS IOC
server

Process Variables (PVs)

???

Hardware

DHE

FPGA

JTAG

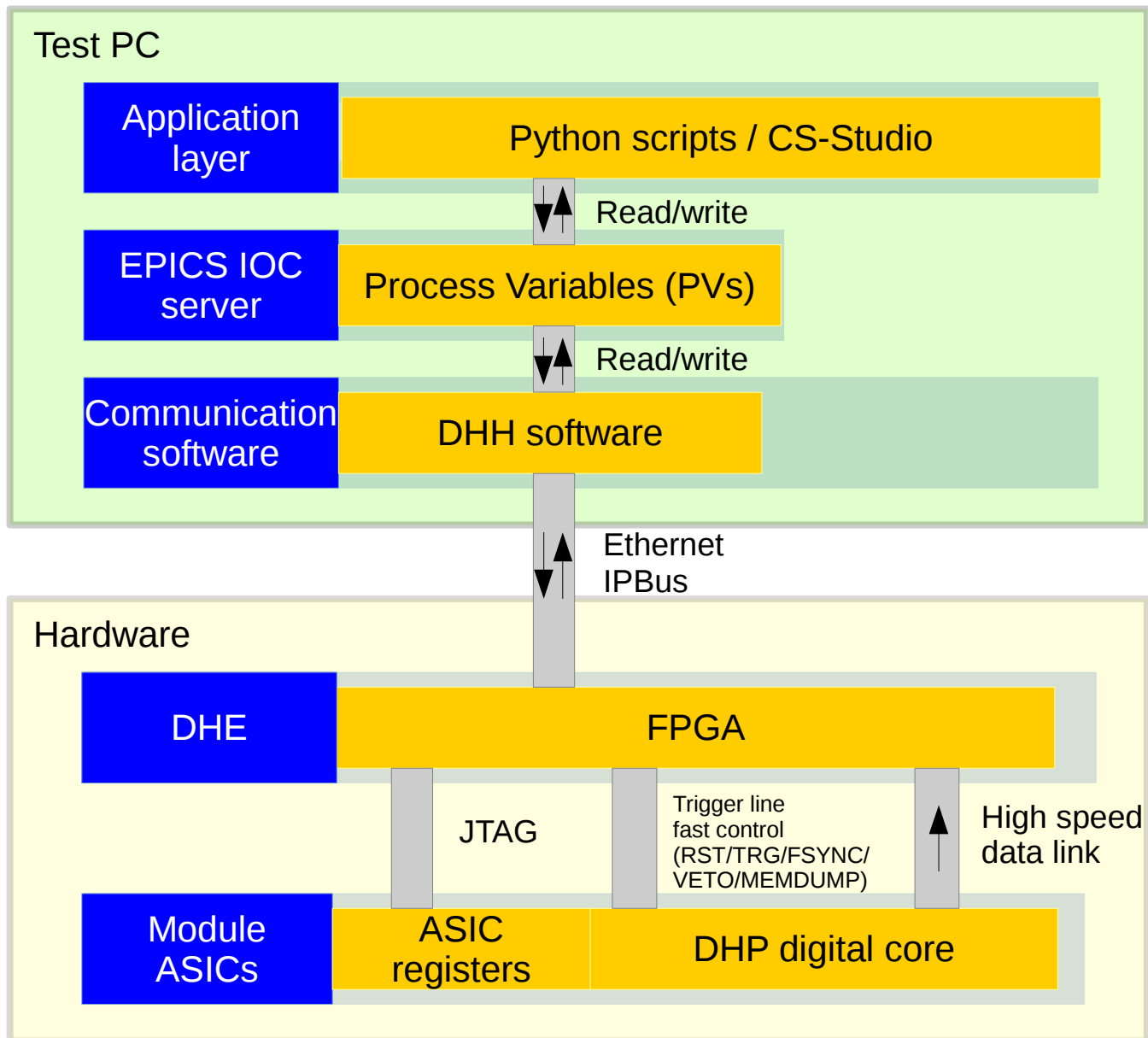
Trigger line
fast control
(RST/TRG/FSYNC/
VETO/MEMDUMP)

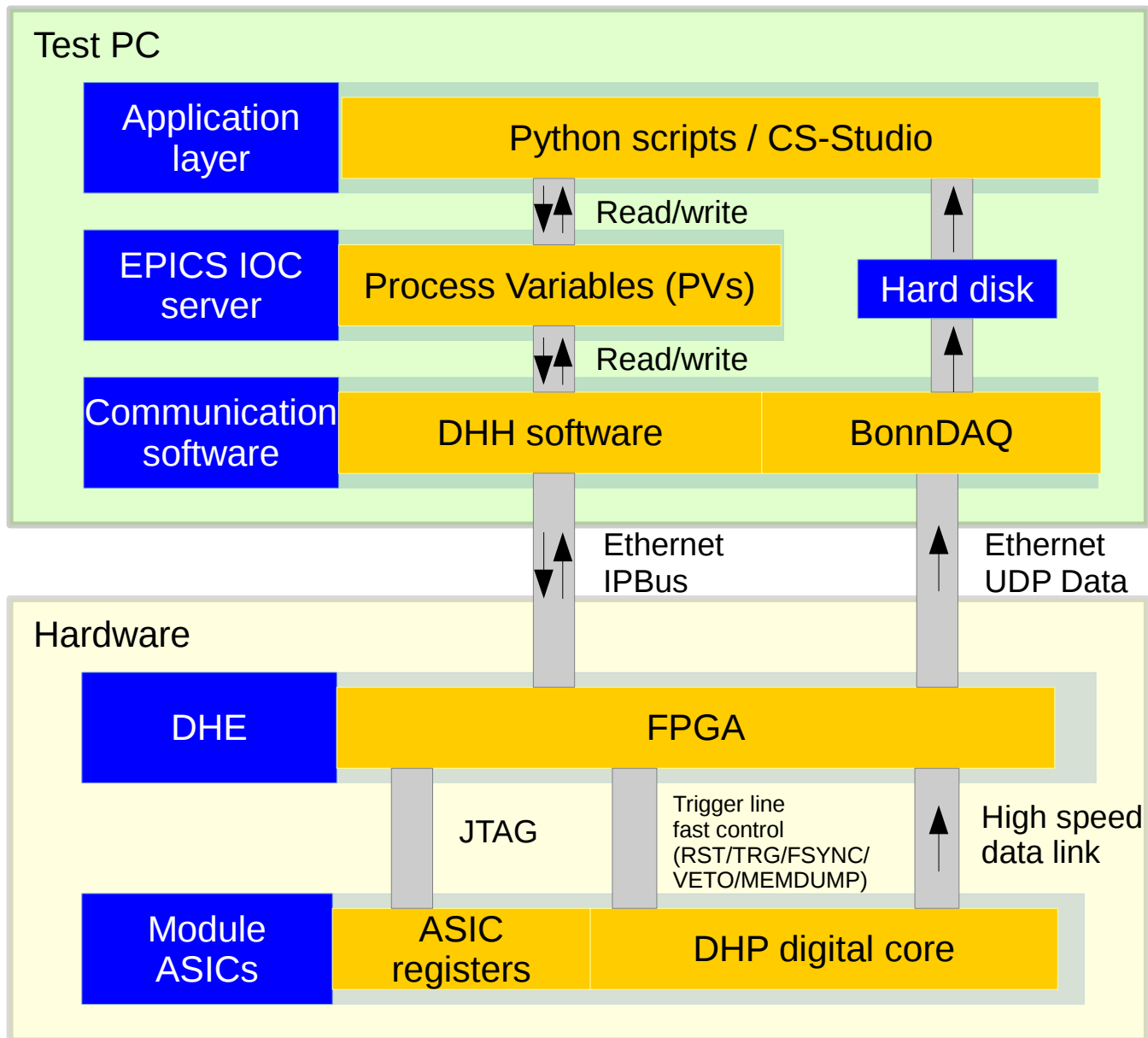
High speed
data link

Module
ASICs

ASIC
registers

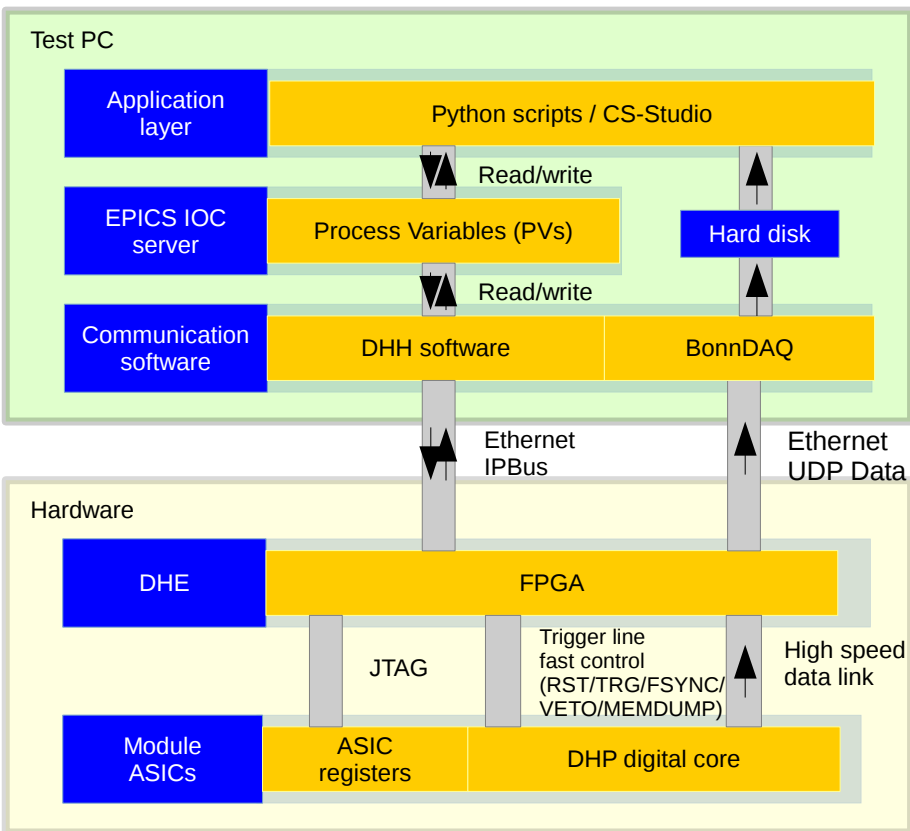
DHP digital core





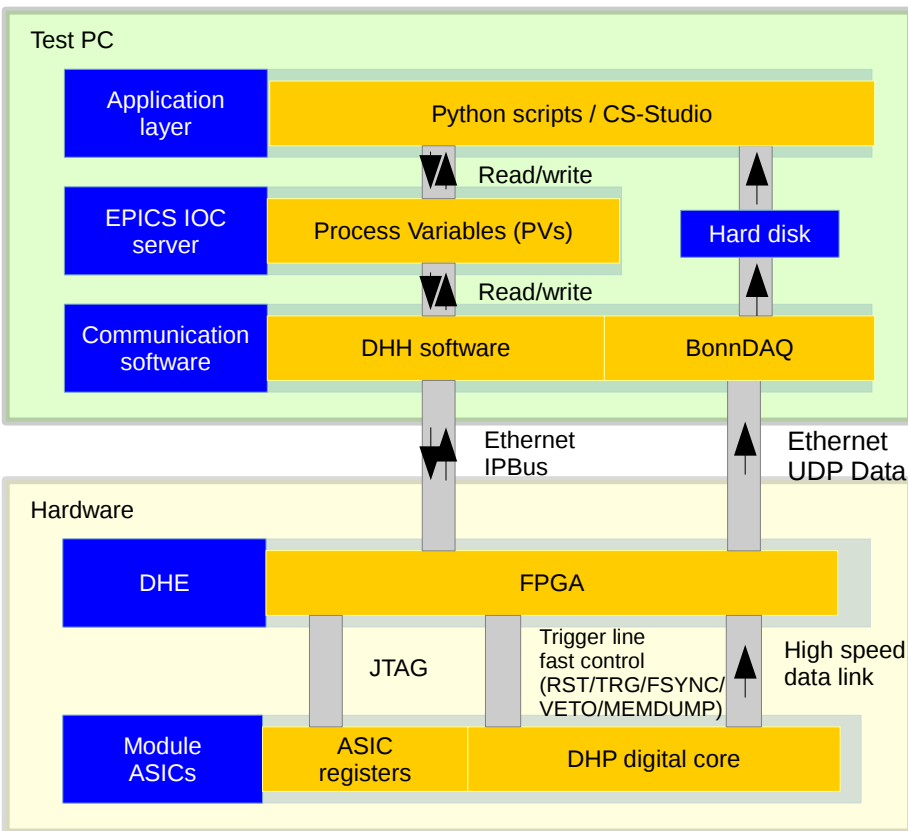
Why is it so complicated?

Laboratory Test System

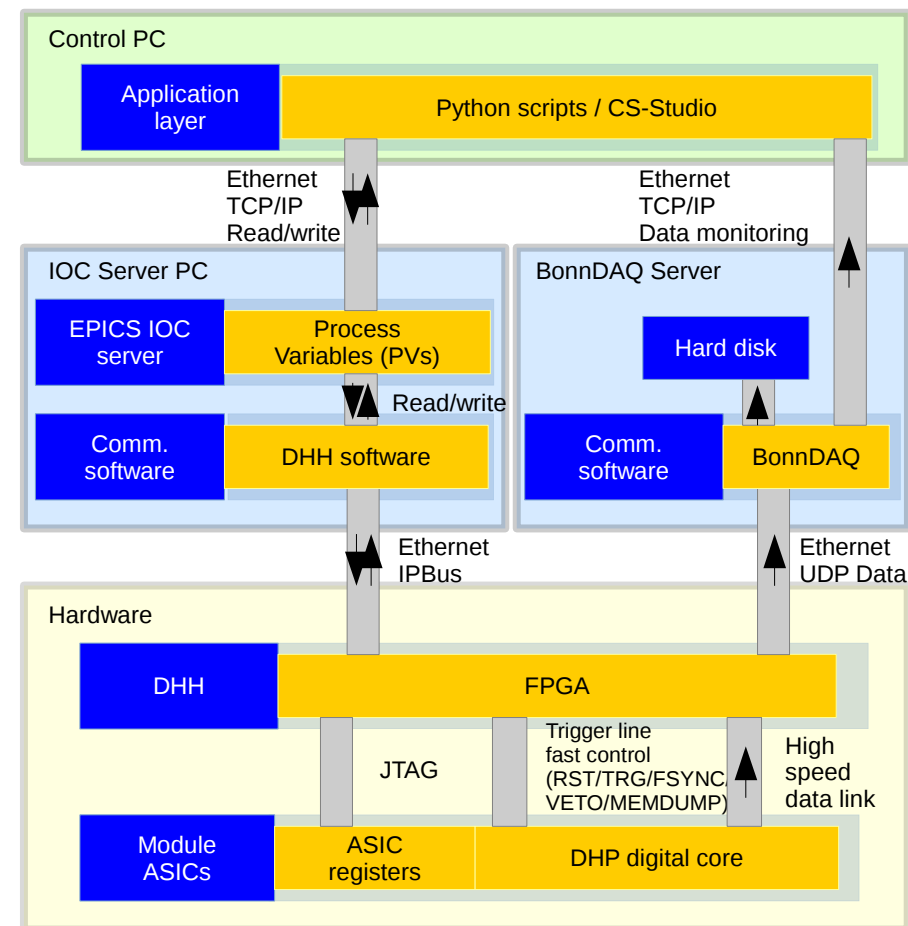


Why is it so complicated?

Laboratory Test System

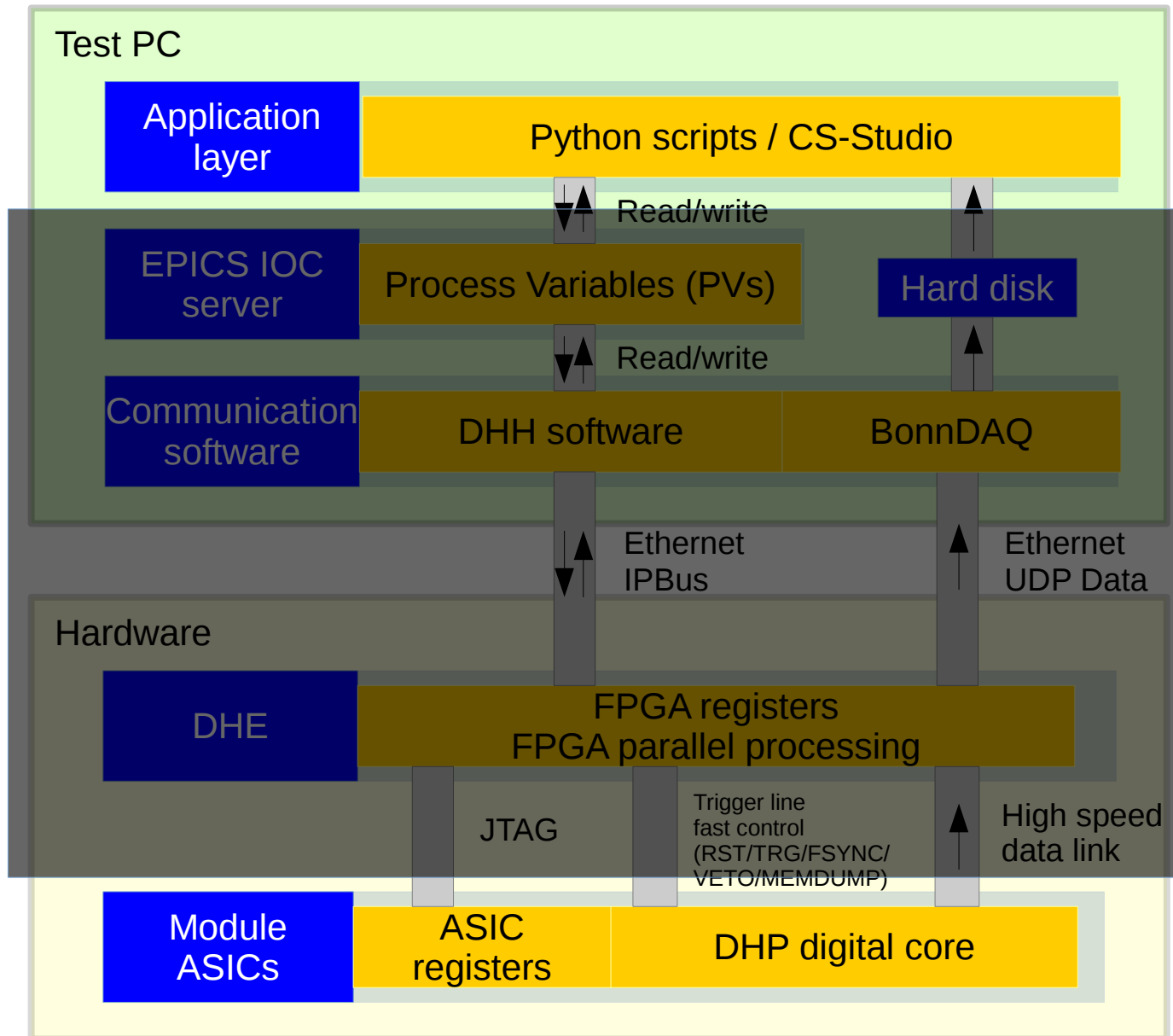


Belle II Experiment (also **PERSY**)



→ The system used for laboratory testing already implements (almost) all the elements for the final Belle II experiment.

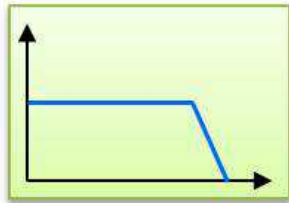
Keep track of what you're doing



- Slow control close to final state
- Can be difficult to debug in the lab environment
- Designing fast scans can be tricky

Timing pitfall – high-speed link scan

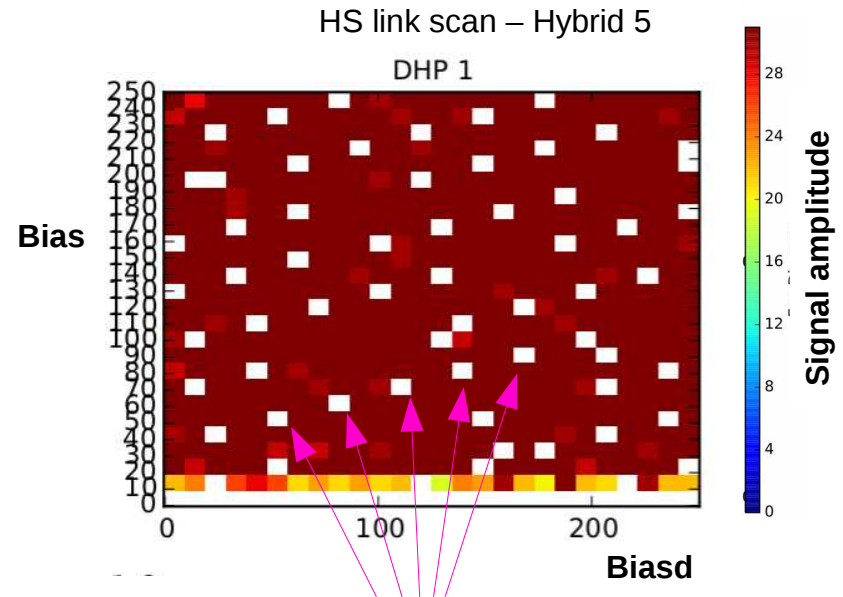
High-speed signal preemphasis



Signal spectrum



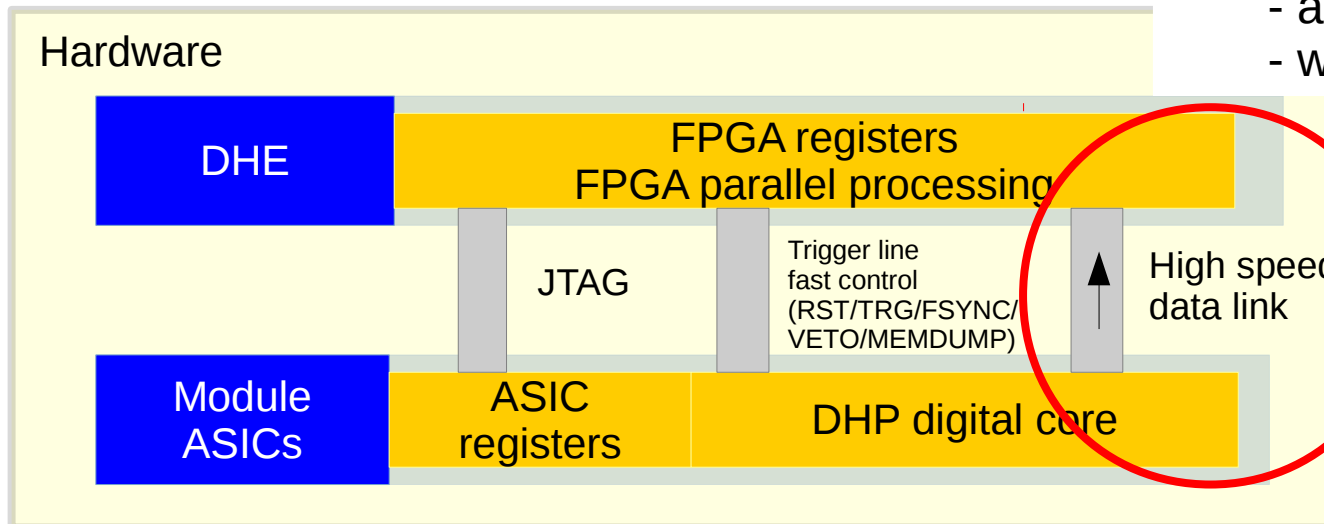
Signal spectrum after preemphasis



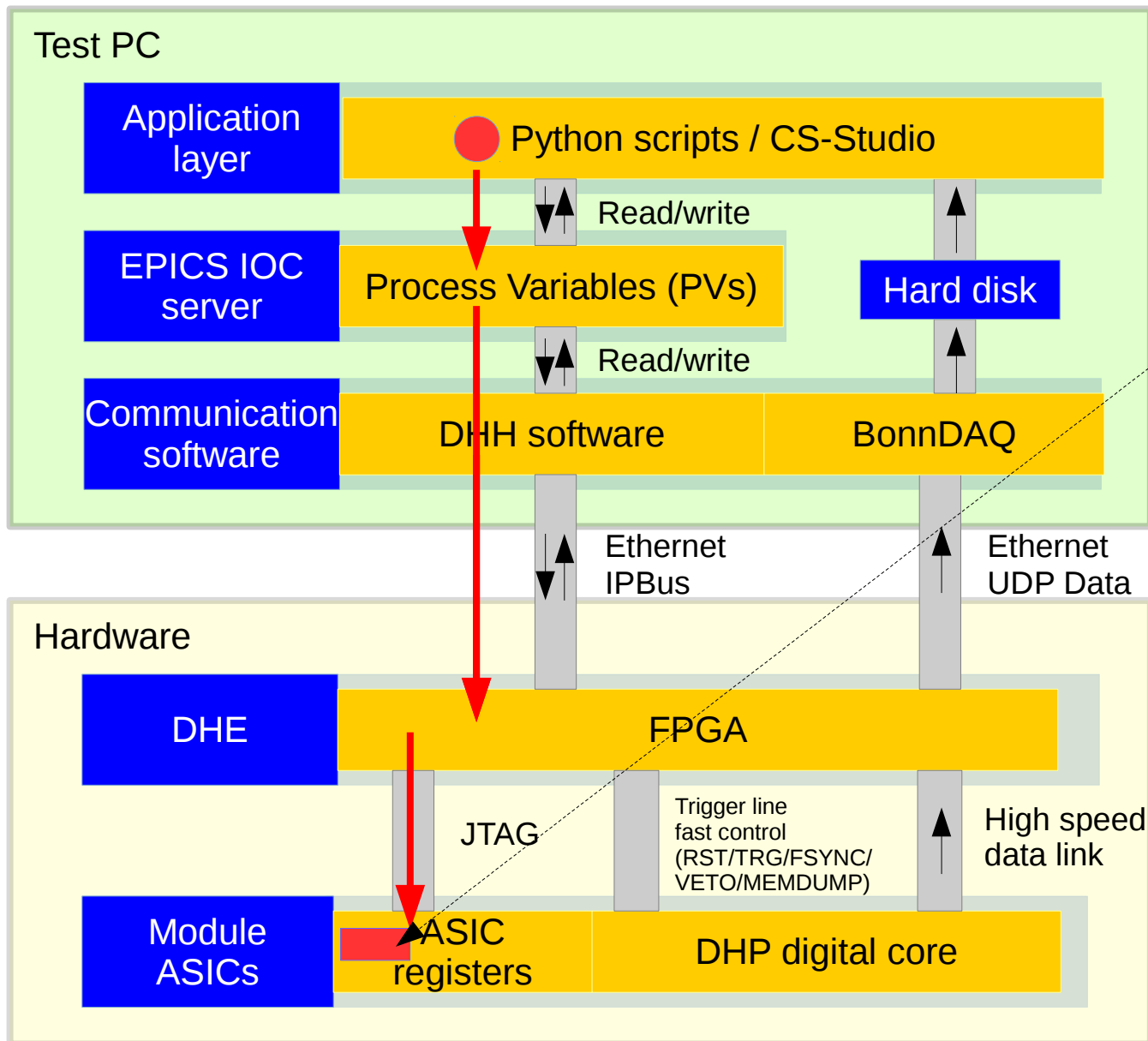
What are these “bad points”?

- are they real?
- why are they so regular?

Hardware



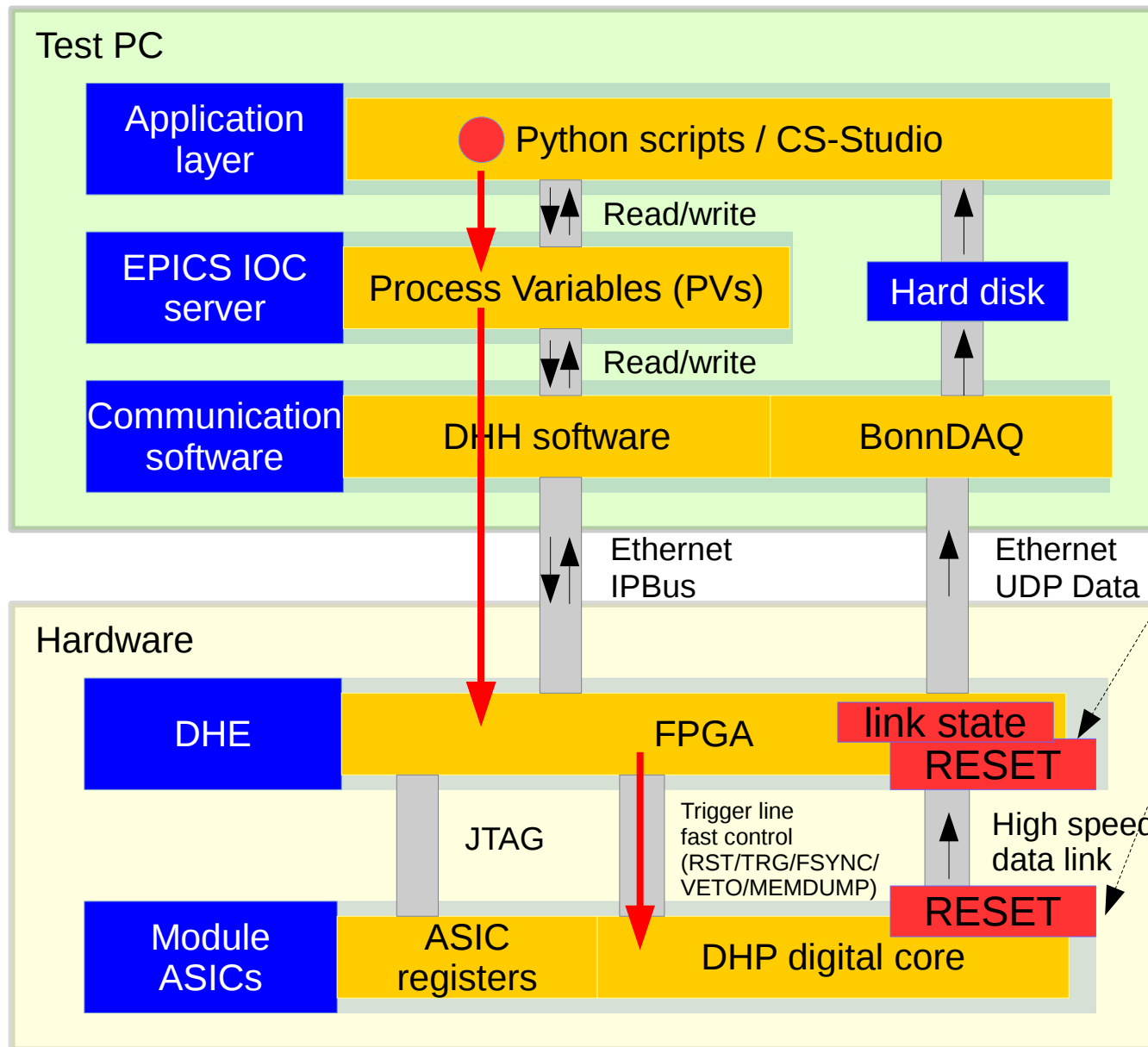
What happens during the scan



1. set pre-emphasis parameters in DHP

bias
biasd

What happens during the scan

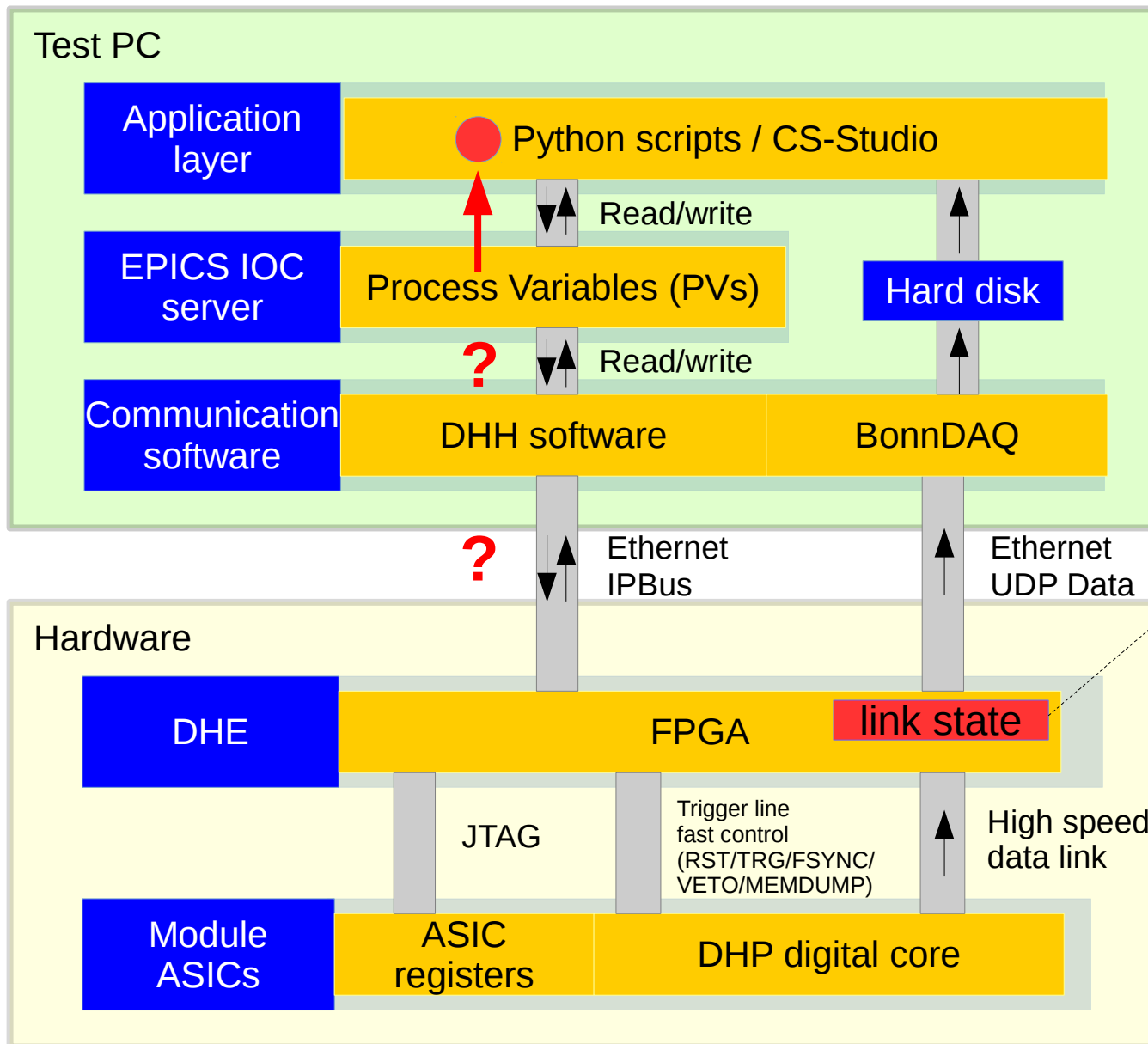


bias
biasd

1. set pre-emphasis parameters in DHP

2. issue link reset commands

What happens during the scan



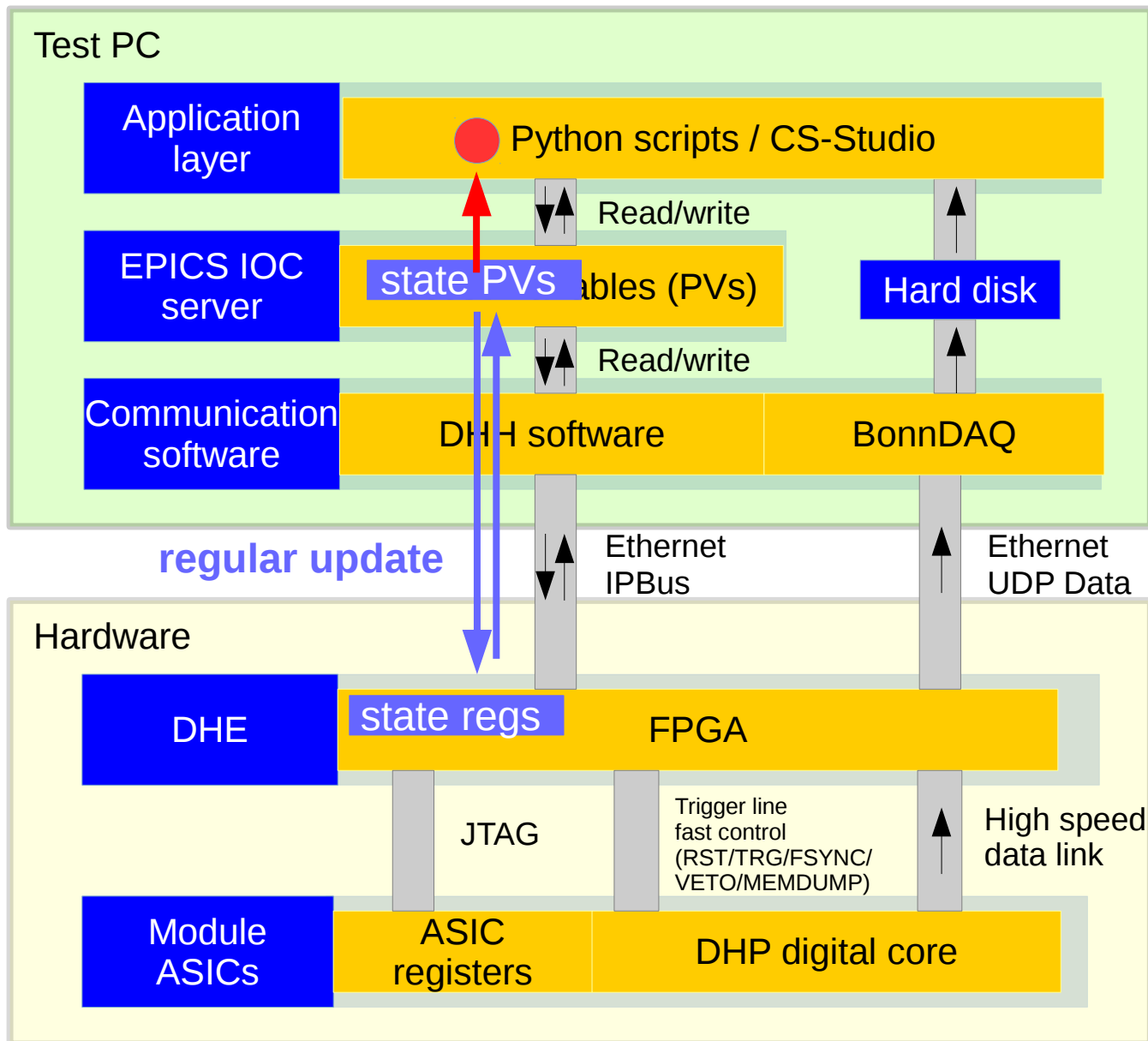
1. set pre-emphasis parameters in DHP

bias
biasd

2. issue link reset commands

3. poll link state (success?)

What happens during the scan



1. set pre-emphasis parameters in DHP

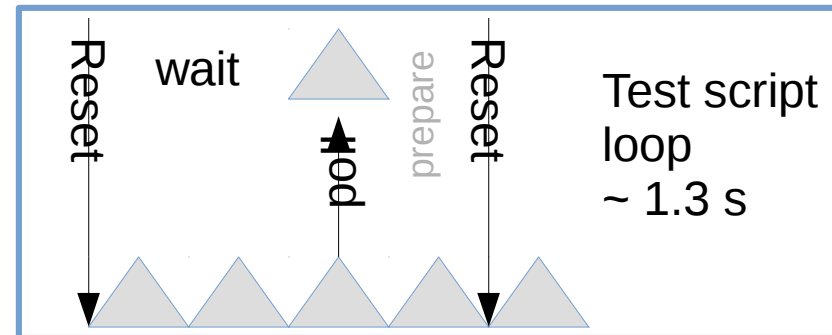
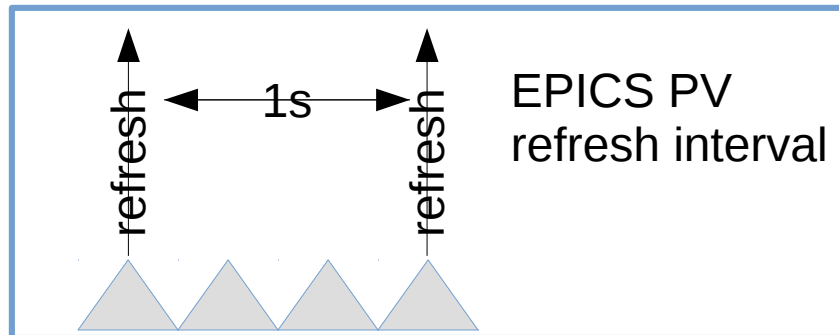
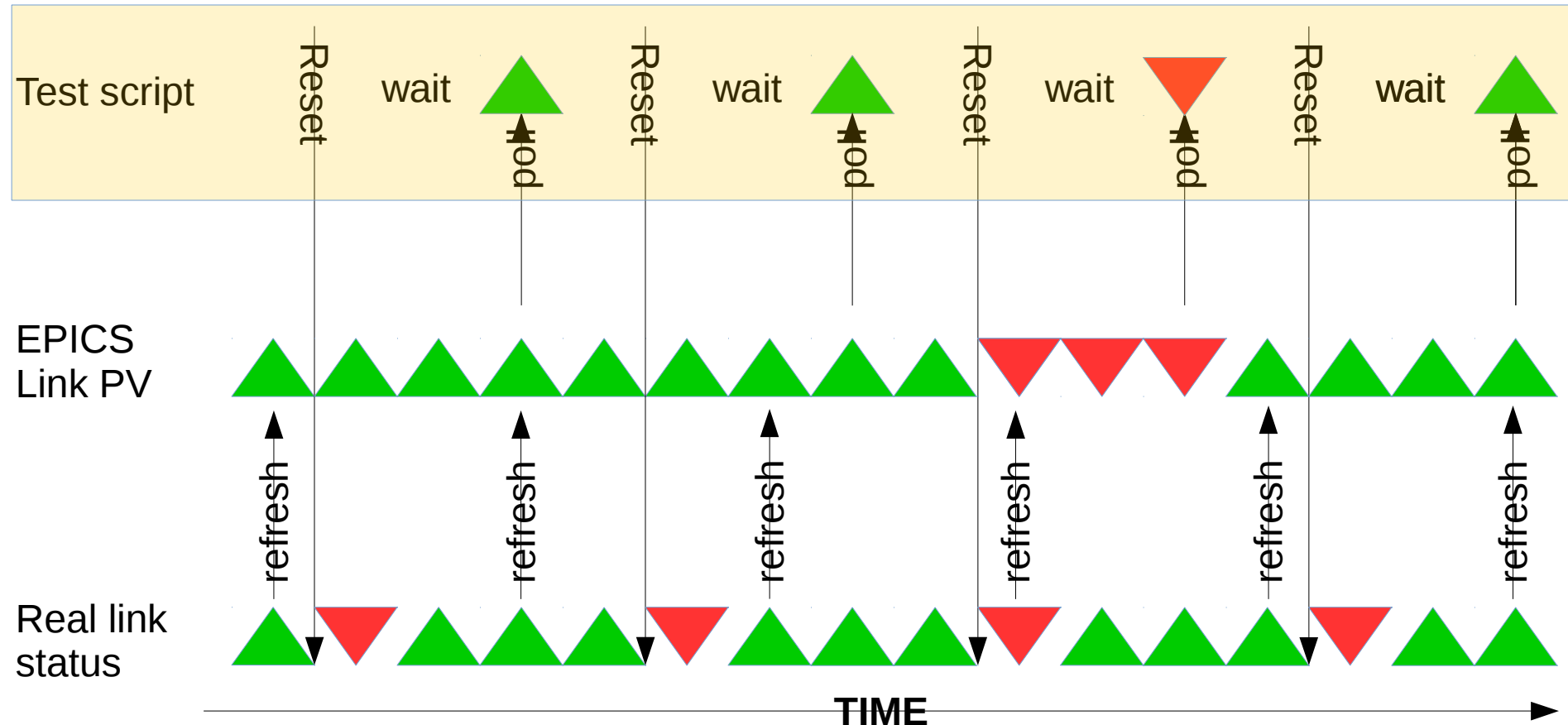
bias
biasd

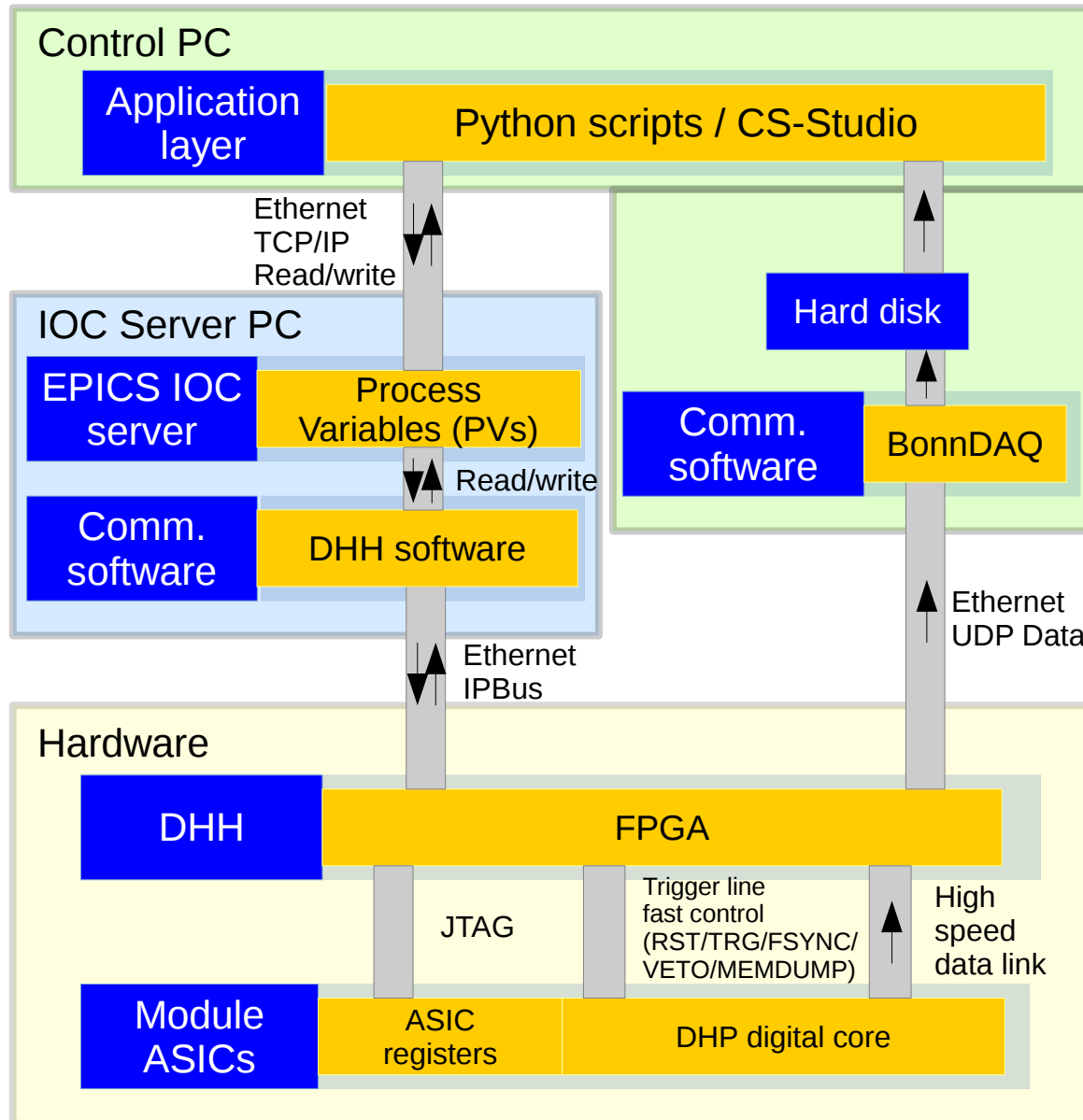
2. issue link reset commands

3. poll link state (success?)
- PV value scan time typically 1s

→ Information can be up to 1s old!

Timing is everything



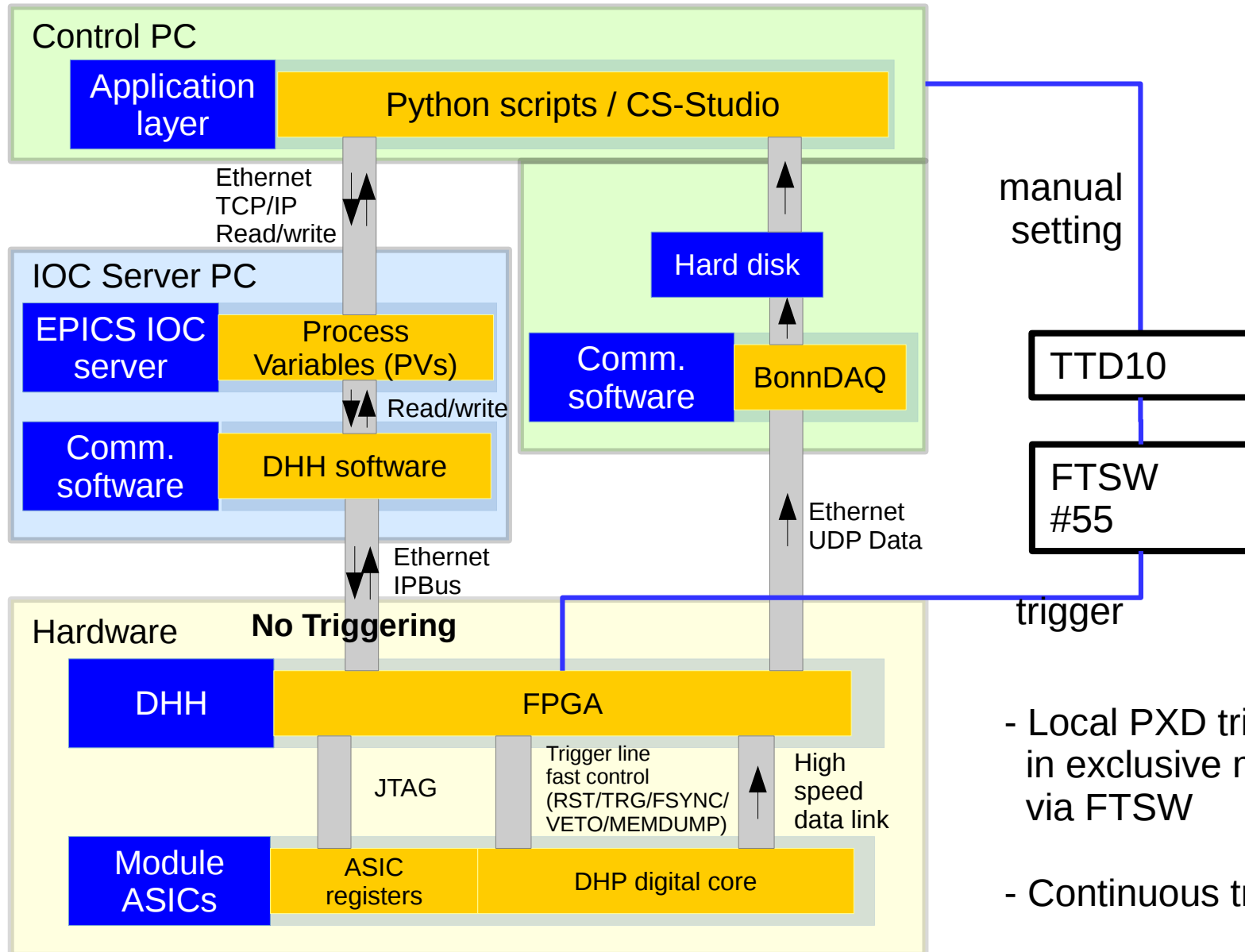


- Close to final phase 2 system:

- Dedicated IOC Server
- DHH system:
DHE + DHC
- Further DAQ:
DATCON
ONSEN
PocketDAQ
- SVD system

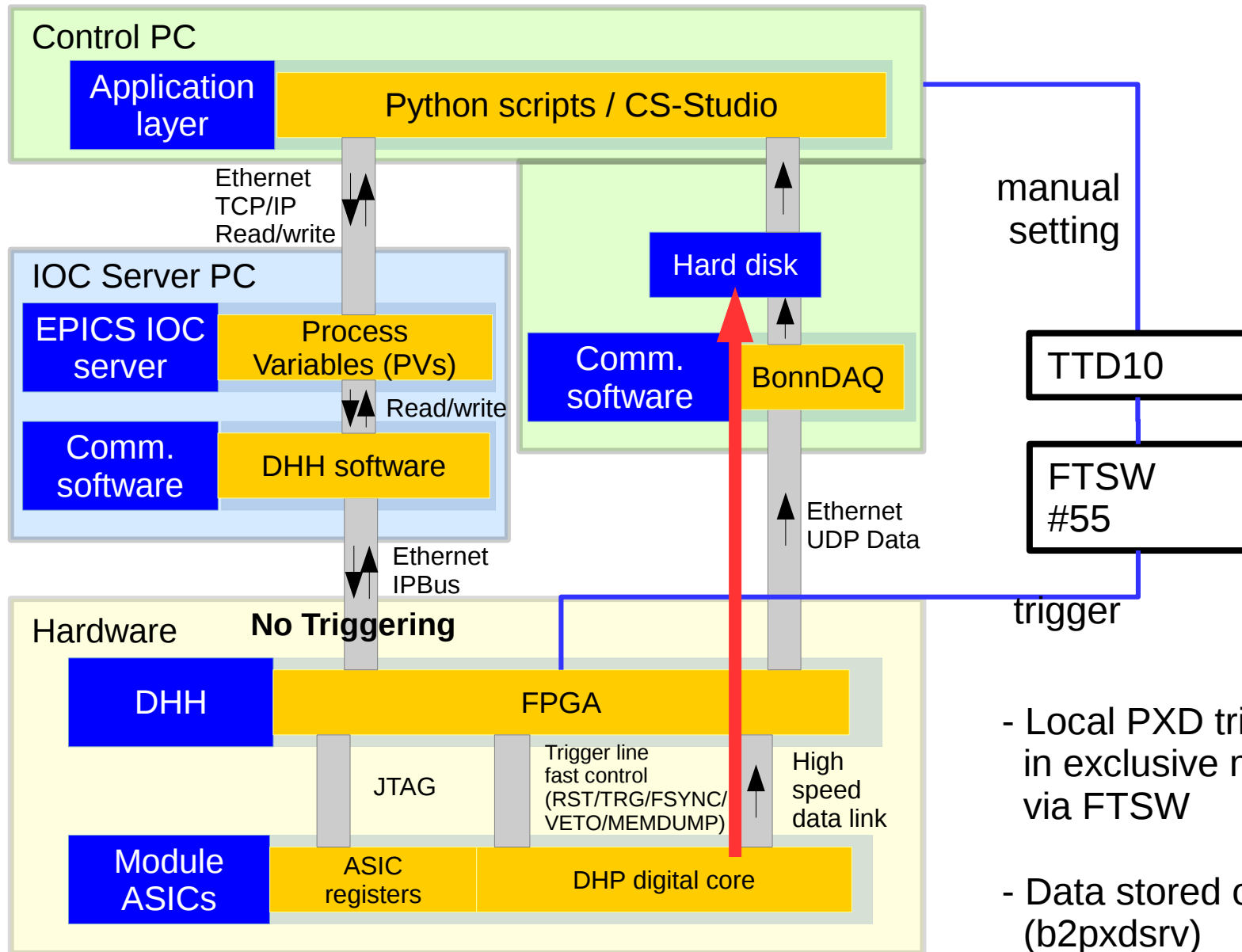
→ Demonstrates what's left to do

Pedestals at PERSY – special triggering



- Local PXD triggering in exclusive mode via FTSW
- Continuous triggering

Pedestals at PERSY – special triggering

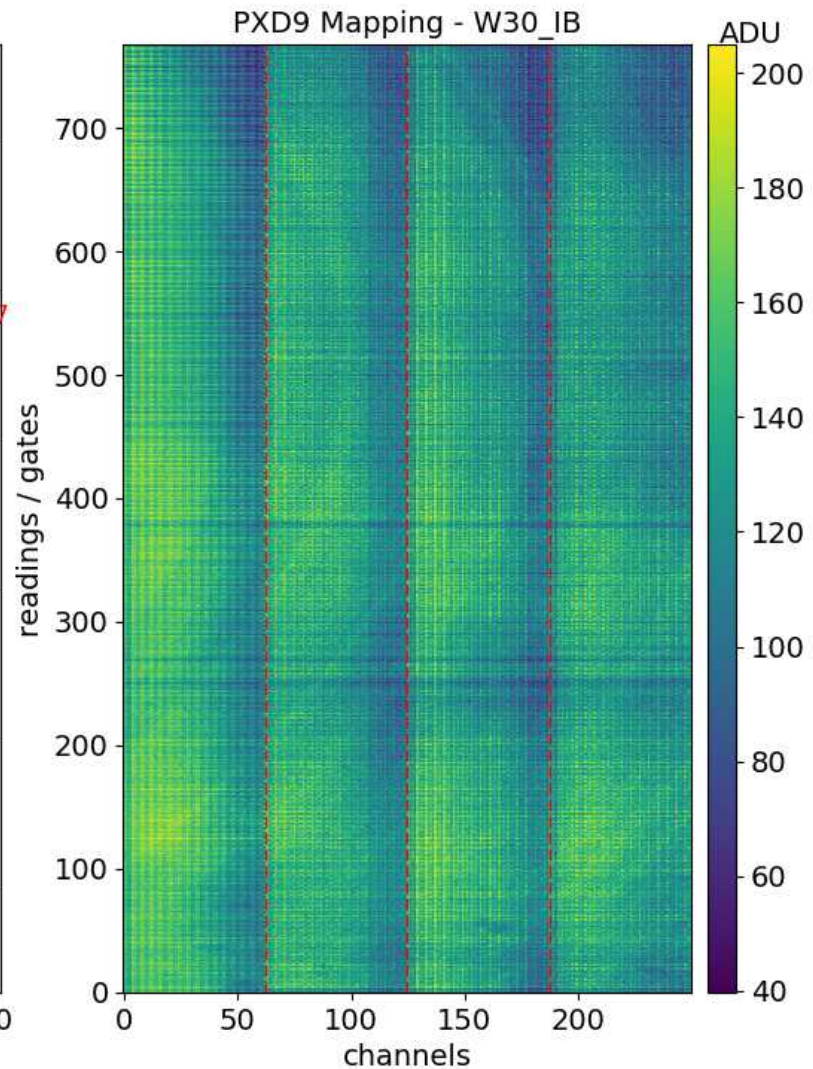
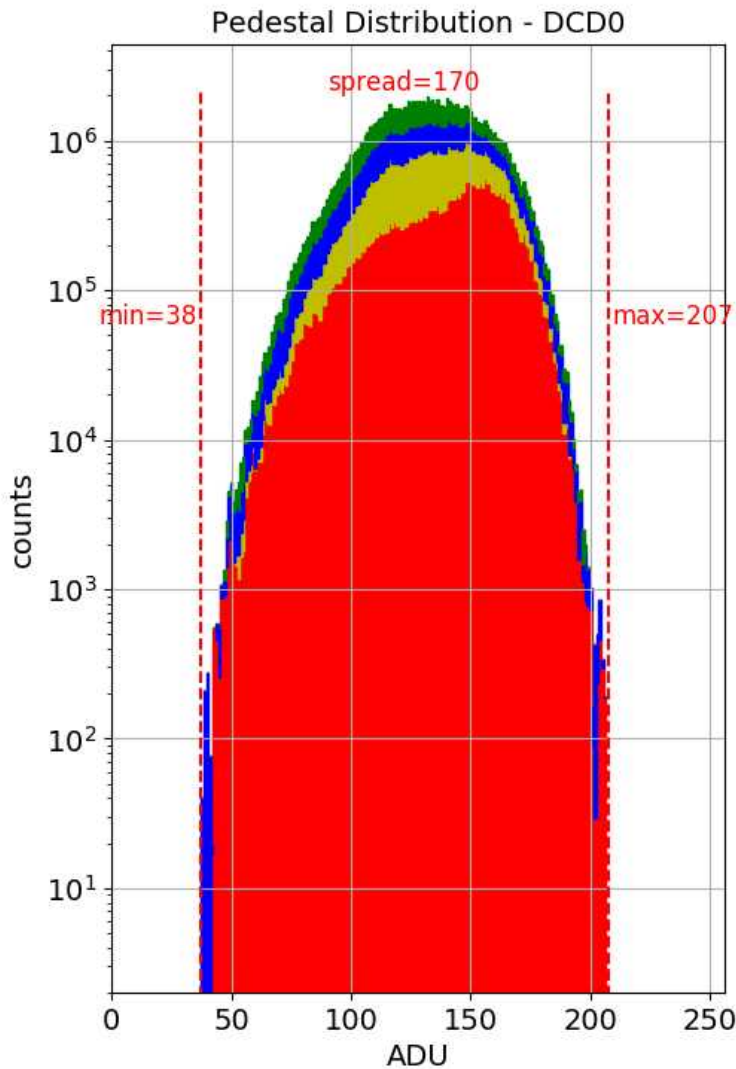


- Local PXD triggering in exclusive mode via FTSW

- Data stored on control PC (b2pxdsrv)

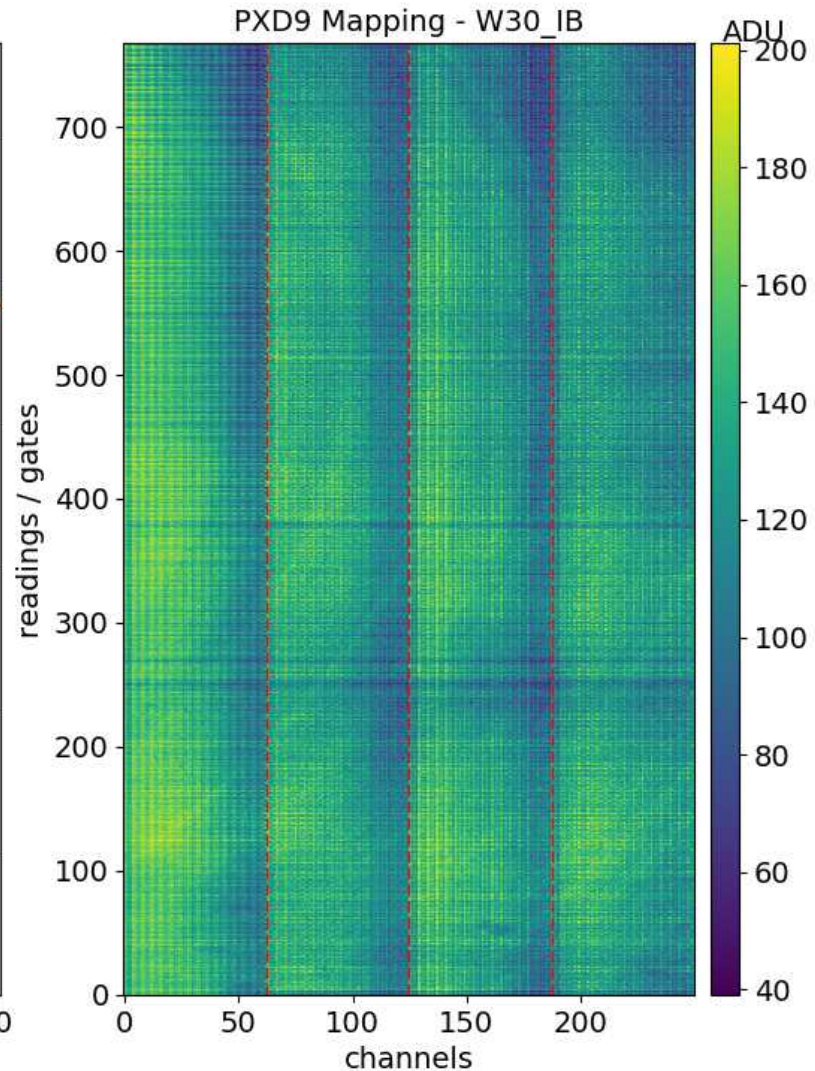
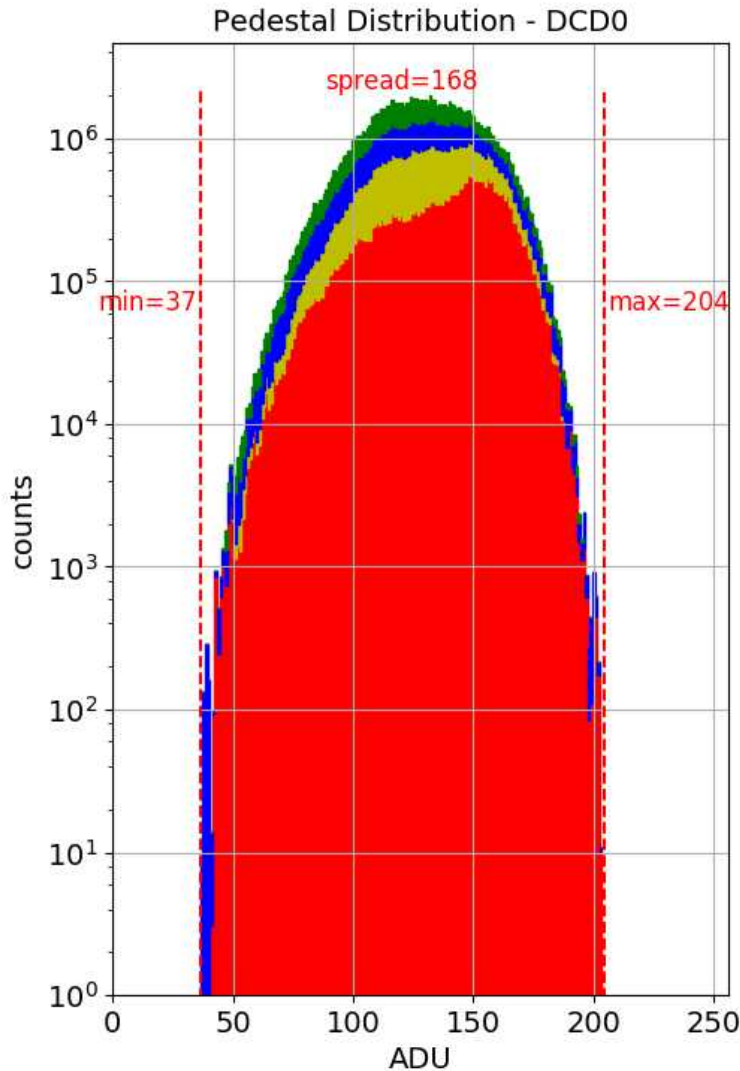
- pedestals on 20th May 2017
- MARCO constant 10 °C

W30_IB:
DHPT1.1, DCDpp



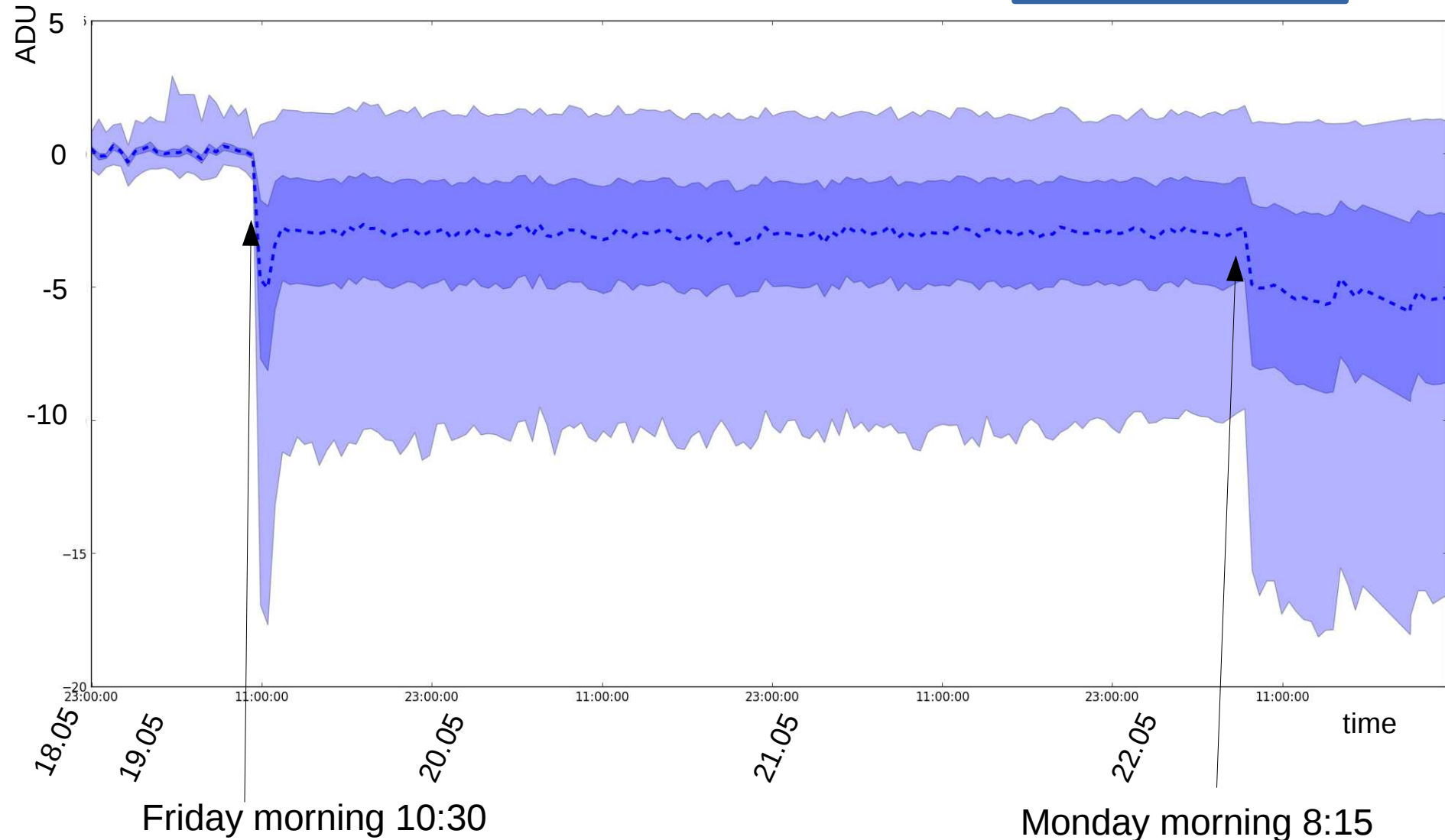
- pedestals on 22th May 2017
- MARCO constant 10 °C

W30_IB:
DHPT1.1, DCDpp



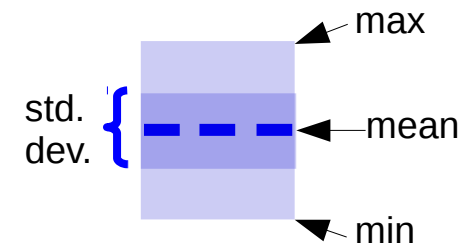
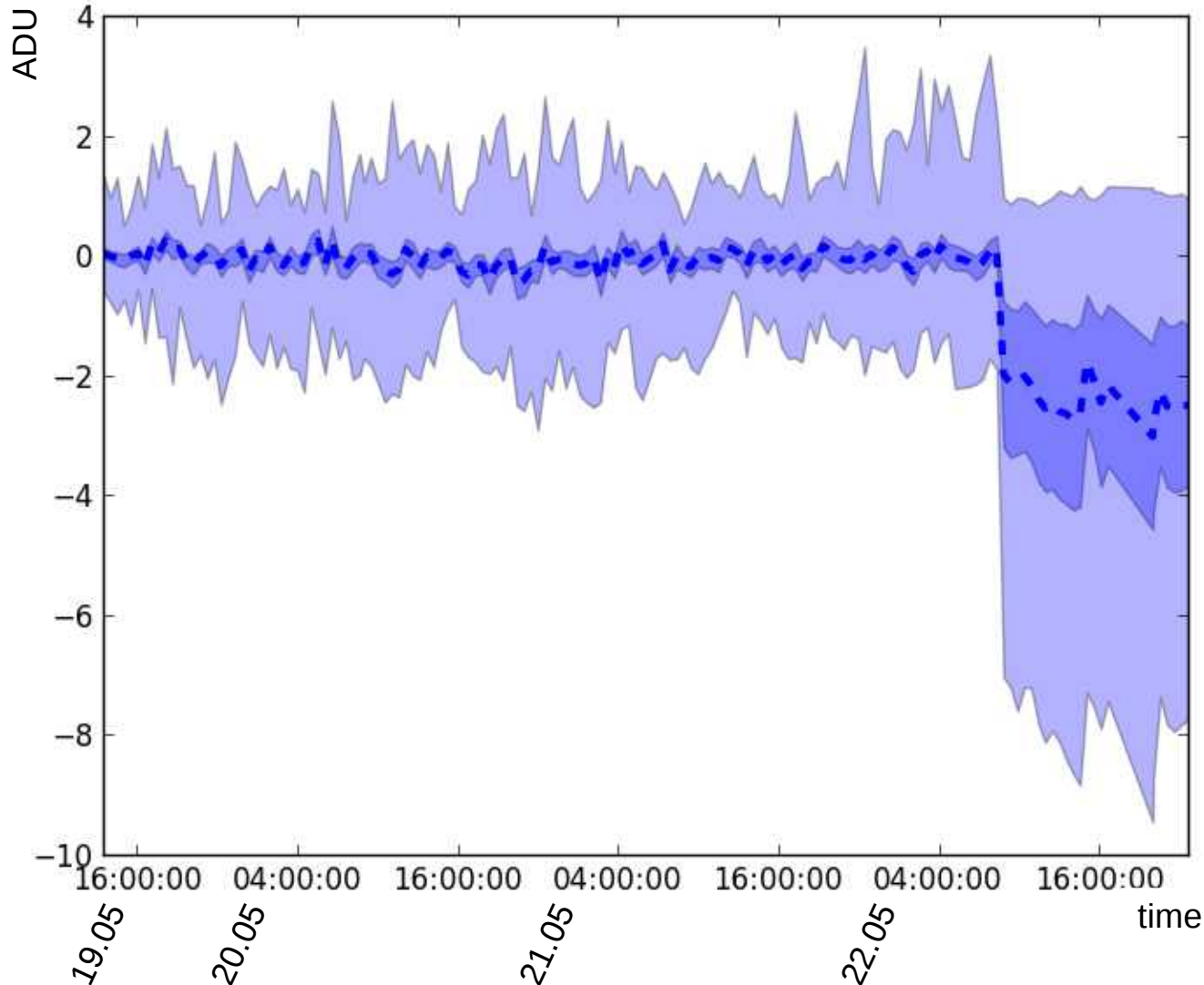
- relative change in pedestals
- 30s x 20 raw frames/s, every 30 minutes

W30_IB:
DHPT1.1, DCDpp



- relative change in pedestals

W30_IB:
DHPT1.1, DCDpp



- Slow control for final experiment already used in laboratory environment
 - To perform fast scans, careful programming is necessary
- PERSY system allows basic PXD long term studies
 - “Local” triggering mechanism still an open issue
- Old TB 2016 W30_IB module shows acceptable pedestal stability over long time: < 3 ADU in 2 days

Thank you