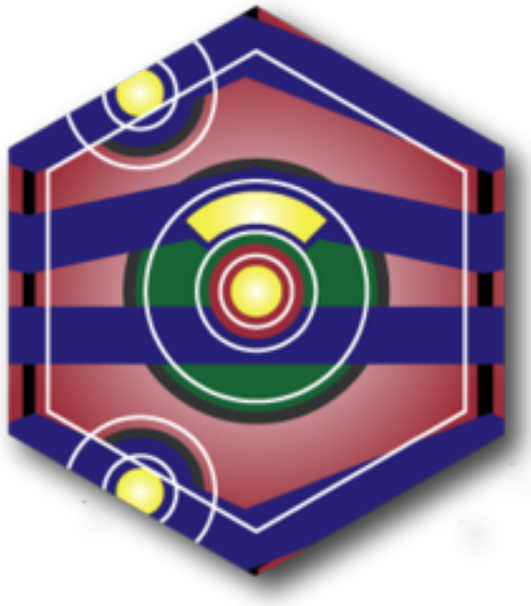

21ST INTERNATIONAL WORKSHOP ON DEPFET DETECTORS AND APPLICATIONS

PROBE CARD TESTING

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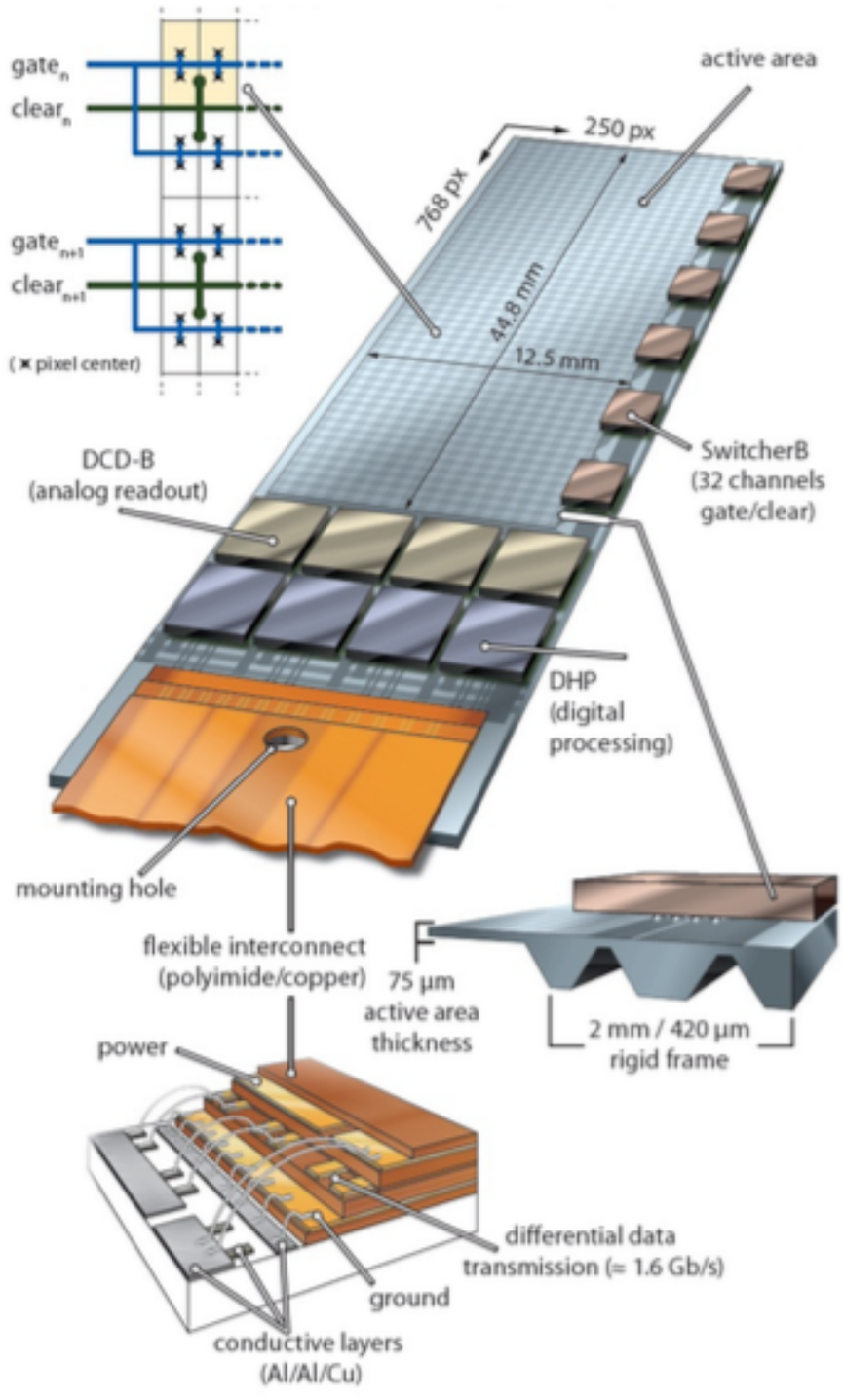
CONTENTS

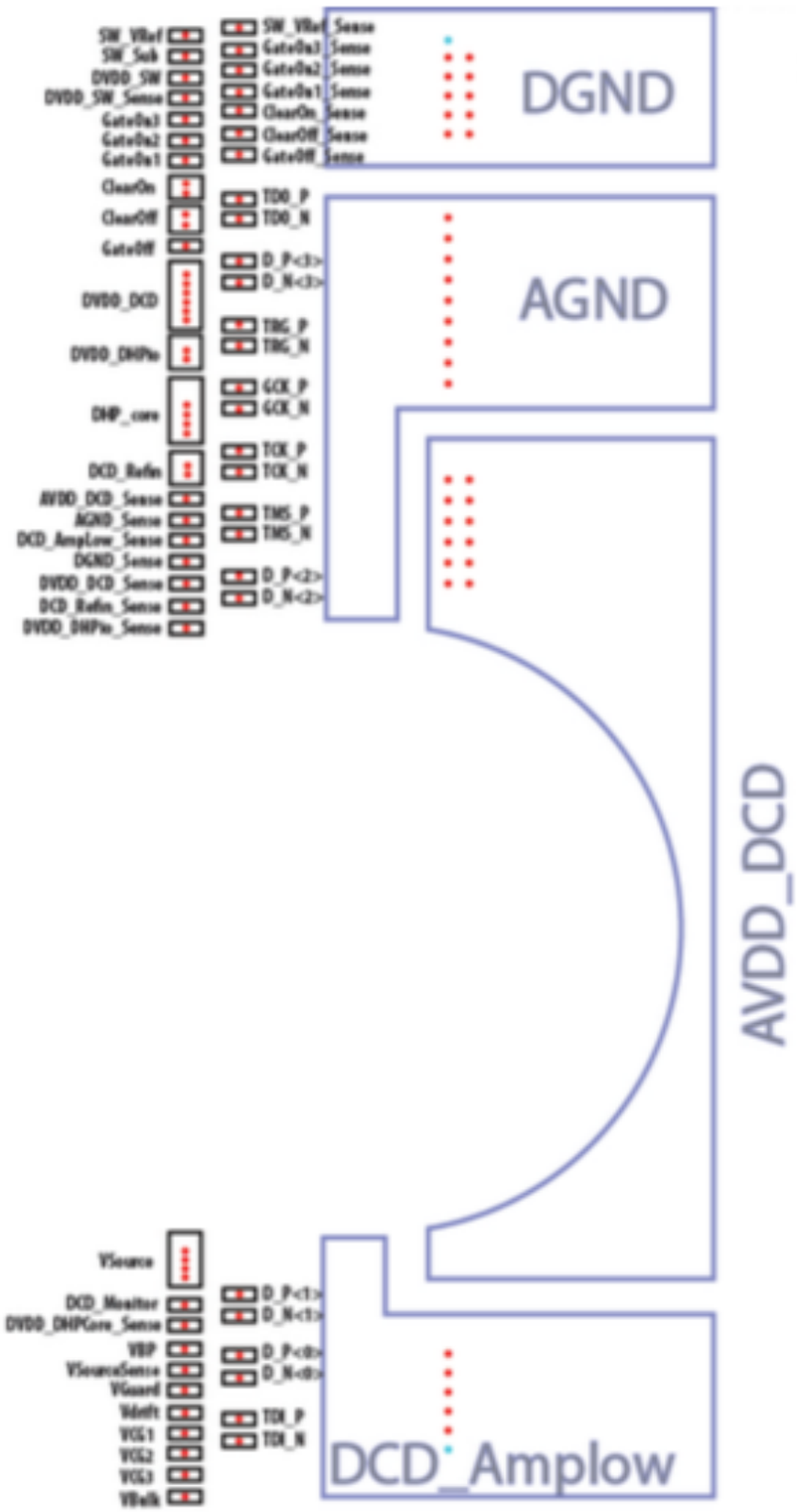
MOTIVATION

- DEPFET modules fully assembled are attached to a kapton cable.
- Pre-testing of the modules before the attachment avoids having to remove the kapton in the case that the module doesn't behave as expected, simplifying the rework procedure.
- A needle card is required for this purpose.



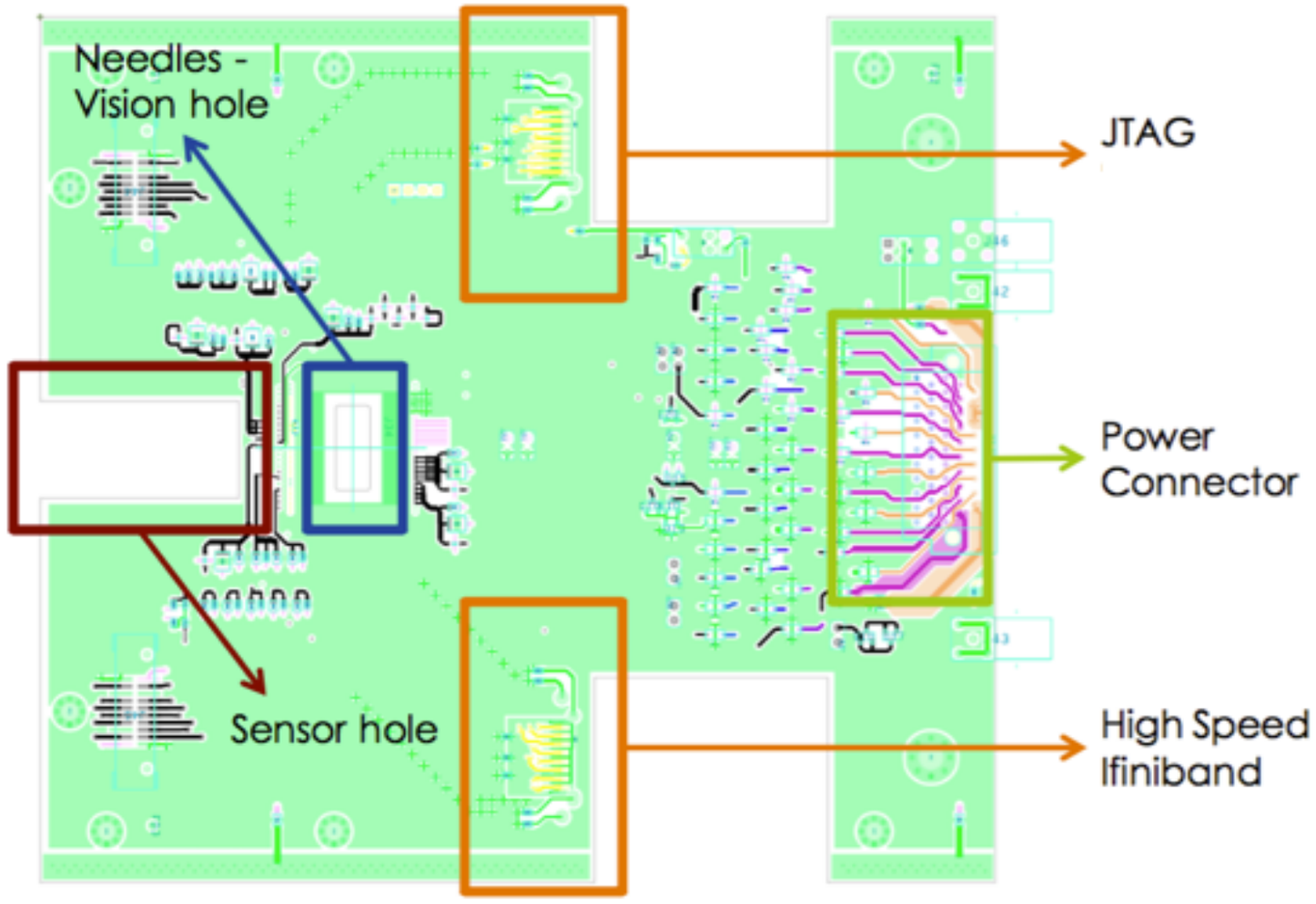
PROBE CARD: FEATURES

- The probe card directly interfaces the PXD9 modules to:
  - RJ45 cable for the slow control signals.
  - Glenair cable for power delivery.
  - Infiniband cable for HSL data transmission.
- In ideal contact, the module can be fully operated (at the lowest frequency and half rate) through the probe card.

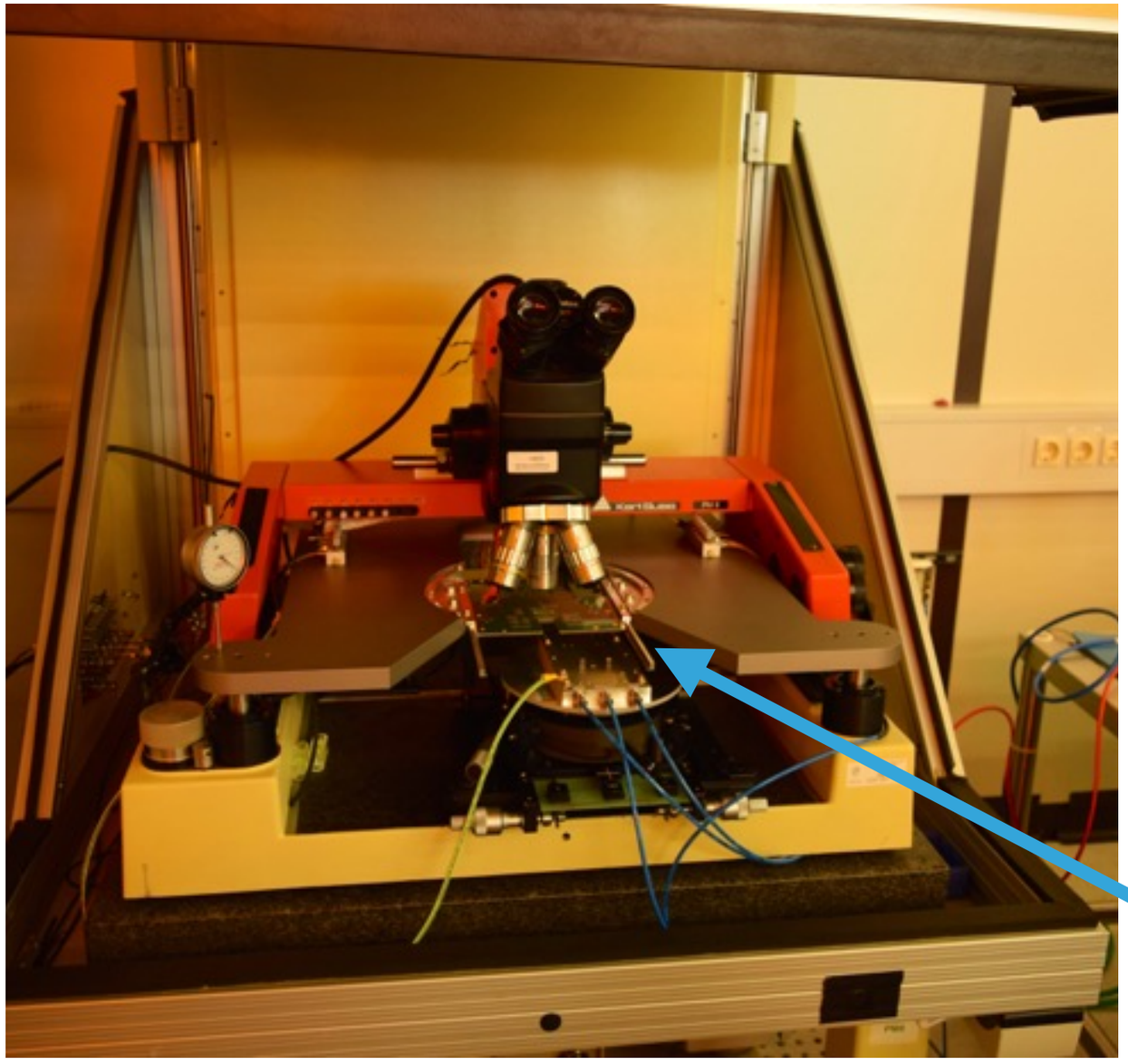


PROBE CARD: DESIGN

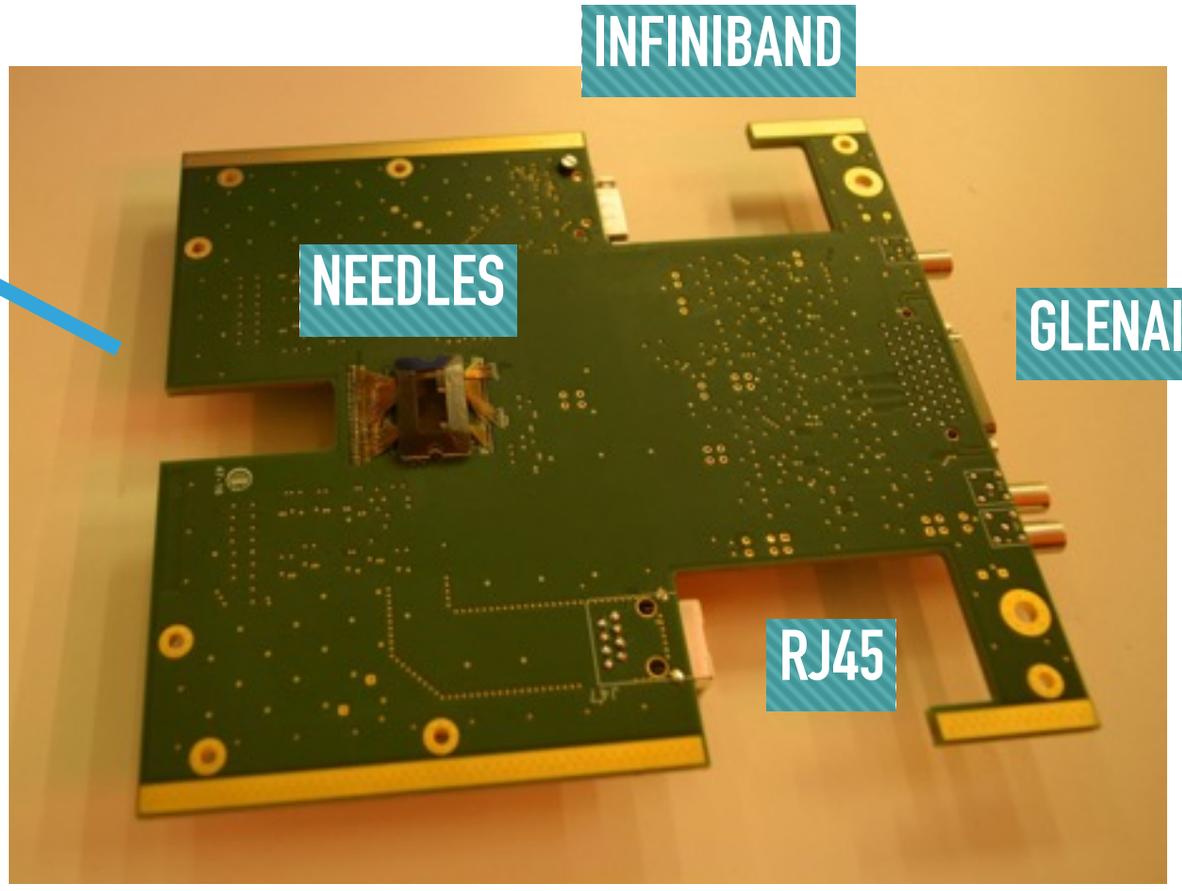
- 2 different probe card designs for the 2 different layouts of PXD9: design A for IF/OB and B for IB/OF
- Pad distribution for PXD9:
  - 59 small aluminium pads, 4 big copper pads.
  - 8 pads for high speed differential lines.
- Design considerations:
  - 114 needles (multiple needles for the big pads) are required.
  - PCB size is limited by connectors for power supply and infiniband.
  - Design priority: rather simple and passive PCB, minimizing the path length of the high speed signals.
- Many thanks to Daniel Esperante for the desing of the probe card.



PROBE CARD: ACTUAL HARDWARE



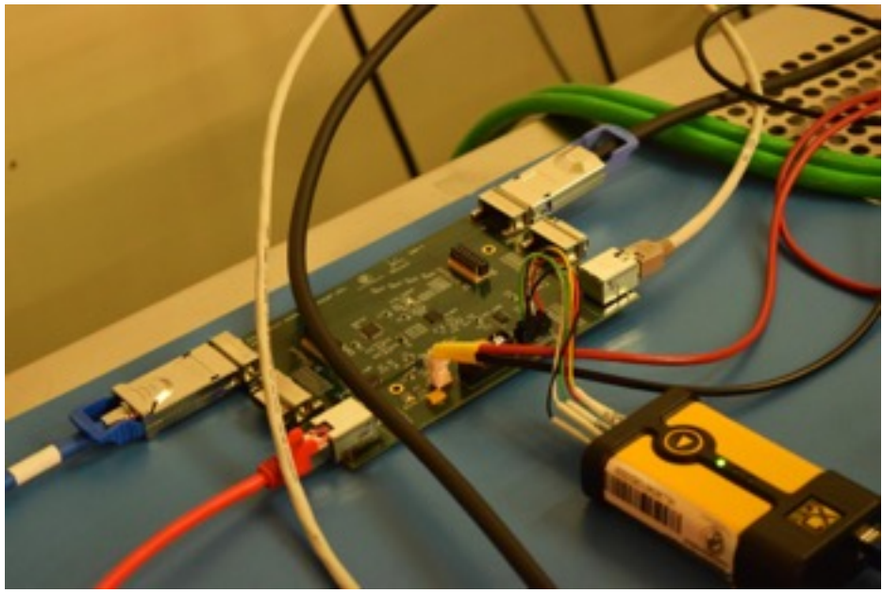
- Modules are placed with their base jig on the cooling jig and secured with screws and vacuum under the probe card.
- Through the optical microscope we can align the needles with the module and calibrate at what point the touchdown is performed.

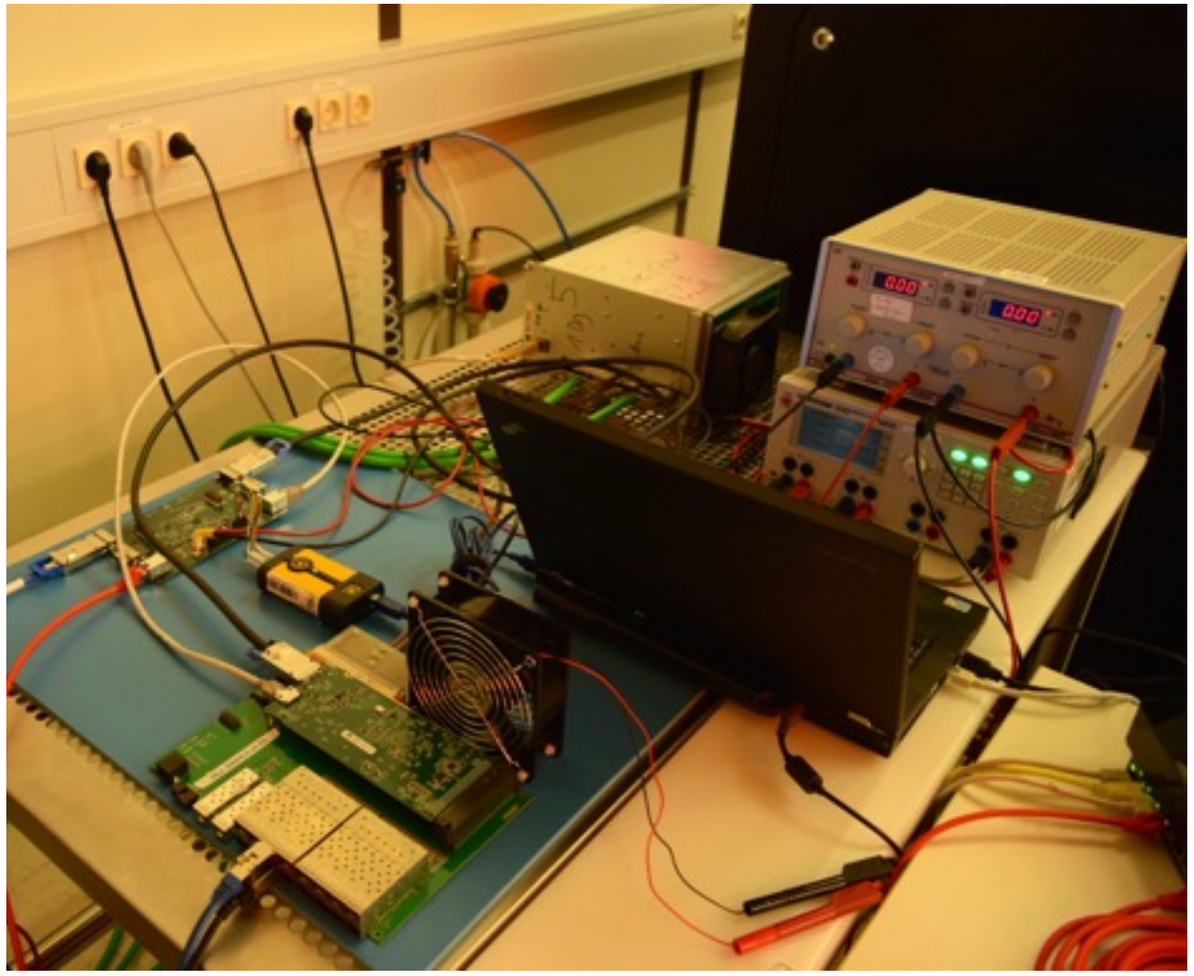


- With the help of the micrometer on the left, we apply the desired overtravel (~40 microns).

PXDTEST6 SETUP @HLL

- 2 probe card A (IF/OB compatible)
- 2 probe card B (IB/OF compatible)
- 1 Power breakout board (LMU_BB-04)
- 1 LMU power supply (LMUPS-05)
- 1 DHH carrier card (DHHCCv0.03)
- 1 DHE (DHE S/N: 0081)
- 1 JTAG breakout board
- 1 XJLink2 controller
- 1 DAQ PC
- 1 Archiver PC
- Cables and services



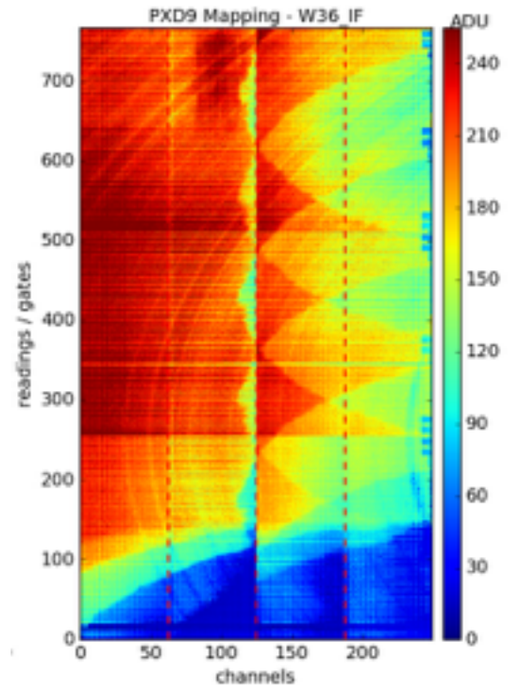


TESTING PROTOCOL: INCREMENTAL STEPS

1. Visual inspection.
2. Check of voltages & currents for DHP, SW and DCD-digital.
3. Chip configuration: JTAG write & read. Retrieving the IDCODEs, uploading and reading SW sequence, …
4. Boundary scan.
5. Getting the HSL connections.
6. Perform a delay scan.
7. Retrieve the testpattern from the DCDB.
8. Enable DCD-analog and check voltage & currents.
9. Enable and check of DEPFET voltages & currents.
10. Read DEPFET pedestals.
11. Saturate the matrix with a light source, calculate the number of working pixels.

TESTS OUTPUT

- One complete report of each of modules with all the details available at http://elog.mpp.mpg.de/DEPFET/
  - For the final production reports will be uploaded also to PERSY's elog
- A check list section into each one of the modules listed at the HephyDB: http://hephy.at/hephydb/hephydb/



	3		Probecard digital tests	Basic health checks with a probecard. Used to decide if the module continues to kapton attachment.	2017-05-10 14:23:47	gomis	action repeated 1 times. Second try after the reflow at IZM.
		3.1	Check voltages and currents	Tests if the connections between ASICs and power supply work.	2017-05-10 14:22:52	gomis	
		3.2	JTAG write and read	Configurate the chips, use automatic configuration script. Change, write and read some parameters. Tests the proper slow control connection and ASIC response.	2017-05-10 14:23:01	gomis	
		3.3	Boundary scan	Tests proper boundary scan structure, chip ID & communication with JTAG controller, check of the digital connections between boundary cells.	2017-05-10 14:23:11	gomis	
		3.4	High speed link stability	DHE software to establish the links, IBERT & Random pattern to debug Tests quality of the data transfer connection	2017-05-10 14:23:47	gomis	Links were extremely stable with eye diagrams of ~30 for all DHPTs.
	4		Probecard analog tests	Basic health checks with a probecard. Used to decide if the module continues to kapton attachment.	2017-05-10 14:40:28	gomis	action repeated 1 times. Repeating to change the fail in the voltages and currents to "skip". Fail doesn't let you continue with the steps.
		4.1	Check voltages and currents	Tests if the connections between sensor and power supply work.	2017-05-10 14:38:52	gomis	
		4.2	Read DCD pedestals		2017-05-10 14:39:02	gomis	
		4.3	Check matrix voltages and currents		2017-05-10 14:39:21	gomis	There seem to be some shorts in between DEPFET voltages: as soon as you power up clear on (12 V), gate off and clear off gain (2.5V) even though they should remain powered off. Also, as soon as you power up clear off (5V), gate on ramps up to 4.8 V (2.3 V on top of the previous 2.5V from the clear on), and gate-on2, gate-on3 also ramp up to 2.2 V. Even with this shorts, we could power all the DEPFET matrix and take some pedestals.
		4.4	read matrix pedestals		2017-05-10 14:40:28	gomis	The matrix was illuminated with a flashlight and the pedestal showed response from all the matrix except the SW1 area.

TESTS RESULTS

10 PXD9 modules and 13 EMCMs have already been tested with the probe card:

- W36_IF: first module to probe, used to qualify the setup. Could take pedestals and everything worked OK.
- W31_IF: only 3 SW were working. Everything else was OK.
- W31_OB1: JTAG chain was broken when including SWs.
- W31_OB2: JTAG chain was broken when including SWs.

MODULE FULLY TESTED AND WORKING
MODULE PARTIALLY TESTED: WORKING SO FAR
PARTIALLY WORKING MODULE
NOT WORKING MODULE

- EMCMs (W27_/IB/IF/OB1/OF1, W28_IB/IF/OB1/OF1/OF2): only DHPTs worked, JTAG chain was fine for them and memdumps were acquired for all of them.
- EMCMsv2(W29_IB/IF/OB1/OF1): JTAG chain was fine, testpattern could be retrieved from all of them.
- Reworked W31_OB1: high ohmic short between clear on-off and gate-off-on2-on3. SW1 also dead.
- Reworked W31_IB: JTAG was fine, testpattern could be retrieved. DCD-dvdd was in the current limit.
- W37_IF: JTAG chain was fine, no HSL could be achieved.
- W38_IB: JTAG chain was broken, sw-dvdd was on the current limit. One of the SW was bumped rotated 180 degrees.
- W37_OF1: JTAG chain was fine, no HSL could be achieved.
- W37_OB1: low ohmic short between clear on-off. Everything else looked fine.

LESSONS LEARNED

- In some of the modules the needles are able to make a really good contact, and a really stable connection is achieved (W31_OB1 ran without losing any HSL for almost an hour).
- But in some other modules (specially lately) it's really tricky to get a good contact. In some of them we can't actually get any kind of HSL. For example, W37_IF:
  - First touchdown: 60 microns top right corner. No dhp-io consumption. All pads are marked.
  - Second touchdown: 50 microns center of the pad. Now dhp-io shows regular values, but no consumption on sw-dvdd, dcd-dvdd rather low (44 mA). JTAG is fine. Boundary scan passed.
  - Third touchdown: 50 microns a bit south of touchdown 2. Now sw-dvdd and dcd-dvdd seems fine. Everything seems okay, dhp-core consumption is ~350 mA and links cannot be achieved.
  - Adding 10 microns: the chain cannot be initialized anymore.
  - Fourth touchdown: 50 microns north of touchdown 2. No consumption on sw-dvdd, dhp-core has a rather low power consumption (~230 mA).
- We see a degradation on the performance of the probe card over time, a cleaning of the residues of the needles could help to recover the original performance.
- We need to try to improve the electrical contact of the needles, as with a good contact the module can be fully operated: ie. more tests and optimizations could be done at the probe card, giving a more comprehensive picture of the module before kapton attachment.

SUMMARY

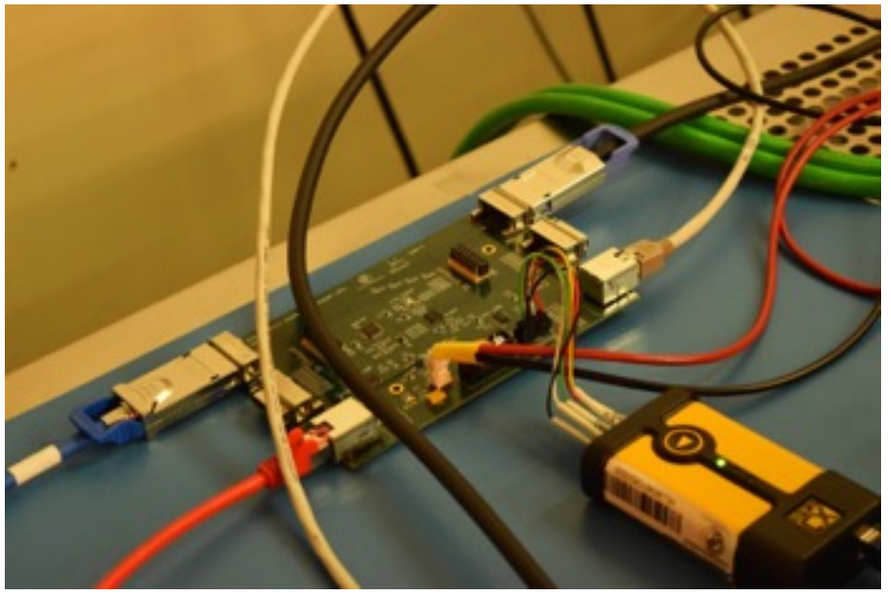
- Two probe card designs to test the PXD9 modules have been produced and are in operation.
- A testing protocol has been developed and tested with real modules.
- Ideally we can fully operate all the modules before kapton attachment.
  - Unfortunately, it's difficult to have a good touchdown on some modules, and not all of them could be fully operated.
- The needle card has already been useful to test 10+13 modules, spotting possible sources of failure before kapton attachment.
- The probe card setup is ready to further receive mass production modules.
  - Minor optimization (ie. needle cleaning) might be needed to improve performance.

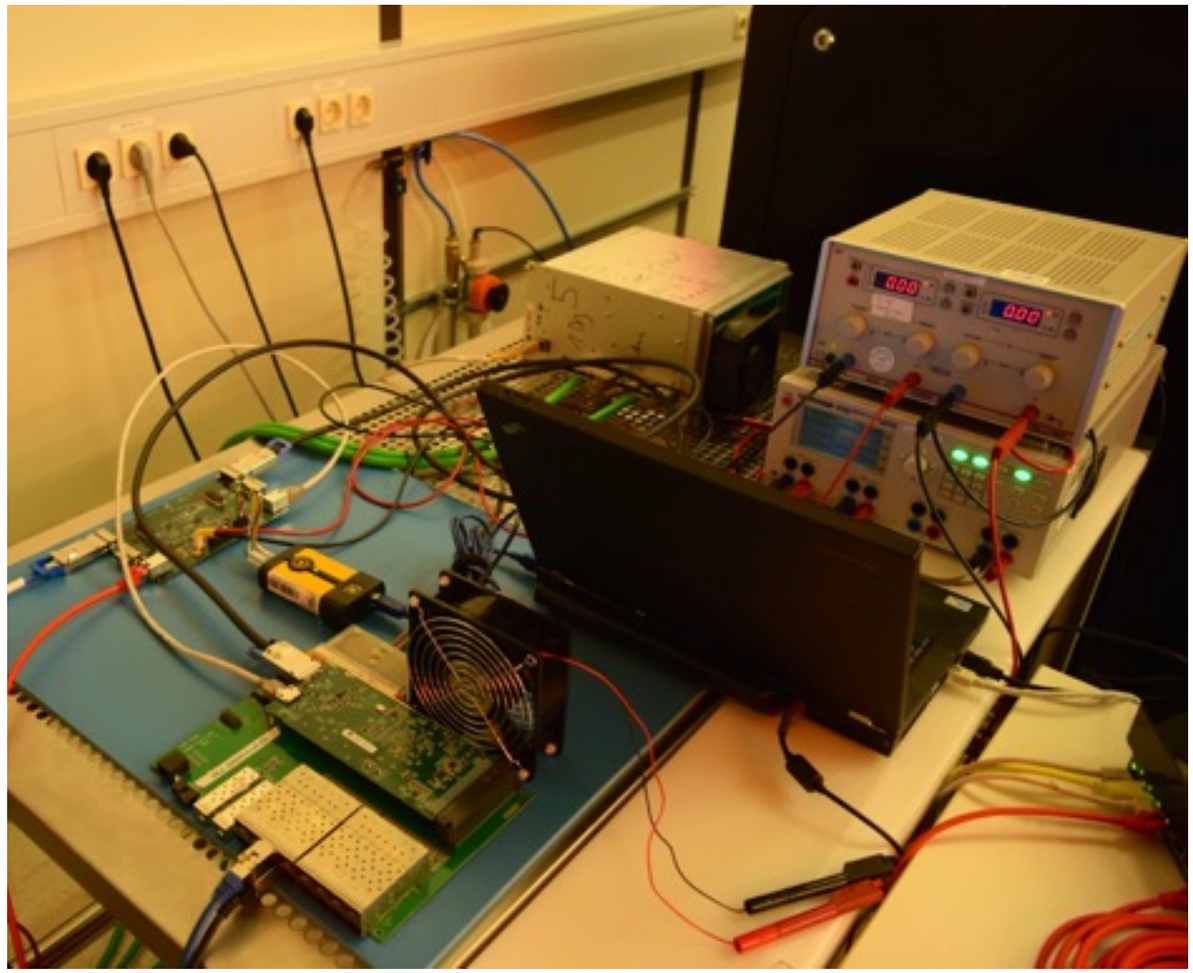
THANKS FOR YOUR ATTENTION

BACKUP

PXDTEST6 SETUP

- 2 probe card A (IF/OB compatible)
- 2 probe card B (IB/OF compatible)
- 1 Power breakout board (LMU_BB-04)
- 1 LMU power supply (LMUPS-05)
- 1 DHH carrier card (DHHCCv0.03)
- 1 DHE (DHE S/N: 0081)
- 1 JTAG breakout board
- 1 XJLink2 controller
- 2 Bench power supplies





PXDTEST6 SETUP

- 2 Infiniband cables, 2 green power cables, a glenair cable, RJ45 cables and banana cables
- 2 SFP adaptors
- 2 Fans to cool the DHE and the LMU PS
- 1 Cooling block (water cooled) with a vacuum pipe
- 2 Network switchers
- pxdtest6 SL7 pc: using the latest software release available at mid november 2016 (for stability/feature reasons), steering the modules with ini files (no DB)
- pxdtest5 SL7 pc: up-to-date software release, compatible with the DB
- edet2 SL7 pc: set up as archiver