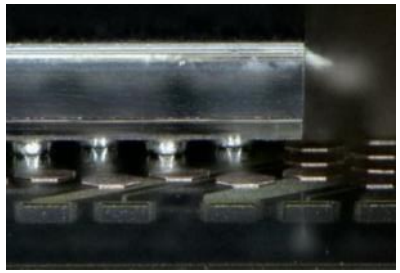
Modules Overview

- May 2017 -

Module Assembly – overview

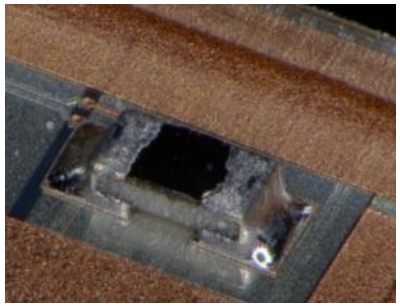
Flip Chip of ASICs (~240°C):

- ▷ Bumped ASICs have the solder balls (SAC305 and AgSn)
  - ↳ DHP bumping at TSMC, DCD bumping via Europractice
  - ↳ **SWB bumping on chip level at IZM Berlin**
- ▷ **@ IZM Berlin**



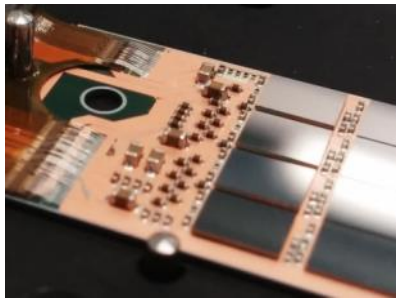
SMD placement (~200°C):

- ▷ Passive components (termination resistors, decoupling caps)
- ▷ Dispense solder paste/jetting of solder balls, pick, place and reflow
- ▷ **@ HLL**



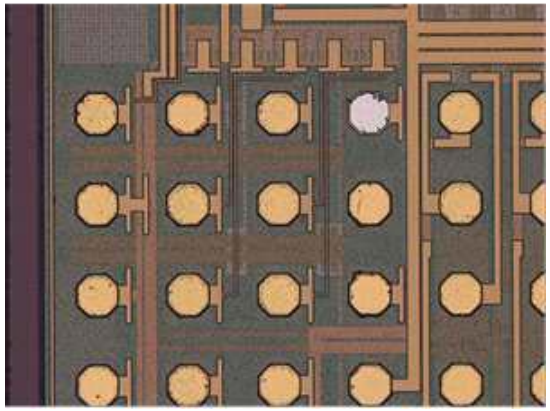
Kapton attachment (~170°C), wire bonding:

- ▷ Solder paste printing on kapton,
  - ↳ SnBi solder
- ▷ Wire-bond, wedge-wedge, 32 µm Al bond wires
- ▷ **@ MPP Munich**

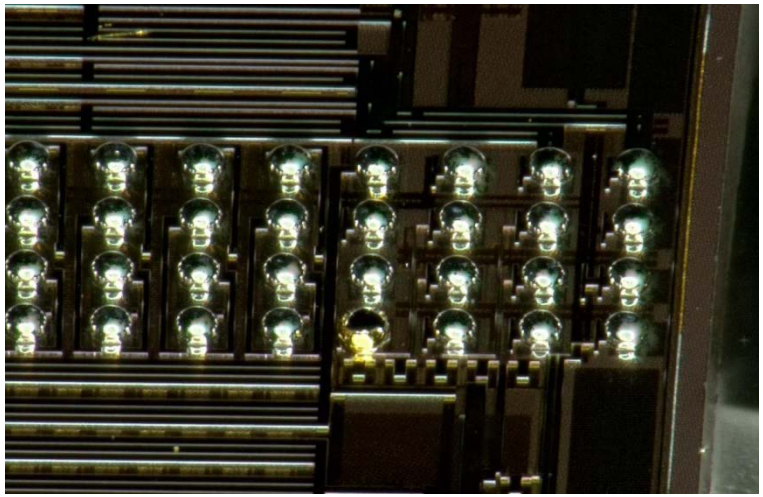


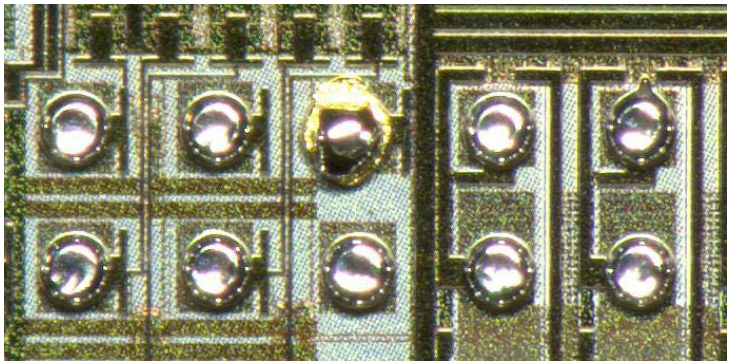
SwitcherBv2.1

- The Switchers have to be bumped on single die level
- Bumping (UBM process) causes problems with the new Switcher
- On one pad – the substrate pad – and only on this pad
  - Very little or no UBM deposition



- Main difference to old SwitcherBv2.0
  - Different passivation (1µm Nitride/Oxide <-> PI)
  - Guard ring of the chip exposed, connected to bulk
- Work around possible but extremely “ugly”

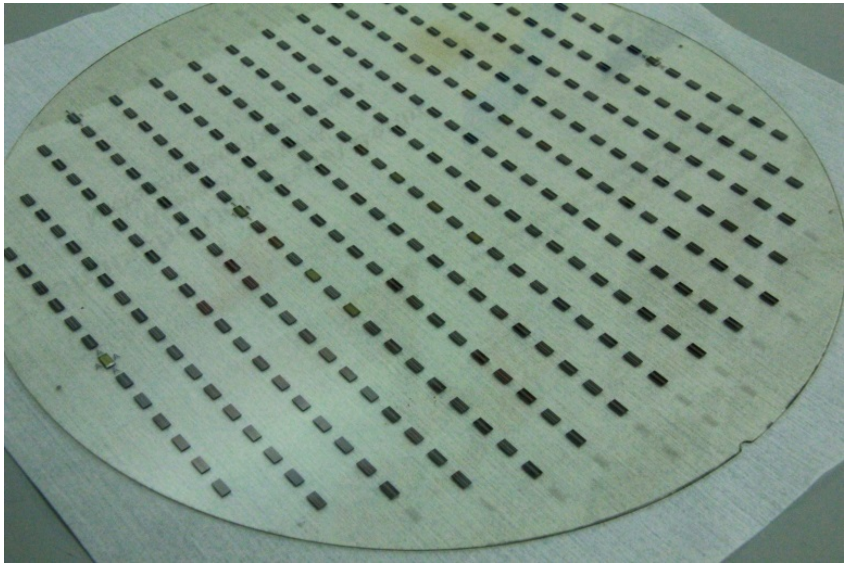


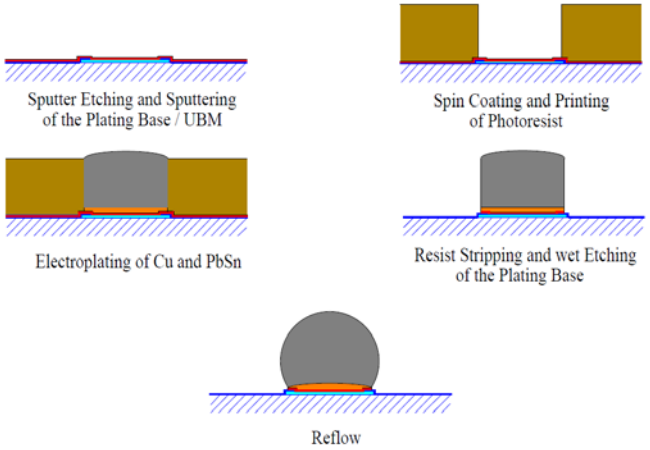


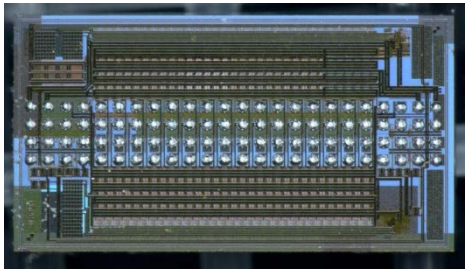
Bumping on “wafer level” at IZM

- Looking for a another bumping technology → IZM

- Assemble a “wafer” (glass) by pick-and-place of Switchers to support with alignment marks
  - Accuracy good enough for 150µm pitch, subsequent wafer level lithography possible
  - Possibility to apply standard technology bumping by electro-plating



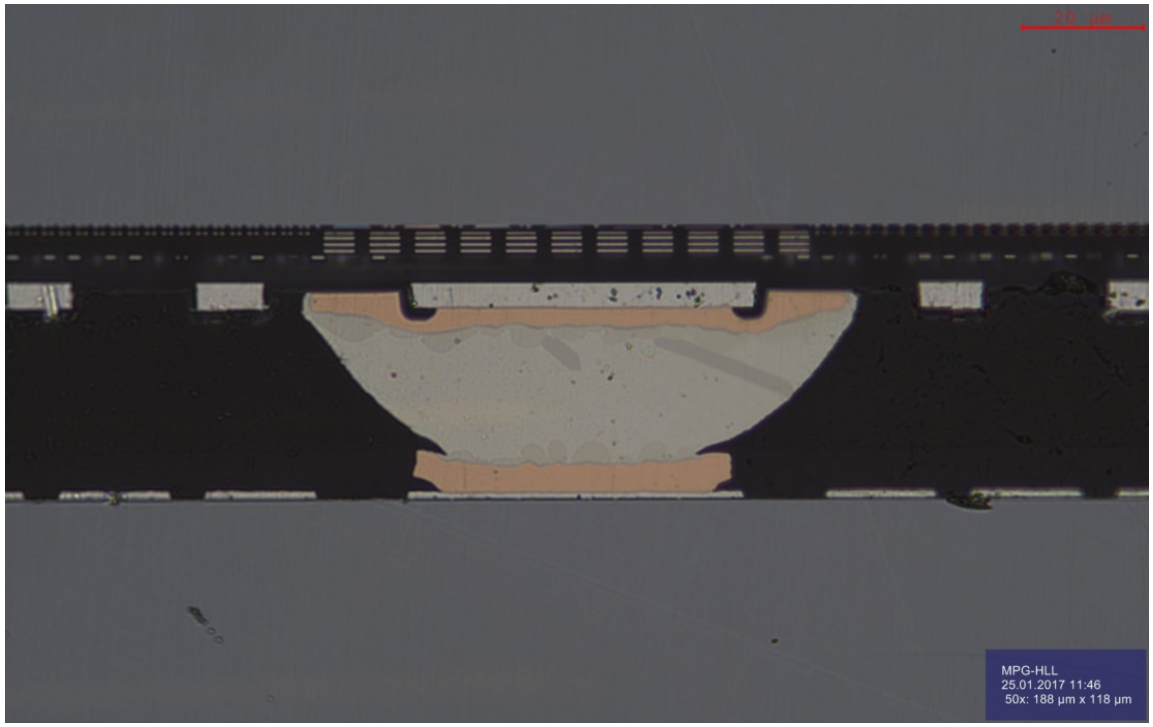




- **Tests run at IZM was positive**, 24 bumped chips delivered, 18 tested to be good

bump bonding w/ new IZM bumps

- Test assemblies and cross sections



- All okay, can't be better …

- **439 SWB2.1 bumped at IZM**
  - ↳ Complicated, expensive and lengthy process

Switcher Chips	Read JTAG ID	Current Consumption (1.8V)	Current Consumption (HV)	64 HV-Channels	Bias Current	Boost Current
89	✓	✓	✓	✓	✓	✓
10	✓	✓	✓	✗*	✓	✓
1	✓	✗	✗	✗	✓	✓

* It seems a contact problem between needles and switcher. Half of the channels are working! (clear or gate signal)

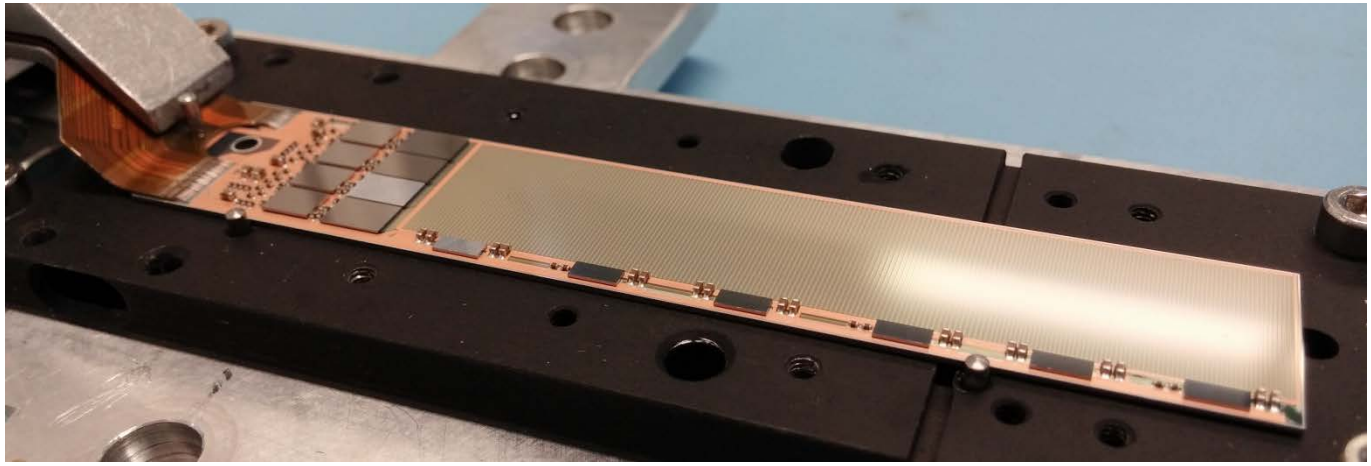
6 modules for PERSY and Beam Test

- **W31-IB, W31-OB, W31-IF (batch "persy1")**
  - DCDB4.2 (final), SWB2.1 (final, "fishy" PacTech bumps), DHPT1.1
- **W31-OF (batch "persy1")**
  - DCDB4.2 (final), SWB2.0 (last samples of the old version), DHPT1.1

- **W37-IB, W31-OB2 (batch "persy2")**
  - DCDB4.2, SWB2.1 (IZM bumps), DHPT1.1

- Flip Chip without any anomalies
  - Apart from the expected issues with the "fishy" switcher bumps

- SMD, Kapton attachment as usual



Status of the "persy1" and "persy2"

- W31-IB and W31-OB1 (batch "persy1")
  - JTAG configuration fails as soon as the Switchers are in the chain
  - DCD, DHPT okay, also boundary scan of EOS
    - Data generators at PERSY/Test beam
    - **JTAG chain repaired after 2nd reflow**
    - **W31-OB1 has clear-on/clear-off/gate-on „short"**

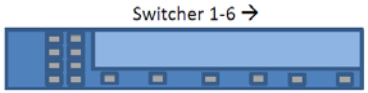
- W31-IF (batch "persy1")
  - JTAG configuration okay, EOS okay
  - See effect of bad substrate bump on the Switchers (3/6 SWBs dead) but operational

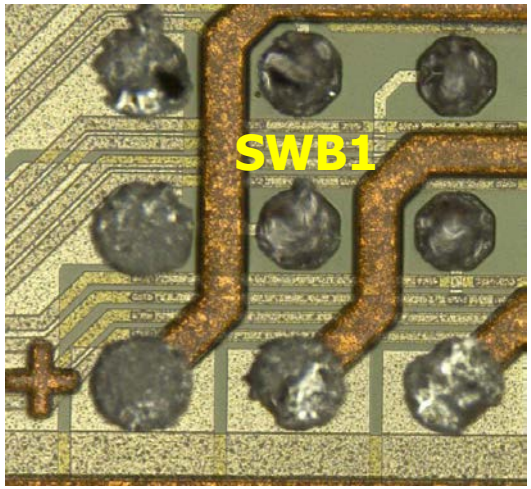
- W31-OF (batch "persy1")
  - JTAG configuration okay, EOS okay
  - Gated mode tests, operational

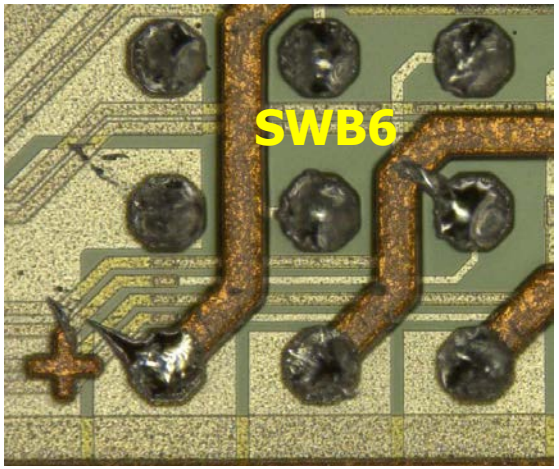
- W37-IB, W31-OB2 (batch "persy2")
  - DCDB4.2, DHPT1.1, SWB2.1 (IZM bumps)
  - **2nd reflow W37-IB** → JTAG okay, W31-OB2 used for destructive tests

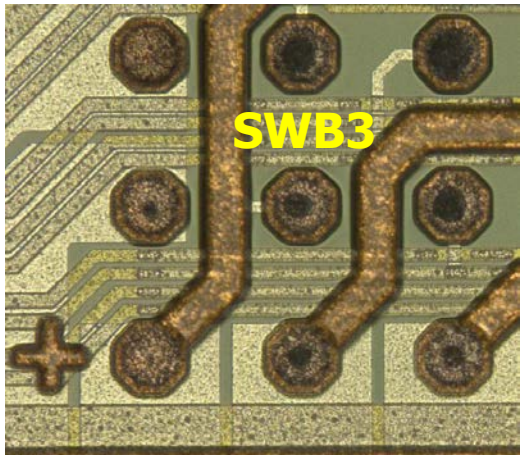
:- a 2nd reflow at higher temperature helped to repair the modules (SWB) JTAG)
:- high ohmic "short" on W31-OB1 **... not understood ...**

W31-OB2: SWBs removed, check solder joint

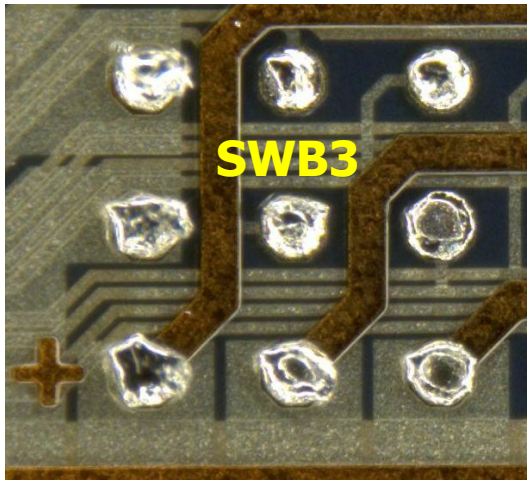








After 2nd FC & removal



reasons, mitigation, "rehearsal"

- Reasons
  - **Reflow temperature not reached** in the middle of the module due bad contact to the heat plate
    - Bowing of the module, too little contact area (perforation on balcony..)
    - In this case a second reflow with HCOOH or flux would help
      - **W31-IB was actually repaired after a second reflow!**
      - **→ increase reflow temperature (~10K)**
  - **Possibly CuO residues on pads**/insufficient pre-treatment before bump bonding
    - **→ Add another cleaning step before bonding**

- Test with sensors with non-functional matrix region (implant accident PXD9-3)
- **Pre-production batch PXD9-EMCM1**
- Production of two sets of modules: 2x(IF/IB) 2x(OF/OB) → 8 modules
  - Now used as data generators for system tests (PERSY)
  - Old chip set DCDB2/DHPT1.1/SWB-Dummy
  - EOS will be fully functional, remove part of dummy SWBs to check wetting of pads
  - … plus 2 modules for destructive tests → **SWB removed, wetting of all pads okay!**

- **PXD9-EMCM2**: set of modules with final chip set (DCDB4.2/DHPT1.2b/SWB dummies)
  - See testing session …

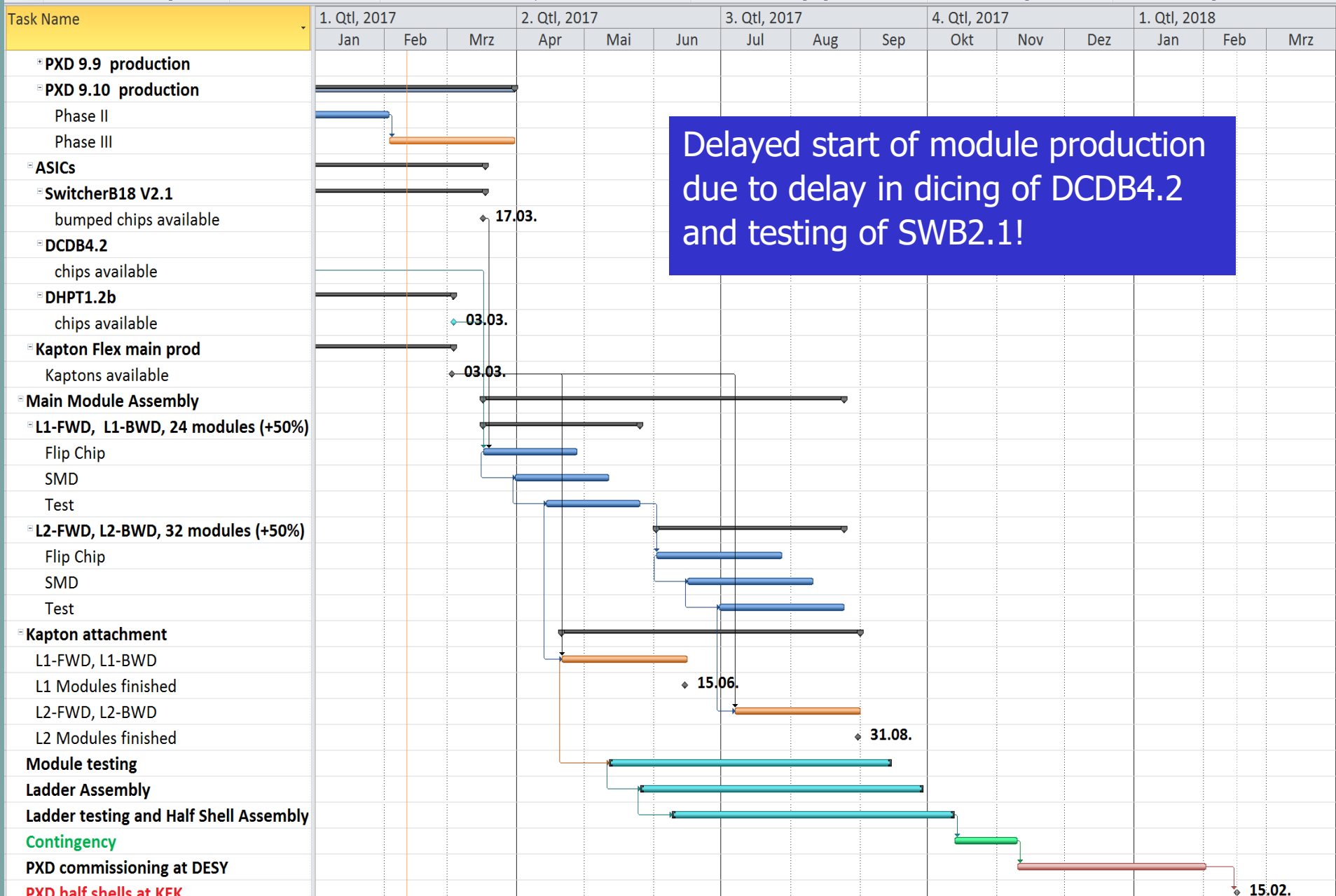
Phase 2 batch with improved reflow profile

- Sensors from pre-production batch PXD9-7
  - set1: W38-IB, W37-IF, W37-OB1, W37-OF1
  - set2: W40-IB, W40-IF, W38-OB1, W40-OF1
- Final ASICs DCDB4.2, DHPT1.2b, SWB2.1 (IZM bumps)
  - All ASICs tested (KIT, Bonn, KIT)
- Flip Chip at IZM of 1st set in about 1 week, SMD at HLL in two days …
- Results after probe card testing (more on this from Pablo..)
  - W37-IB
    - EOS okay, but one SWB wrongly placed
    - now at IZM for replacement, to be re-tested as soon as back
  - W37-OB1
    - EOS fully functional, JTAG of Switchers also okay. **Biasing of the matrix revealed a short between clear-on and clear-off.**
  - W37-OF1
    - EOS and balcony is functional, module ready for kapton attachment
  - W37-IF
    - EOS and balcony is functional, module ready for kapton attachment

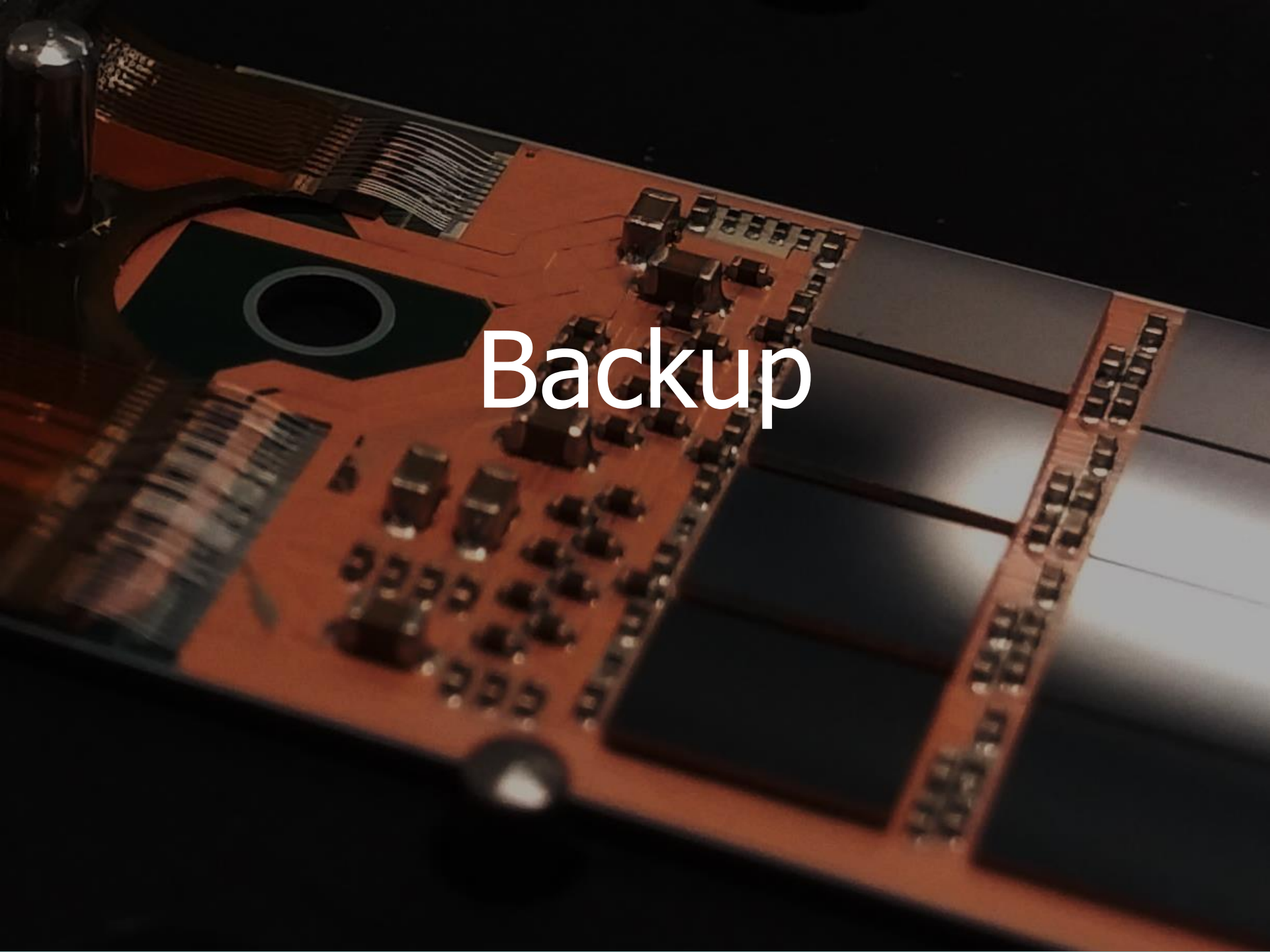
What's next

- The problem of the bad soldering seemed to be solved
- If not, a second reflow will help….
  - Continue with FC of 2nd set of batch "phase2"
  - To be ready still this week → SMD, testing, next week
- Wrong orientation of SWB must not happen again, IZM acknowledges their mistake
  - The orientation is clearly described in interface document
  - https://confluence.desy.de/download/attachments/43903269/FC-SMD-Interface-document-version-15.pdf?version=2&modificationDate=1484808702509&api=v2
- **Most worrisome**
  - Not understood short between clear-on/clear-off (W37-OB1 and W31-OB1)
  - Remove all SWB, one by one and check where the short is … **have to understand this!!**
  - In an ideal world, I would wait for the conclusion before doing 2nd set, but there is no time …
- Production for phase 3
  - Have to start production of inner modules soon, will prepare all still this week
    - All ASICs, Sensors available

Schedule from Jan. 2017



Delayed start of module production due to delay in dicing of DCDB4.2 and testing of SWB2.1!



Backup