# 21st International Workshop on DEPFET Detectors and Applications

## 28th – 31th May 2017
## Ringberg Castle

# Status DHPT 1.2b

Leonard Germic, B. Paschen, F. Lütticke,
T. Hemperek, C. Marinas, H. Krüger
and Norbert Wermes

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# Status DHPT 1.2b

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- 200 chips tested (2 Wafers) – yield 97%
  - 6 not working
    - 3/6 no jtag response
    - 2/6 memory errors
    - 1/6 low power consumption (not responding)

- Temperature sensor
  - Script is ready
    - Used for Hybrid 5 and PXD-EMCM2

  - Read out is limited by DHE software
    - Number of JTAG clock cycles is 2.5M instead of 120k
    - Cycles send in bursts of 655 and Period of 5ms → overall time ~20s

# Script - Temp Sensor

```
if __name__ == "__main__":

    ''' Here you have to load the conig.ini
    '''

    irefTrim = config.getint("param","iref_trimming")
    nbits    = config.getint("param","nbits")
    gain     = config.getint("param","gain")
    rp       = config.getint("param","vrp")

    params = [irefTrim, nbits, gain, rp]
    sensor = UBTEMP(dhePrefix=dhe, asicpair=asicpair, params=params, verbose=False)
    print sensor.updateTemperature()
```

# DHPT - Signal Integrity

## PXD9-EMCM2 modules

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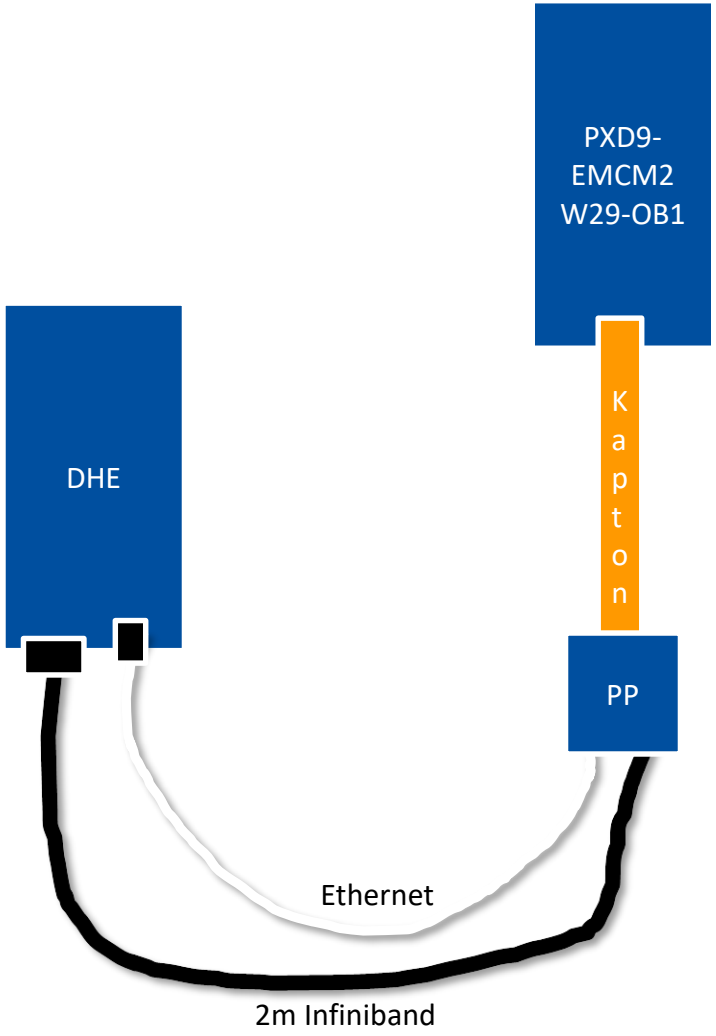
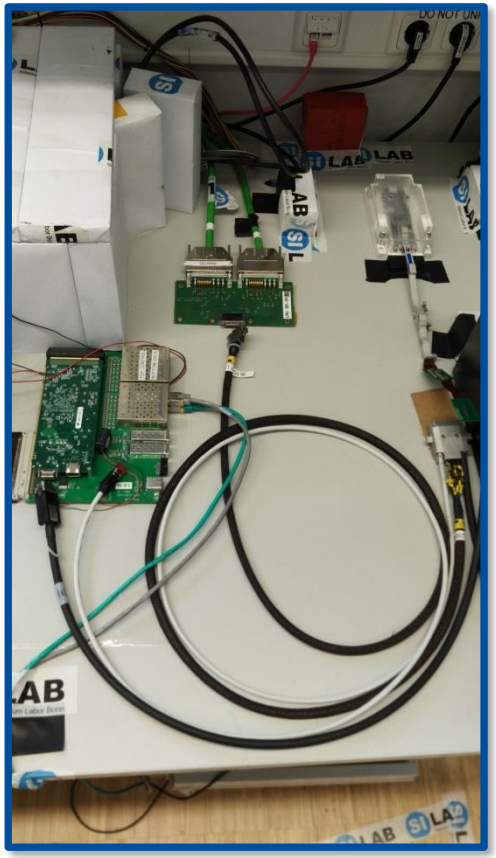
# Test Setup

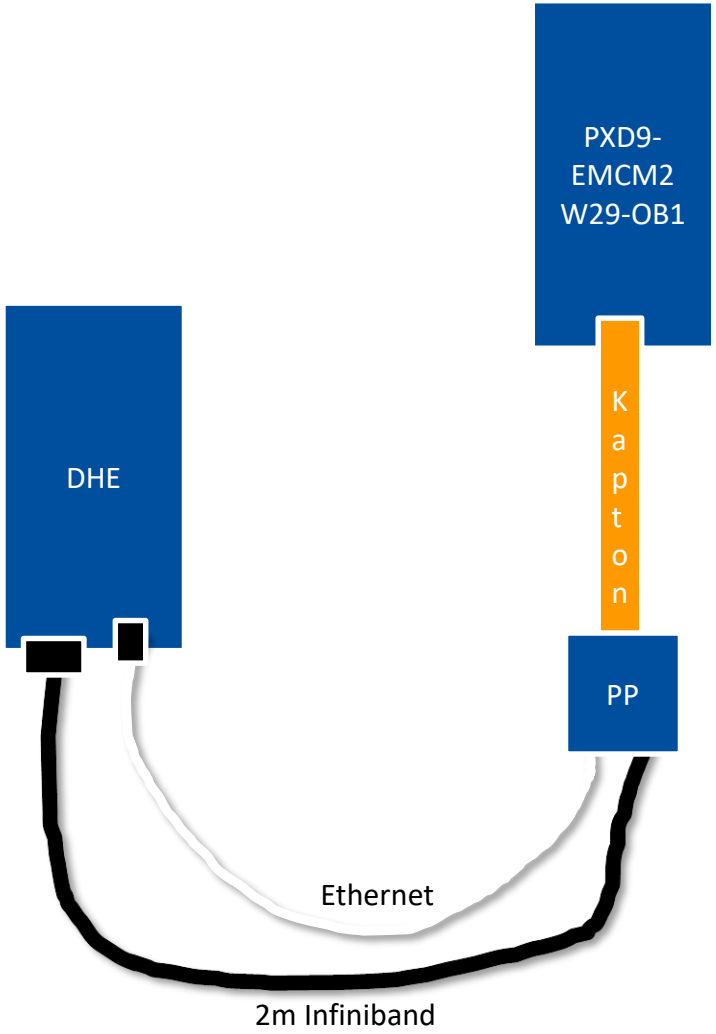


One Infiniband connector

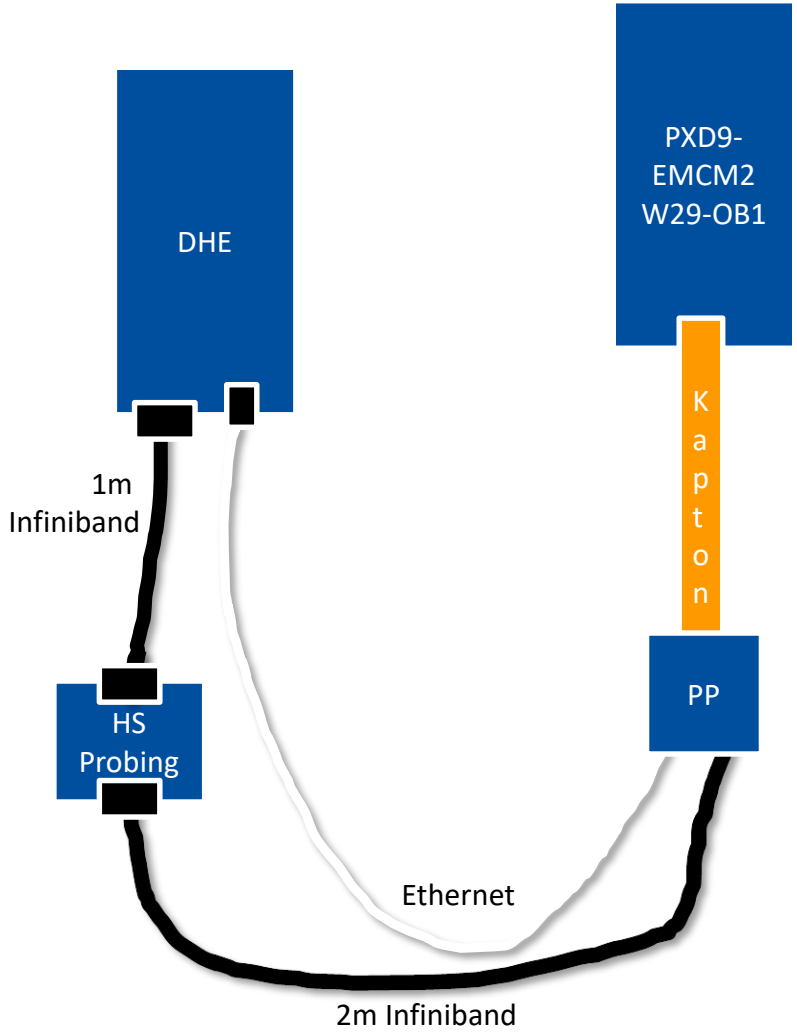
Kapton + 2m Infiniband

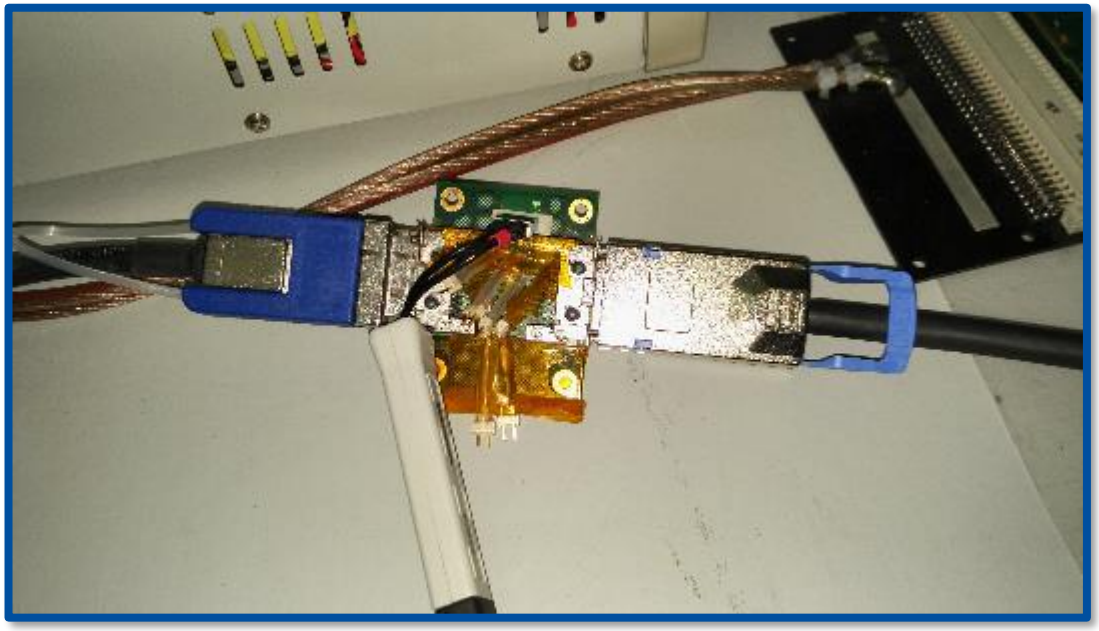
# Test Setup




| Transmissionline Kapton + Infiniband | PDPP_L2BWD-04 | PDPP_L2BWD-03 |
|---|---|---|
| AWG | 24 | 28 |
| Diameter [mm] [%] | 0.511 100% | 0.321 63% |
| Cross section [mm²] [%] | 0.205 100% | 0.081 40% |
| Vendor | Madison | Meritec |

# Test Setup

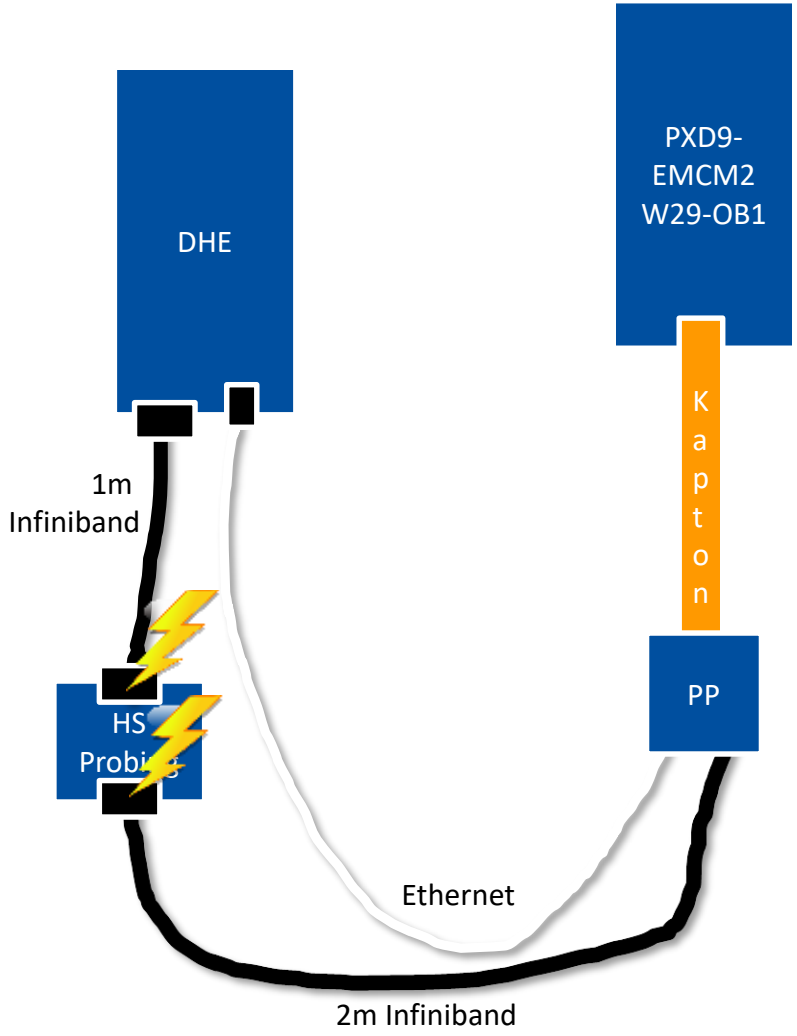


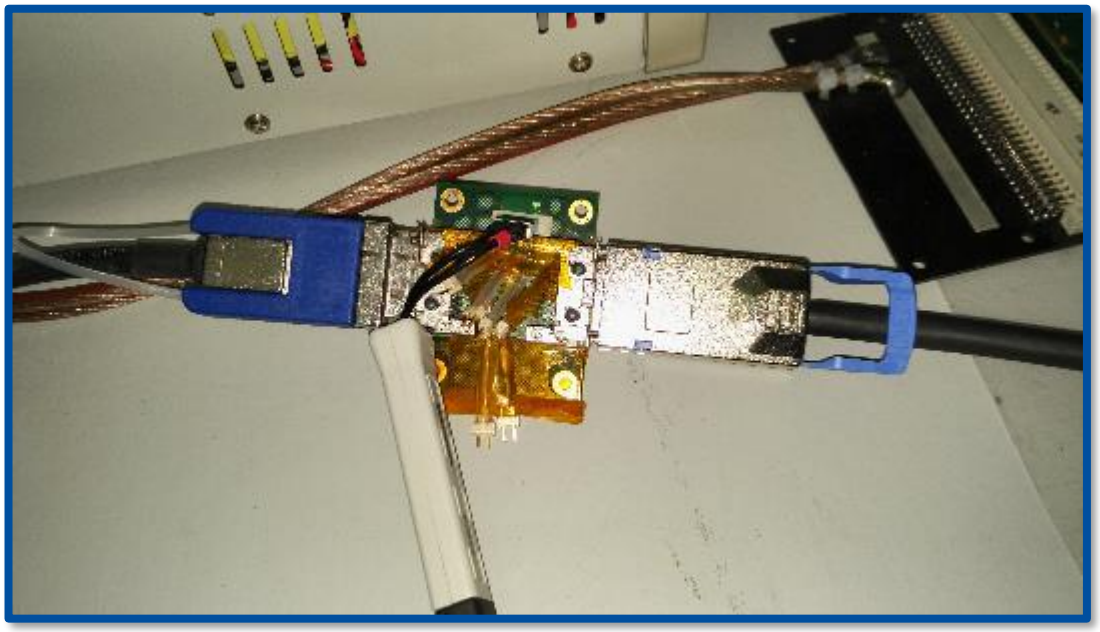



Three Infiniband connectors

Kapton + 2m Infiniband + 1m Infiniband

# Test Setup



Three Infiniband connector

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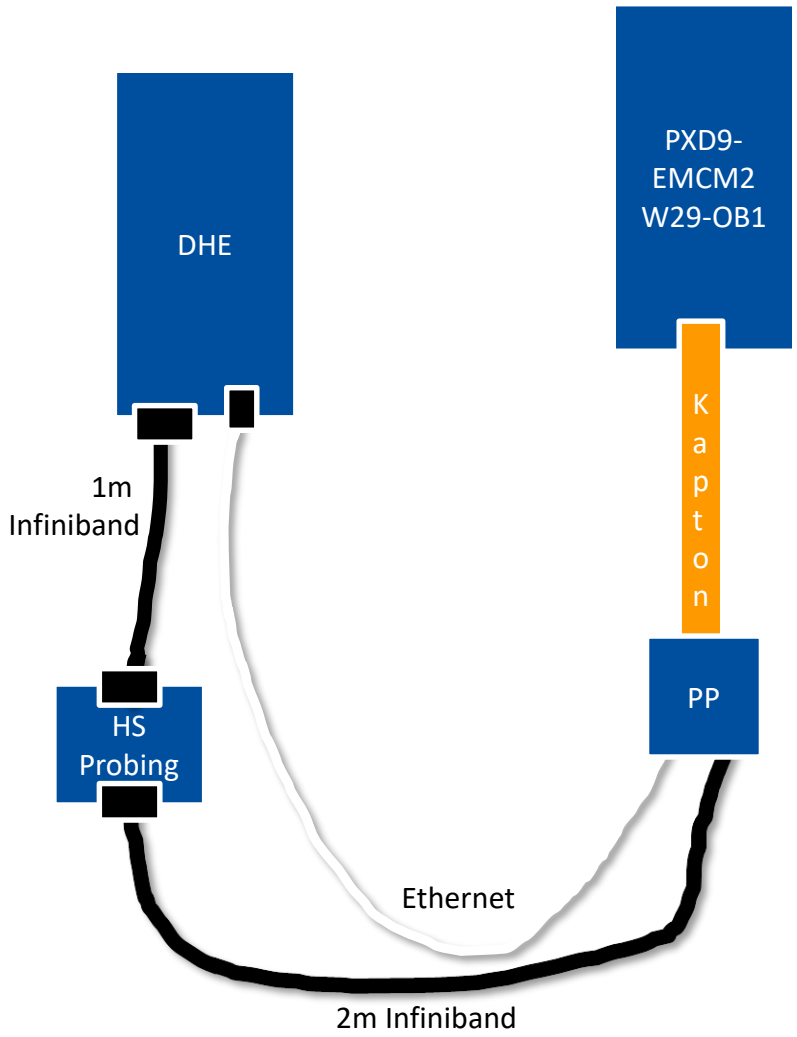
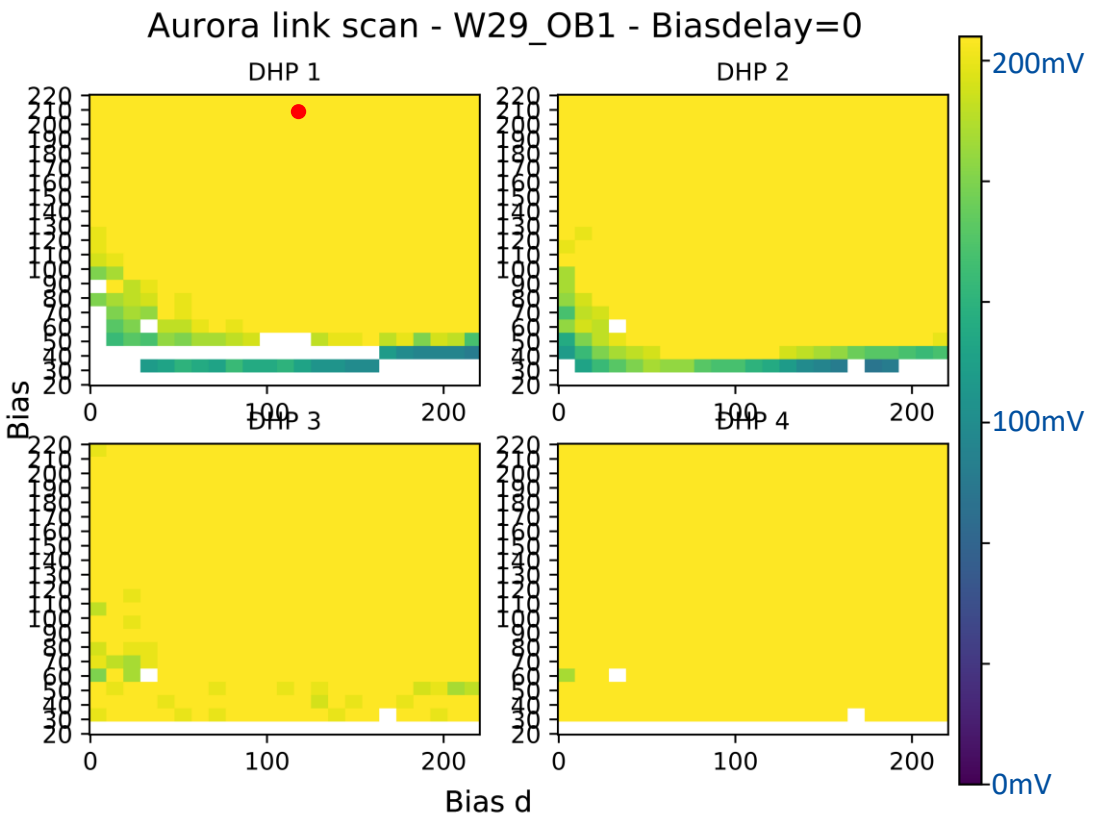
# Test Setup




- For proper operation AC coupling capacitors have been exchanged by 0Ω bridges (GCK, Trigger)
- Only DHP1 has been probed

# Signal Integrity measurements

- Signal Integrity measurements on PXD9-EMCM2 (W29-OB1)
  - AWG24, HS link scan 0.1s



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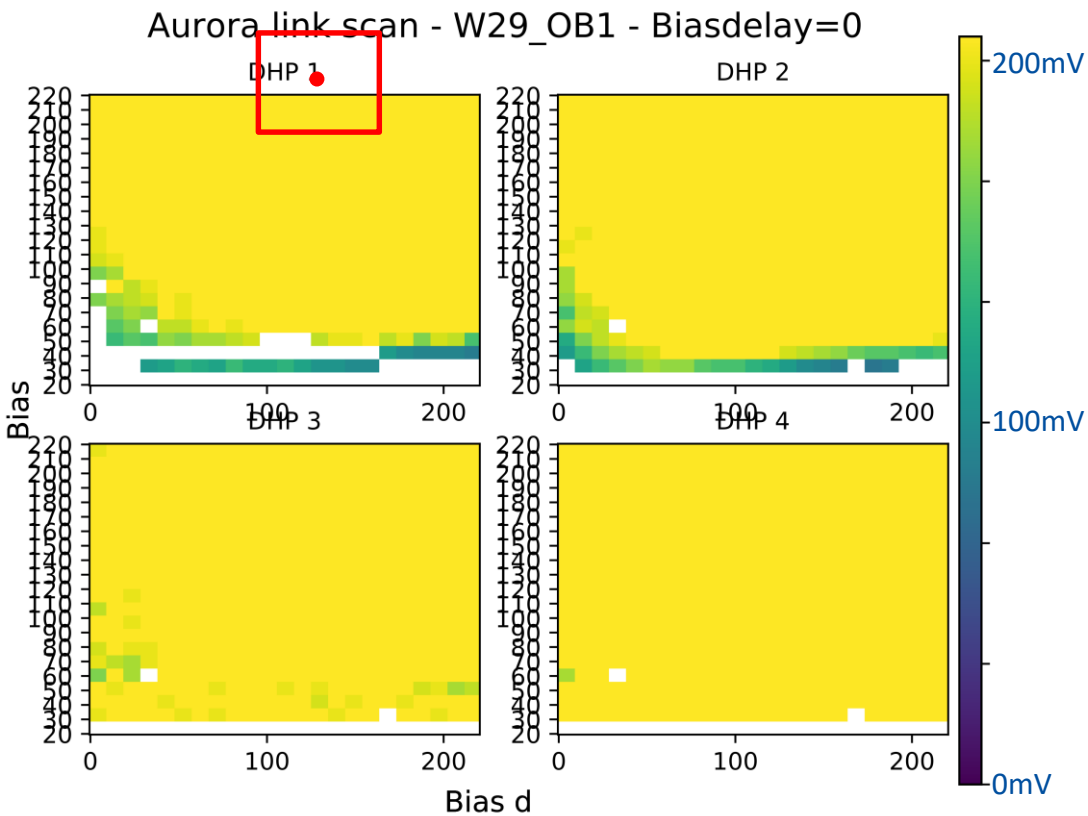
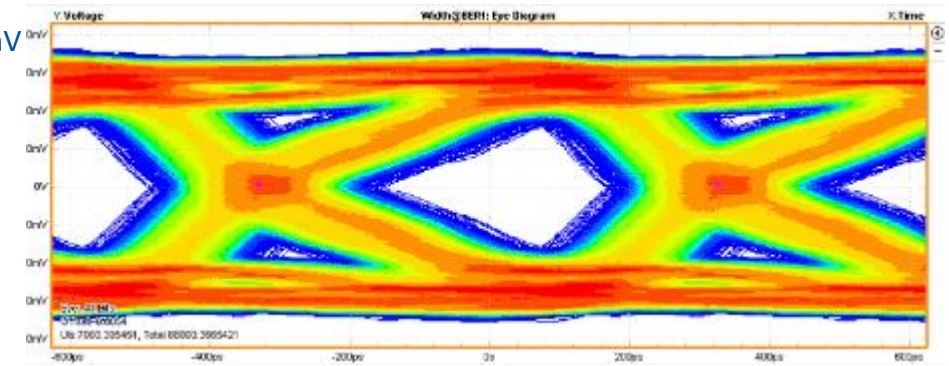


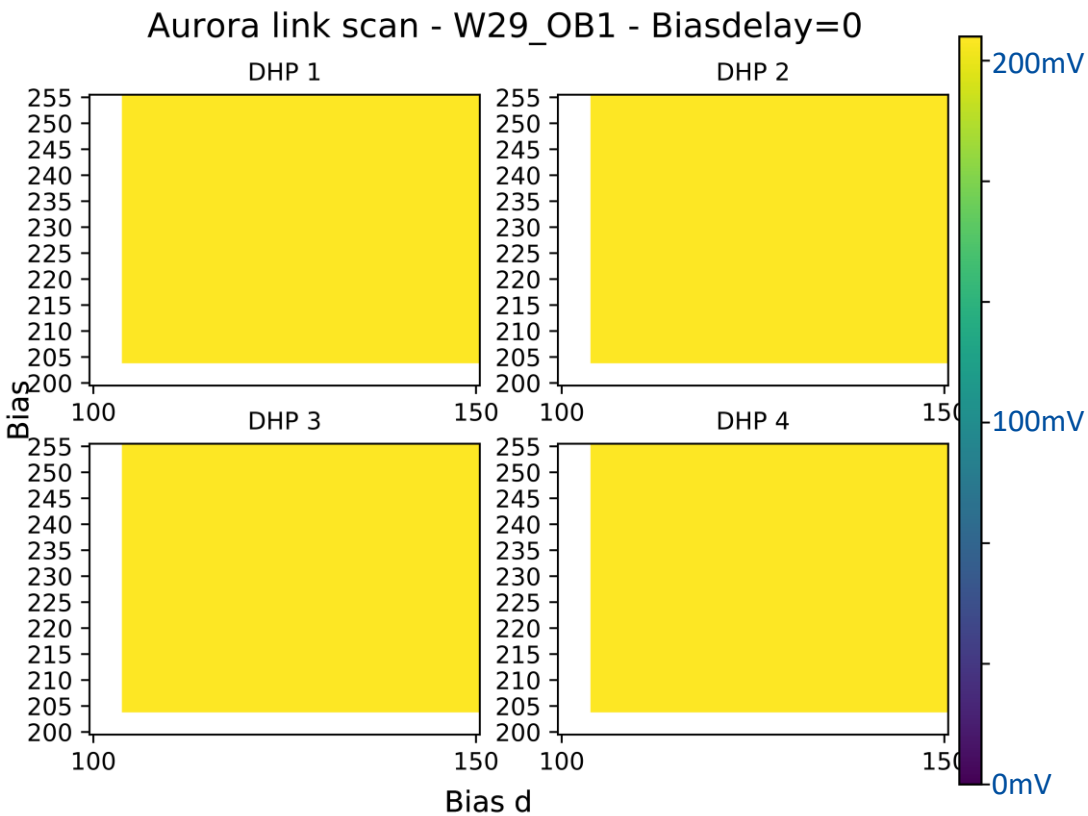
Opening ~ 220mV @ t=0ps (nominal)

Why Asymmetry ?

Why large Jitter content ?

# Signal Integrity measurements

- Signal Integrity measurements on PXD9-EMCM2 (W29-OB1)
  - AWG24, HS link scan 5min

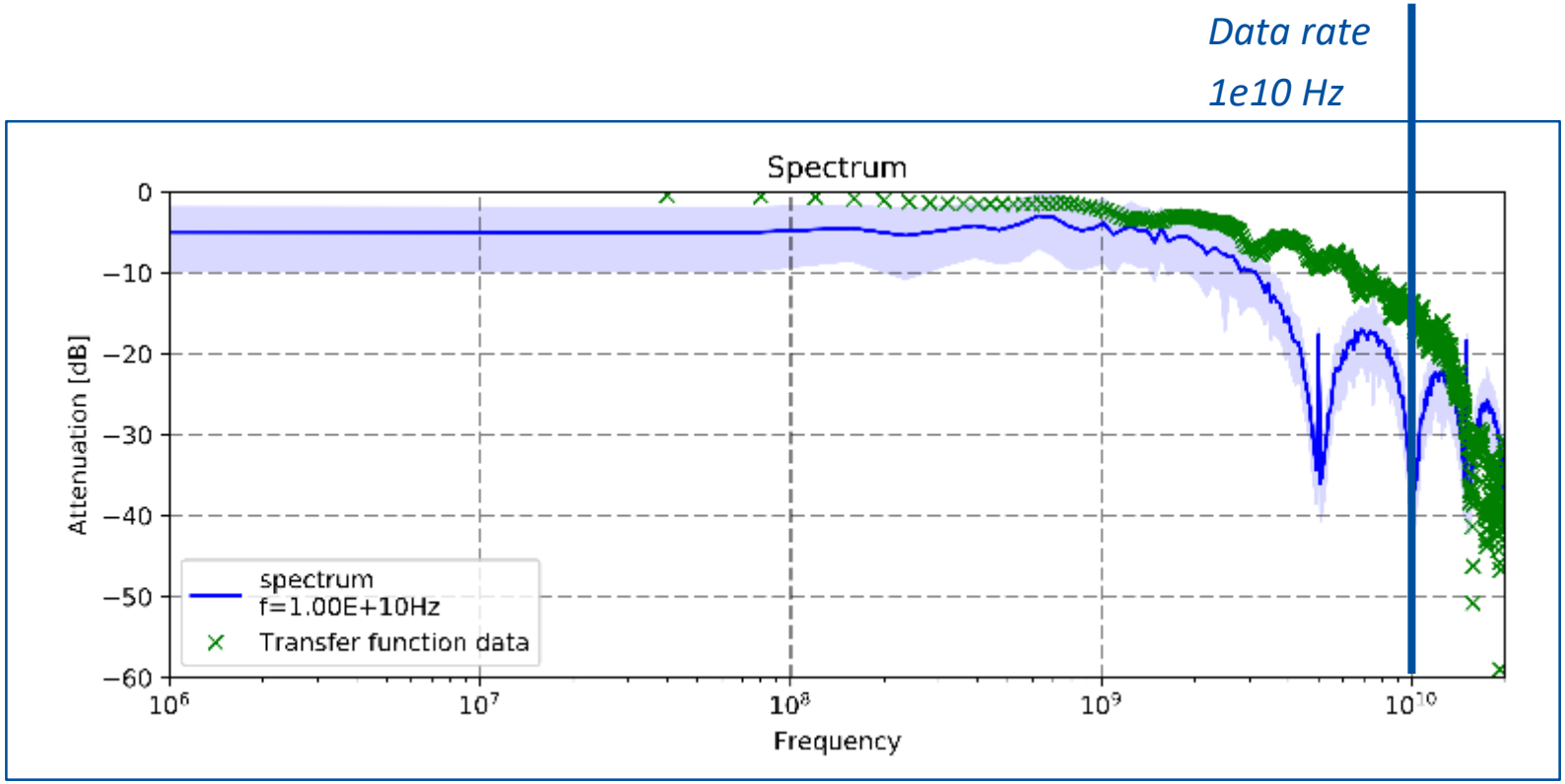



| B, bd dly=0 | Vertical Opening [mV] stdDev 10mv | Jitter Deter. [ps] stdDev 2ps | Jitter Rand. [ps] stdDev 0.5ps |
|---|---|---|---|
| 200,100 | 225 | 263 | 24 |
| 200,150 | 232 | 234 | 21 |
| 255,100 | 225 | 268 | 21 |
| 255,150 | 228 | 224 | 18 |
| 225,125 | 233 | 238 | 20 |

# Signal Integrity Simulation Examples

One cause of Data Dependent Jitter (included in deterministic jitter)

- Inter-symbol interference



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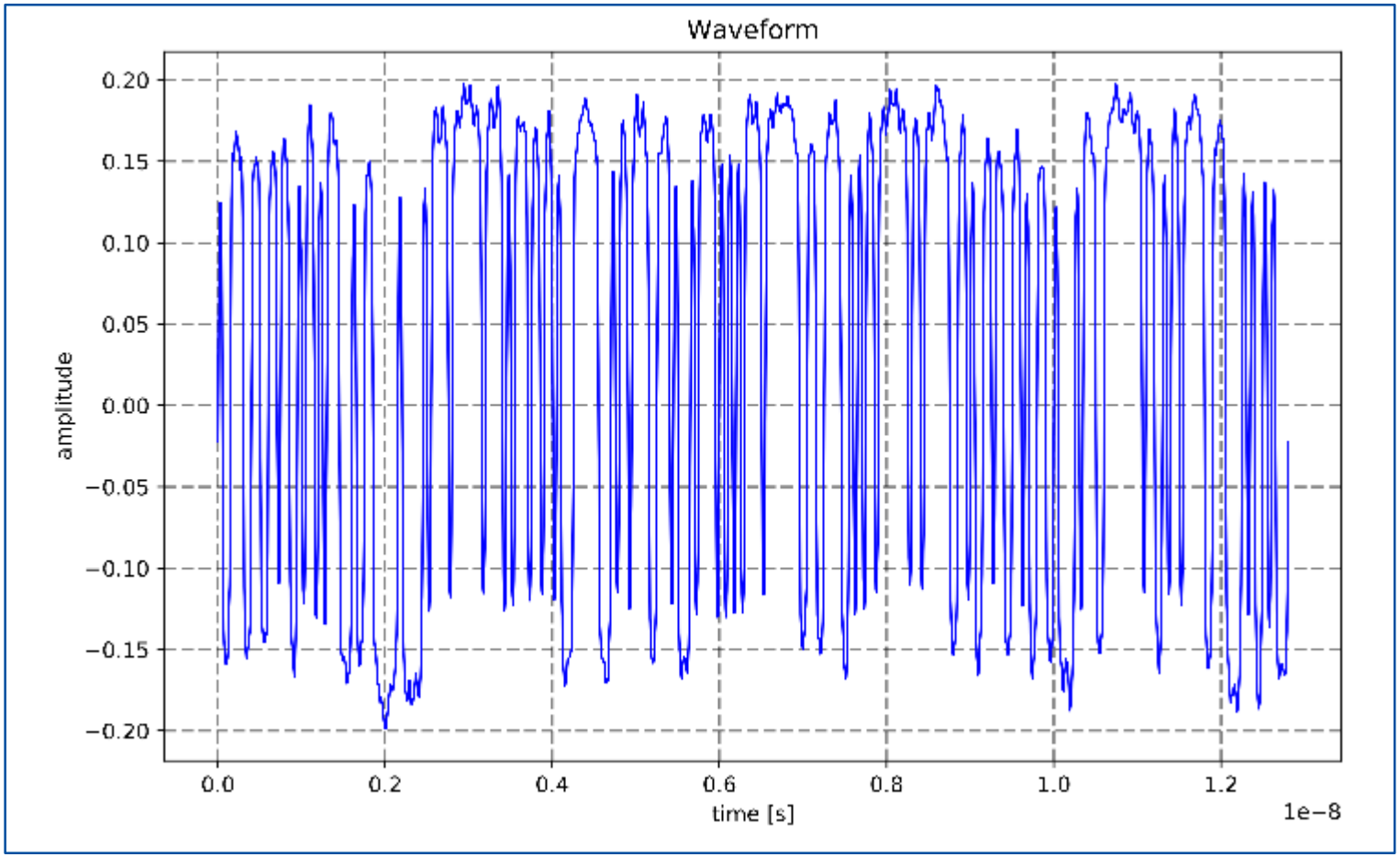

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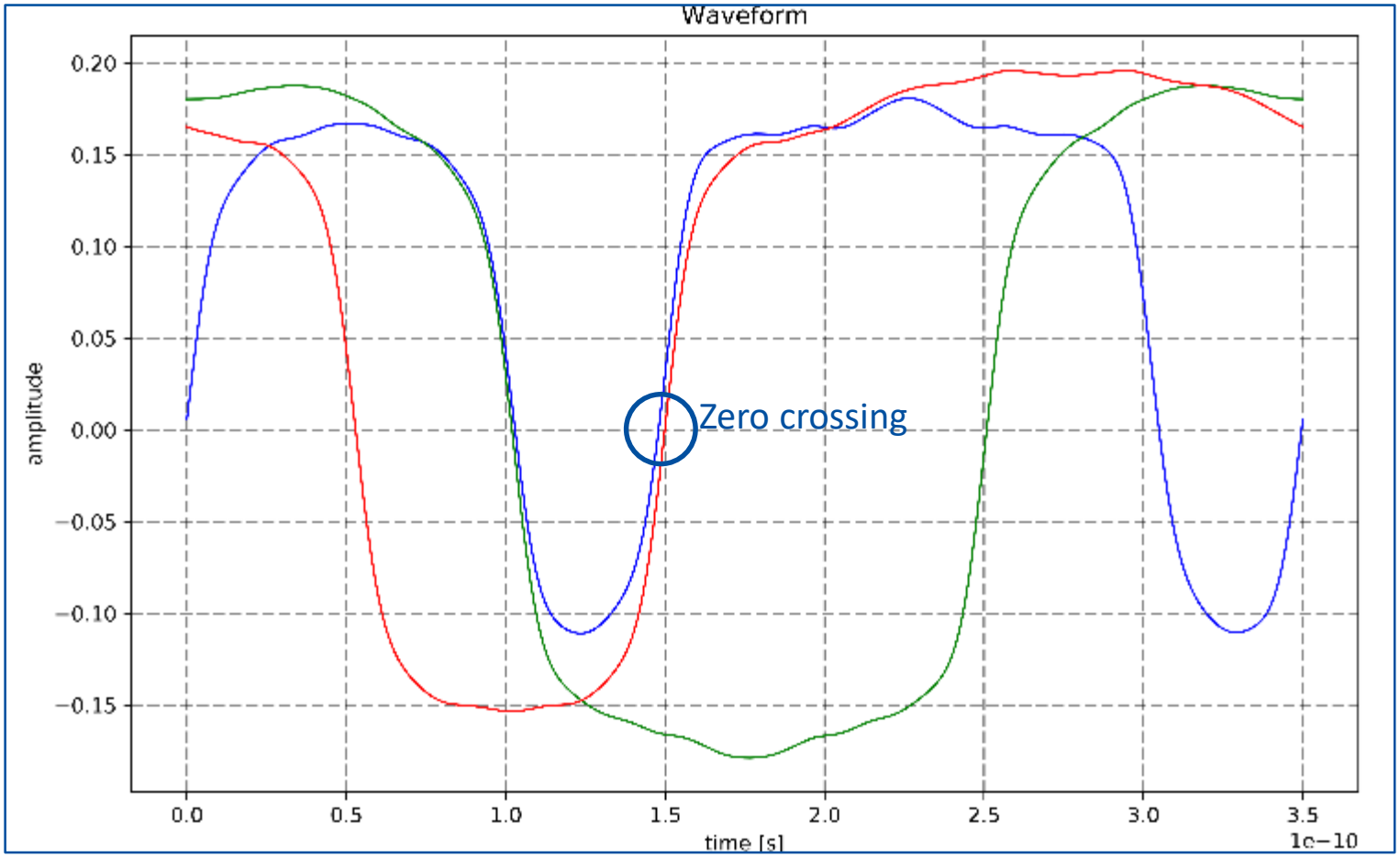

# Signal Integrity Simulation Examples

One cause of Data Dependent Jitter (included in deterministic jitter)

- Inter-symbol interference (ISI)

Cure ISI with limiting bandwidth (low frequency suppression)

- 8b/10b encoding (max. 4/5bits of equal value)

Example Simulation:

| Jitter Deter. [ps] 7 bit LFSR | Jitter Deter. [ps] Data 8b/10b |
|---|---|
| ~260 | ~180 |

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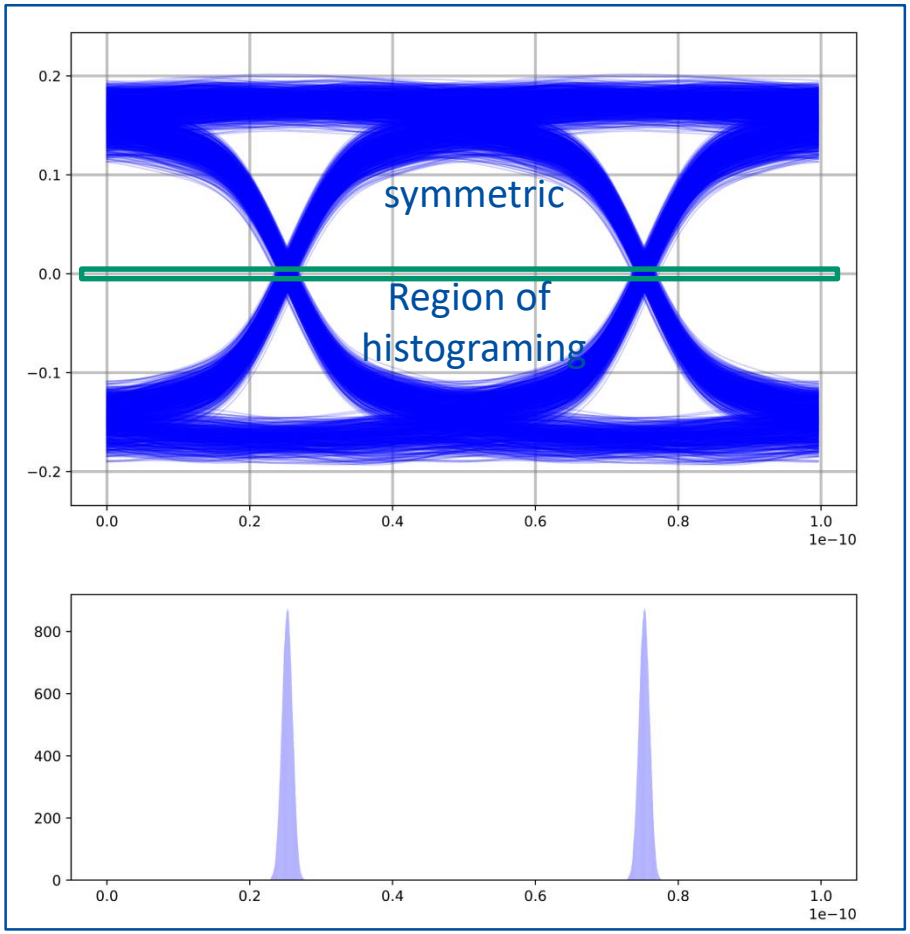
Example Simulation:

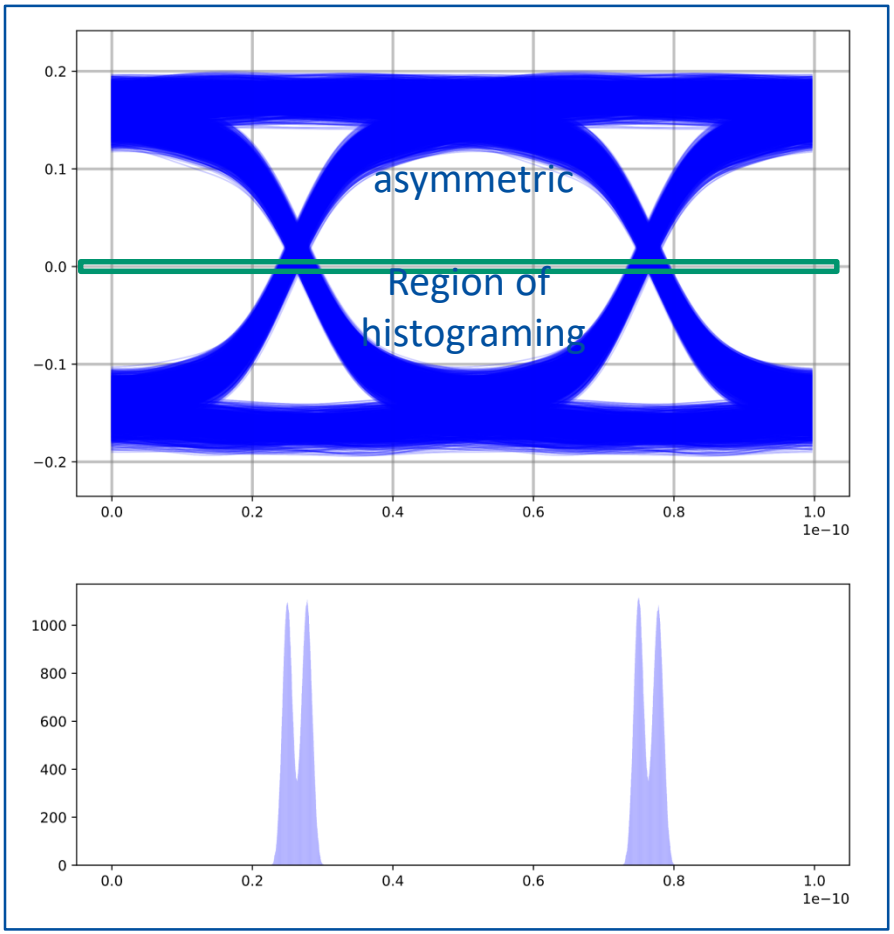
| Jitter Deter. [ps] 7 bit LFSR | Jitter Deter. [ps] Data 8b/10b |
|---|---|
| ~260 | ~180 |

Additional cause: Asymmetric edges (rise and fall times)

# Signal Integrity Simulation Examples

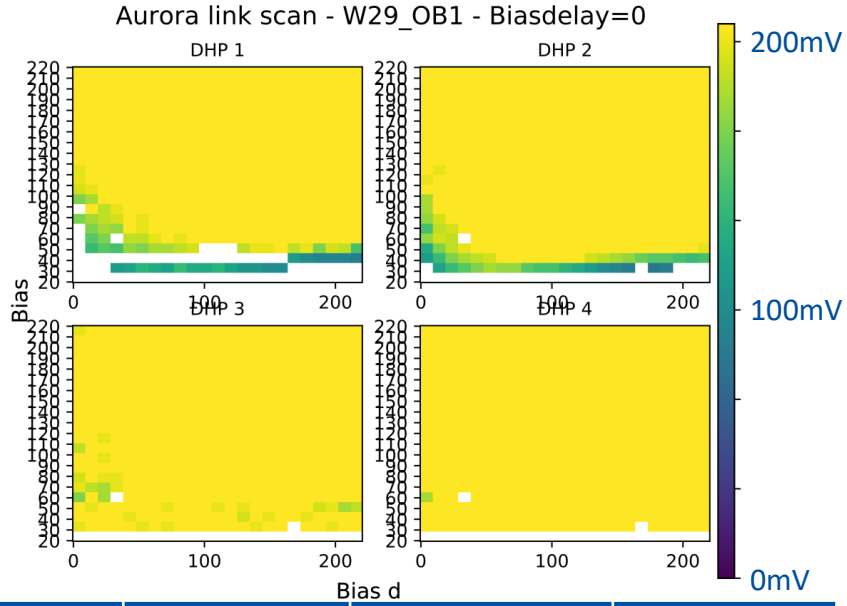
One cause of asymmetric edges (included in deterministic jitter)



# Signal Integrity measurements

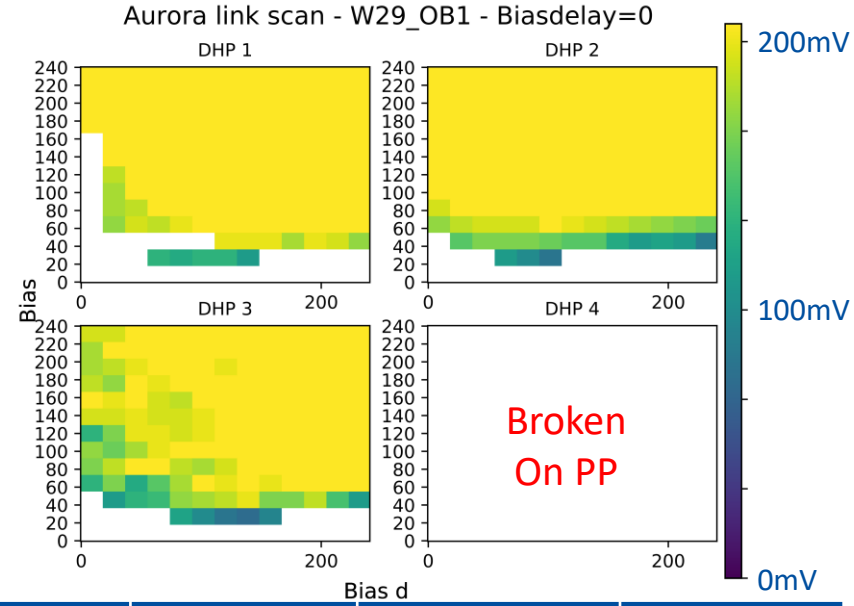
## AWG 24 fast scan 0.1s




| B, bd dly=0 | Vertical Opening [mV] | Jitter Deter. [ps] | Jitter Rand. [ps] |
|---|---|---|---|
| 200,100 | 225 | 263 | 24 |
| 200,150 | 232 | 234 | 21 |
| 255,100 | 225 | 268 | 21 |
| 255,150 | 228 | 224 | 18 |
| 225,125 | 233 | 238 | 20 |

vs

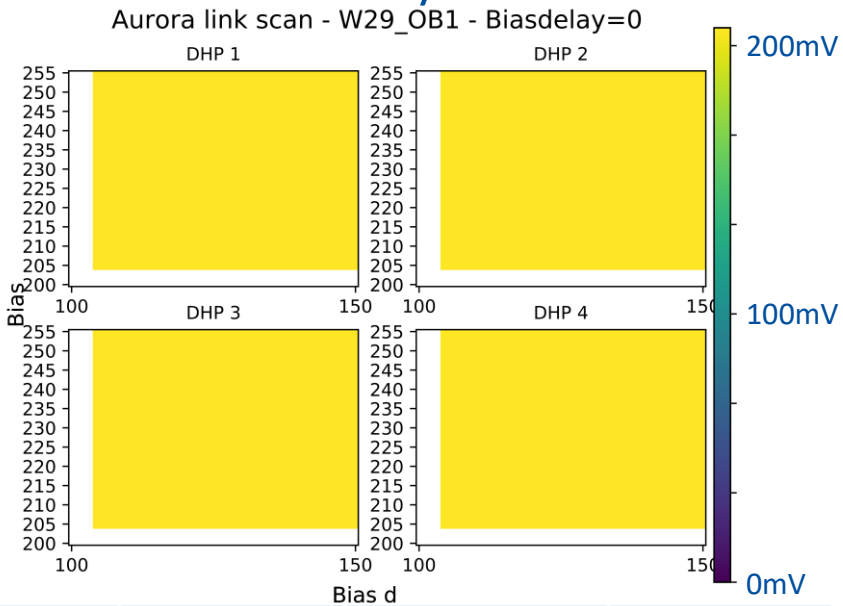
## AWG 28 fast scan 0.1s

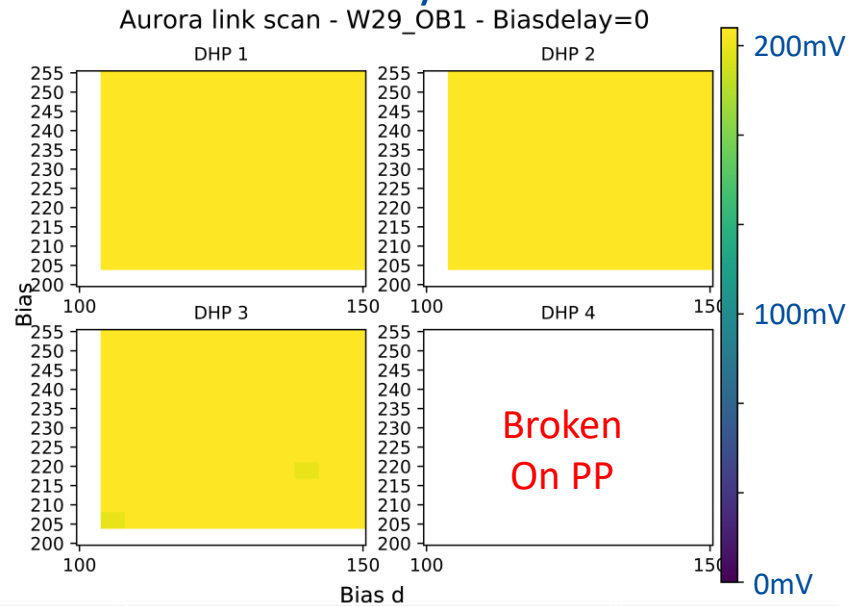



| B, bd dly=0 | Vertical Opening [mV] | Jitter Deter. [ps] | Jitter Rand. [ps] |
|---|---|---|---|
| 200,100 | 174 | 358 | 20 |
| 200,150 | 182 | 315 | 21 |
| 255,100 | 171 | 309 | 21 |
| 255,150 | 184 | 326 | 20 |
| 225,125 | 184 | 339 | 21 |

# Signal Integrity measurements

## AWG 24 stability scan 5min vs AWG 28 stability scan 5min



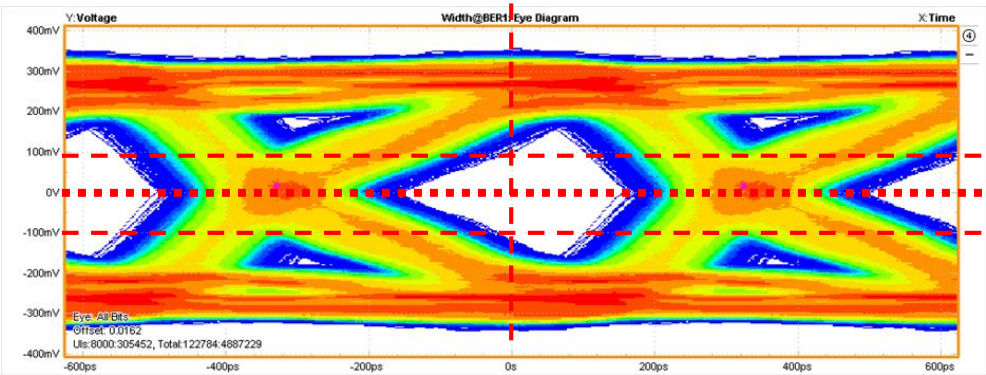



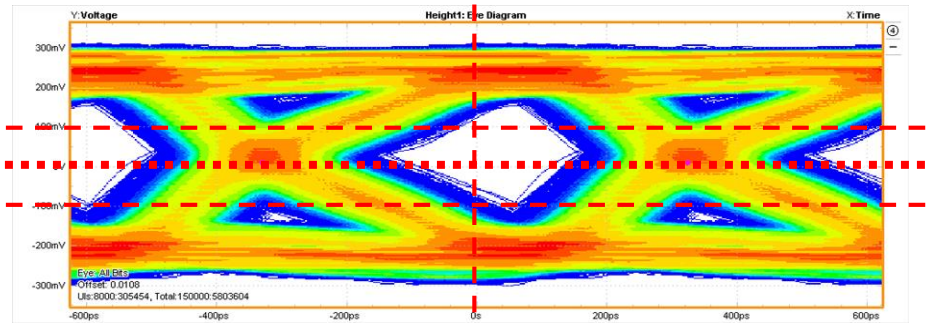

| B, bd dly=0 | Vertical Opening [mV] | Jitter Deter. [ps] | Jitter Rand. [ps] |
|---|---|---|---|
| 200,100 | 225 | 263 | 24 |
| 200,150 | 232 | 234 | 21 |
| 255,100 | 225 | 268 | 21 |
| 255,150 | 228 | 224 | 18 |
| 225,125 | 233 | 238 | 20 |

| B, bd dly=0 | Vertical Opening [mV] | Jitter Deter. [ps] | Jitter Rand. [ps] |
|---|---|---|---|
| 200,100 | 174 | 358 | 20 |
| 200,150 | 182 | 315 | 21 |
| 255,100 | 171 | 309 | 21 |
| 255,150 | 184 | 326 | 20 |
| 225,125 | 184 | 339 | 21 |

# Signal Integrity measurements

AWG24 opt. eye vs AWG 28 opt. eye




| B, bd dly=0 | Vertical Opening [mV] | Jitter Deter. [ps] | Jitter Rand. [ps] |
|---|---|---|---|
| 200,100 | 225 | 263 | 24 |
| 200,150 | 232 | 234 | 21 |
| 255,100 | 225 | 268 | 21 |
| 255,150 | 228 | 224 | 18 |
| 225,125 Optimal | 233 | 238 | 20 |

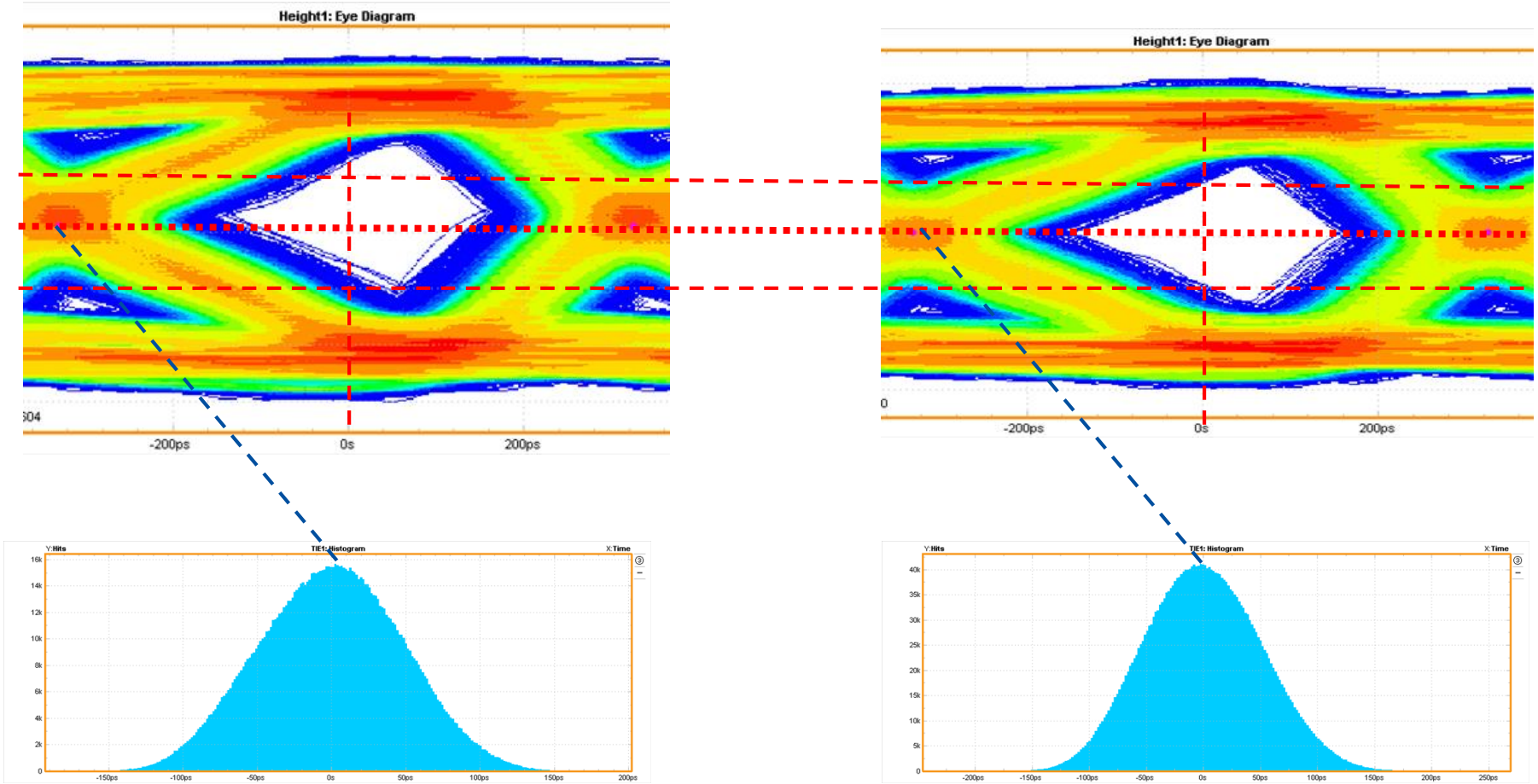
| B, bd dly=0 | Vertical Opening [mV] | Jitter Deter. [ps] | Jitter Rand. [ps] |
|---|---|---|---|
| 200,100 | 174 | 358 | 20 |
| 200,150 | 182 | 315 | 21 |
| 255,100 | 171 | 309 | 21 |
| 255,150 | 184 | 326 | 20 |
| 225,125 | 184 | 339 | 21 |
| 255,255 optimal | 200 | 273 | 20 |

# Signal Integrity measurements

AWG 28 7bit LFSR
200 mV, DJ 273ps

vs

AWG 28 8b/10b
220mV, DJ 240ps



# Summary

We conclude…

- Eye opening of PDPP_L2BWD-03 (AWG 24) ~ 230mV

  compared to

  Eye opening of PDPP_L2BWD-04 (AWG 28) ~ 200mV

- High jitter though
  - Further investigation needed

# Summary

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What have we learned so far?

- Signal integrity highly depends on system
  - Hybrid 5 (Infiniband only) vs EMCM2 (Kapton+PP+Infiniband)
  - Impedance discontinuities has a high impact
    → Quality control of PP (soldering, etc.)

- Additional optimization
  - Understanding the source of jitter (GCK, DHPT PLL, …)
  - Bit Error Rate for region of interest
    - HS link scan does not give sufficient information
  - Increase statistics
    - Probe all DHP HS links
    - Test multiple PP assemblies

# Thank you

# Backup

# Mass production - What is tested?

- Sanity check
- Power consumption, visual inspection (mechanical damage)

- **Internal chip functionality**: DHP digital logic
- JTAG registers (programmability of DHP)
- Memory qualification (SRAM testing)
    - Raw data mem., Offset data mem. And Sw data mem.
- Digital logic:
    - Data processing
    - Common mode (CM) correction
- Test data with simulated CM
- Trigger zero-suppressed data

- **Interchip communication**: DHP<->DCD, DHP->Switcher and DHP<->DHE
- I/O en-/disabling
- Data transmission;
- DHP->DCD, DHP<-DCD, DHP->Switcher and DHP->DHE, DHP<-DHE
- Test pattern generation and r/w by FPGA based system
- Signal integrity, i.e. Bit Error Rate

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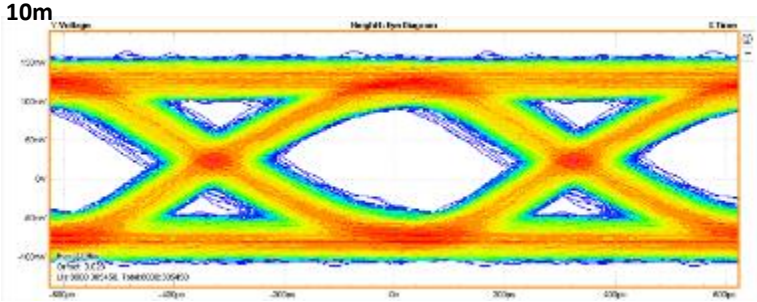
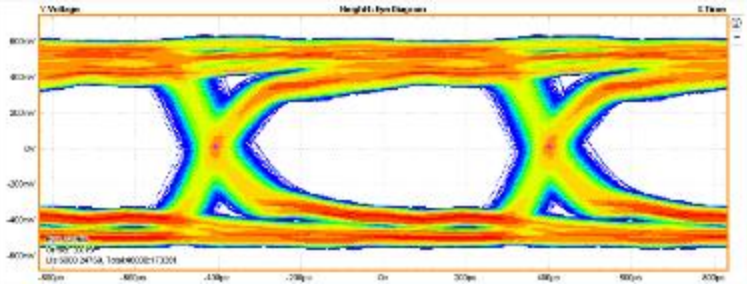
(6 connectors)

DHE<->BB<->**Probe<->Hyb5**
1m 1m **10m**

Bias 65
Biasd 255
Biasdly 0
opening ~ 117mV



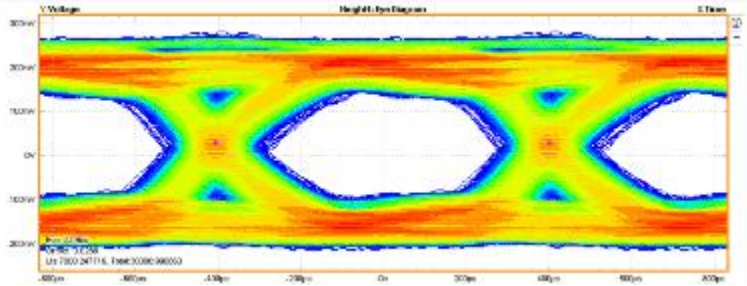
(4 connectors)



DHE<->BB==**Probe<->Hyb5**
1m **1m**

Bias 255
Biasd 0
Biasdly 0

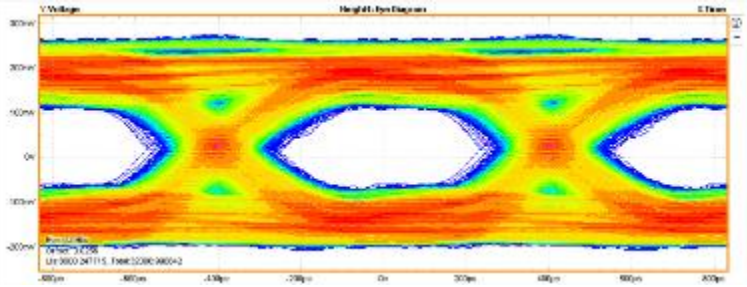
opening ~ 656mV



DHE<->BB==**Probe<->Hyb5**
1m **10m**

Bias 120
Biasd 255
Biasdly 0

opening ~ 285mV



DHE<->BB==**Probe<->Hyb5**
1m **15m**

Bias 120
Biasd 255
Biasdly 0

opening ~ 172mV