Plans for series module testing at MPP

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HALBLEITERLABOR
DER MAX-PLANCK-GESELLSCHAFT

measurements for each module in detail

- power up and JTAG configuration, voltage checks (digital, analog, matrix)
- JTAG Boundary-Scan
- DHPT link parameter
- DHPT - DCD communication delay-scan
- pedestals (number of working pixels)
- ADC transfer curves
- 2bit offset DACs
- sample point
- DEPFET optimization with Cd-109 source
- clear efficiency with infrared laser
- Gated Mode

- Optimal settings will be detected in those tests and will be stored in a configuration database.
  > 10 000 process variables per module
- Analyzed data/results will be uploaded to a production database. Upon this basis the modules will be evaluated and sorted in to classes.
- The best modules will be used for the PXD.

Responsibilities lab_framework

Responsibilities

Philipp Wieduwilt posted on 09. Mar. 2017 14:32h · last edited by Christian Koffmane on 22. Mar. 2017 17:19h

See the following table for assignment of responsibilities for the lab-framework software development.

measurement	responsibility	tested on new PXD9	comply with coding guidelines	to do	comment
HS Link Scan	Bonn	TESTED @ TB	NO		
HS Link iBert Scan	Bonn/Munich	IN DEVELOPMENT	NO		
Delays	Bonn	TESTED @ TB	NO		
ADC Optimization (also calibration (DHE current source))	Gö	TO BE TESTED @ PERSY	NO	test on new PXD9 modules	
Offset DACs & Pedestals	Bonn/Munich	TO BE TESTED @ PERSY	NO		
Gated Mode (& clear efficiency)	HLL/MPP	MEASURED @ HLL	NO		setup specific, like pulse generator and laser control
Source Scans	HLL/MPP	TO BE TESTED @ PERSY	NO		
Laser Scans	HLL/MPP	TO BE TESTED ON PXD9	NO		setup dependent (control of laser)
DHP Temperature Diode	Bonn	IN DEVELOPMENT	NO		
DEPFET IV-curve	Gö/Munich	IN DEVELOPMENT	NO		characterization of DEPFET, determine threshold voltage for radiated modules
sample point curve	Bonn/Munich	IN DEVELOPMENT	NO	verify fast enough DCD sampling time	
mapping.py and Plotting	Gö	IN DEVELOPMENT	NO	use u-v coordinates, label ASICs in plots, rotate by 90°	decided to use Belle II mapping and displaying of matrix frames
number of bad pixles	IFIC/Munich	IN DEVELOPMENT	NO	compare pedestal maps for different gate on voltages	should be part of the probe card testing before the kapton attachment
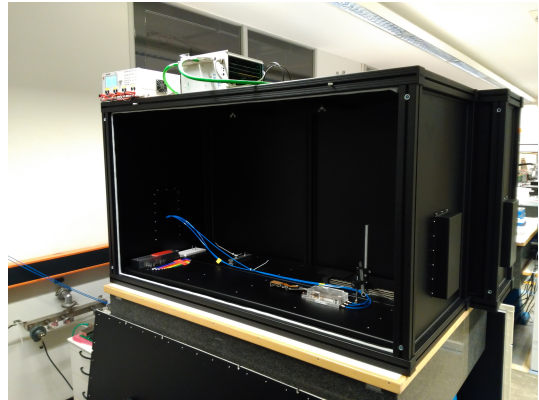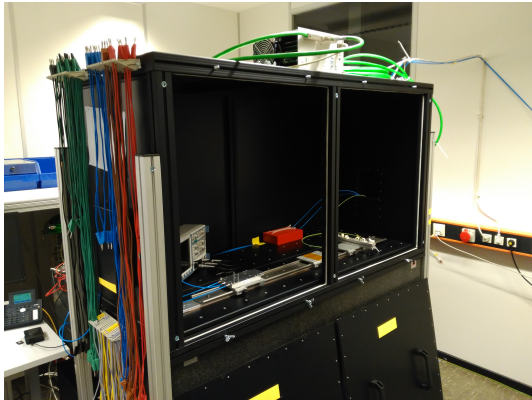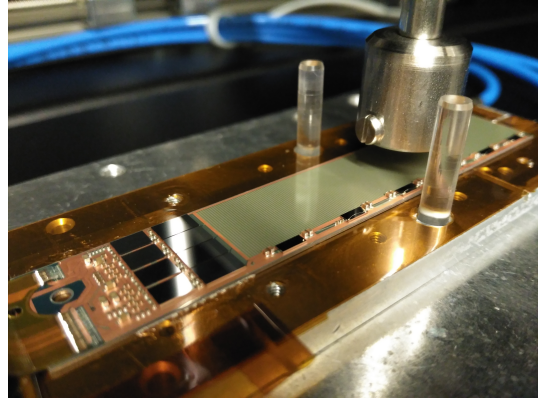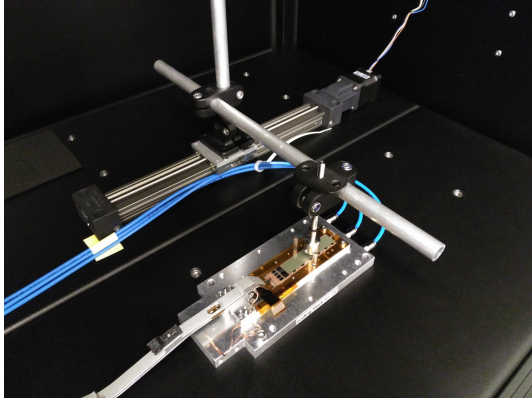
What do we want to do?
What we can do:

- cool down the cooling jig to about $-30°C$ with the Julabo chiller
- flush with N_2 to avoid condensation
- make a "cold start" of the module and perform sanity checks
  (voltages / currents, JTAG configuration / readout)
- monitor the temperature at the module / base jig (DHPT sensor?)
  (find a way to determine when stable conditions are reached)

- Do we want to run at further temperatures / do thermo cycles?
  $\rightarrow$ time constraints!