Front End Read-Out for Fast Photosensors

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Outlook

I. **Introduction**
II. PACTA: High Dynamic range Preamp
III. MUSIC: Multipurpose SiPM RO chip
IV. FlexToT: linearized ToT RO chip
V. New developments

I. Introduction

- Plenty of readout ASICs for photosensor read-out…

Chip name	group	year	Technology	channels	Application
FLC_SiPM	OMEGA	2004	BiCMOS 0.8µm	18	ILC HCAL
NINO	CERN	2004	CMOS 0.25µm	8	ALICE TOF
MAROC2	OMEGA	2006	SiGe 0.35µm	64	ATLAS lumi
SPIROC	OMEGA	2007	SiGe 0.35µm	36	ILC HCAL
PETA	Heidelberg	2008	CMOS 0.18µm	40	PET
RAPSODI	Krakow	2008	CMOS 0.35µm	2	Snooper
BASIC	Bari	2009	CMOS 0.35µm	32	PET
SPIDER	Ideas	2009	CMOS 0.35µm	64	Spider rich

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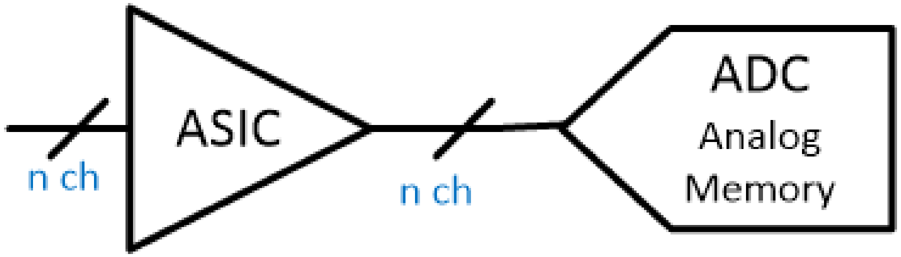
- New members: STiC, Petiroc, Citiroc, ToFPET, PACIFIC, etc

I. Introduction

- Many of them are designed for specific applications
  - Of course… they are **AS**ICs
  - However it means that the readout architecture constrains the use of the chip to particular systems
    - For instance many of them are designed for PET applications and it becomes difficult to use them elsewhere
- The goal of this talk is **not** to present one more ASIC
- But to discuss how to build different FE systems for different applications based on ASICs which provide
  - **Flexibility**
  - **High performance**

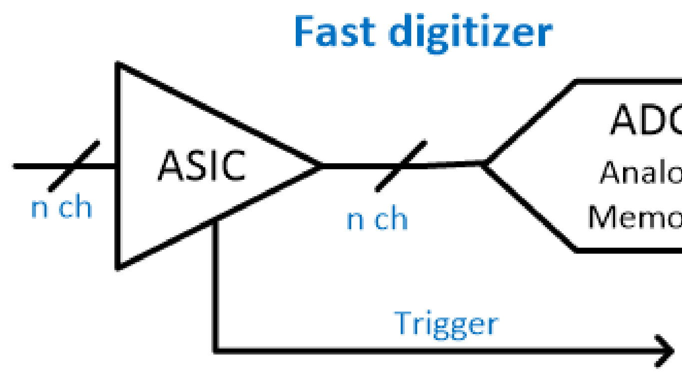
I. Introduction

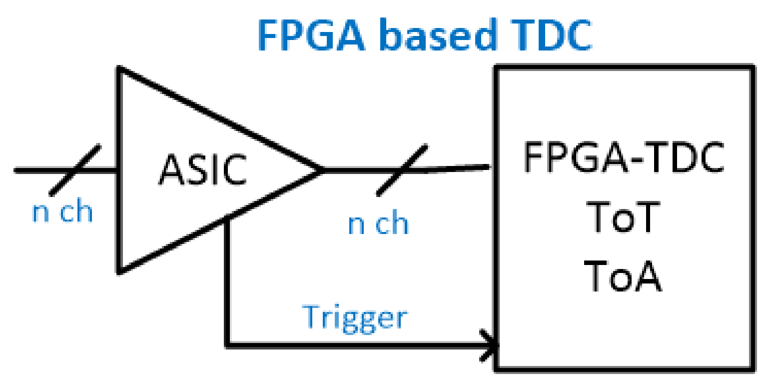
- **Our approach combines:**
  - **An ASIC performing key analog functions**
  - **A digitizer that can be adapted and optimized for a given application**



I. Introduction

- This digitizer can range from:
  - A high performance waveform sampling system (SCA)
    - Many examples: DRS, NECTAr, SAM, etc
  - A TDC based on a low cost FPGA
    - 10 ps resolution is possible





I. Introduction

- **Regarding the ASIC: what key analog functionalities should it perform?**
  - Impedance adaptation
  - Current mode approach for timing
    - High speed & low noise
  - Input voltage control (for SiPMs)
  - Shaping
  - Summation
    - To build large are photodetectors
  - Discrimination
  - Time-over-threshold (ToT)
    - Linearization
    - Low cost digitizer (FPGA TDC)

All our designs (Impedance adaptation; Current mode approach for timing; Input voltage control)

Section III (MUSIC chip) (Shaping; Summation; Discrimination)

Section IV (FlexToT chip) (Discrimination; Time-over-threshold (ToT))

I. Introduction

- Must say we did not invent this approach…

NINO

Chip designed by CERN group for ALICE TOF RPCs

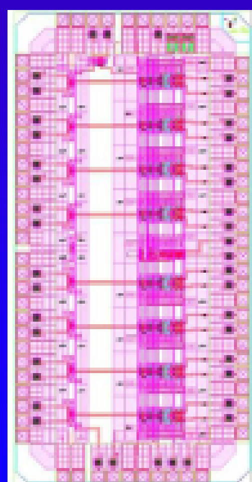
[F. Anghinolfi, P. Jarron et al. NINO: an ultra-fast and low-power front-end amplifier/discriminator ASIC designed for the multigap resistive plate chamber, NIM A, 2004, Vol. 533 page 183-187]

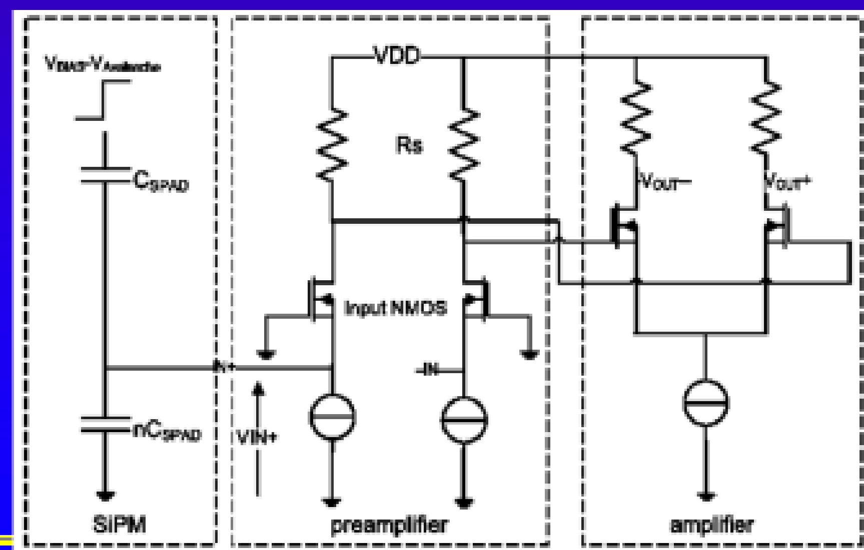
8 channels amplifier and discriminator

Common grid current conveyor, high speed differential discriminator

High speed time measurement (10 ps), Amplitude through time over threshold technique

Pd = 25 mW/ch, Manufactured in IBM 0.25 um





15 JUN 2012 CDLT PHOTODET CONFERENCE

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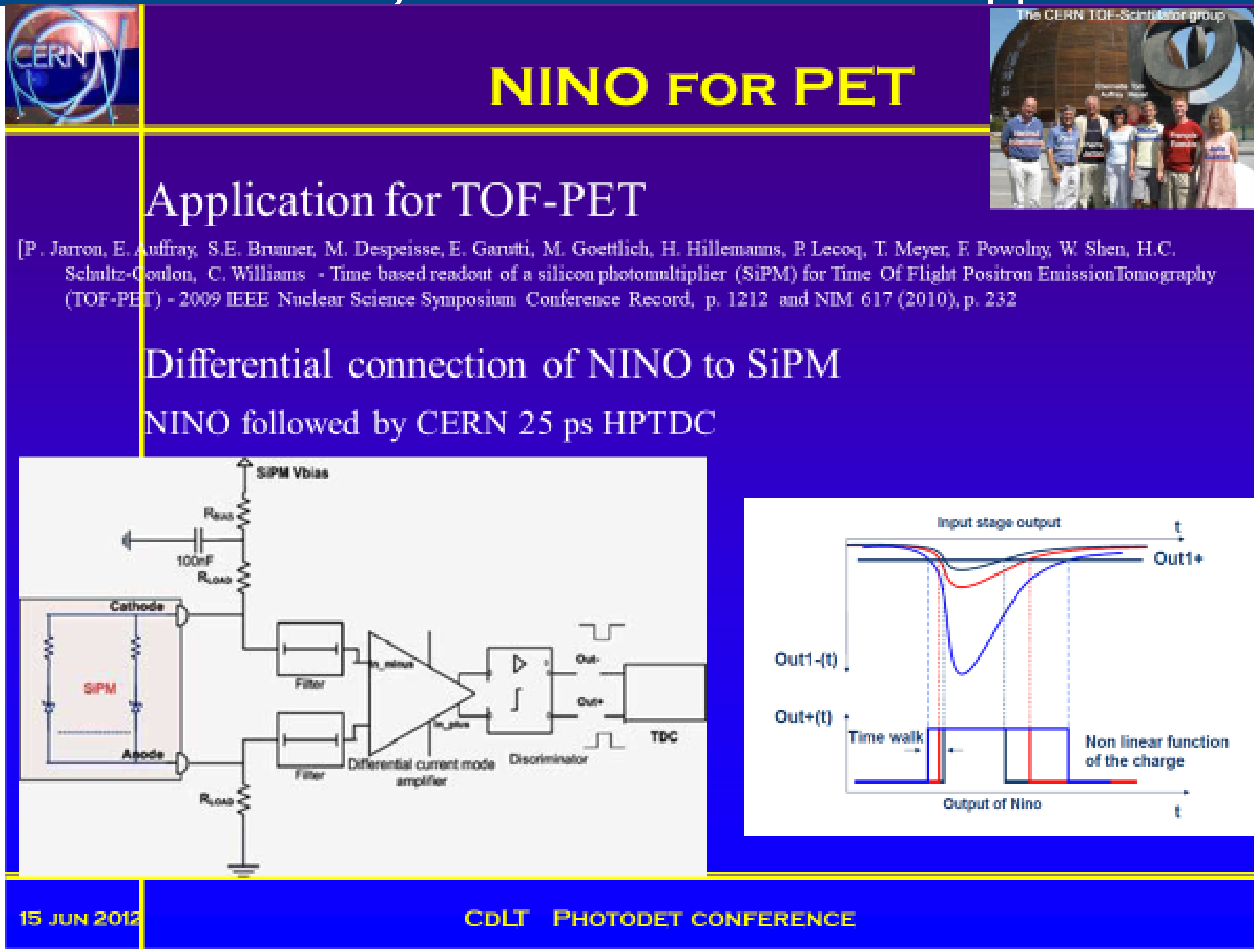
I. Introduction

- Must say we did not invent this approach…



Outlook

I. Introduction

II. PACTA: High Dynamic range Preamp

III. MUSIC: Multipurpose SiPM RO chip

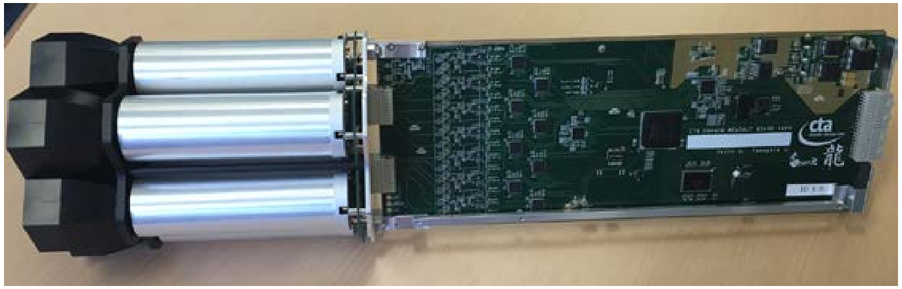
IV. FlexToT: linearized ToT RO chip

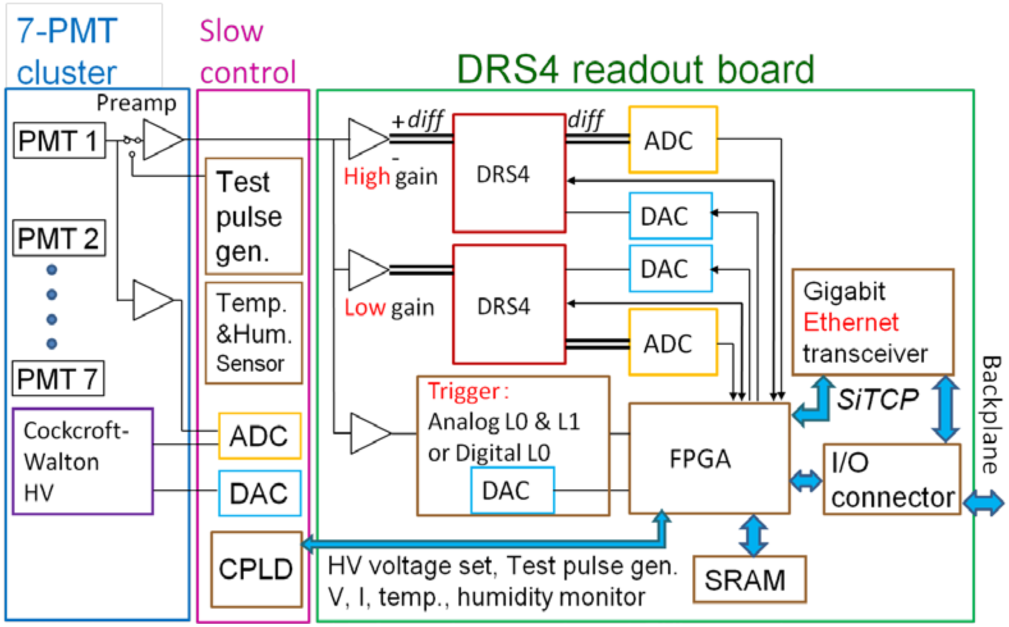
V. New developments

II. PACTA: High Dynamic range Preamp

- CTA LST and MST (NECTAr) cameras
  - Based on PMT at low gain(40k)
  - Requires high dynamic range preamp
    - From single photon to > 1000 pe
    - High BW
    - Low noise
  - Readout is based on a proven concept
    - Waveform sampling at > 1 GS/s
    - Analog/digital trigger

LST cluster





LST PMT unit

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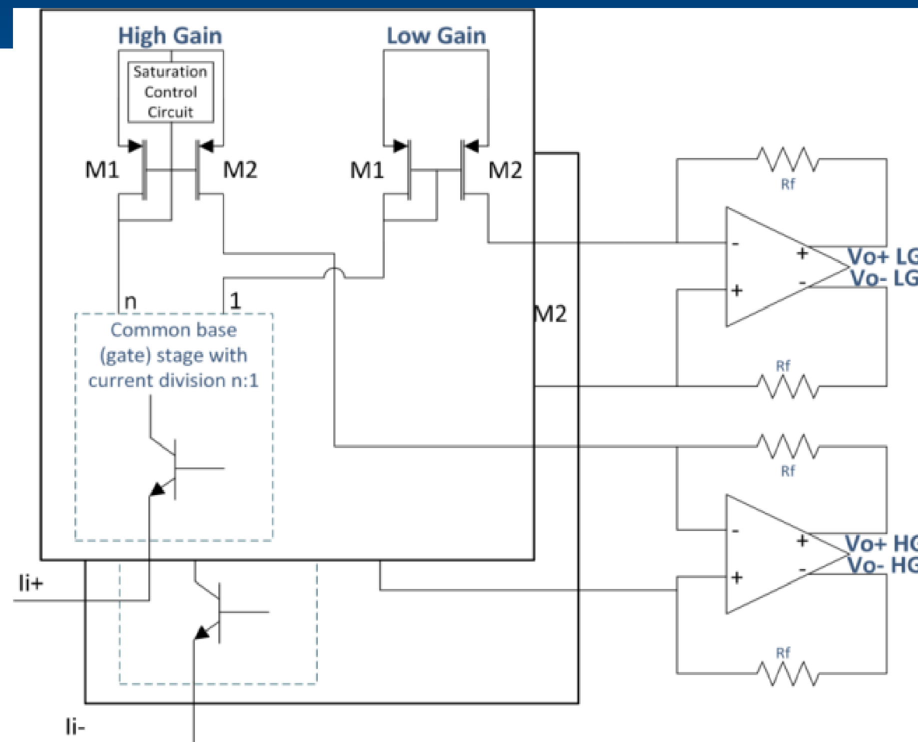
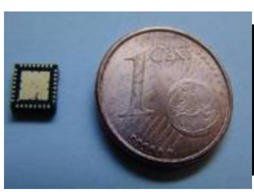
II. PACTA: High Dynamic range Preamp

- **Double transimpedance gain: 1.2kΩ (HG) and 80 Ω (LG)**
- **Dynamic range > 15 bits**
- **-3 dB bandwidth of 450 MHz**
- **Low input referred noise: 10 pA/√Hz**
- **Noise (ENC): 4700 electrons**
  - **10 ns of integration time**

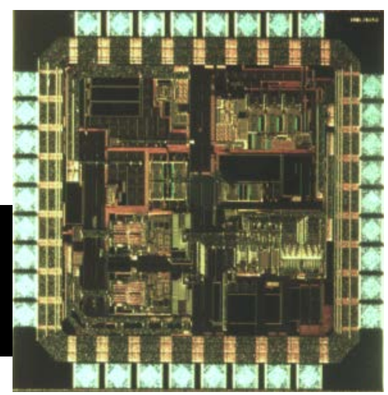


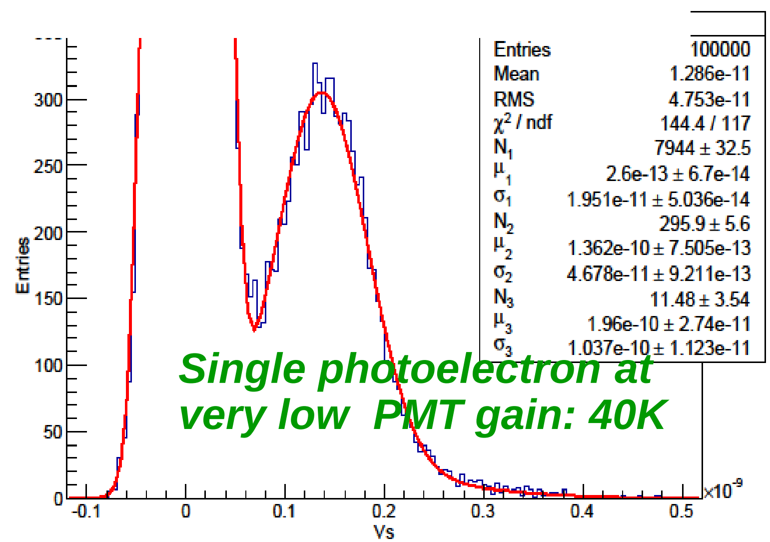
2400 chips for the first LST camera

15000 chips being produced for next LSTs and MSTs cameras



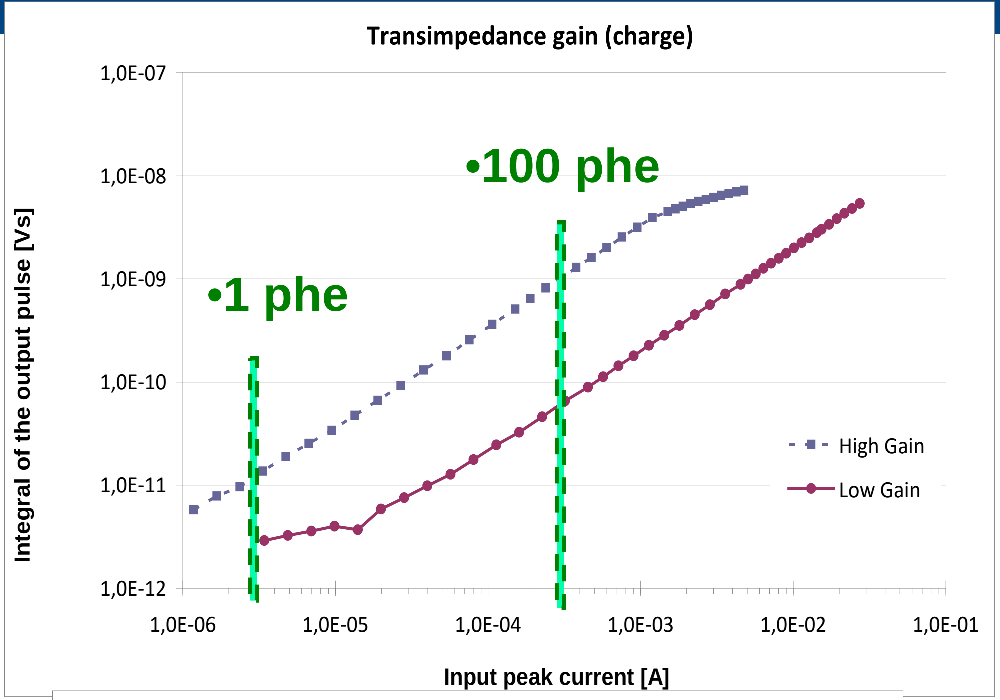
PACTAv1.4 chip 2 mm²
QFN32 package
Back from foundry Oct. 2012

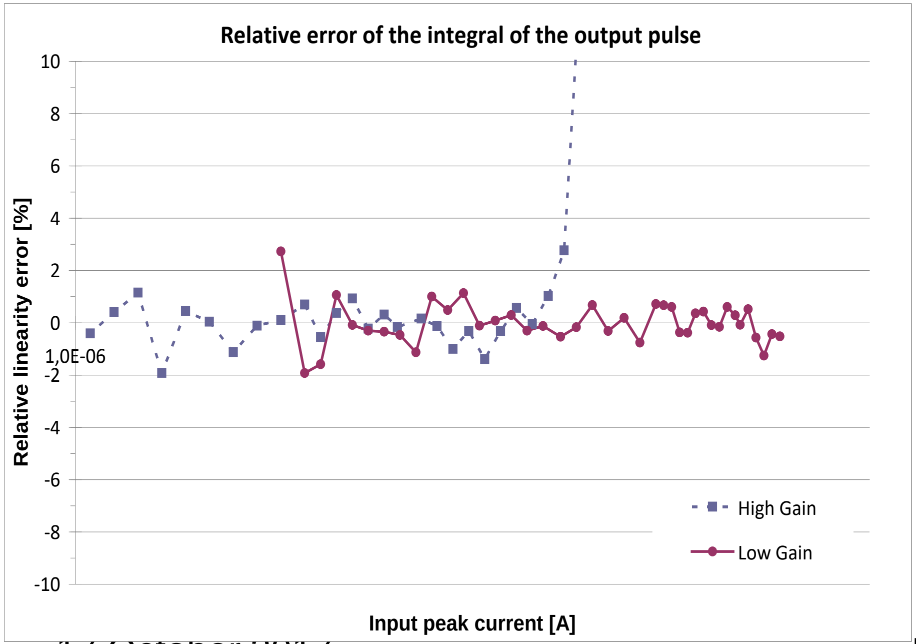


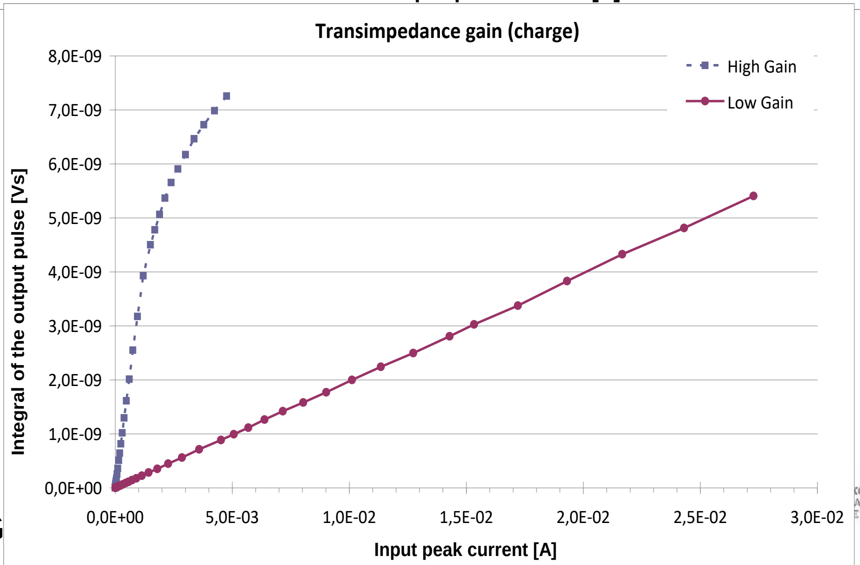


II. PACTA: High Dynamic range Preamp

- Transimpedance gain (integral of the pulse) and linearity
  - HG about 1 KOhm
  - LG about 50 Ohm
  - Relative non-linearity error < 2 %
    - 100x(Meas-Fit)/Fit

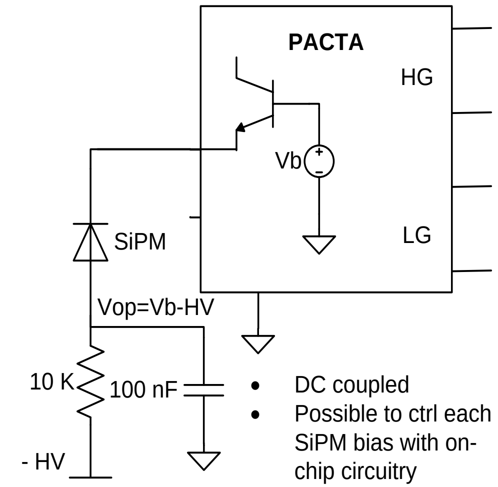




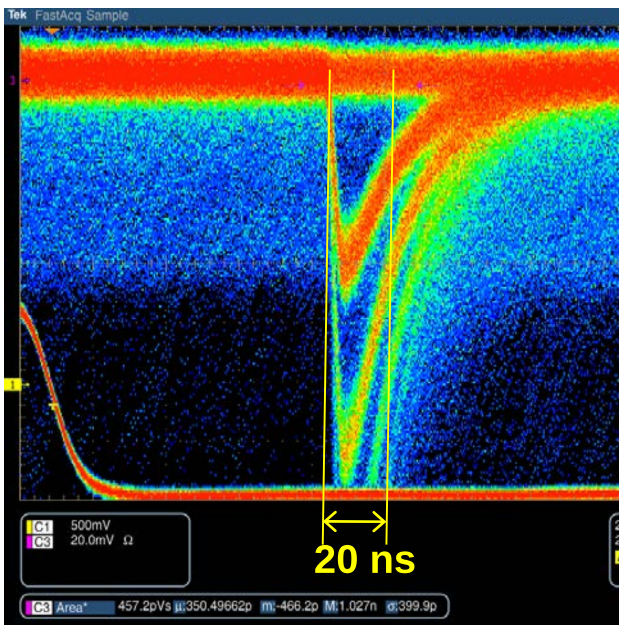


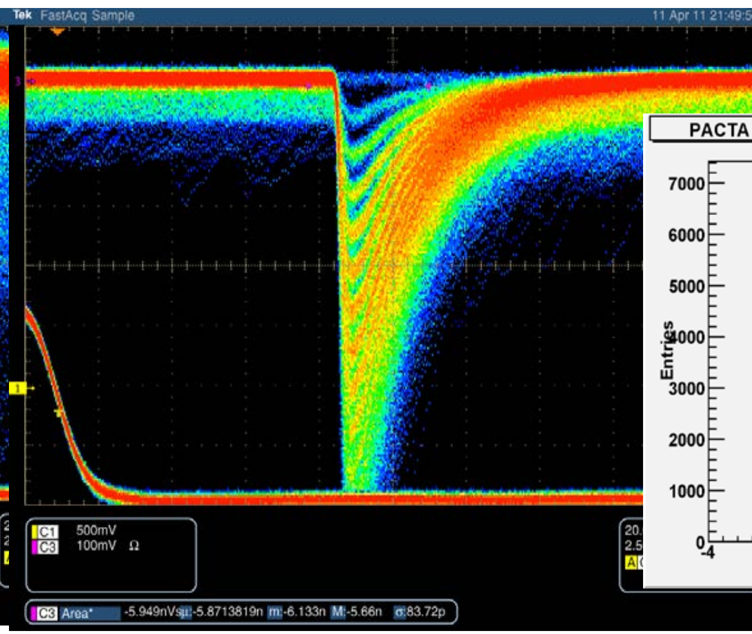
II. PACTA: High Dynamic range Preamp

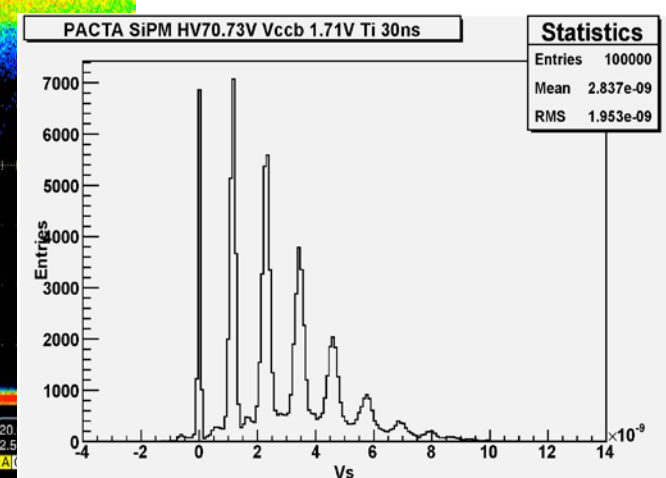
- Tests with SiPM
  - Low Zin current mode circuit are well suited for SiPM readout
  - DC coupling without external components
  - We just took an available MPPC (S10931-050P)
    - 1 V overvoltage
  - Recovery time seems to be dominated by internal SiPM time constant



- DC coupled
- Possible to ctrl each SiPM bias with on-chip circuitry







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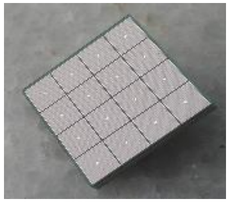
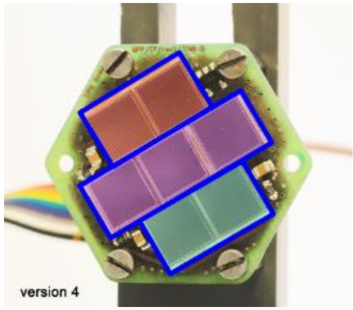
III. MUSIC: Multipurpose SiPM RO chip

- SiPMs are replacing PMTs in many applications

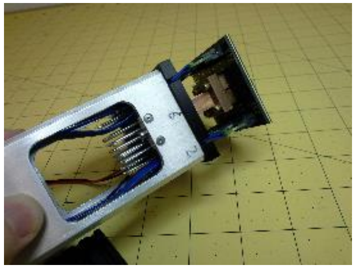
Eg: IACTs



CTA-SCT (dual mirror)
cta-us.physics.ucla.edu
inspirehep.net/record/1306235



D. Fink et al. "SiPM Based Focal Plane Instrumentation Prototype for the MAGIC Telescopes", PD15, 2015



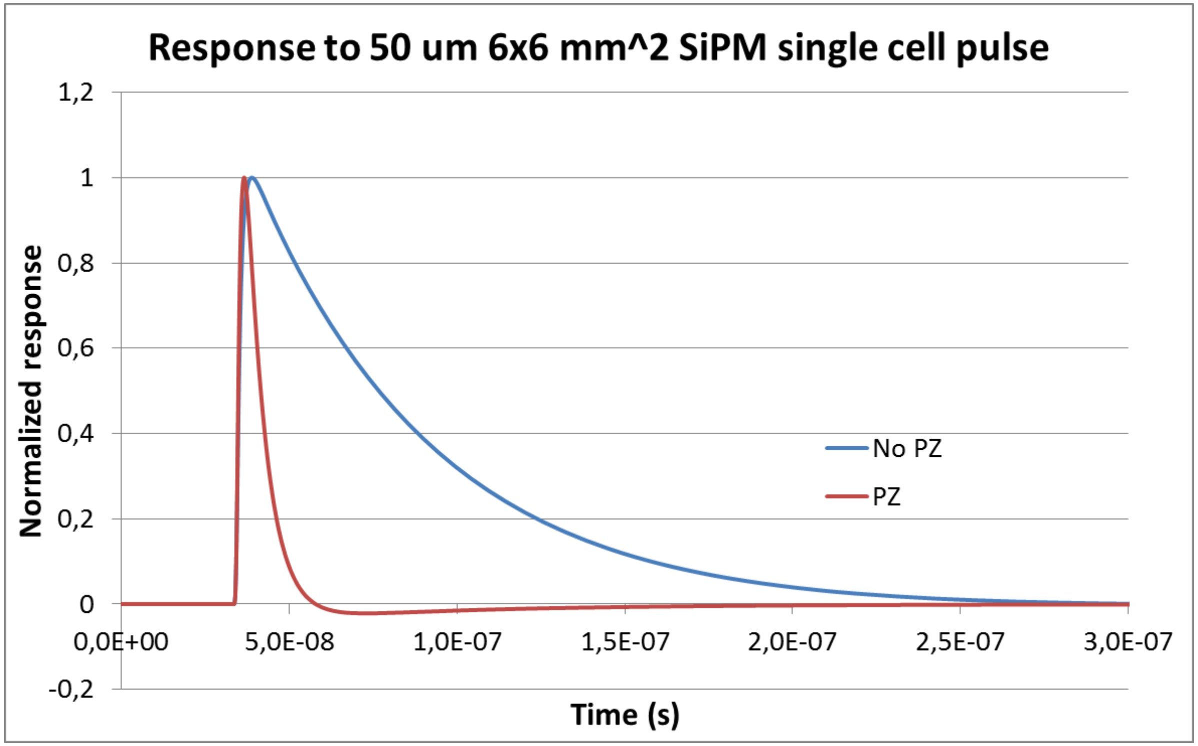
T. Montarulli et al. "The small size telescope projects for the Cherenkov Telescope Array", ICRC2015

- **Dedicated FE electronics is needed to fully exploit SiPM performace**
- **We present a multipurpose chip integrating many of those functions**:

MUSIC

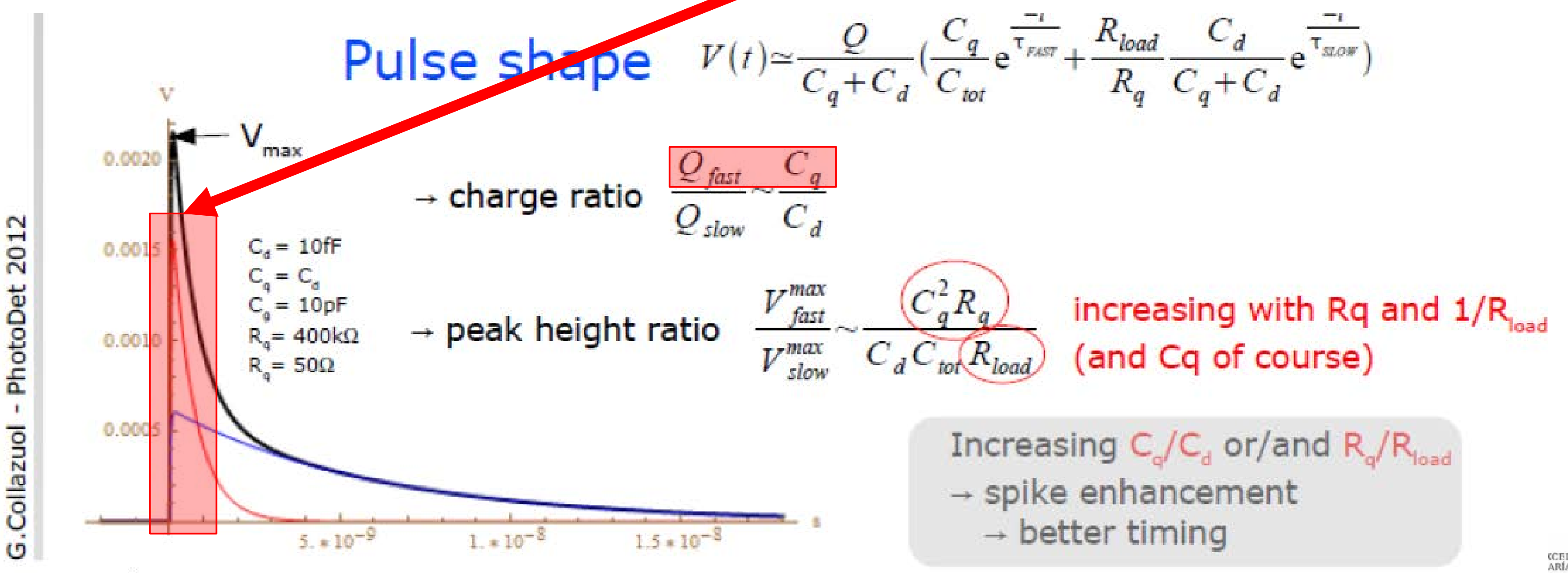
III. MUSIC: Multipurpose SiPM RO chip

- Front end electronics for SiPM is needed to:
  - Shape the input signal
    - Large SiPM recovery time constant may cause saturation or distortion because of pile up
    - Pole-zero cancellation or high-pass filters are often used



III. MUSIC: Multipurpose SiPM RO chip

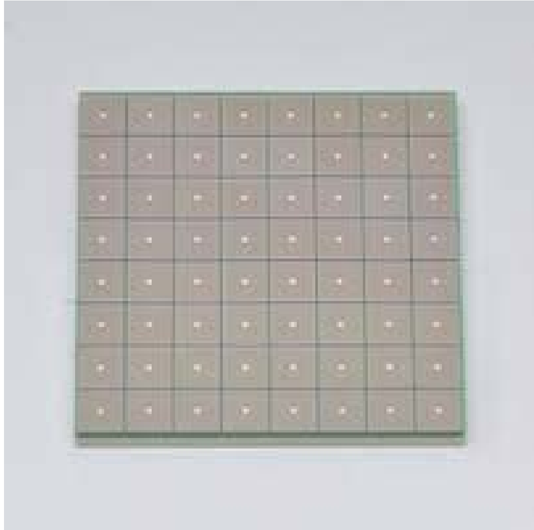
- Front end electronics for SiPM is needed to:
  - Preamplify for SNR optimization
    - Even if "nominal" gain is in the order of 10^6 only a fraction of the charge is used for fast read-out systems
    - The "effective" for a fast system can be between 2 and 10 times lower than the nominal gain

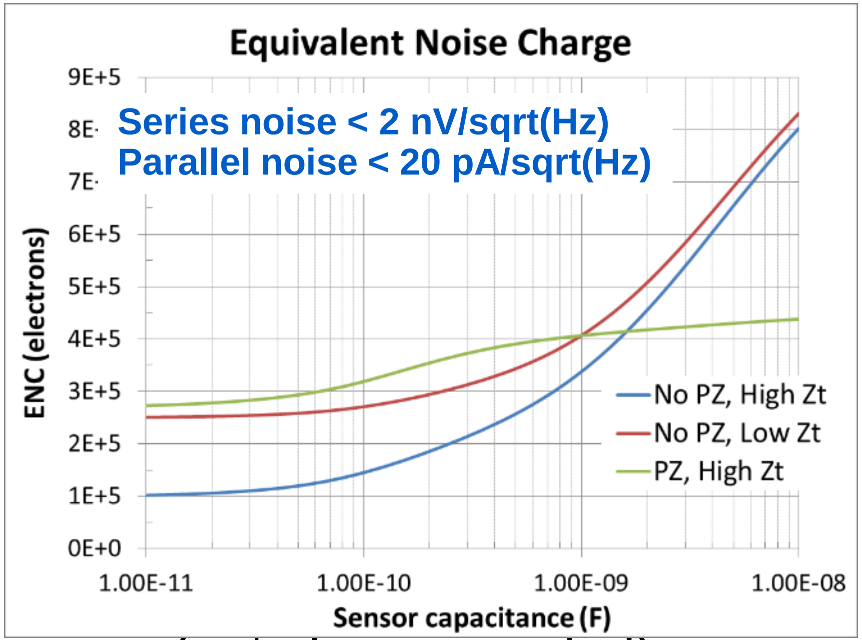


III. MUSIC: Multipurpose SiPM RO chip

- Front end electronics for SiPM is needed to:
  - Impedance adaptation: low input impedance for fast systems
  - Low noise front end is required for large SiPMs

SiPM capacitances range from 10s pF to more than several nF





  - Equalize over-voltage in SiPM arrays (not always needed)

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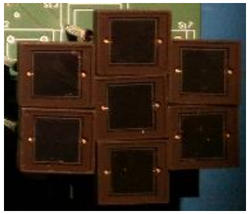
III. MUSIC: Multipurpose SiPM RO chip

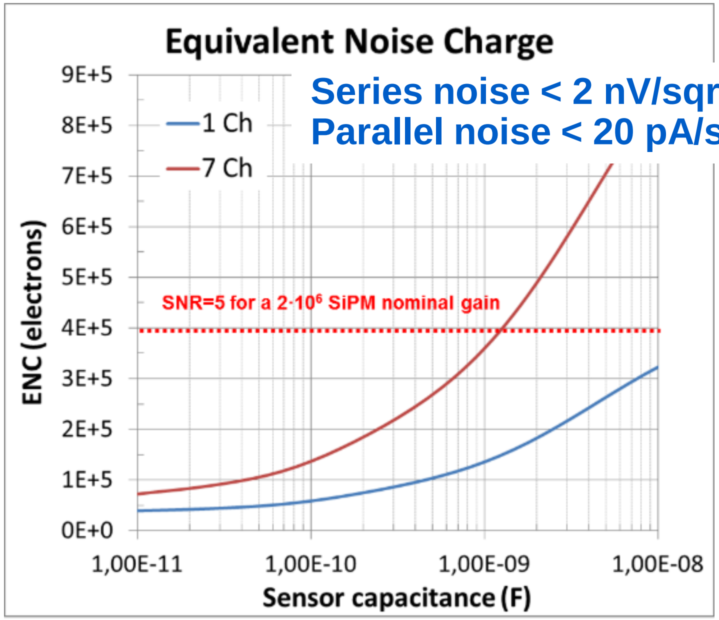
- Front end electronics for SiPM is needed to:
  - Combine (sum) the signal of several SiPMs
    - Typically SiPM size ranges from 1x1 to 6x6 mm^2*
    - To replace a PMT in some application SiPMs signals need to be added
    - Low noise FE electronics becomes mandatory !

7 x SIPM
6x6 mm^2 each



≈

1 x PMT
18 mm diameter



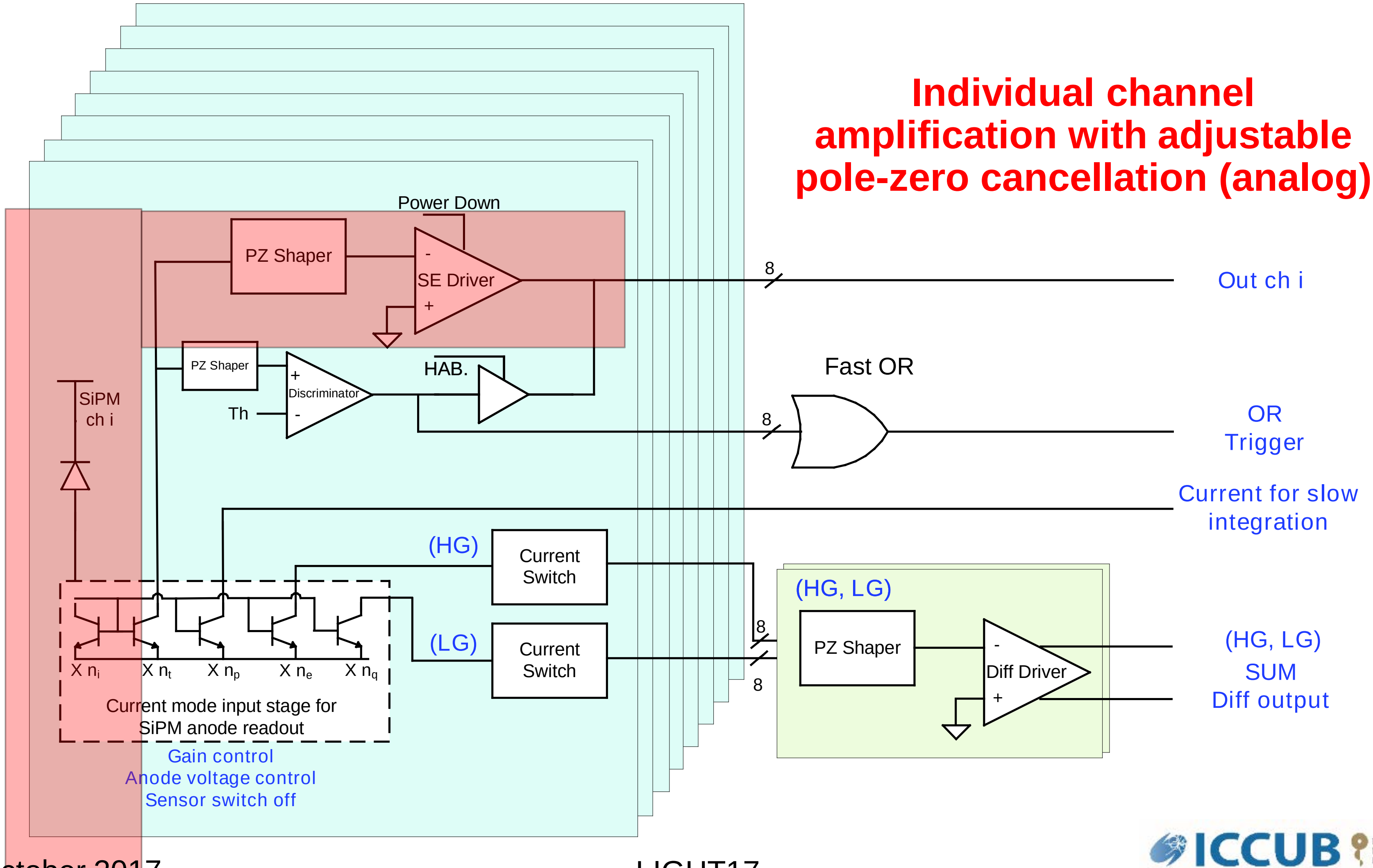
$$ENC = \frac{Output\ Noise}{Charge\ Gain} \leftarrow 10\ ns\ integration$$

*7x7mm^2 and some custom larger SiPMs exist

III. MUSIC: Multipurpose SiPM RO chip

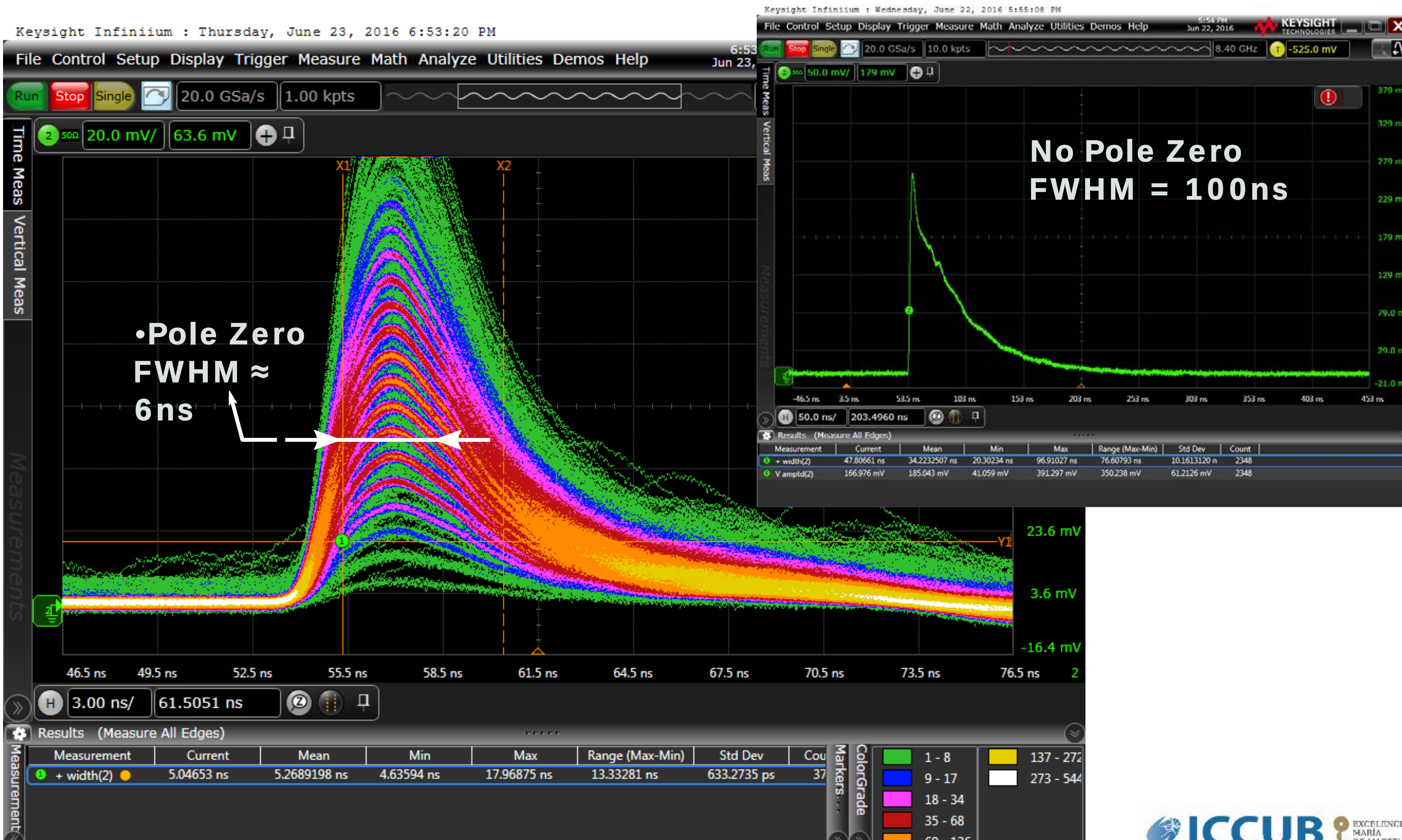
- MUSIC 8 ch ASIC integrates all those functionalities

Individual channel amplification with adjustable pole-zero cancellation (analog)



III. MUSIC: Multipurpose SiPM RO chip

- Output for a LCT4 MPPC (3x3 mm^2)



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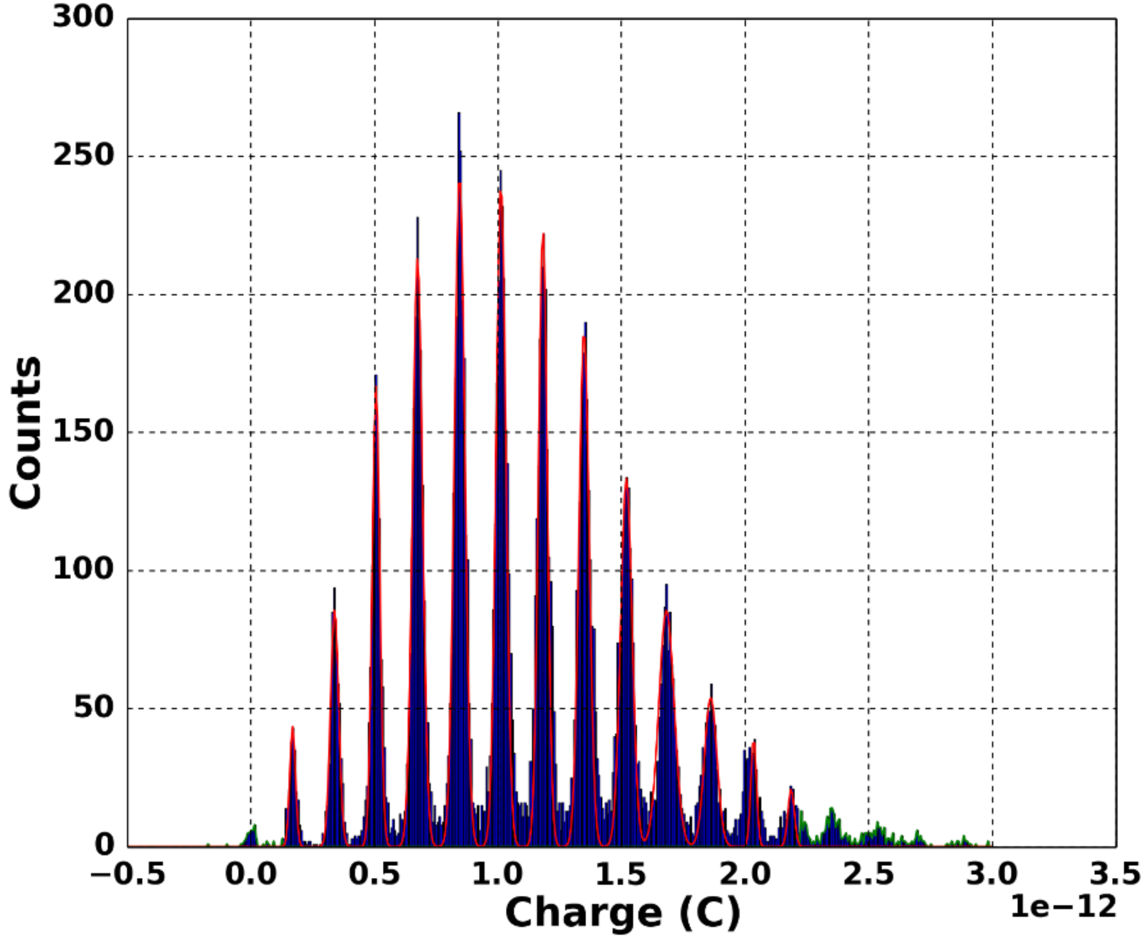
III. MUSIC: Multipurpose SiPM RO chip

- Charge spectrum for a LCT4 MPPC (3x3 mm^2)
- Pole-zero cancellation
- Excellent resolution with FWHM of 5 ns



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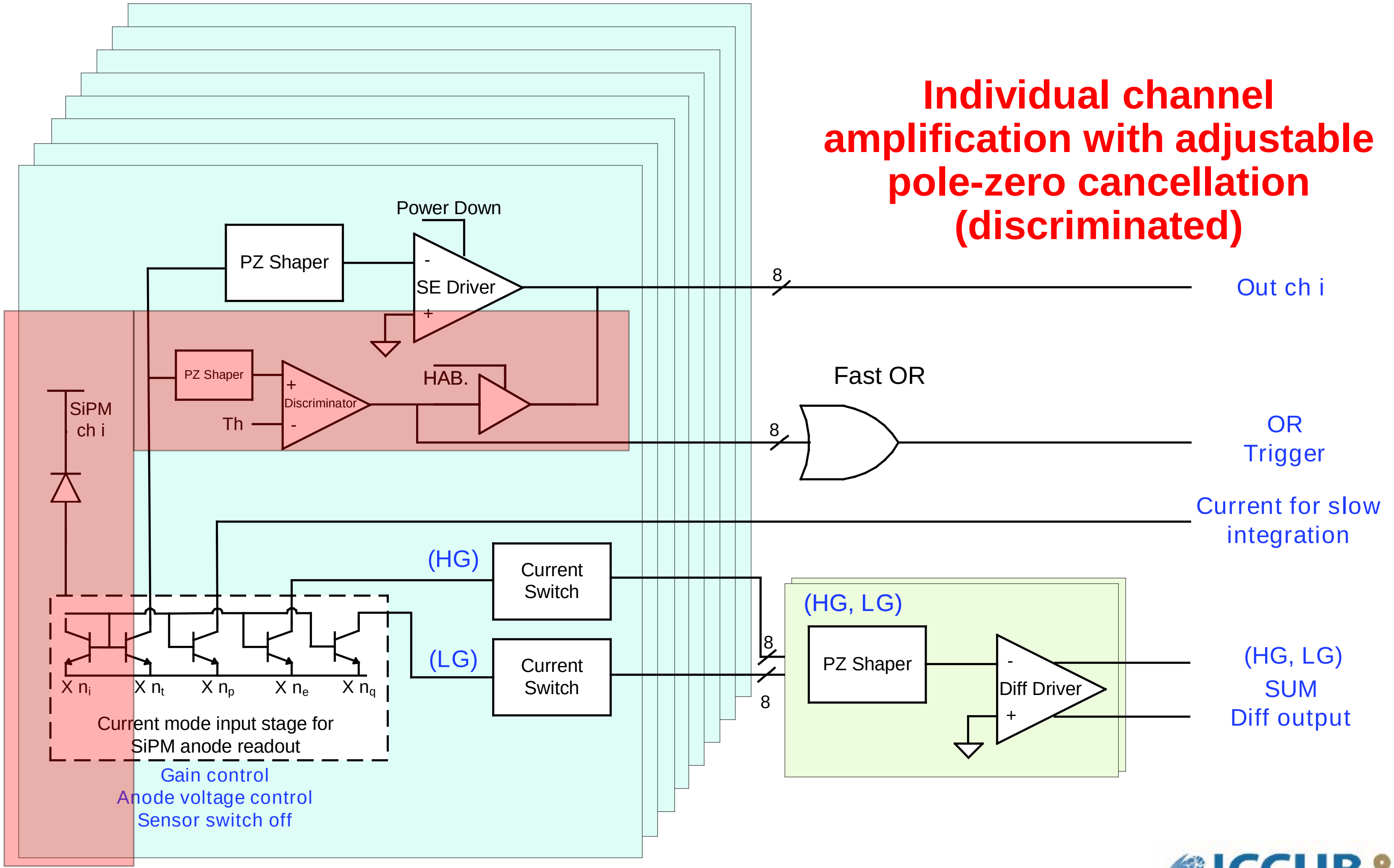
III. MUSIC: Multipurpose SiPM RO chip

- MUSIC 8 ch ASIC integrates all those functionalities



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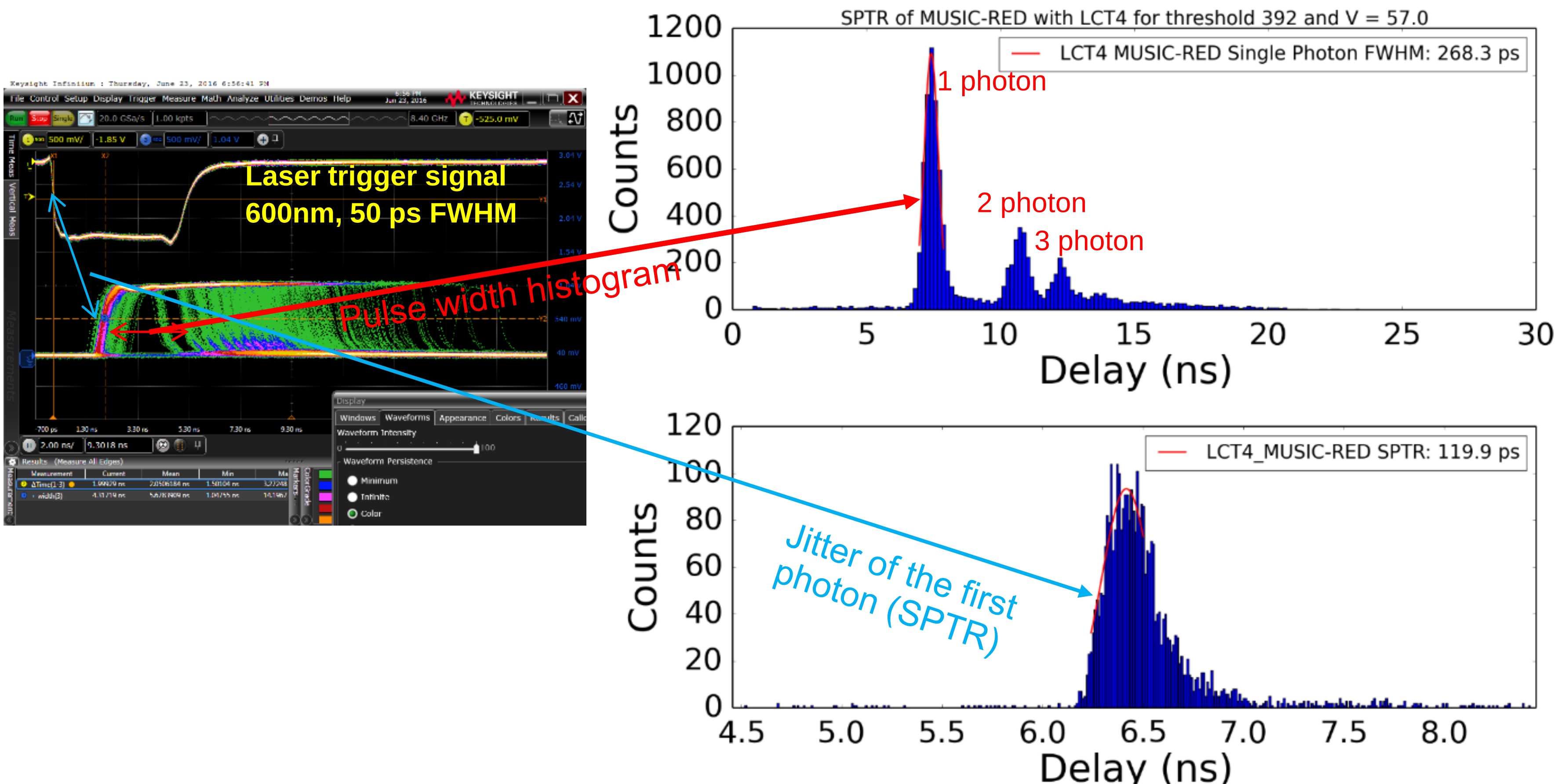
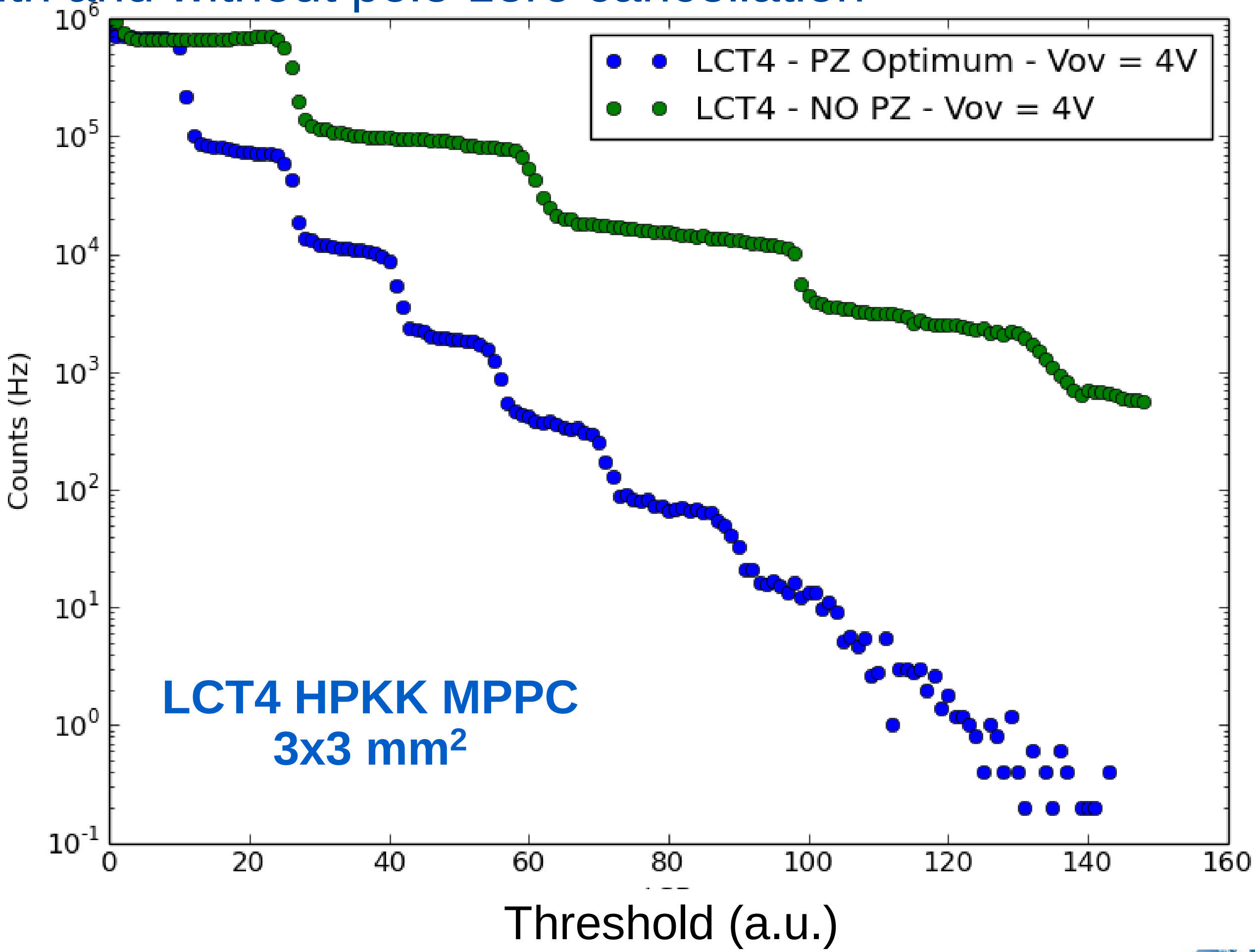
III. MUSIC: Multipurpose SiPM RO chip

- Output for a LCT4 HPKK MPPC (3x3 mm^2)
  - Picosecond laser
  - Pole-zero cancellation
  - Single Photon Time Resolution about 100 ps (@ 5V OV)



III. MUSIC: Multipurpose SiPM RO chip

- Dark count rate staircase plot (no laser signal):
  - Scan the rate of the SiPM signals that are over a certain threshold
- With and without pole-zero cancellation



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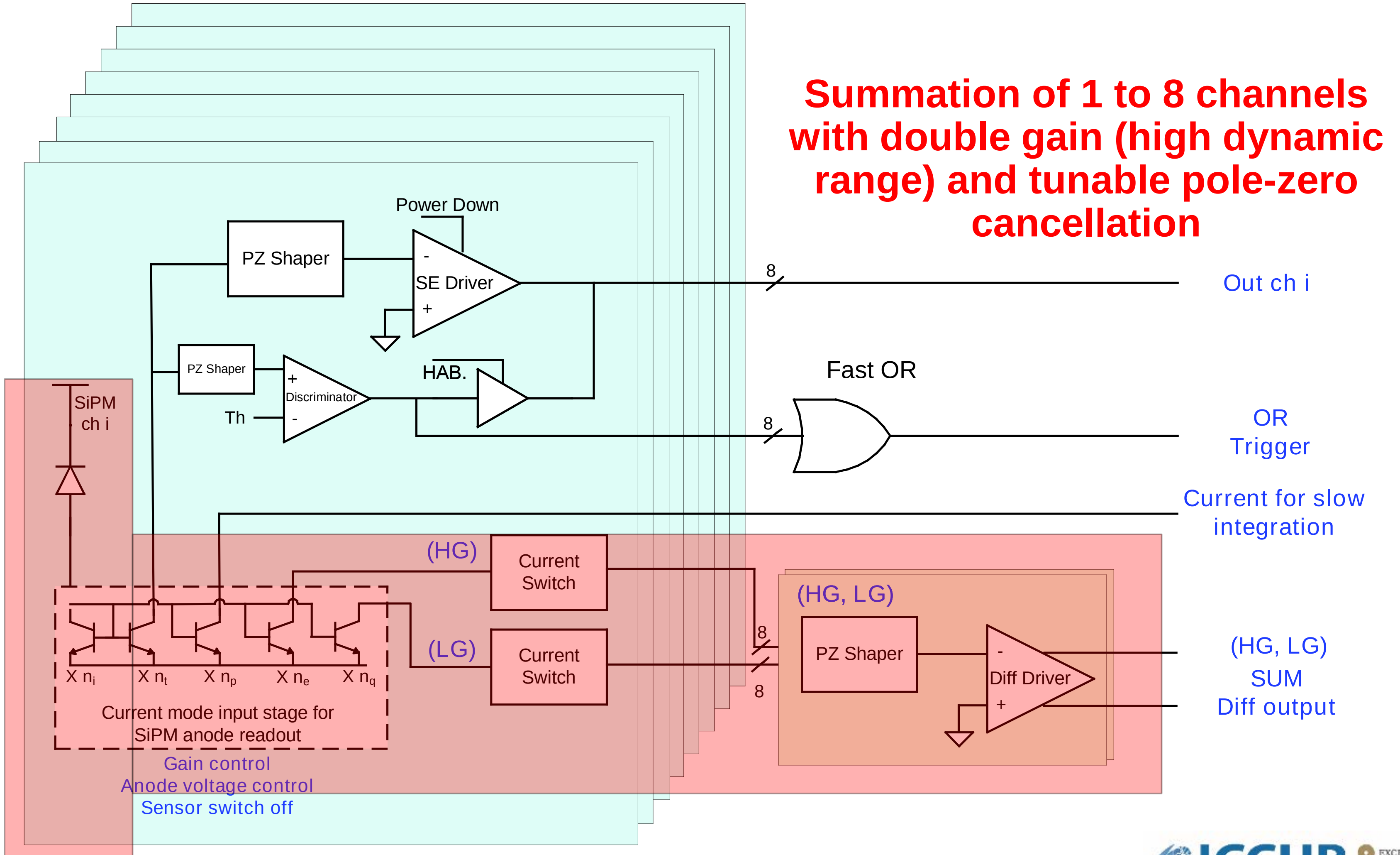
III. MUSIC: Multipurpose SiPM RO chip

- MUSIC 8 ch ASIC integrates all those functionalities



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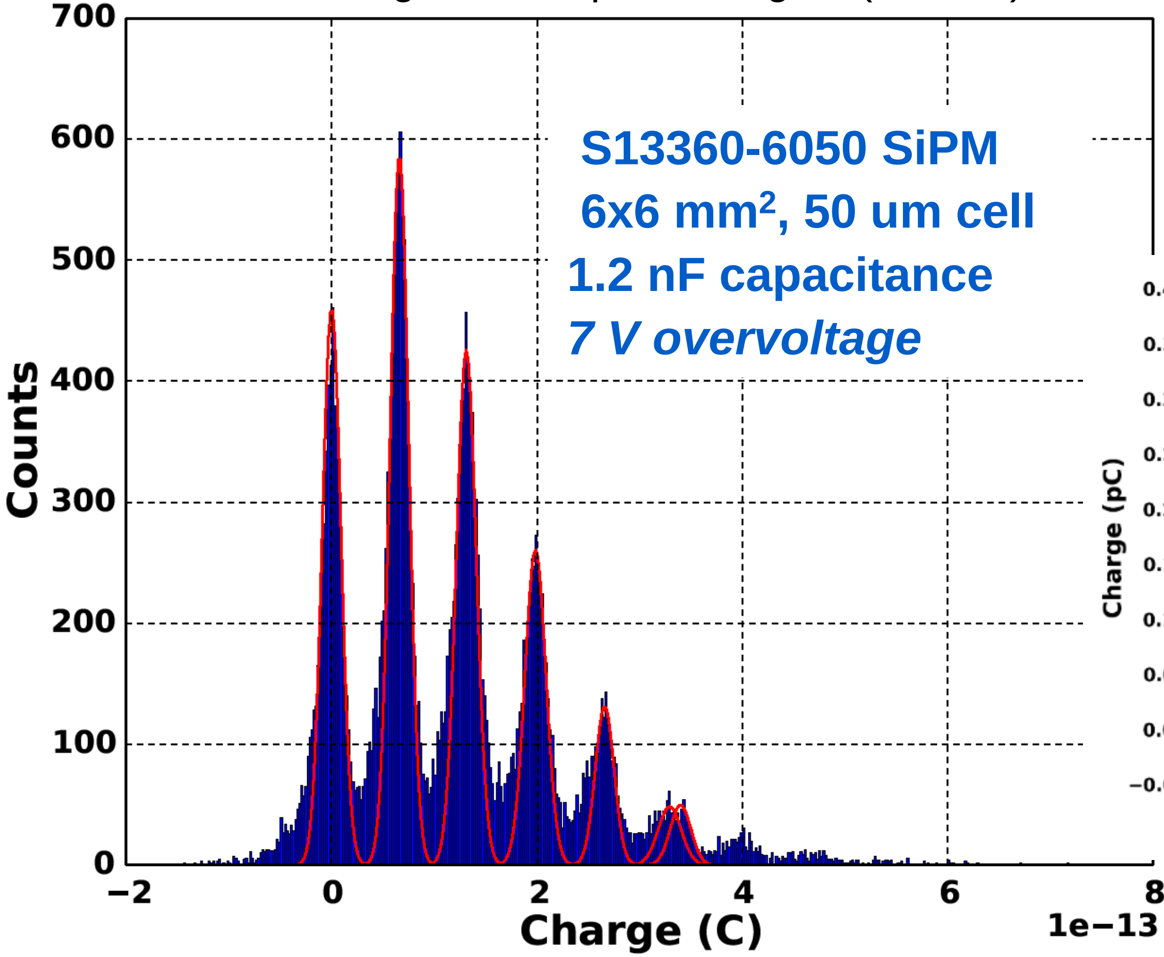
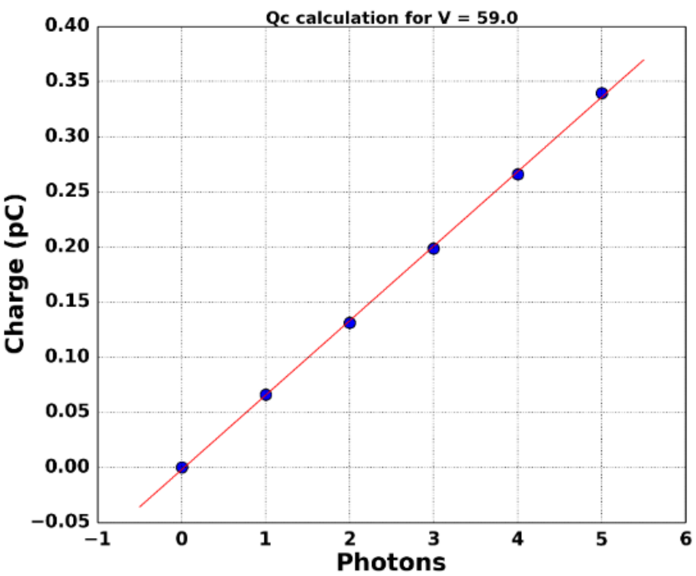
III. MUSIC: Multipurpose SiPM RO chip

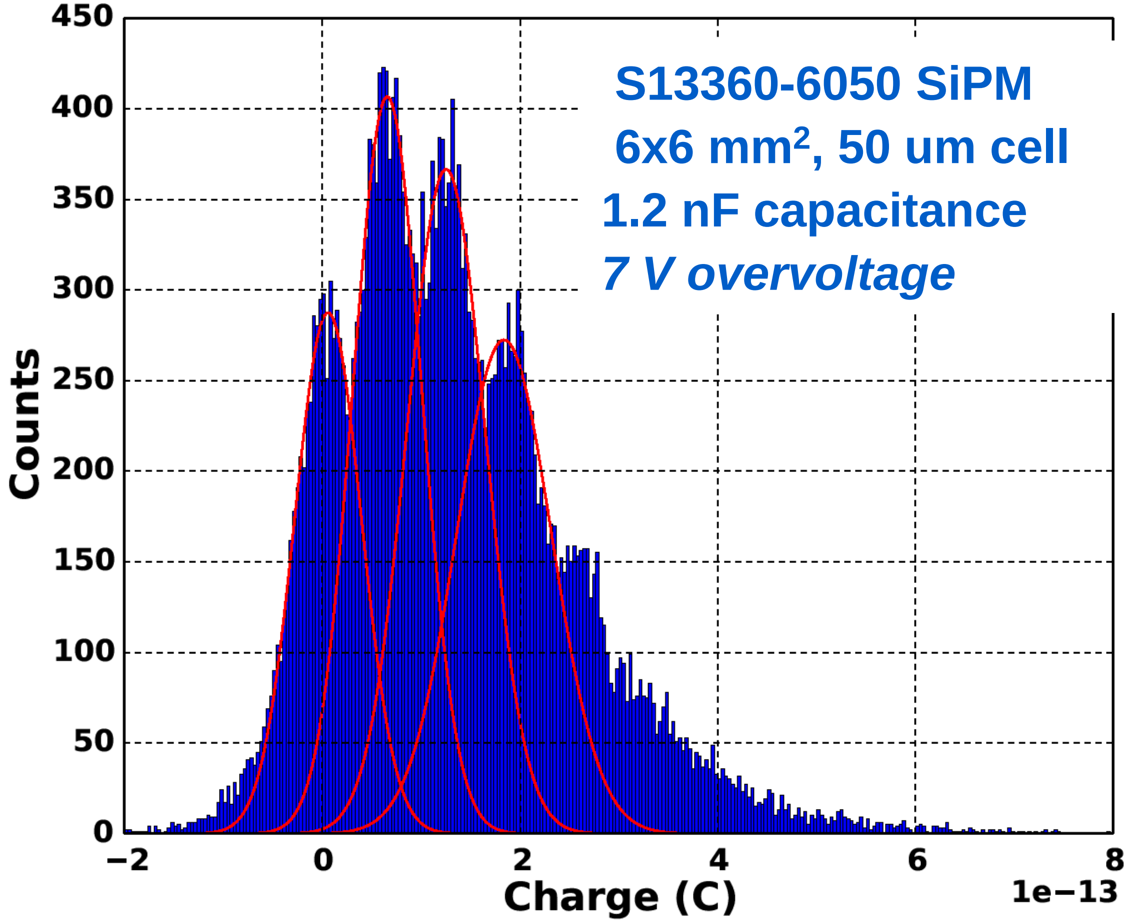
- MUSIC configuration: the adder takes only 1 channel
  - Pole-zero cancellation: trade-off between resolution and speed
  - High transimpedance gain (MUSIC)

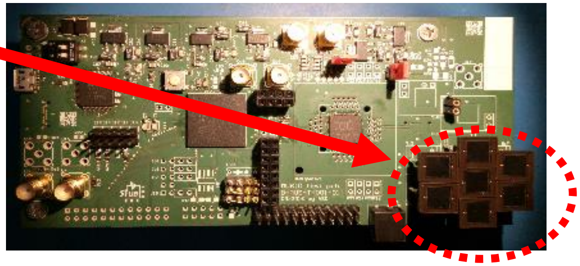




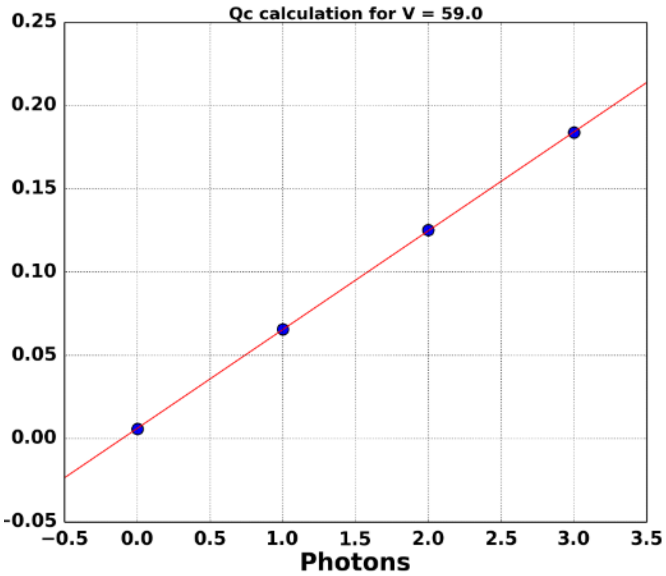
III. MUSIC: Multipurpose SiPM RO chip

- MUSIC configuration: the adder takes 7 channels
  - Noise is much higher (sqtr(7))
  - But pe (cell) peaks can still be identified
  - Channels have been equalized by MUSIC anode ctrl voltage





1 x PMT
18 mm diameter
≈
7 x SIPM
6x6 mm²
each



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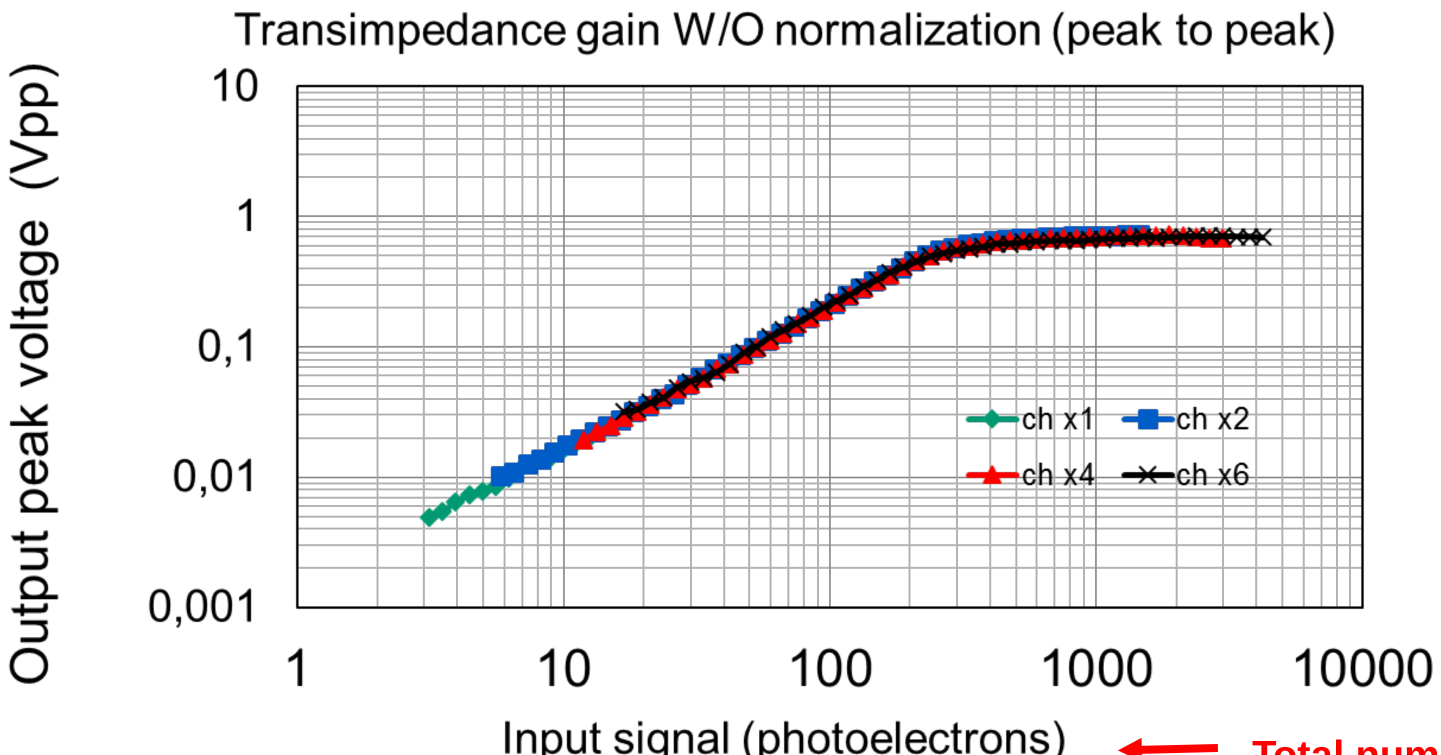
III. MUSIC: Multipurpose SiPM RO chip

- Dynamic range for S13360-6050@6V overvoltage
- Optmized pole-zero cancellation
- High gain path output
- Response for n input channels (signal injected in n channels)



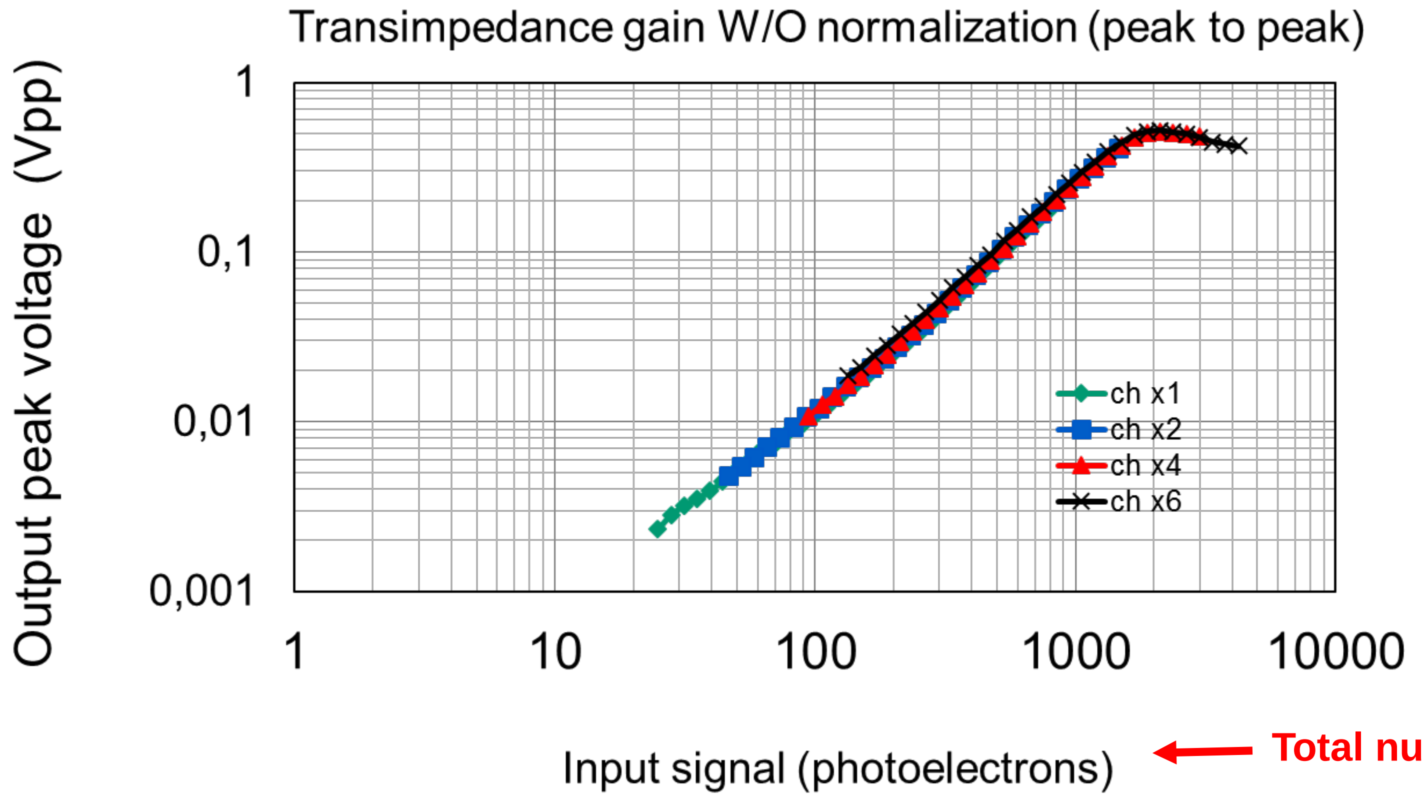
Reponse independent on the number of active channels

Summation works

Total number of pe

III. MUSIC: Multipurpose SiPM RO chip

- Dynamic range for S13360-6050@6V overvoltage:
  - Optmized pole-zero cancellation
  - Low gain path output
- Response for n input channels (signal injected in n channels)
- The bi-gain system allows to achieve a dynamic range of > 1000 pe
  - Dynamic range limited by signal injection circuit



Reponse independent on the number of active channels

Summation works

III. MUSIC: Multipurpose SiPM RO chip

- SHIP experiment is a new general-purpose beam dump facility at the SPS (CERN) to search for hidden particles
  - Predicted by a very large number of recently elaborated models of Hidden
  - Dark matter, neutrino oscillations, and the origin of the full baryon asymmetry

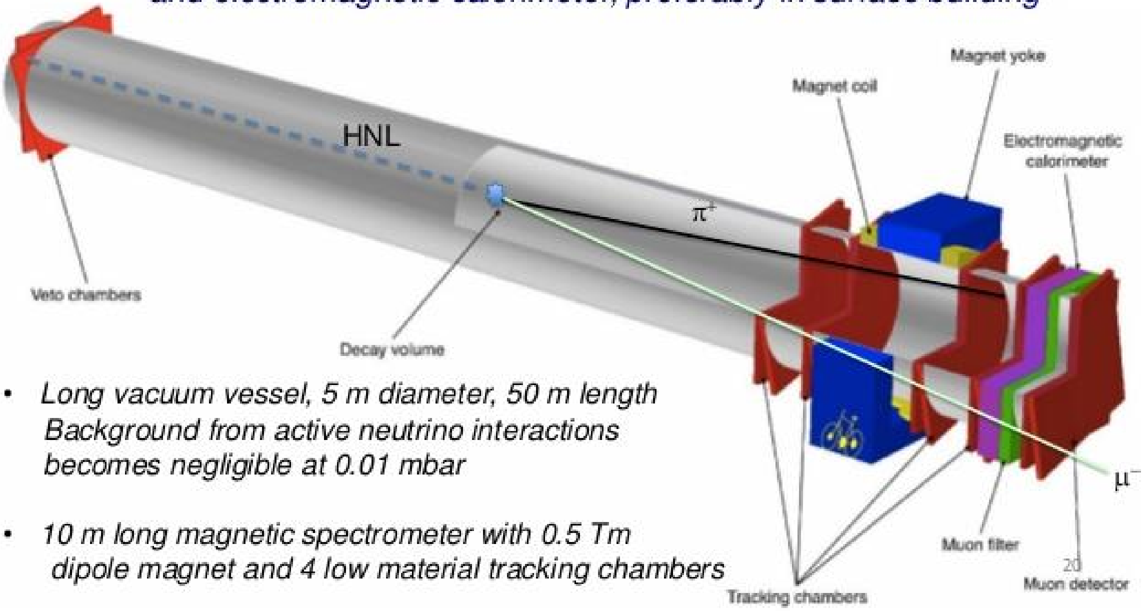
SHiP
Search for Hidden Particles

Imperial College London

INFN

- *Reconstruction of the HNL decays in the final states: $\mu^-\pi^+$, μ–ρ^+ & $e^-\pi^+$*

→ *Requires long decay volume, magnetic spectrometer, muon detector and electromagnetic calorimeter, preferably in surface building*



- *Long vacuum vessel, 5 m diameter, 50 m length Background from active neutrino interactions becomes negligible at 0.01 mbar*

- *10 m long magnetic spectrometer with 0.5 Tm dipole magnet and 4 low material tracking chambers*

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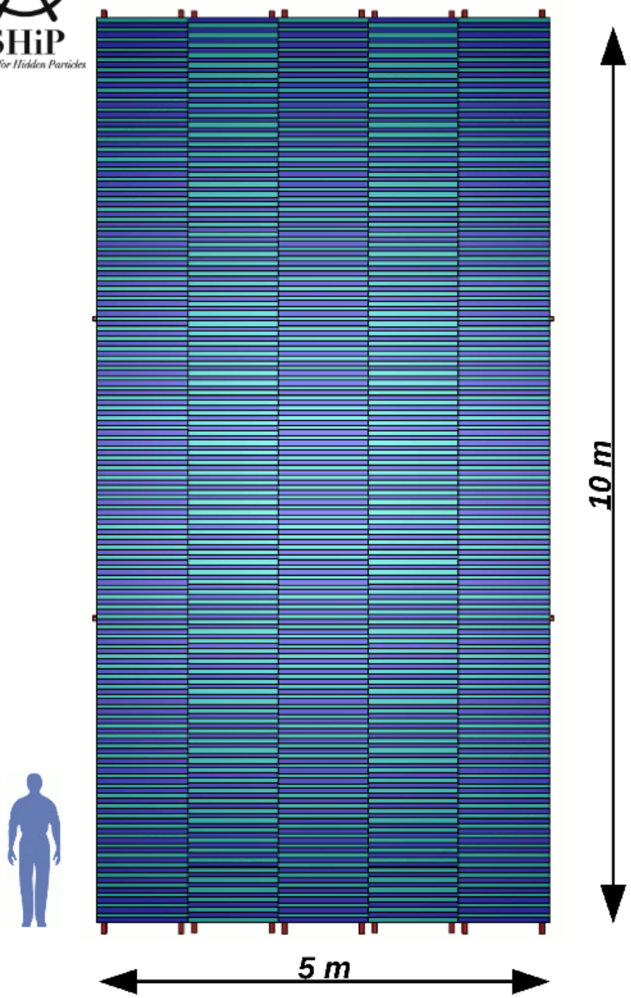
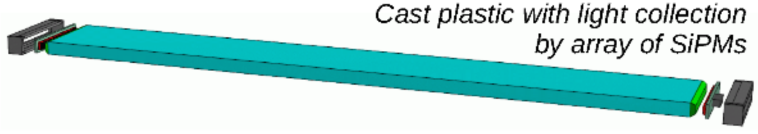
III. MUSIC: Multipurpose SiPM RO chip

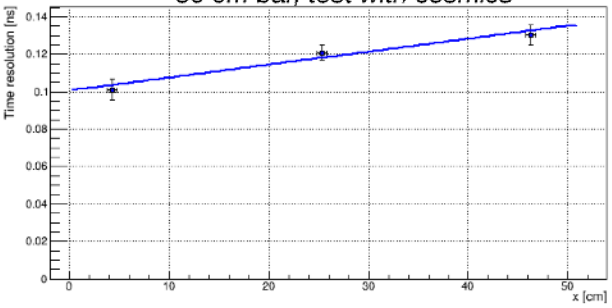


Timing Detector in SHiP



- For the TD of size 5 m x 10 m with a bar ***100 cm x 6 cm x 1 cm***
  - 5 col x 182 row = 910 bars =>
  - 910 bars x 2 = 1820 ch =>
  - 1820 x 8 = 14560 SiPMs
- The resolution at 50 cm is ~140 ps => we can use with 1 m bar and 2-side readout to be within 100 ps.

50 cm bar, test with cosmics



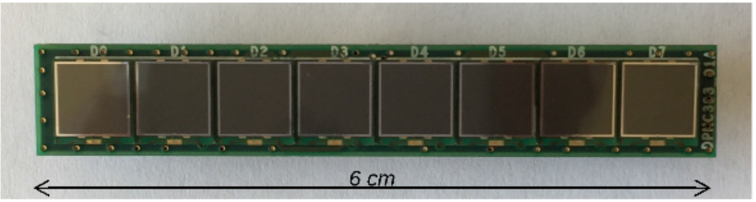
5

III. MUSIC: Multipurpose SiPM RO chip

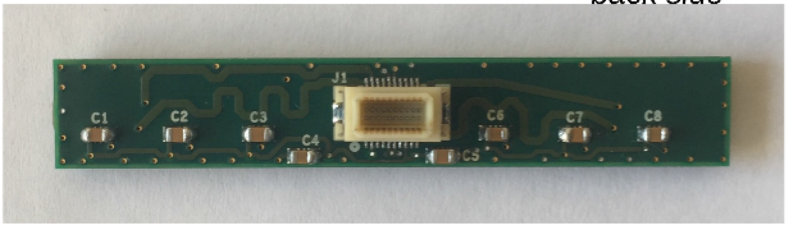
Bar and sensors for ToF/ND280

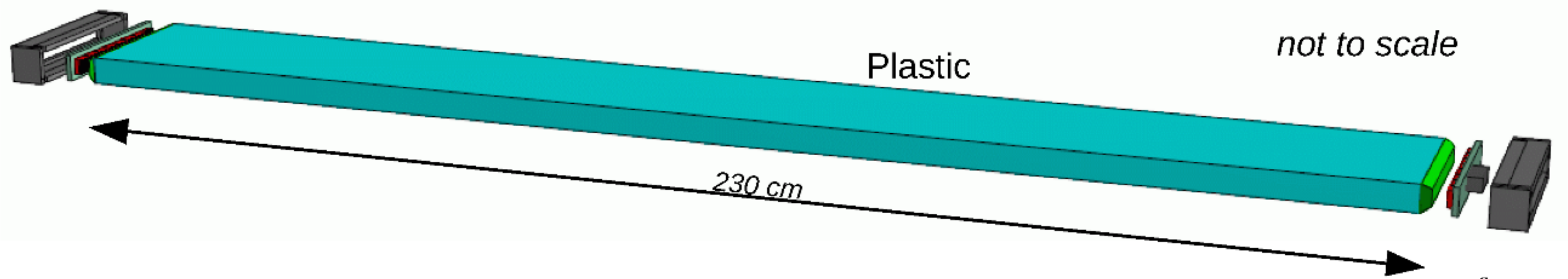
- Bar: 230 cm x 6 cm x 1 cm
- Plastic material:
  - EJ200 (BC408) or EJ208(BC412)
  - Attenuation length ~4 m
  - 1.42 kg/bar
- Readout from both ends
  - 8 sensors of 6 mm x 6 mm
  - Example: S13360-6050PE

front side



back side





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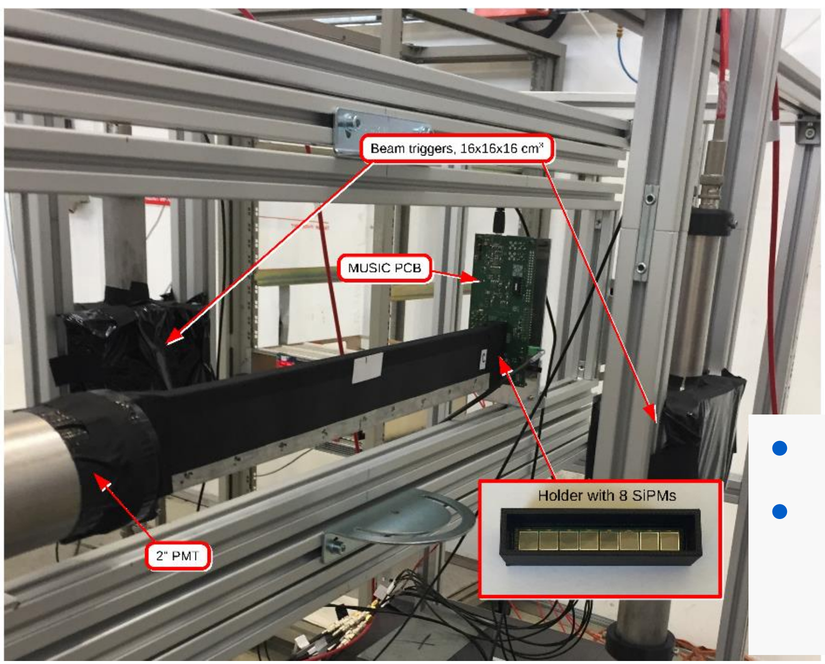
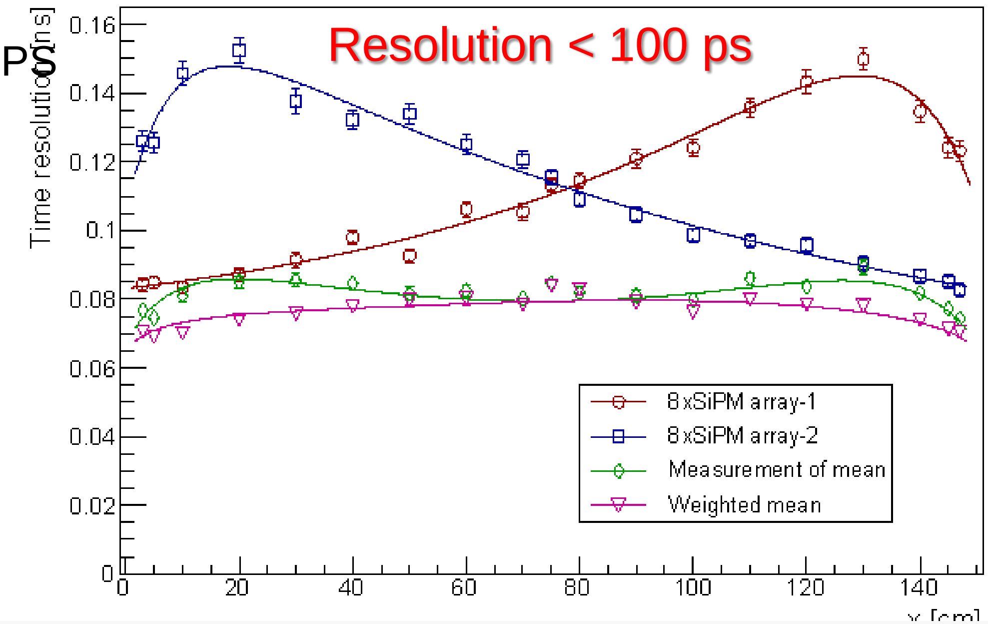
III. MUSIC: Multipurpose SiPM RO chip

- Timing sub-detector test beam with MUSIC chip
  - By Univ. Geneva & Univ. Zurich
  - MUSIC in summation mode (8 6x6 mm^2 SiPMs)
    - Bar read-out at both ends
  - 2.5 GeV/c muon beam at the CERN PS
  - Readout with Wavecatcher
    - Fast analog memory (LAL & IRFU/CEA)



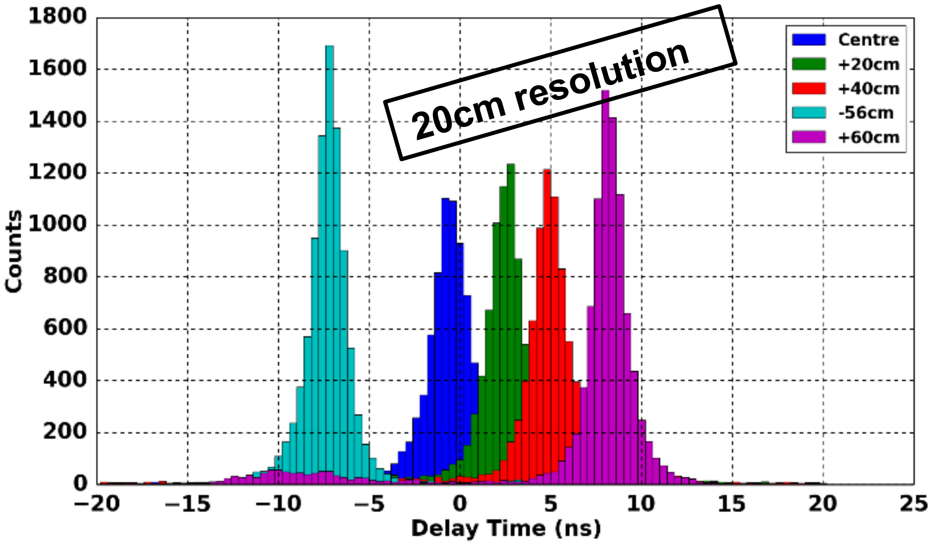


- Measurements with the 150 cm x 6 cm x 1 cm bar.
- Time resolution as measured by the SiPM arrays at both ends of the bar as a function of the interaction point along the bar.

© A. Kornezev (Univ. Geneva)

III. MUSIC: Multipurpose SiPM RO chip

- Studying the possibility to develop a beam loss monitoring system based on scintillating fibers
  - Collaboration with Alba synchrotron General idea:
  - Fiber along the beam pipe or in selected regions
  - Losses are detected by a rate increase
  - With timing information, additional postion information
    - Preliminary results: 20 cm resolution for a 2 m fiber of 1 mm diameter



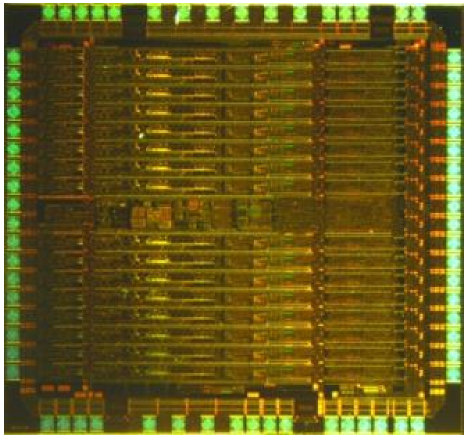
Thanks to C. Joram (CERN) for providing SciFibers

Outlook

I. Introduction
II. PACTA: High Dynamic Preamp
III. MUSIC: Multipurpose SiPM RO chip
IV. FlexToT: linearized ToT RO chip
V. New developments

IV. FlexToT: linearized ToT RO chip

- Joint project with CIEMAT to develop a time-over-threshold ASIC for SiPM based PET
  - ICCUB: expertise on electronics and microelectronics design for detector FE
  - CIEMAT: expertise on PET and medical imaging instrumentation



FlexToT

16 channel

SiGe BiCMOS 0.35um

Aaustriamicrosystem

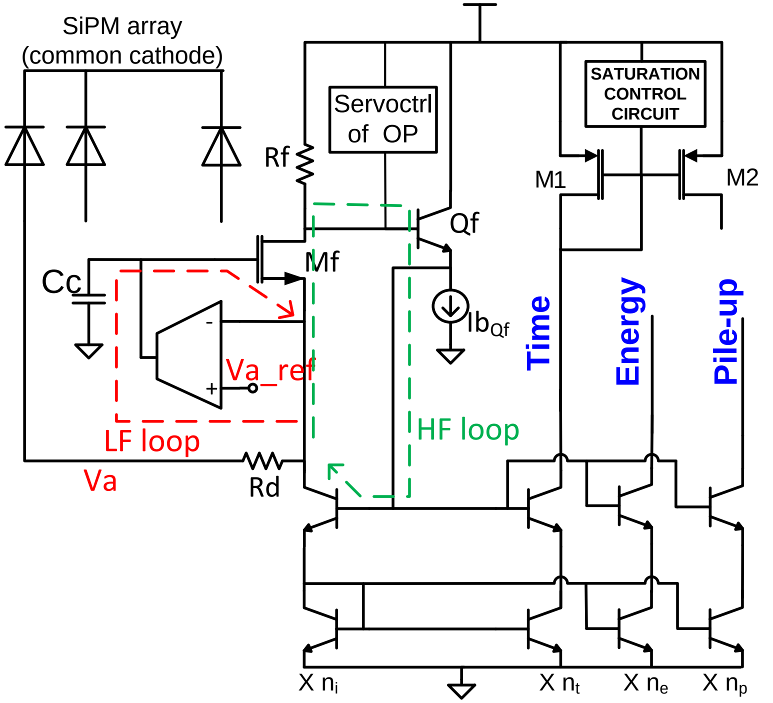
10 mm^2

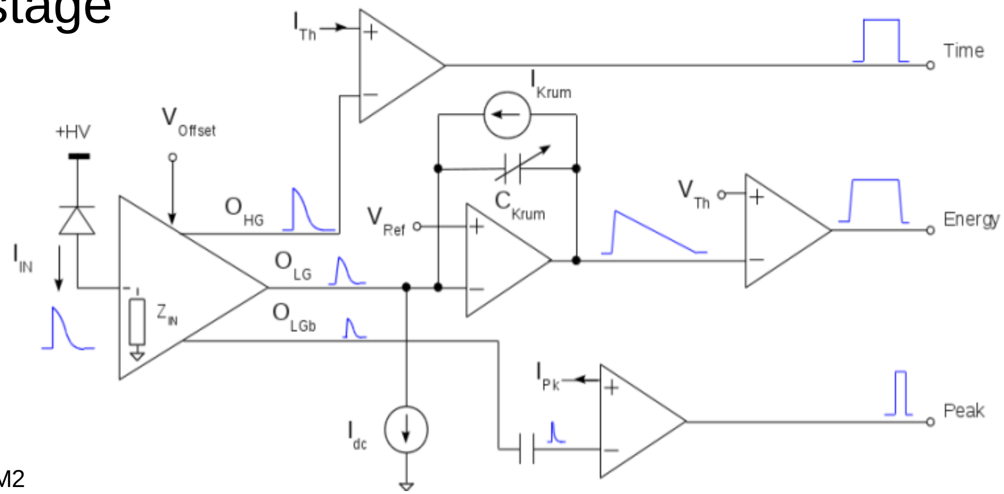
3.3 V (10 mW/ch)

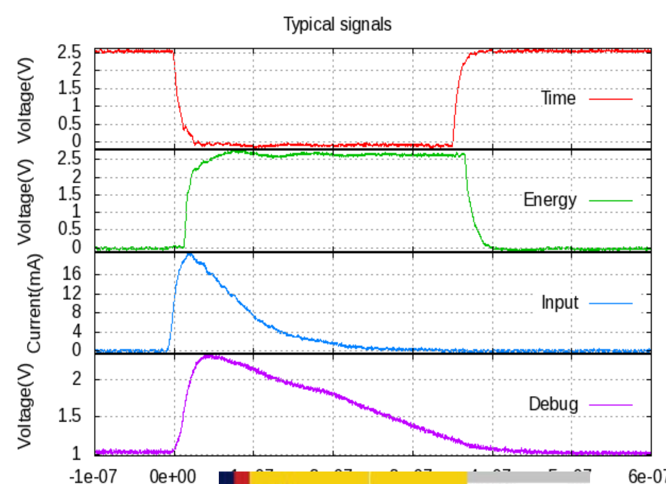
QFN 64

IV. FlexToT: linearized ToT RO chip

- A Flexible ASIC for SiPM RO (PET, SPECT, Compton)
  - Novel current mode input stage
  - Time resolution for ToF
  - Time over Threshold RO
    - **No ADC**

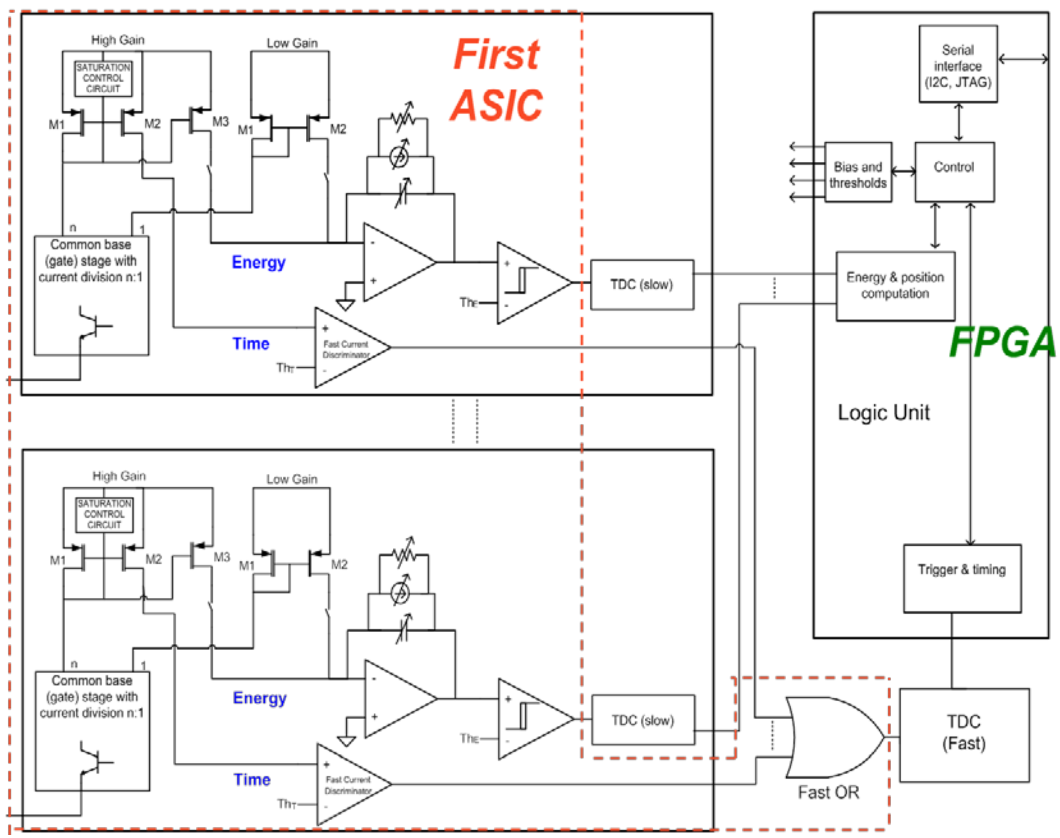






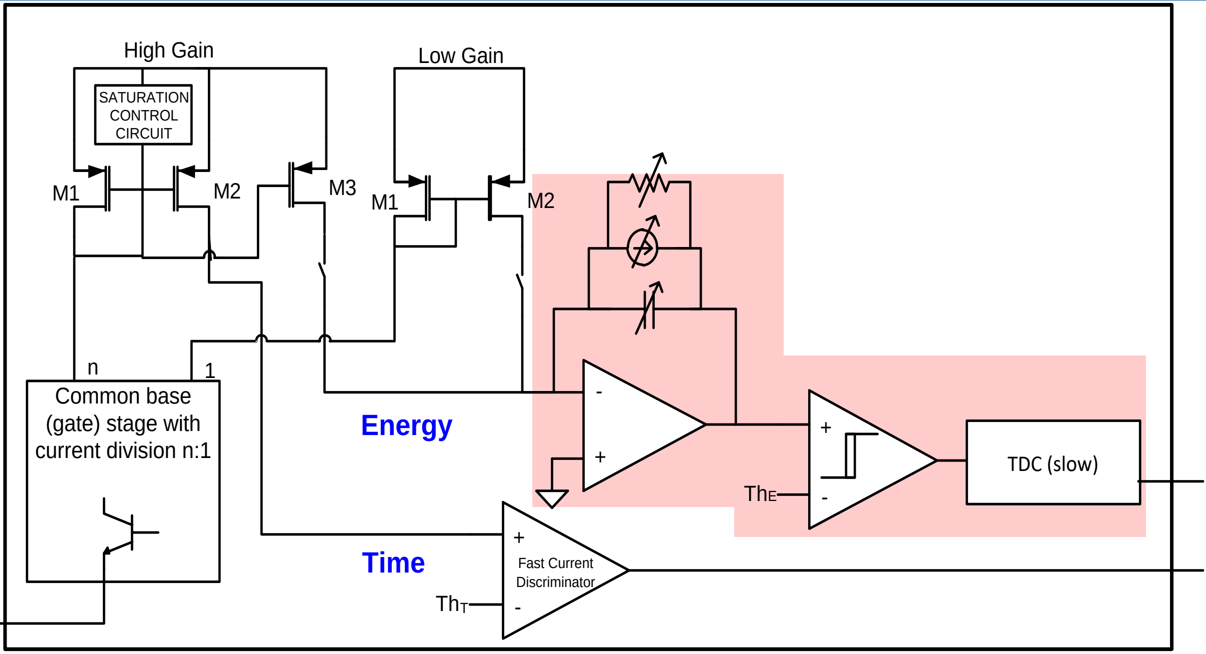
IV. FlexToT: linearized ToT RO chip

- Why FlexToT is flexible?
  - Different scintillator time constants
  - Trading-off resolution versus rate
  - Accurate analog processing directly connected to FPGA
    - TDCs and signal processing are in FPGA: reconfigurable !

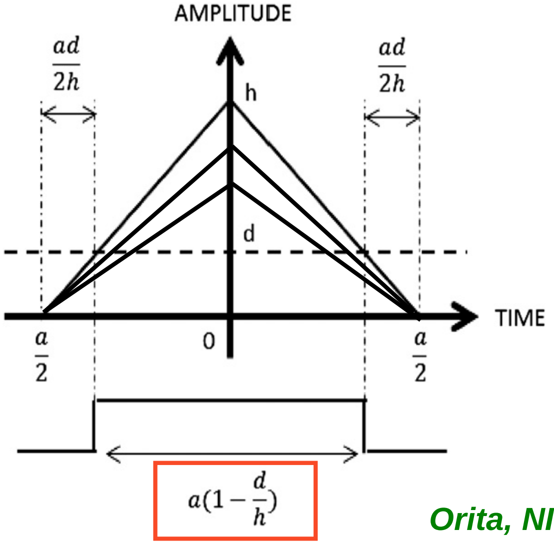


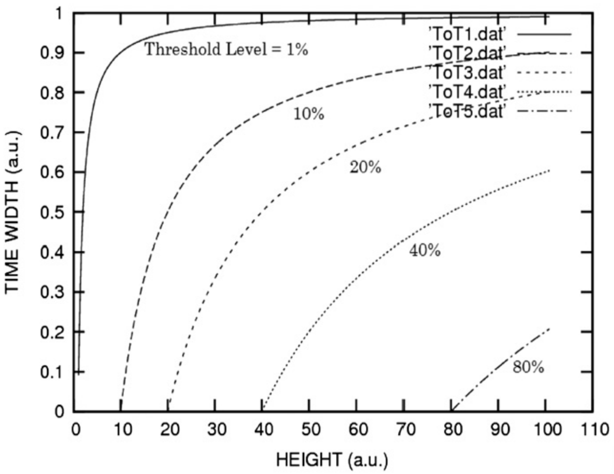
IV. FlexToT: linearized ToT RO chip

- **Configurable ToT**
  - **Non-linear vs linear**
  - **Tuneable feedback current**
    - **Rate vs resolution**



- **Classical ToT is non-linear**
  - **CSP+Shaper+Discriminator**





Orita, NIMA 648, S24-27, 2011

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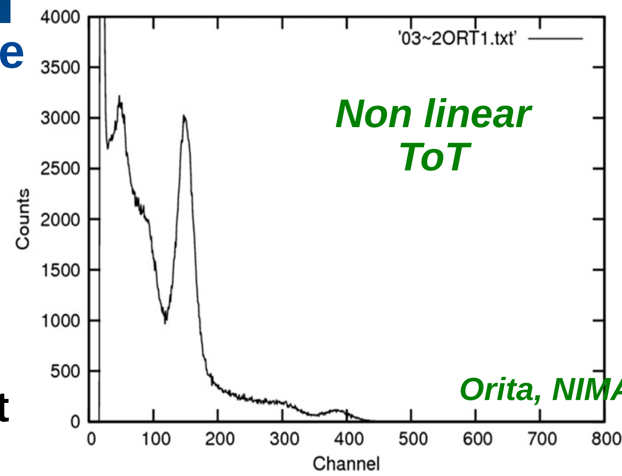
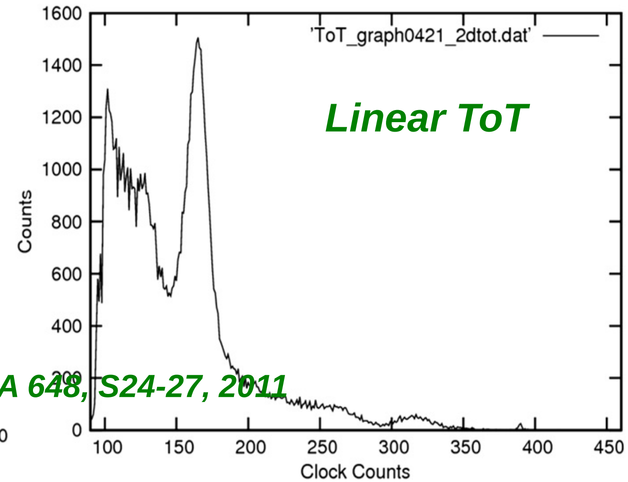
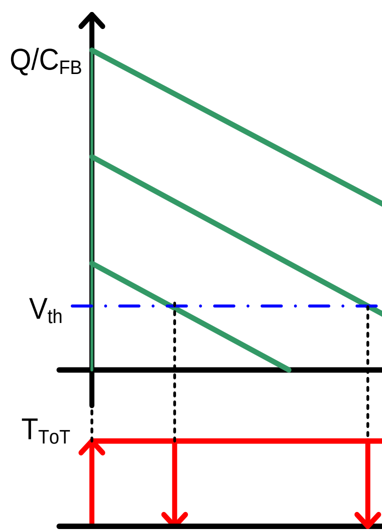
IV. FlexToT: linearized ToT RO chip

- **No linear ToT may degrade resolution**
- **Linear ToT is possible**
  - **Used in Medipix, Timepix, Dosepix ASICs family**
  - **Also proposed for PET**
  - **Tuneable feedback current (IFB)**
    - **Rate vs resolution**

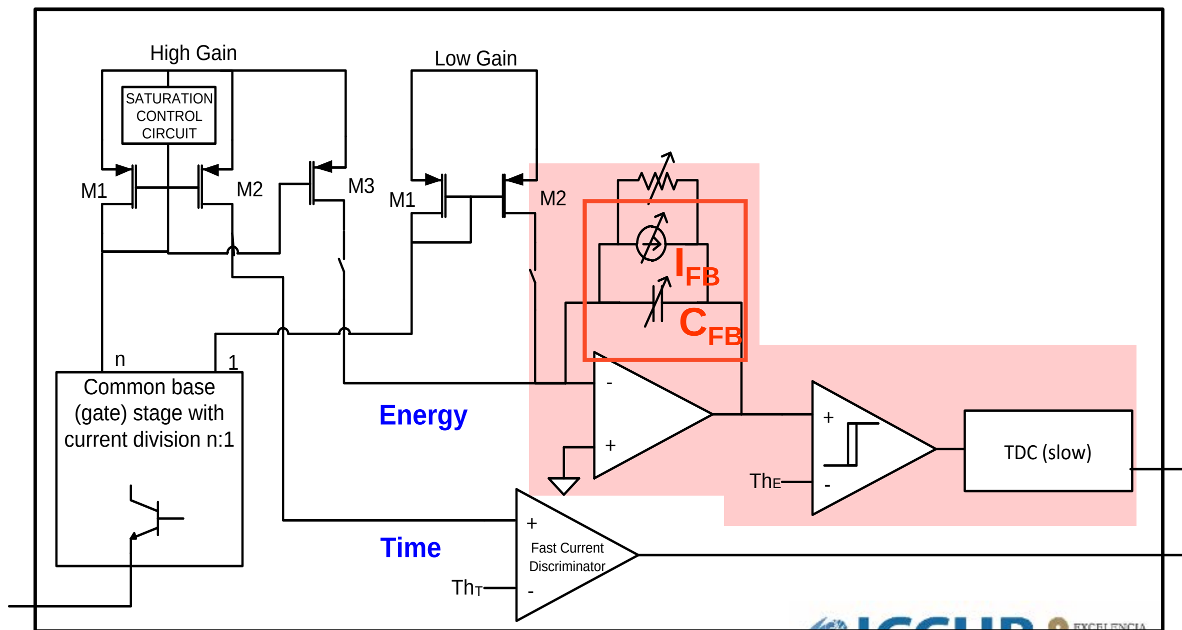




Orita, NIMA 648, S24-27, 2011

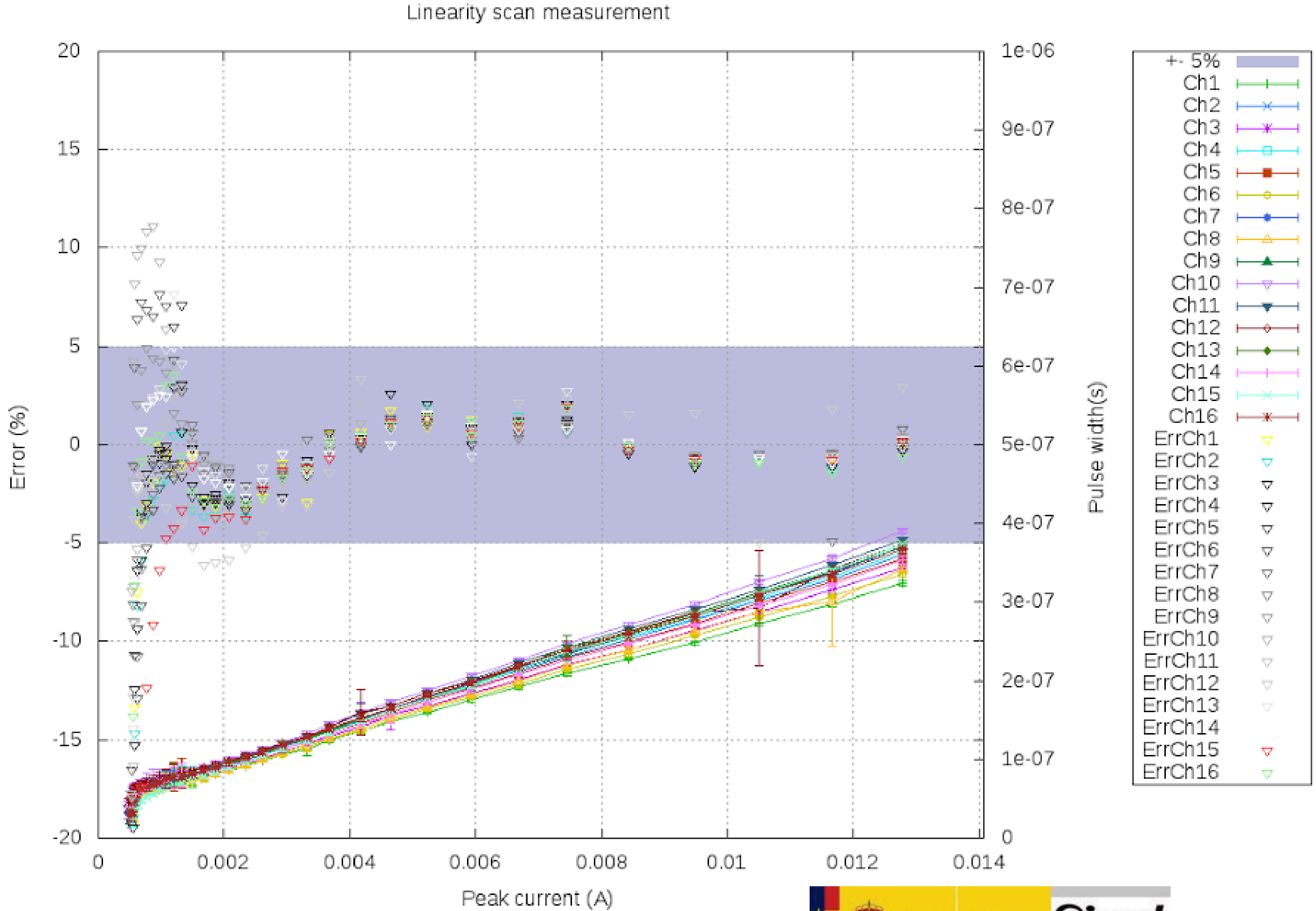


$$T_{ToT} = \frac{Q}{I_{FB}} - \frac{V_{th} C_{FB}}{I_{FB}}$$



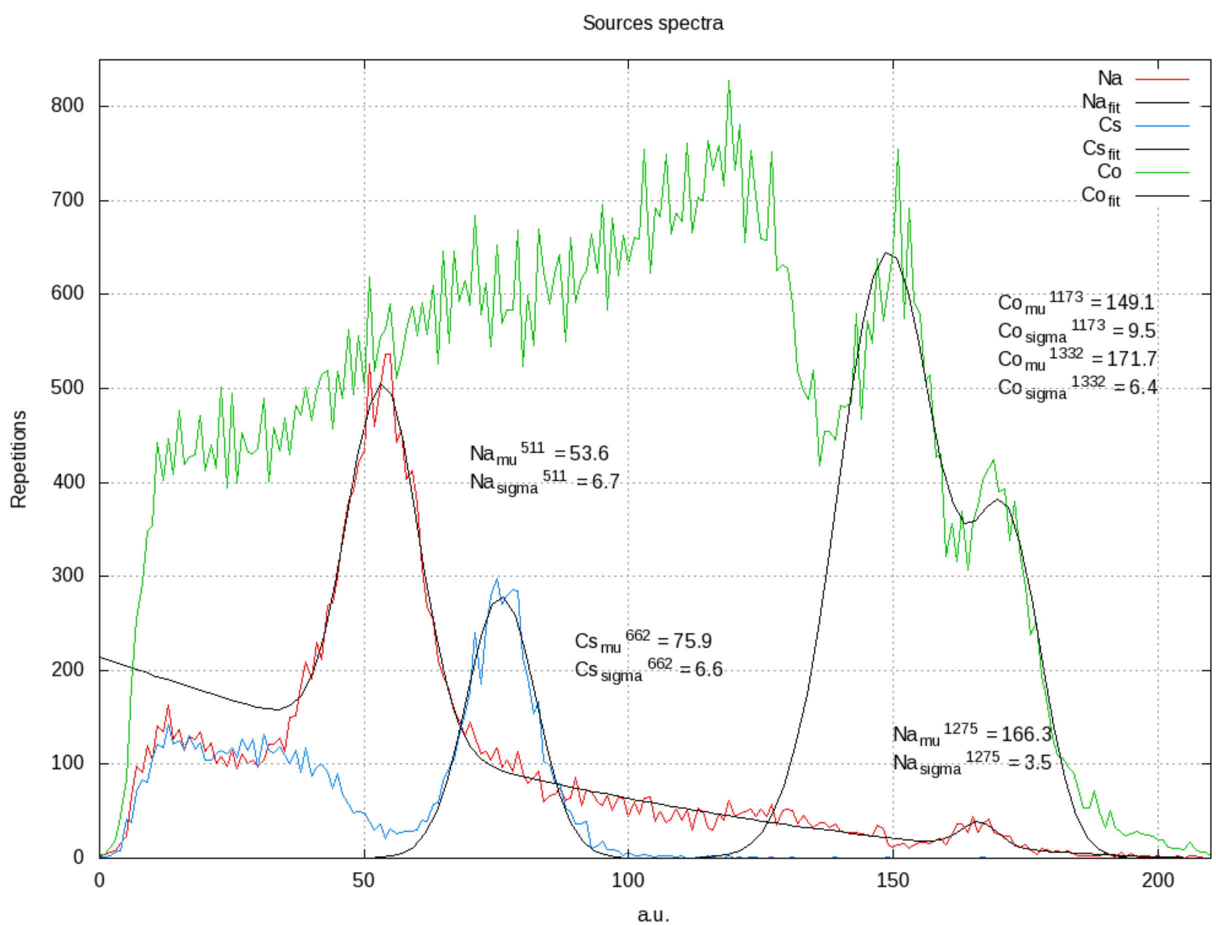
IV. FlexToT: linearized ToT RO chip

- **Good linearity and uniformity**
  - With only comparator threshold offset equalization
- **Different operating ranges can be covered**



IV. FlexToT: linearized ToT RO chip

- **Spectroscopy with linear ToT**

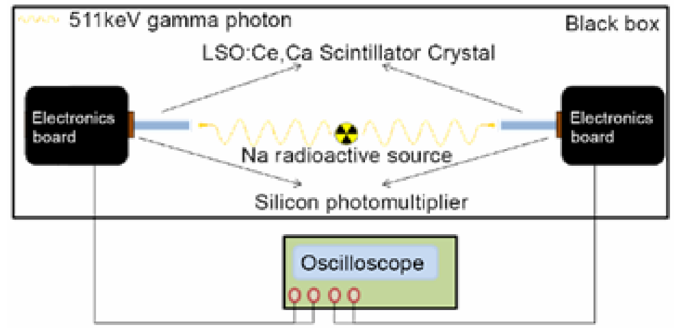


IV. FlexToT: linearized ToT RO chip

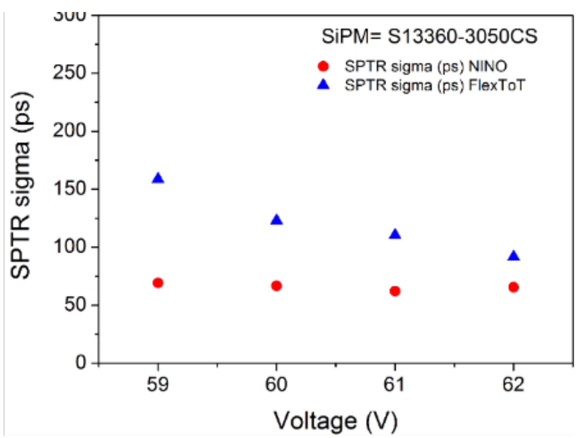
- Measured @ CERN:
  - Single Photon Time resolution (SPTR)
  - Coincidence Time Resolution (CTR)
  - Supported by FAST COST ACTION
    - Many thanks to E. Auffray and S. Gundacker
  - Similar results as for NINO but 3 times lower power consumption

Coincidence Time Resolution (CTR): 128 ps FWHM

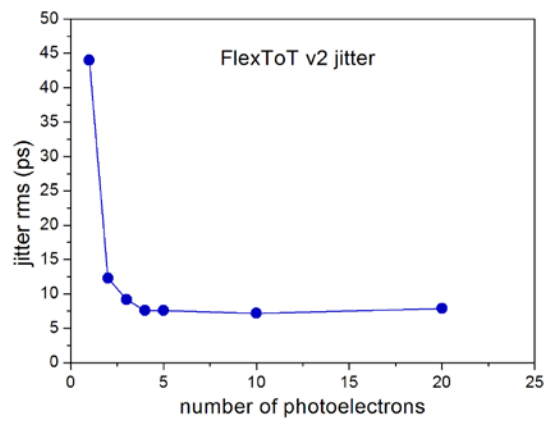
- 2x2x5 mm3 LSO:Ce,Ca crystals.
- Measurements performed in a black-box at 15 ºC.
- Coincidences corresponding to 511 KeV photopeak (±3σ).



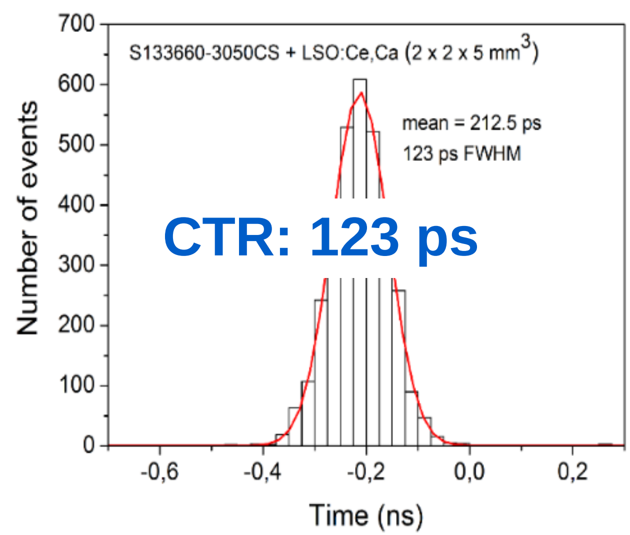
Coincidence Time Resolution (CTR) test bench setup



SPTR=90ps



Jitter floor: 7 ps rms



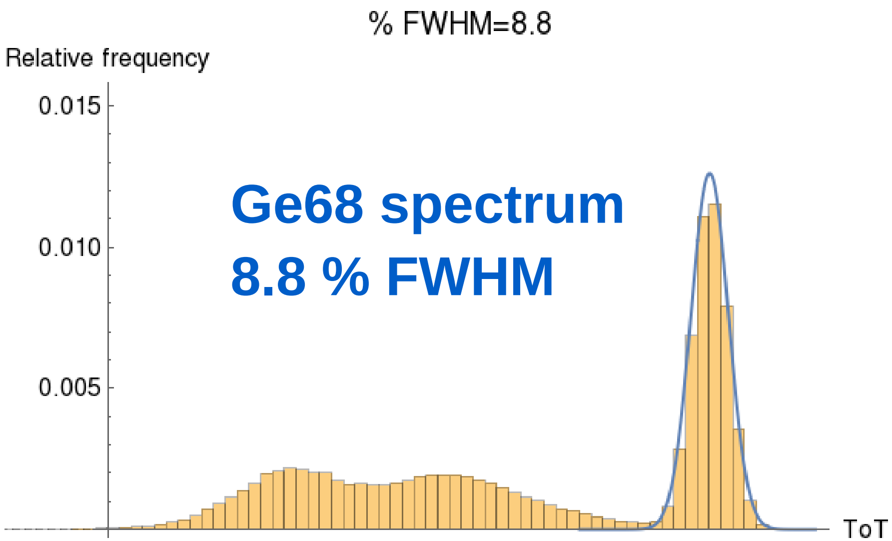
LIGHT

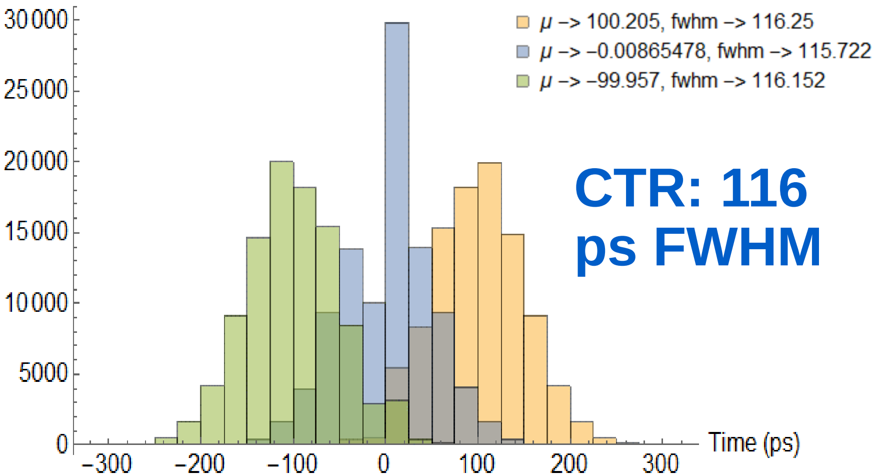
IV. FlexToT: linearized ToT RO chip

- Pisa University has develpped a FPGA based TDC readout for FlexToT
  - Based on Arria 10 FPGA
    - TDC: 38 ps resolution
  - System CTR: 116 ps FWHM !
  - Energy resolution: 8 % FWHM @ 511 KeV
  - Dead time < 5ns

P. Catra,
G. Sportelli

2 LYSO xtals 3x3x5 mm3
NUV-SiPM





Timing distributions for different source positions

Outlook

I. Introduction
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IV. FlexToT: linearized ToT RO chip
V. New developments

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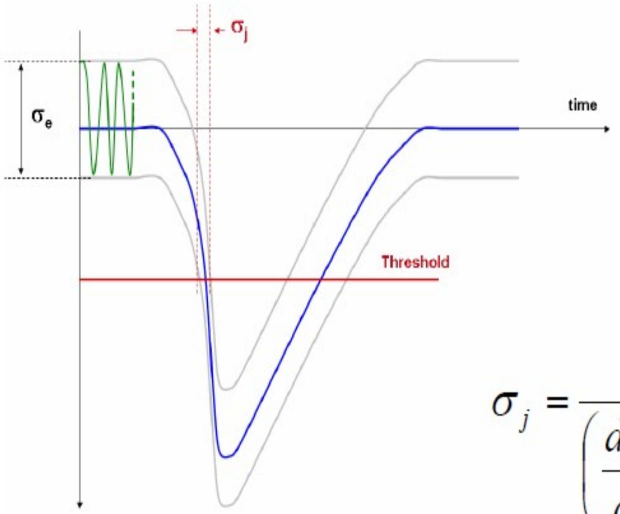
V. New developments

- FE electronics must have low jitter to achieve good timing
  - Low noise
  - High slew rate: dV/dt
    - Not only high BW !
- High BW and low noise are the key for low electronics jitter
- Differential readout can help in:
  - Increasing dV/dt (if coupled to a differential sensor)
  - Rejecting common mode noise
  - But intrinsic noise increases: problem for SE sensors



$$\sigma_j = \frac{\sigma_e}{\left(\frac{dV}{dt}\right)_{threshold}}$$

C. De La Taille, Photodet conference, 2012

Example: NINO ASIC
See C. Williams talk at NDIP2014

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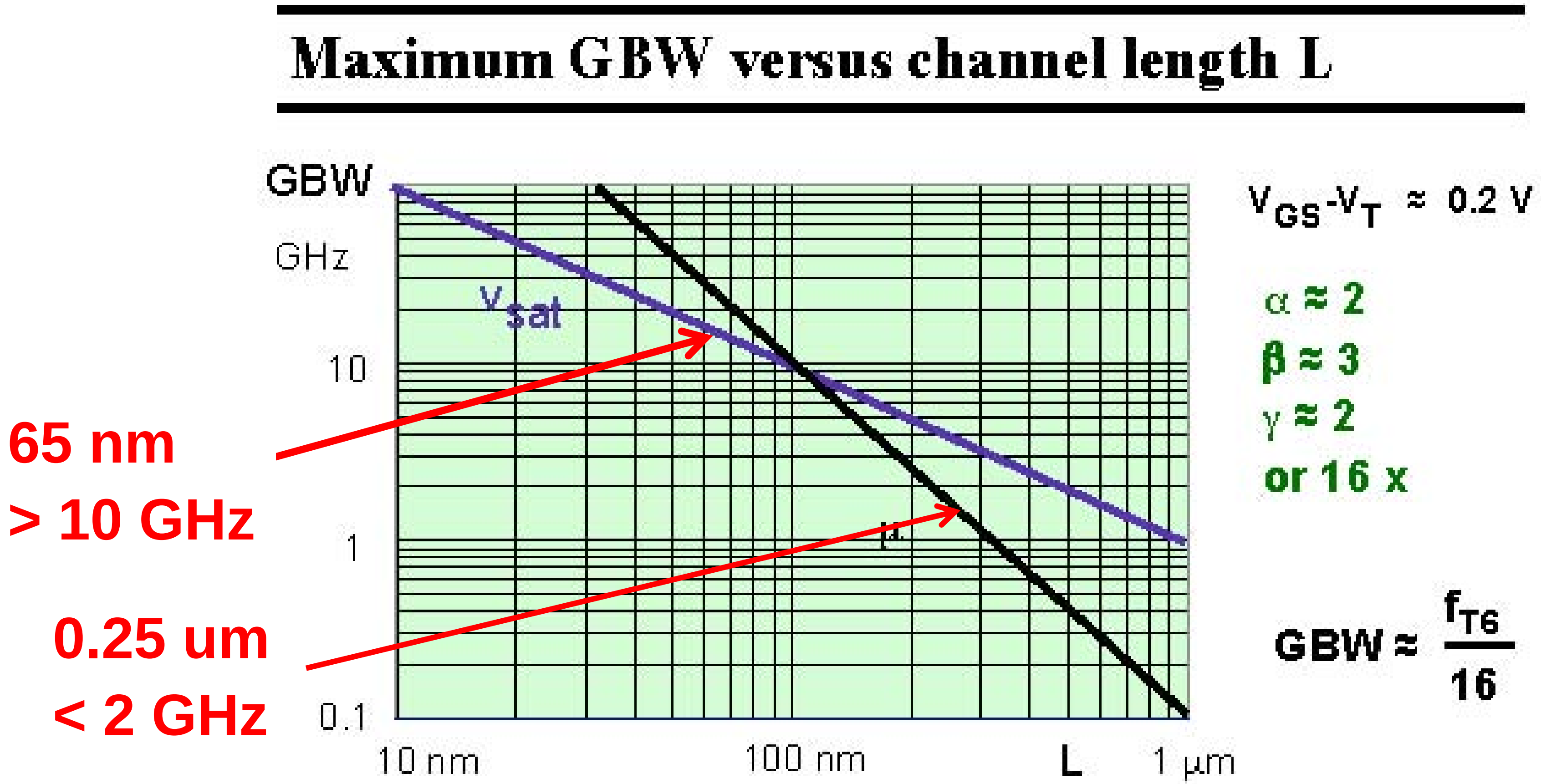
V. New developments

- NINO is a FE chip used in many applications
  - "Old design" in 250 nm
  - Could gain a lot in BW (dV/dt) and jitter by scaling down the design !



W. Sansen, "Analog IC Design in Nanometer CMOS Technologies," VLSI Design, 2009 22nd International Conference, 2009

V. New developments

- Collaboration between CERN and ICCUB to develop a 65 nm FE chip optimized for timing applications
  – First user meeting was held recently: https://indico.cern.ch/event/646451/
    - Please let us know if you are interested
- Different types of fast photo-sensors:
  – PMTs and MCPs
  – SiPMs
  – New structures: Typsy, LAPPD, micromegas, etc
- Use previous concepts:
  – Current mode
  – Flexibility and configurability
  – Linearized ToT

M. Campbell
R. Ballabriga
J. Fernandez

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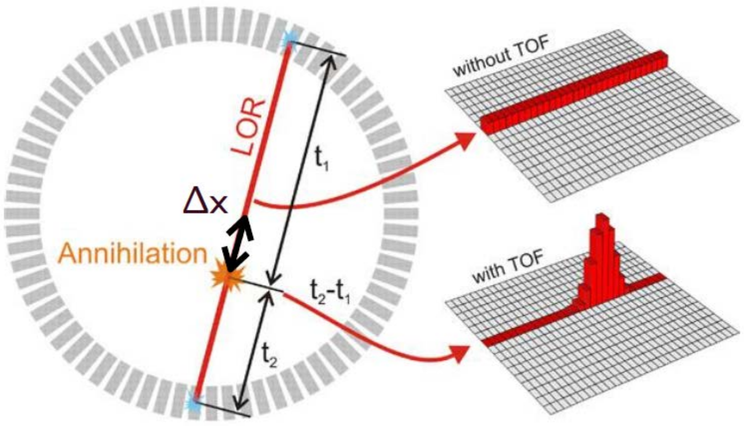
V. New developments

- Why do we need to improve time resolution?



Direct 3D PET

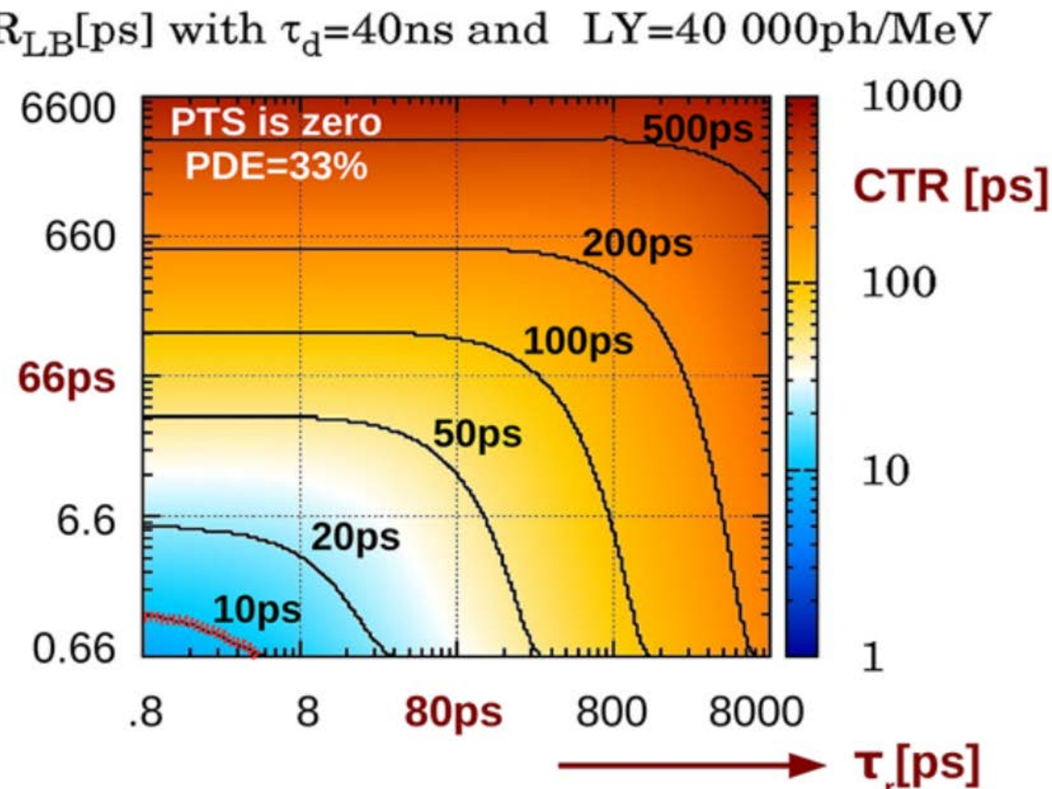
< 20 ps gives mm resolution !

- Enabling direct 3D PET event localization eliminating the need for statistical image reconstruction.
  - Recent results: 100 ps time resolution barrier can be broken
  - A new technological breakthrough is required to achieve direct 3D event localization

V. New developments

- How to achieve it?

http://iopscience.iop.org/article/10.1088/0031-9155/61/7/2802/pdf



Timing resolution of the sensor for a single photon

↓

New developments in photo-detection and FE electronics

↓

SPTR < 20 ps !!!

Scintillator rise time (light emission)

↓

New scintillators: prompt light emission (Cherenkov light, nanocrystals)

V. New developments

	PMT*	SPAD	aSiPM	dSiPM	MCP
PDE	35% (blue)	70% (green)	~45% (blue)	~25% (blue)	35%
SPTR	200ps	20ps	80ps (3x3mm2)	120ps	20ps
Gain					
DCR					
ENF	1.1	1.0x	1.1	?	1.05
Radiation hardness	Good	lower	lower	lower	Good
Reliability/Life	Good	Good	Good	Good	moderate
magnetic field tolerance	bad	Good	Good	Good	moderate
Temperature sensitivit	Good	Good	Good	Good	Good

Excellent SPAD timing resolution is degraded by the current aSIPM and dSIPM architectures: interconnection, skew, etc

V. New developments

- No detector is yet valid to reach a SPTR of 20 ps !!!
- The problem can not be solved only by FE optmization
- ***NEW SENSOR+FE system is required !!!***

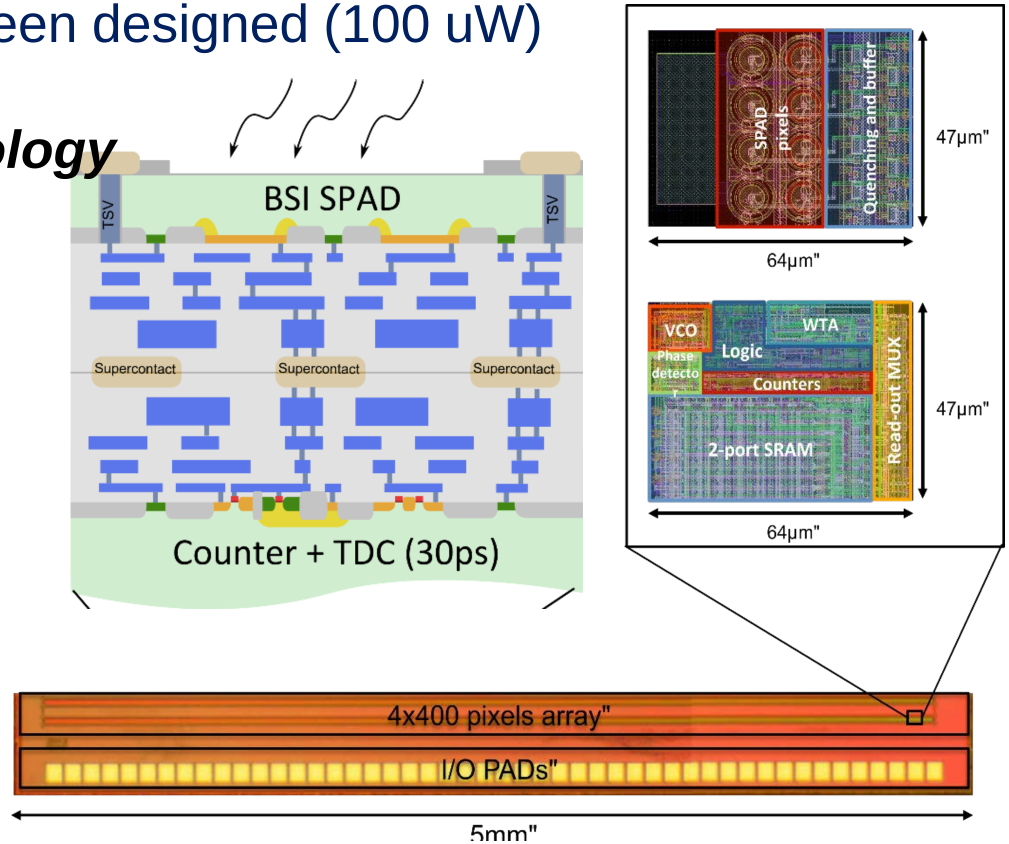
V. New developments

- 3D integration allows 1 TDC per SPAD: no interconnection problem
- Very low power TDCs have been designed (100 uW)

SPAD arrays in CMOS technology
Research at TU Delft
(group of E. Charbon):

- **SPADnet**
- **3D-integration (flip chip)**

Courtesy of E. Charbon



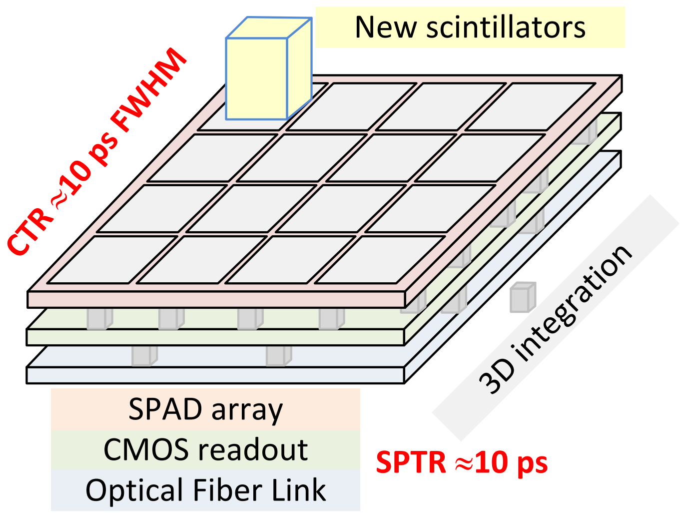
ata Pavia, M. Wolf, E. Charbon, IEEE NSS, 2014

Anyway a typical SiPM has thousands cells
3600x100uW=360 mW (40 mW/mm^2)
per cristal/SiPM not affordable !!!!

V. New developments

- Two enemies to fight to:
  1) Capacitance: Slope (dV/dt) and noise !
  2) Interconnection and non-uniformities: TTS, delay, etc

- R&D on new **hybrid** sensors
  - SiPM microcells divided in subgroups
    - Each subgroup is readout by analog buffer and processed: sum, disc, TDC…
  - Use **best** technology for **sensor** and for **electronics**
    - Similar as for pixel detectors in HEP: exploit vertical integration technology
    - *Cooperation between sensor industry and FE developpers is required* !



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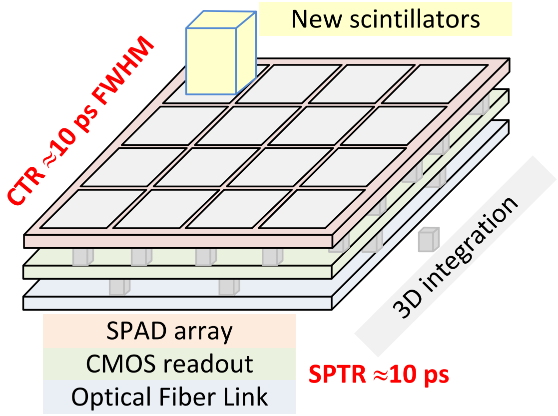
V. New developments

- Two enemies to fight to:
  1) Capacitance: Slope (dV/dt) and noise !
  2) Interconnection and non-uniformities: TTS, delay, etc

HYBRID APPROACH

For SiPM/SPAD and *also* *for other techs…*



- SPTR should approach to the one of the SPAD
  – Sensor capacitance is much smaller
  – Interconnection can be equalized
- Other advantages: high PDE & "clean" technology

Thanks a lot for your attention !!!

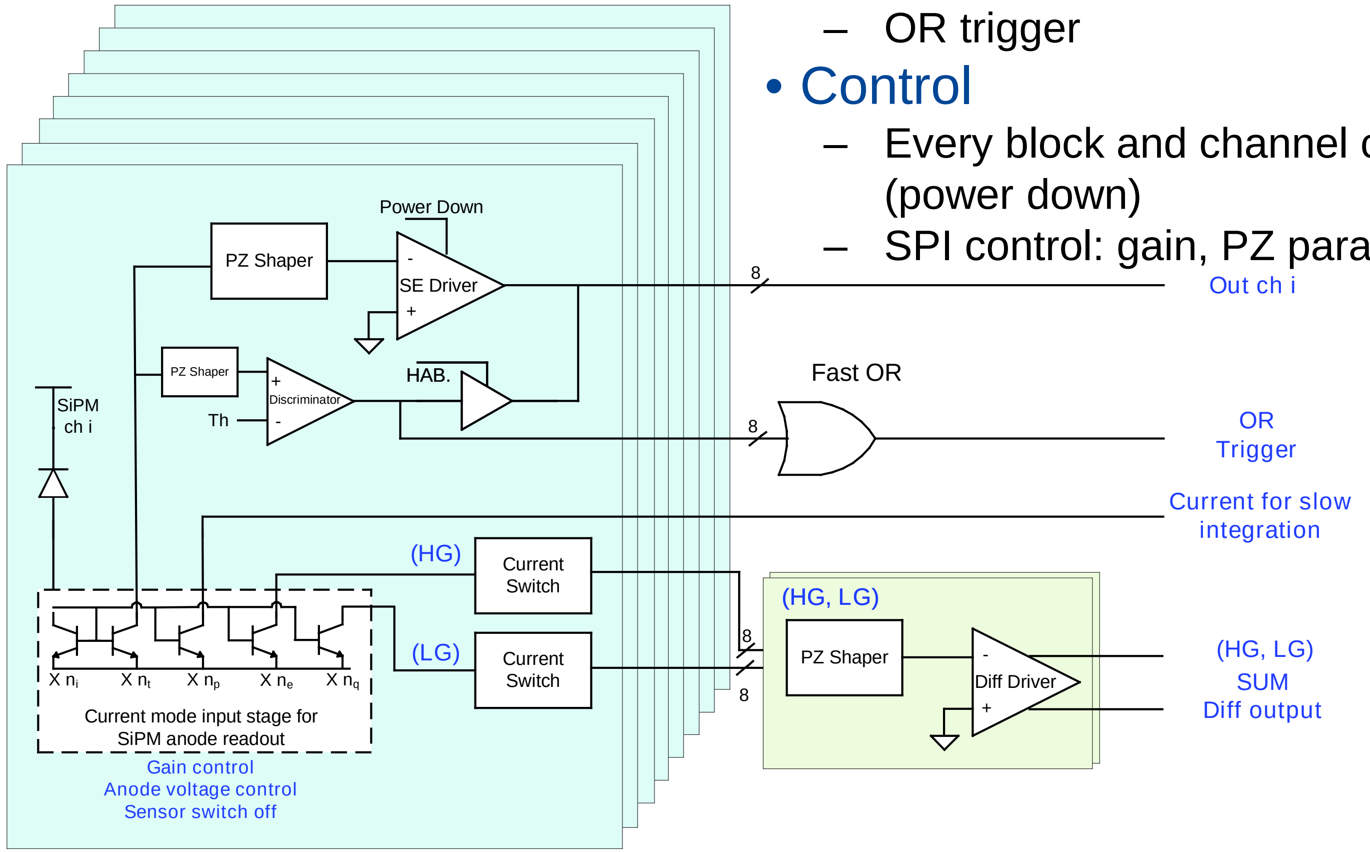
Questions ?

dgascon@fqa.ub.edu

III. MUSIC: Multipurpose SiPM RO chip

- Additional features

- Input
  - Up to 8 pixels (6x6 mm^2 SiPMs)
  - Possible to disable each input reducing overvoltage by 4V
- Outputs:
  - OR trigger
- Control
  - Every block and channel can be disabled (power down)
  - SPI control: gain, PZ parameter, disc th



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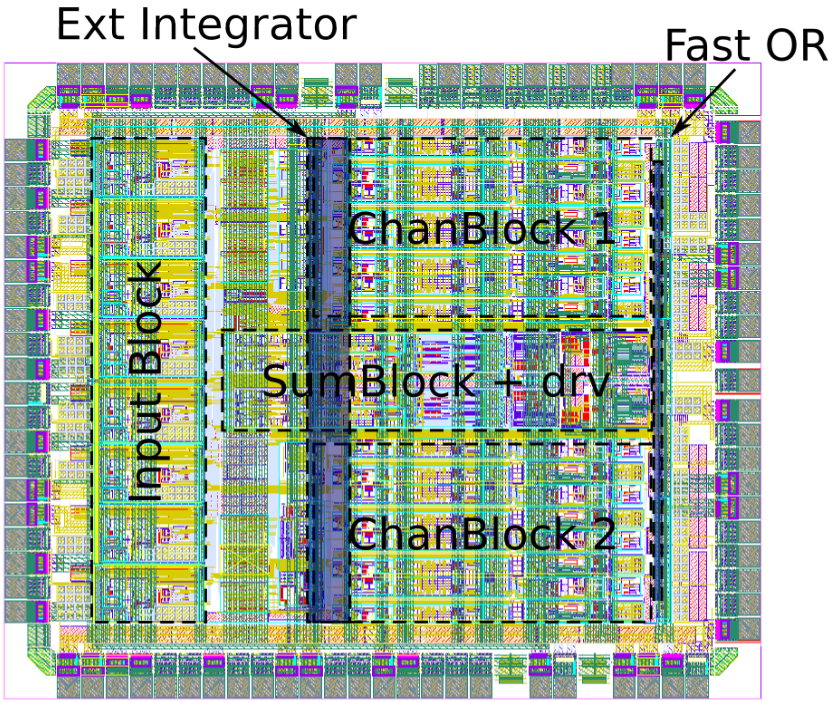
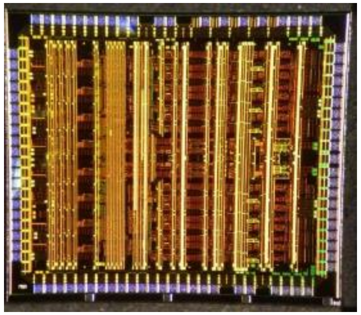
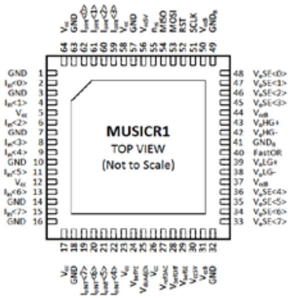
III. MUSIC: Multipurpose SiPM RO chip







- AMS SiGe 0.35um BiCMOS
- Area: 9 mm^2
- 64-QFN 9x9mm package
- Power consumption between 15 and 30 mW/ch depending on the operation mode
- Received in Q2 2016

III. MUSIC: Multipurpose SiPM RO chip

MUSIC evaluation board

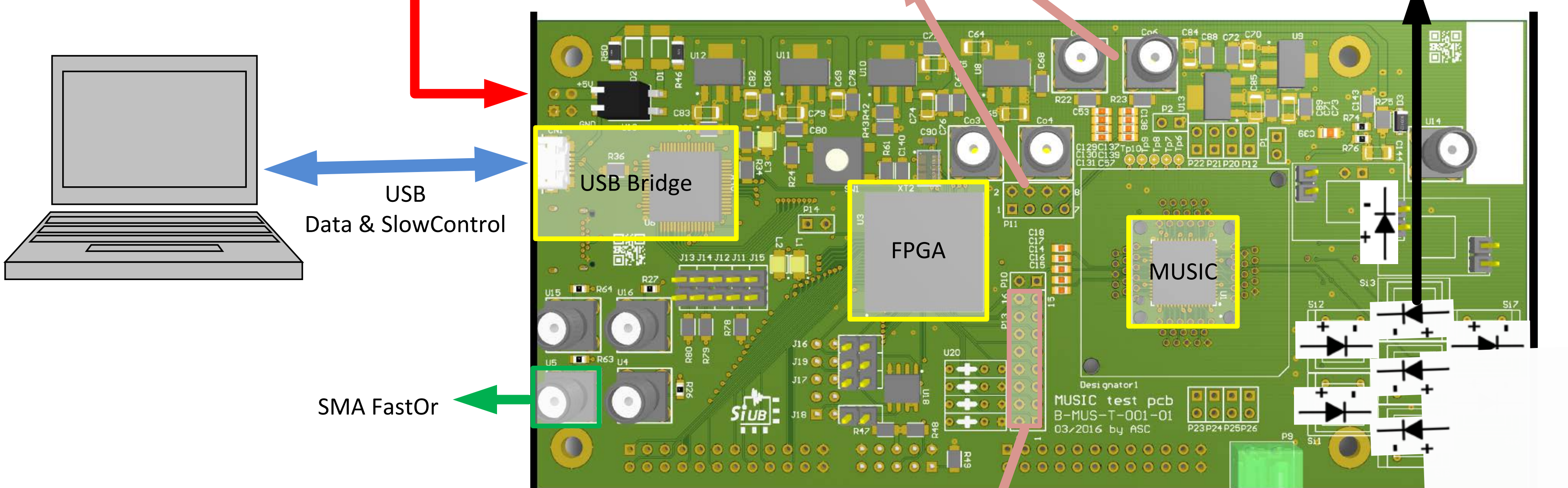
Power supply
(DC 5 V)

Differential Sum
(HG&LG)

Two input methods:

1) Custon card: SIPM_TP1 connector on (bottom)

2) SiPM connector (top)
Designed for 7 (xx SiPM) + 1 (yy SIPM)

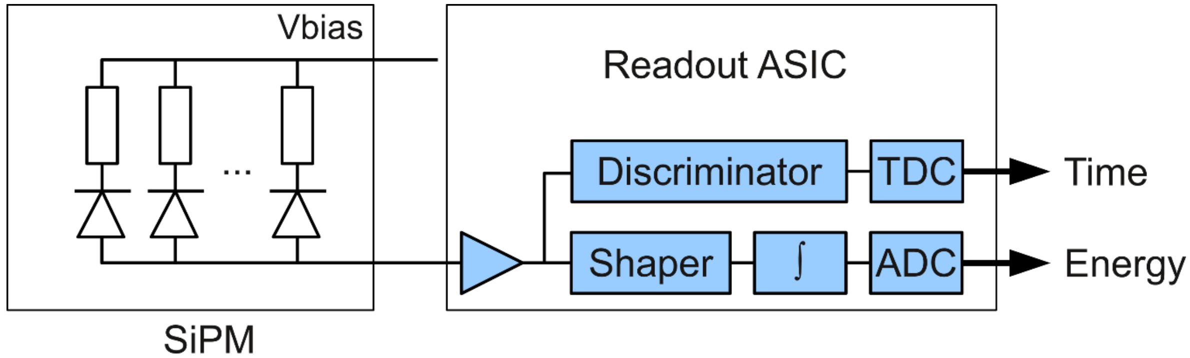


Single Ended Output (8 Channels)
An additional card provides SMA/ LEMO connectivity

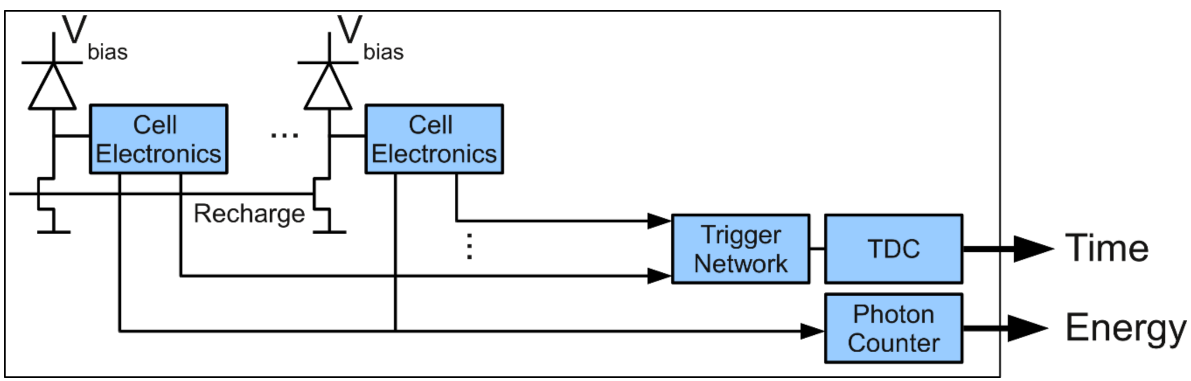
SiPM Supply Voltage

V. New developments

Analog SiPM



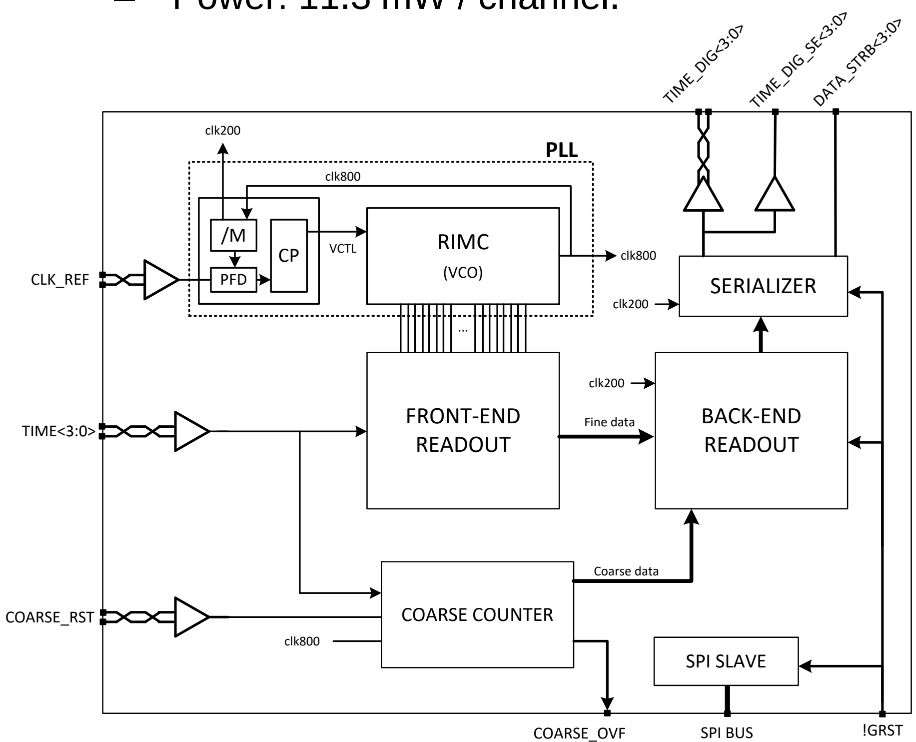
Digital SiPM

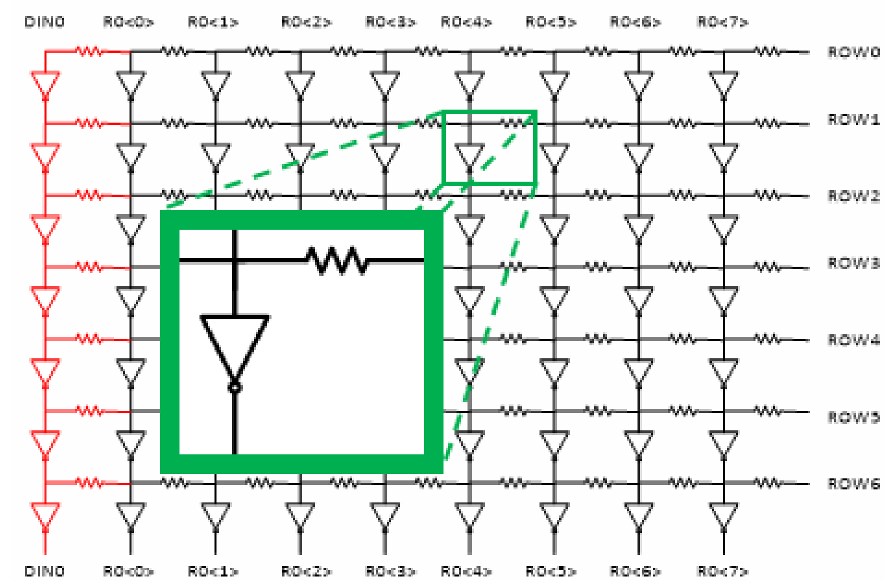


Courtesey of T. Frach & PDPC

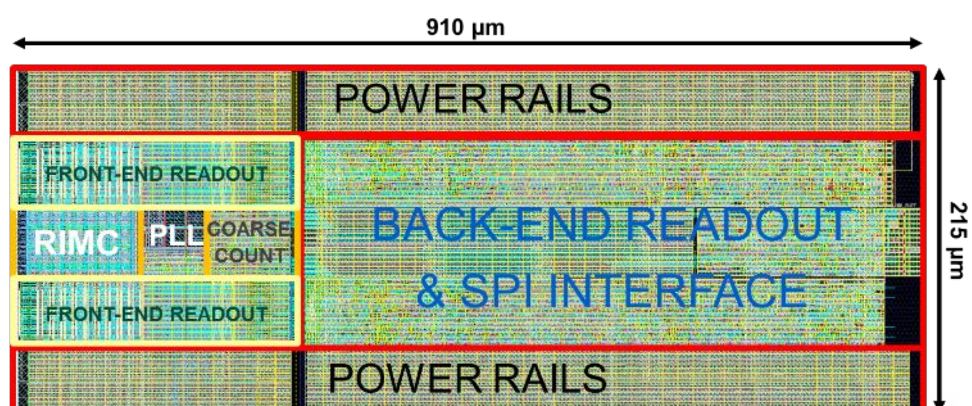
II. MATRIX TDC

- MATRIX is a 4 ch 15 ps TDC
  - 4 input channels.
  - 15-ps nominal time bins.
  - Jitter: 10 to 20 ps.
  - Linearity: 4 ps.
  - Power: 11.3 mW / channel.





RIMC schematic: an array of Ring Oscillators

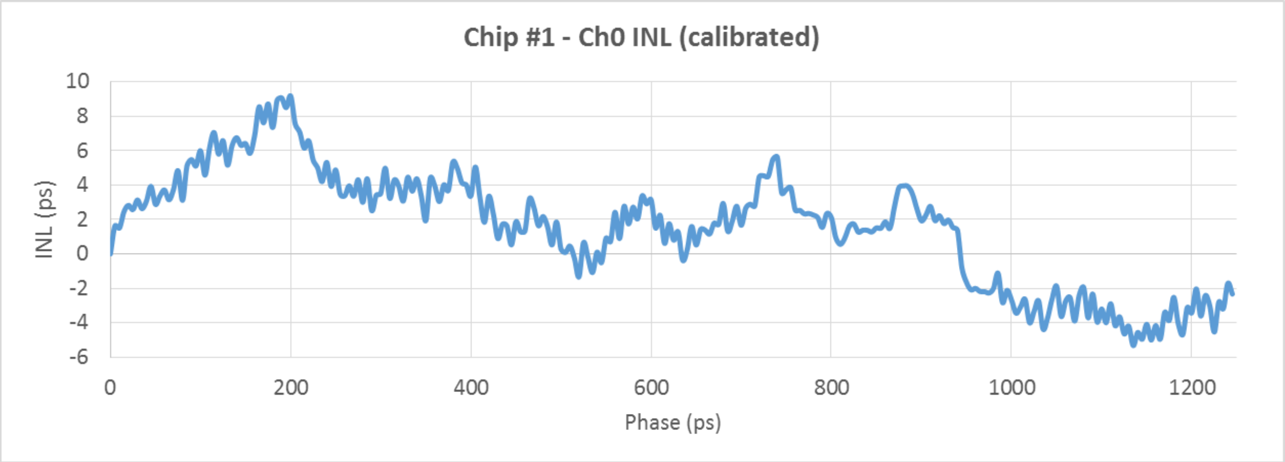


Technology: CMOS 180 nm

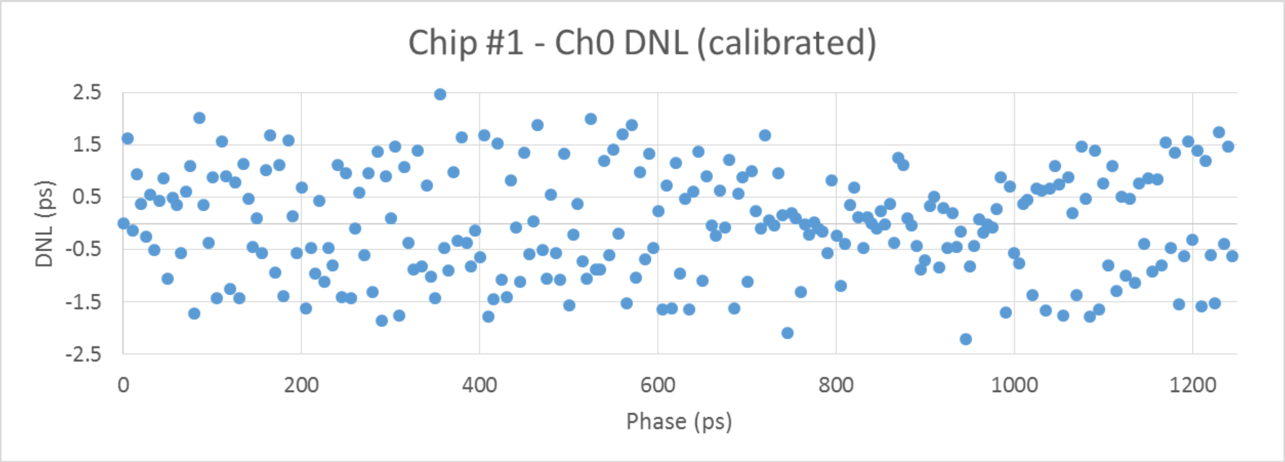
J. Mauricio et alt. “MATRIX: a 15 ps resistive interpolation TDC ASIC based on a novel regular structure”, JINST 2016.

Measurement Results

- Linearity:



- INL = ± 10.2 ps
- RMS INL < 3.7 ps



- DNL = ± 4.7 ps
- RMS DNL < 1.1 ps

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Measurement Results

- Jitter (pulse generator + MATRIX TDC):

PLL M	TDC Jitter (ps)	
	Uncalibrated	Calibrated
4	9.7	9.3
8	13.4	12.9
16	21.2	20.6

– TDC jitter is dominated by PLL.

- M = 4 has a natural frequency (ω_n) 2X M = 8 and thus jitter improves.
- Improved by factor > 2 in MATRIXV2 TBC: just received

$$\omega_n = \sqrt{\frac{K_{VCO}.I_{CP}}{M \cdot C_1}}$$

$K_{VCO} = VCO\ gain \left[\frac{Hz}{V}\right]$

$I_{CP} = CP\ current\ [A]$

$M = fb\ divisor$

$C_1 = large\ loop - filter\ \ cap\ [F]$

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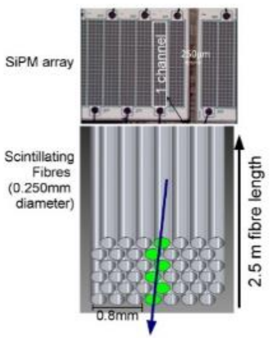
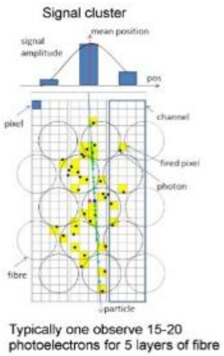
MATRIX TDC Specifications

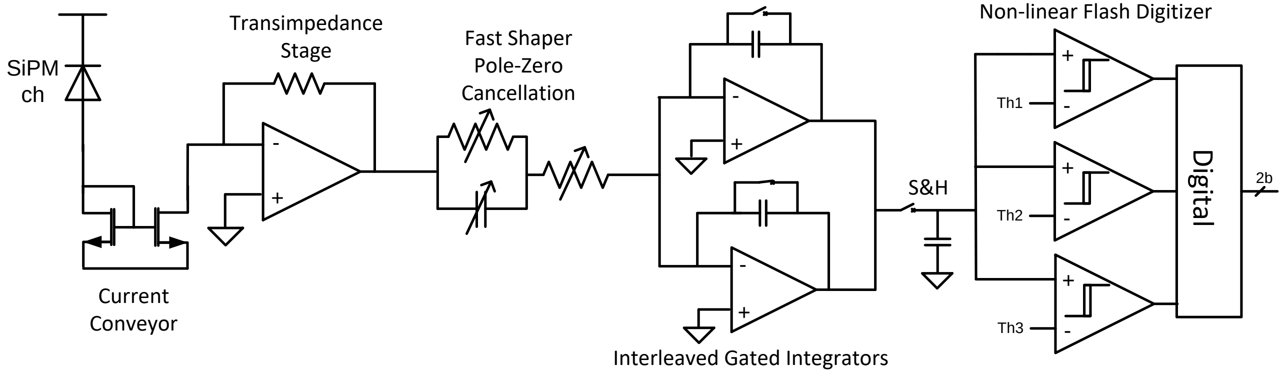
#Channels	4
Resolution	15 ps (sub-delay), 10 ps (statistical)
Linearity	< 4 ps RMS
Jitter	< 10 ps (v1), < 5 ps (v2)
Power consumption	45 mW
Dynamic range	1280 ns
Max. Input rate	10 MHz (sustained), 50 MHz (peak)
Dead time	< 20 ns
Reference clock	50 / 100 / 200 MHz
Outputs	Individual • Single Ended • LVDS
Configurability	SPI

Other FE ASICs: PACIFIC

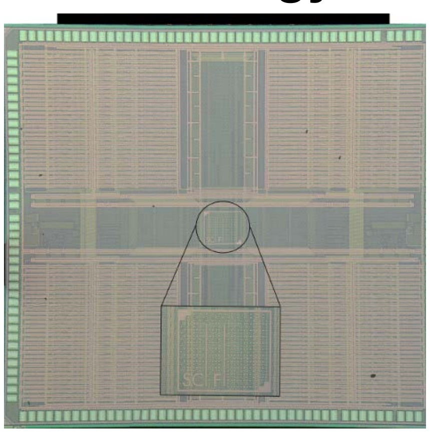
- PACIFIC: A 64 ch ASIC for Scintillating Fiber Tracking in LHCb Upgrade
- Collaboration with Heidelberg, LPC-Clermont, IFIC-Valencia







130 nm CMOS technology



- Similar input current conveyor as in FlexToT
- Current conveyor with very low impedance input (≈ 30Ω)
  - Adjustable gain / dynamic range
  - Input voltage adjustment
- Fast tunable shaper
  - Pole-zero cancellation to cancel slow SIPM time constant
  - A FWHM of 5 ns is achieved for single-cell signal
- Dual interleaved 25ns gated integrator
  - Almost no dead time
  - Average photo-statistical fluctuations
  - Maximize charge collection (25 ns integration)
- 2 bits 40MS/s flash non-linear ADC
- Power consumption < 8mW/channel @ 1.2 V

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