Assembly of Large-Area Planar MCP-based Photo-Detectors without Vacuum Transfer of the Window

Andrey Elagin
University of Chicago

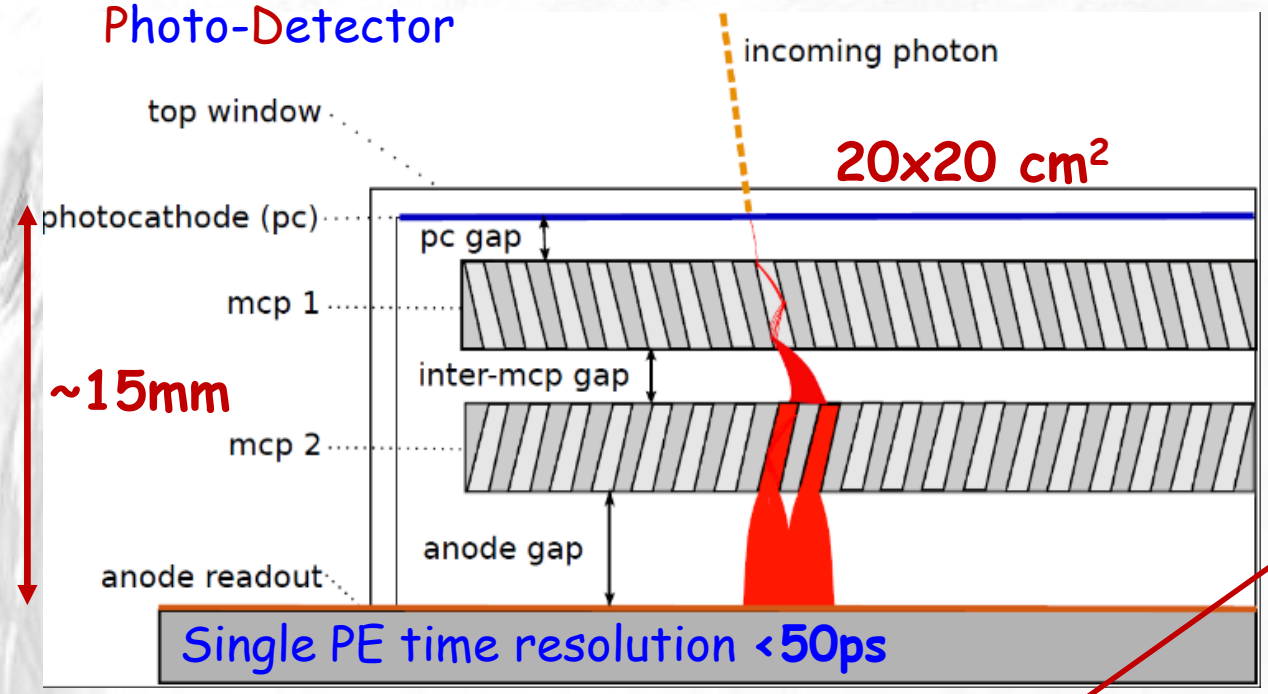
UChicago PSEC Team:

Evan Angelico, AE, Henry Frisch, Rich Northrop, Carla Pilcher, Eric Spieglan
plus Eric Oberla and Mircea Bogdan on electronics
plus 12 high school and undergrad students last summer

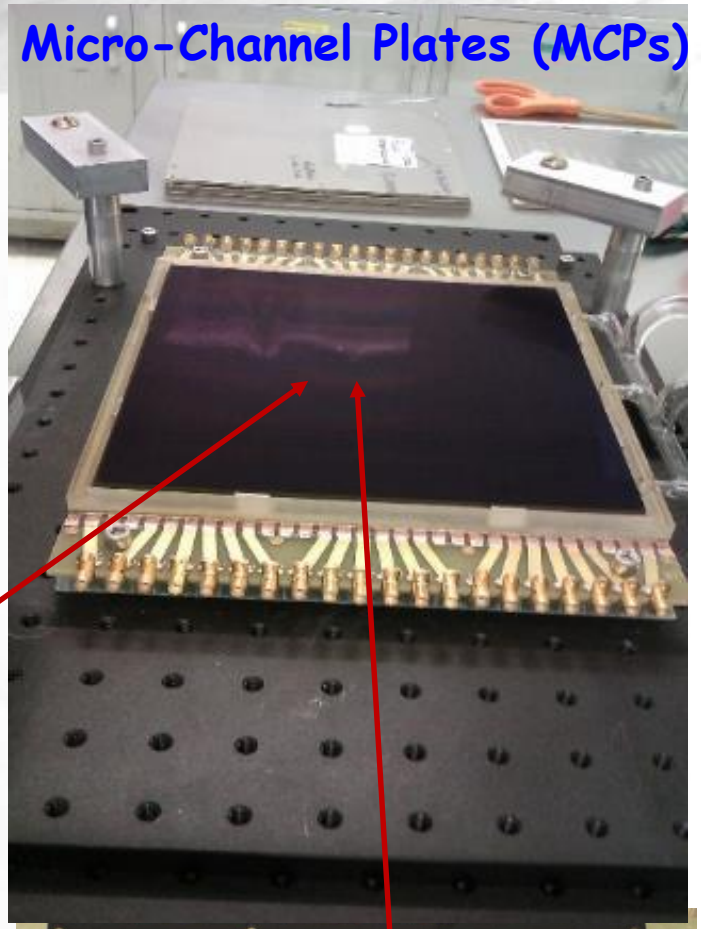
LIGHT-17, Ringberg Castle, October 17, 2017

LAPPD™

Large-Area Picosecond Photo-Detector

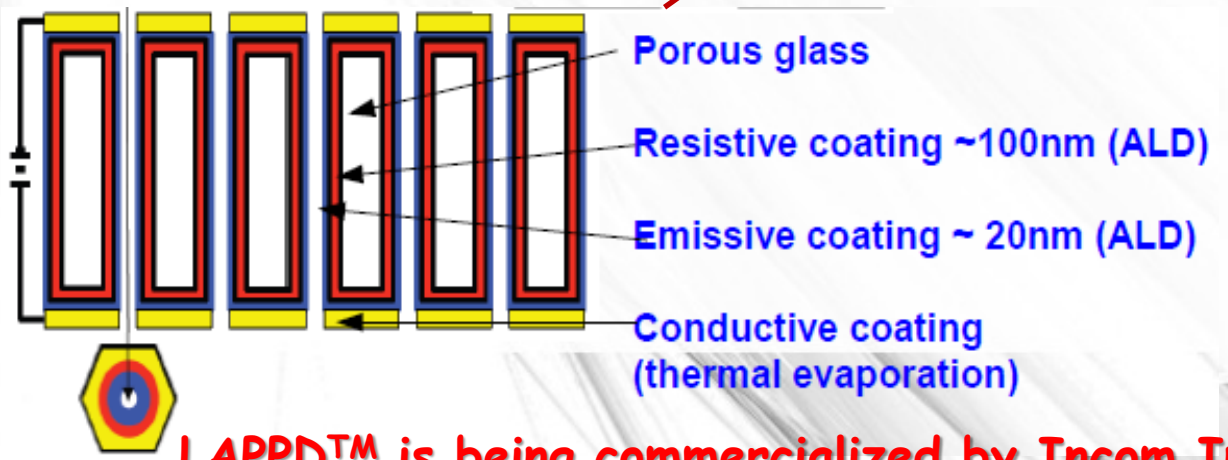


Micro-Channel Plates (MCPs)



Atomic Layer Deposition (ALD)

- J.Elam and A.Mane at Argonne
(process is now licensed to Incom Inc.)
- Arradiance Inc. (independently)

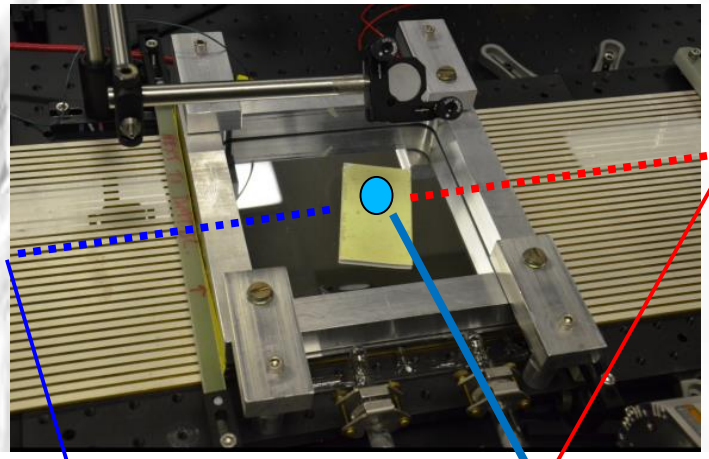


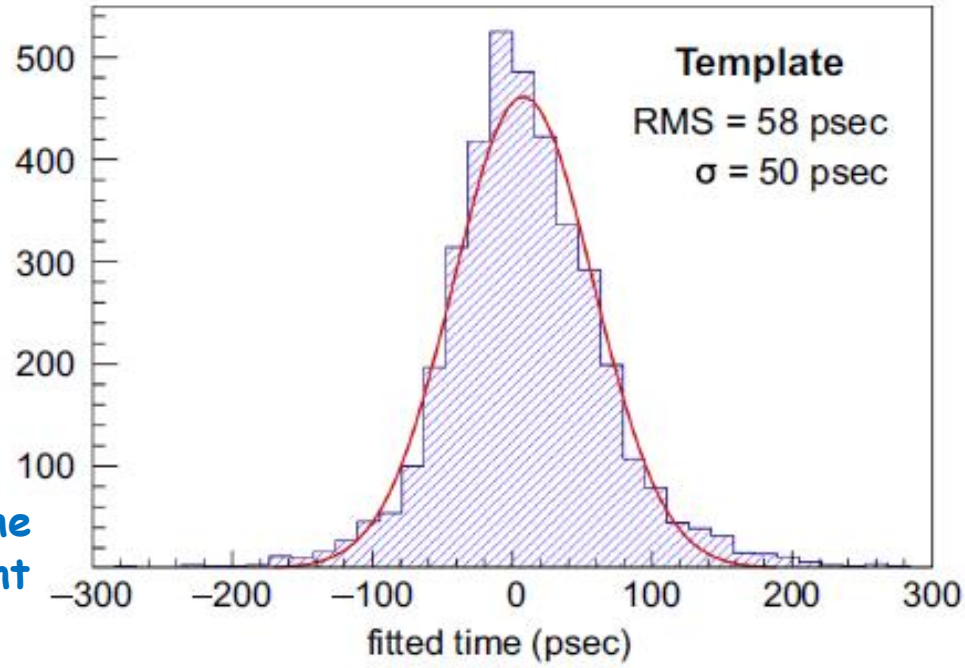
Micro-Capillary Arrays by Incom Inc.

LAPPD™ is being commercialized by Incom Inc.

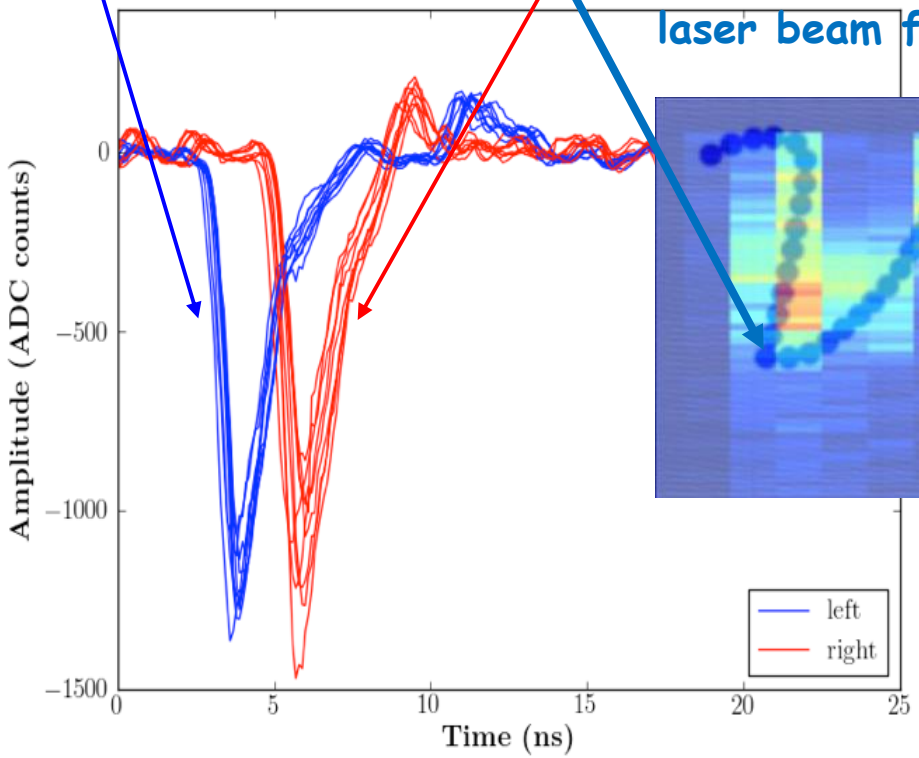
LAPPD Prototype Testing Results

Single PE resolution





Reconstruction of the laser beam footprint

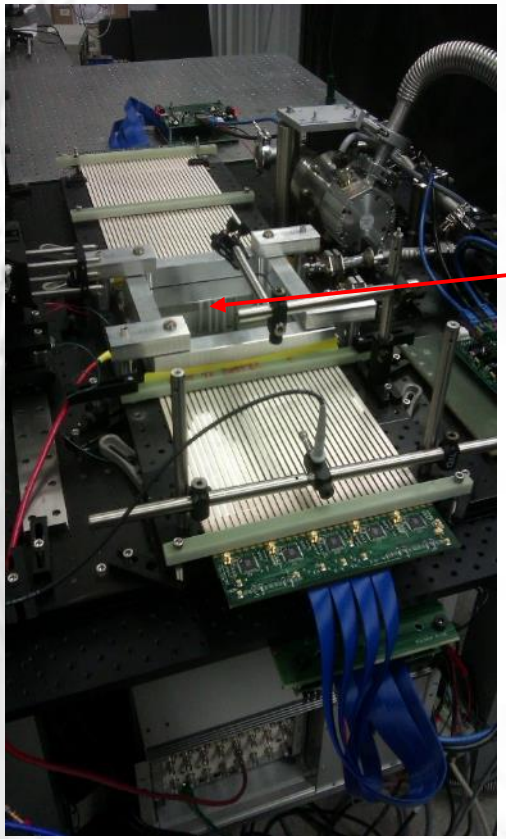


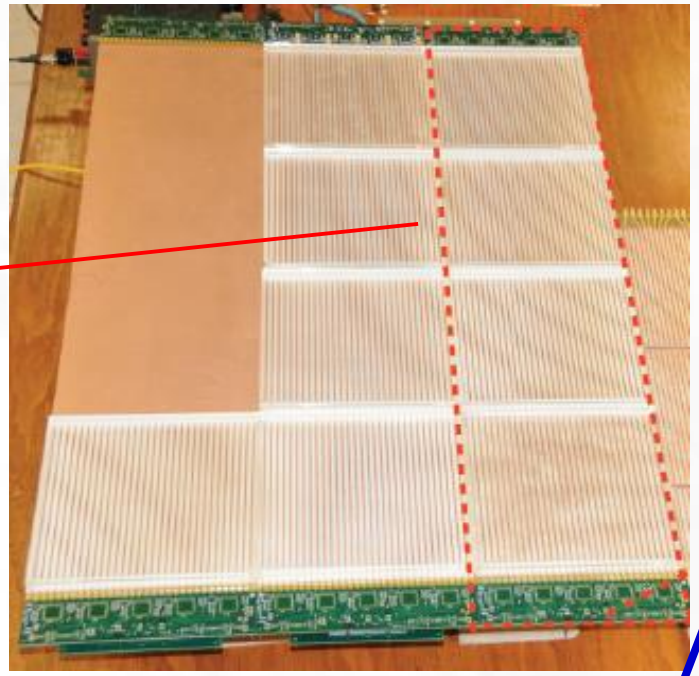
Demonstrated characteristics:
single PE timing ~50ps
multi PE timing ~35 ps
differential timing ~5 ps
position resolution < 1 mm
gain >10^7

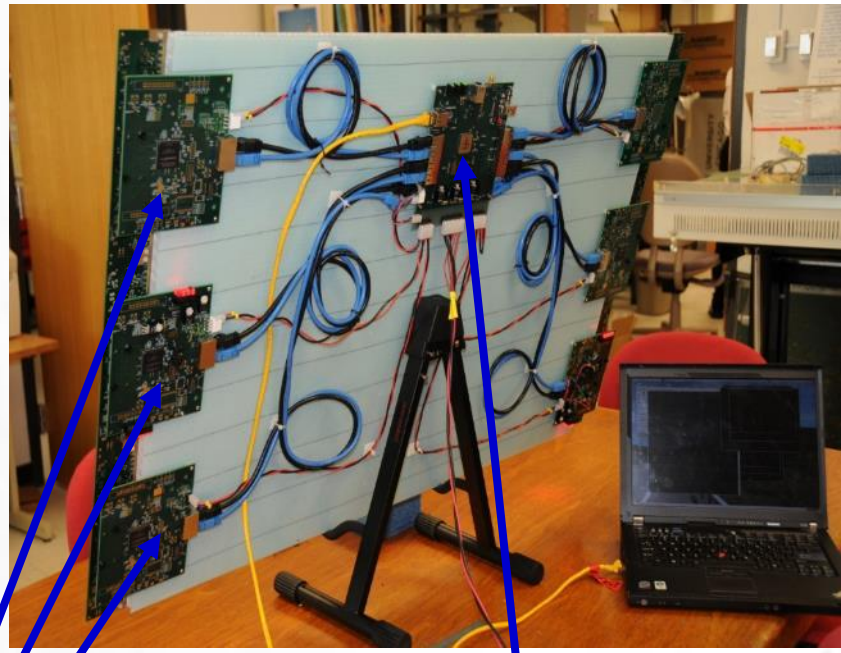
RSI 84, 061301 (2013),
NIMA 732, (2013) 392
NIMA 795, (2015) 1
arXiv:1603.01843

See our doc library at:
http://lappddocs.uchicago.edu/

LAPPD Electronics at Chicago



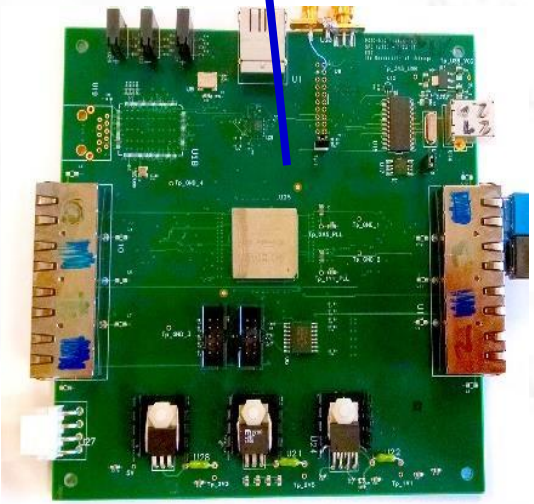




NIM 711 (2013) 124

Delay-line anode
- 1.6 GHz bandwidth
- number of channels
  scales linearly with area

30-Channel ACDC Card
(5 PSEC-4)

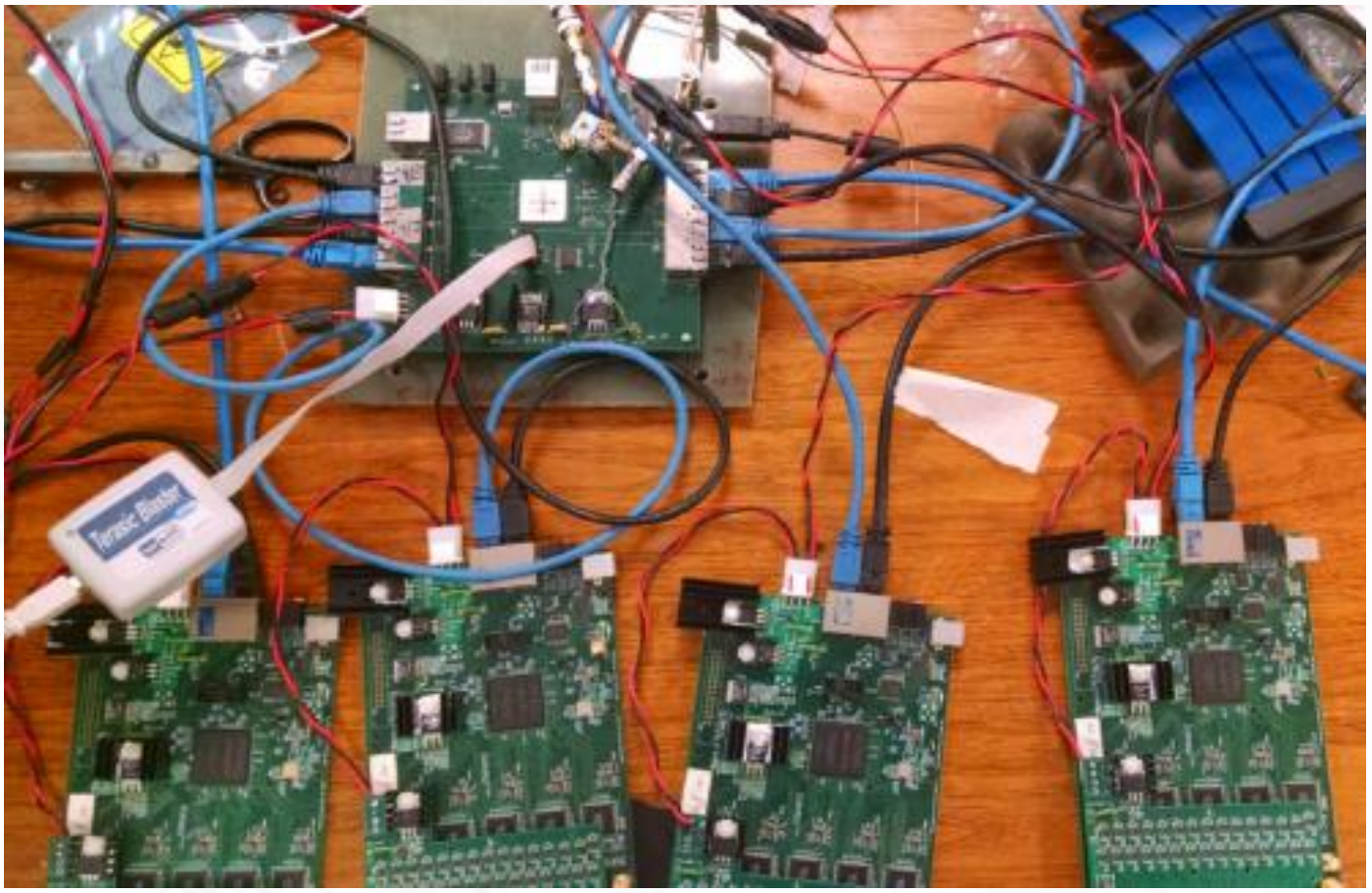


Central Card
(4-ACDC;120ch)

NIM 735 (2014) 452

PSEC-4 ASIC chip
- 6-channel, 1.5 GHz, 10-15 GS/s

Multichannel Systems

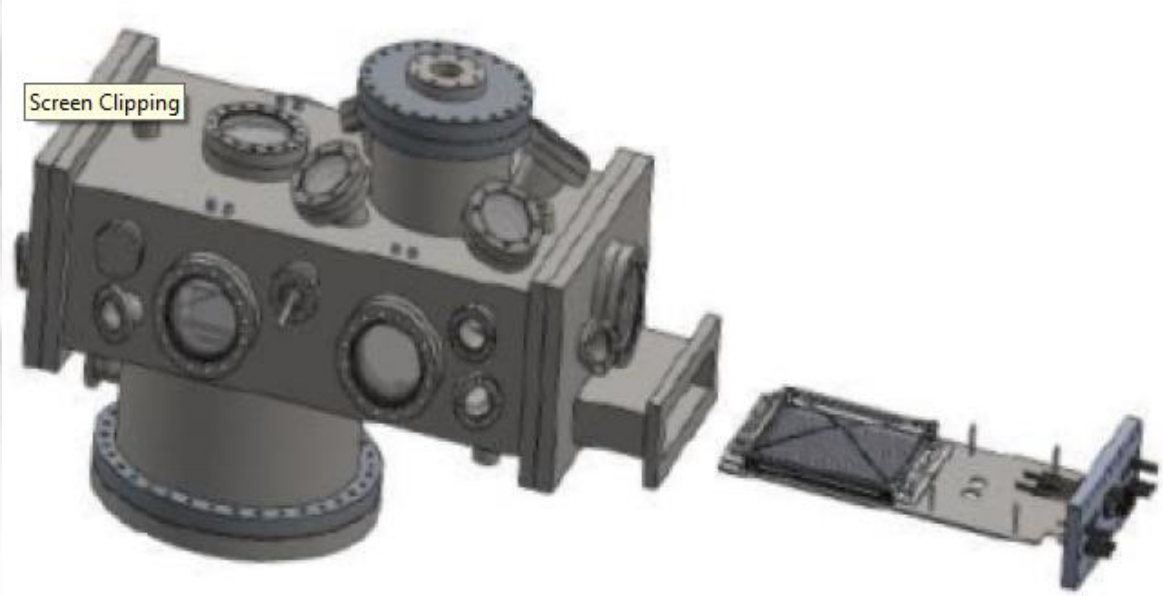


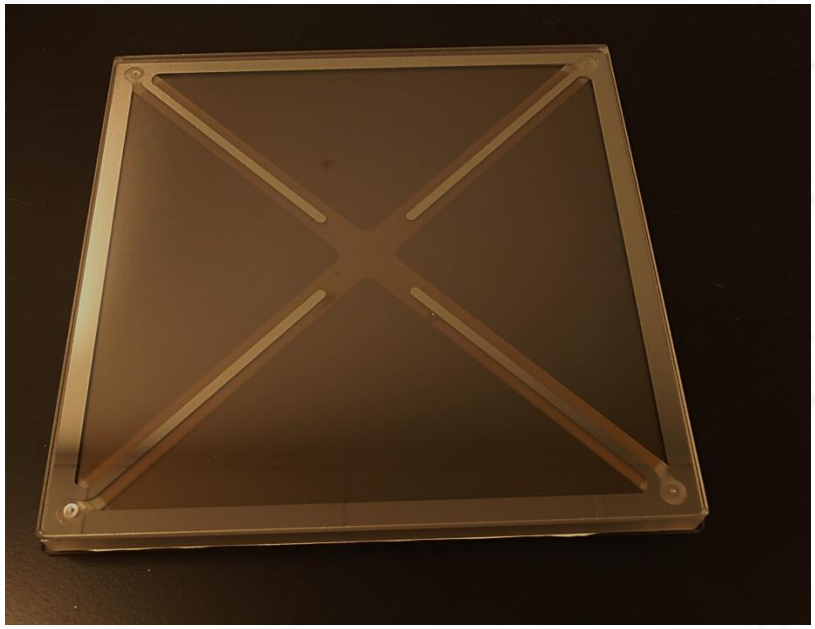
- 60-channel LAPPD prototype at the ANL Laser Lab
- 180-channel self-triggered Optical TPC at Fermilab
- Central card controls several front end boards
- New central cards by Mircea Bogdan handles 1920 channels
- PSEC4A is back from Mosis (funded by Sandia, work by E.Oberla)

LAPPD™ Commercialization

Incom Inc. (Charlton, MA) is working on making LAPPD™ commercially available

Supported by DOE via SBIR grant



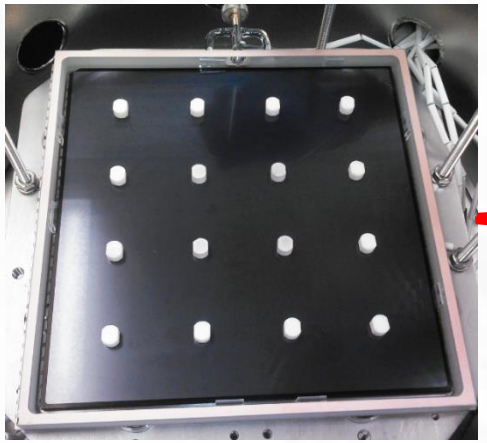


For more information contact Michael Minot, Director R&D, Incom Inc., mjm@incomusa.com

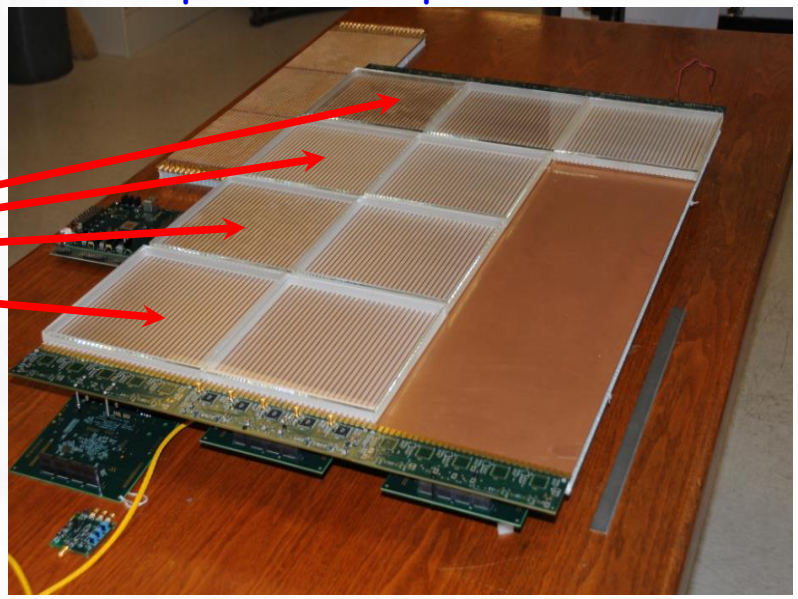
Goal of the R&D Effort at UChicago

Affordable large-area many-pixel photo-detector systems with picosecond time resolution

LAPPD module 20x20 cm^2



Example of a Super Module

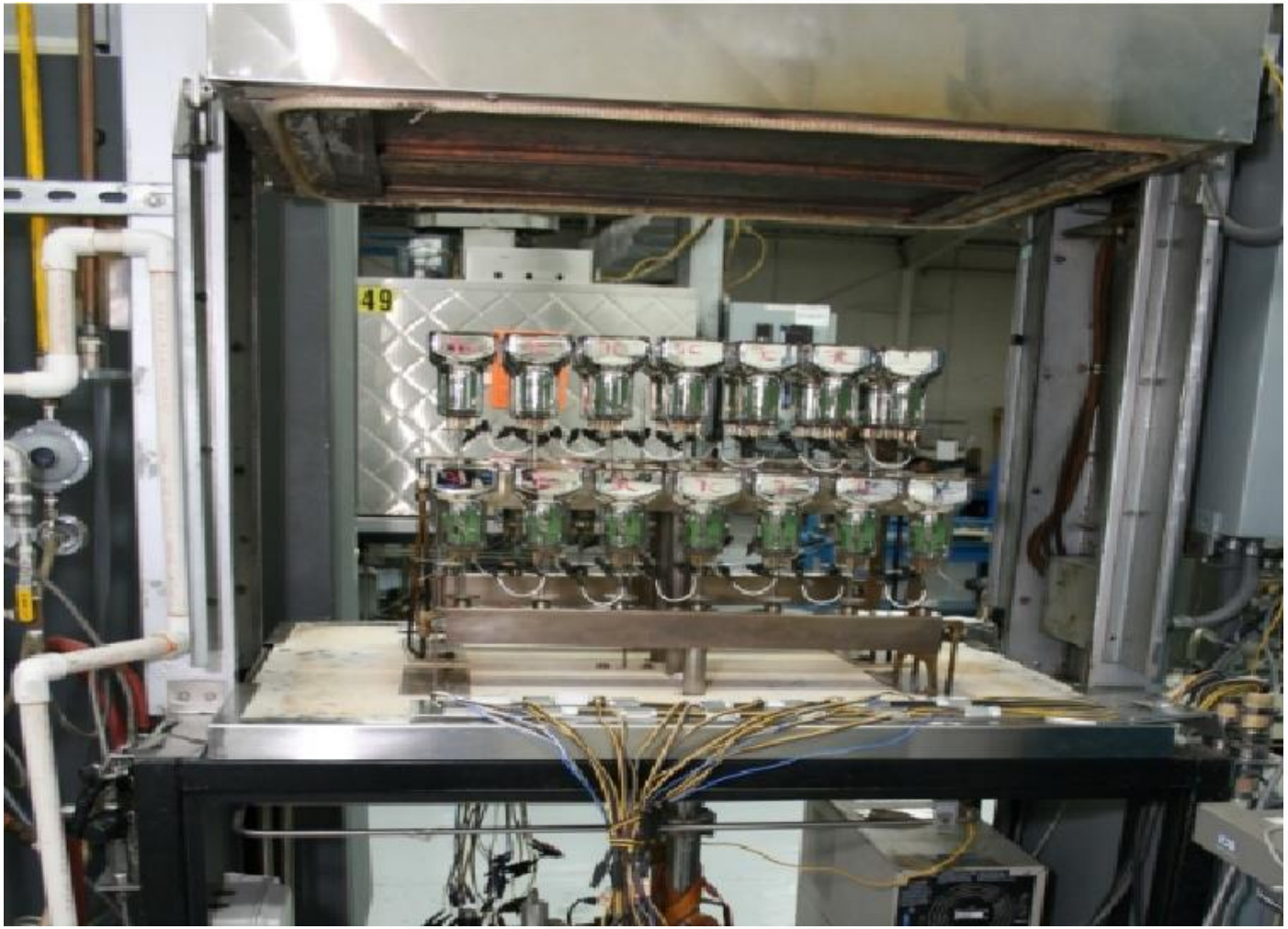


We are exploring if an *In-Situ* process (without vacuum transfer) can be inexpensive and easier to scale for a very high volume production

Production rate of 50 LAPPDs/week would cover 100m^2 in one year

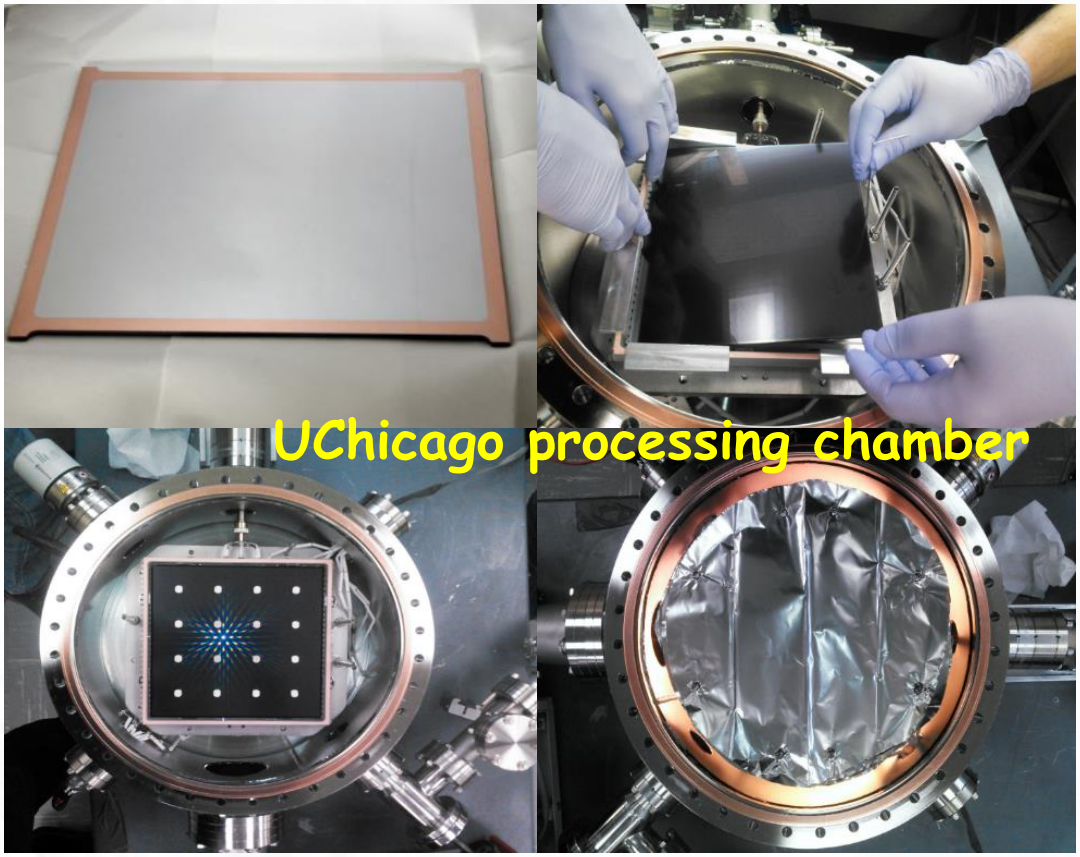
UChicago goal is to develop alternative high volume, scalable, low cost processing options (in close collaboration with Incom Inc.)

Can We Make LAPPDs in Batches Like PMTs?



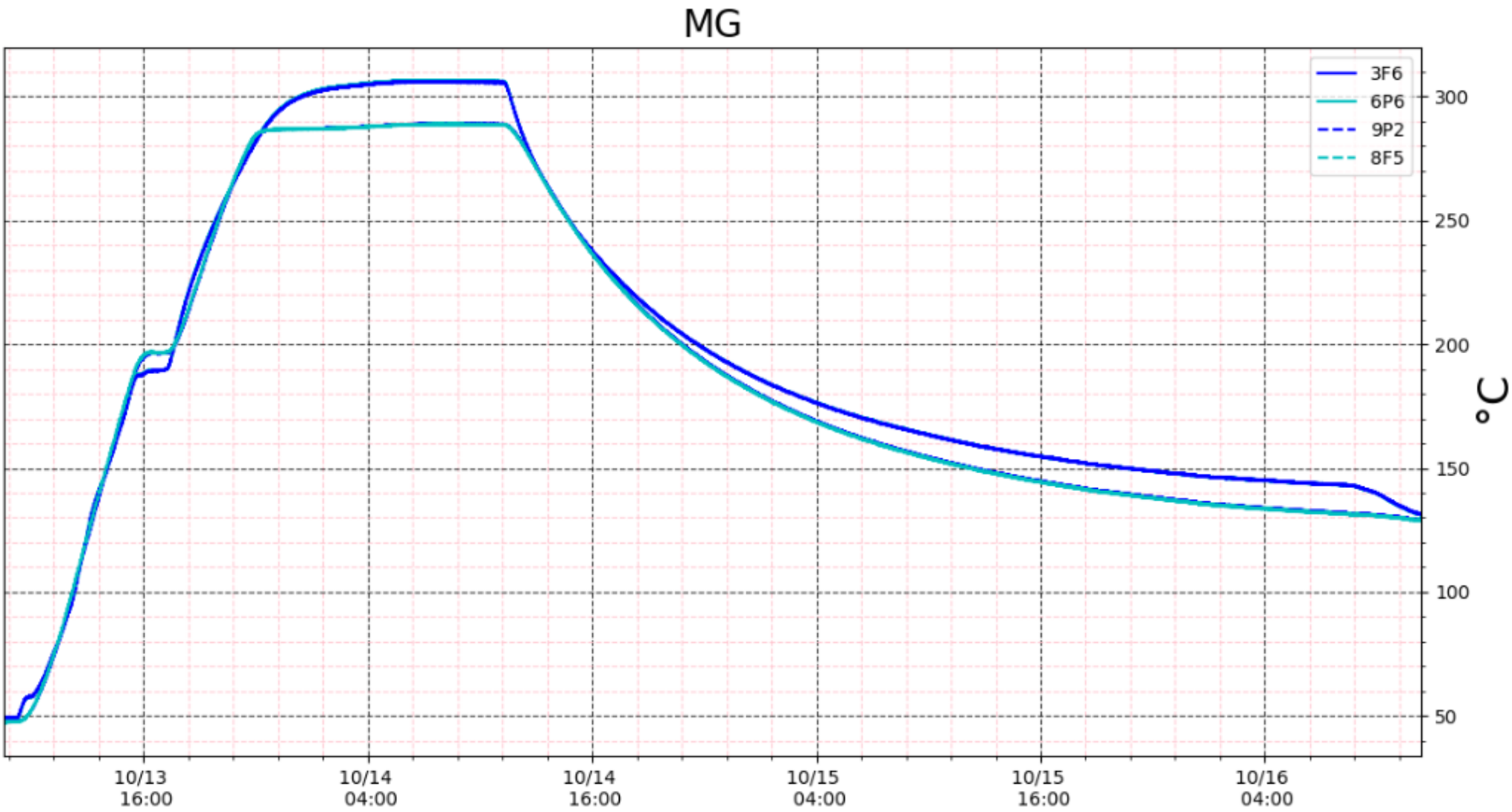
In-Situ Assembly Strategy

Make photo-cathode after the top seal
(PMT-like batch production)

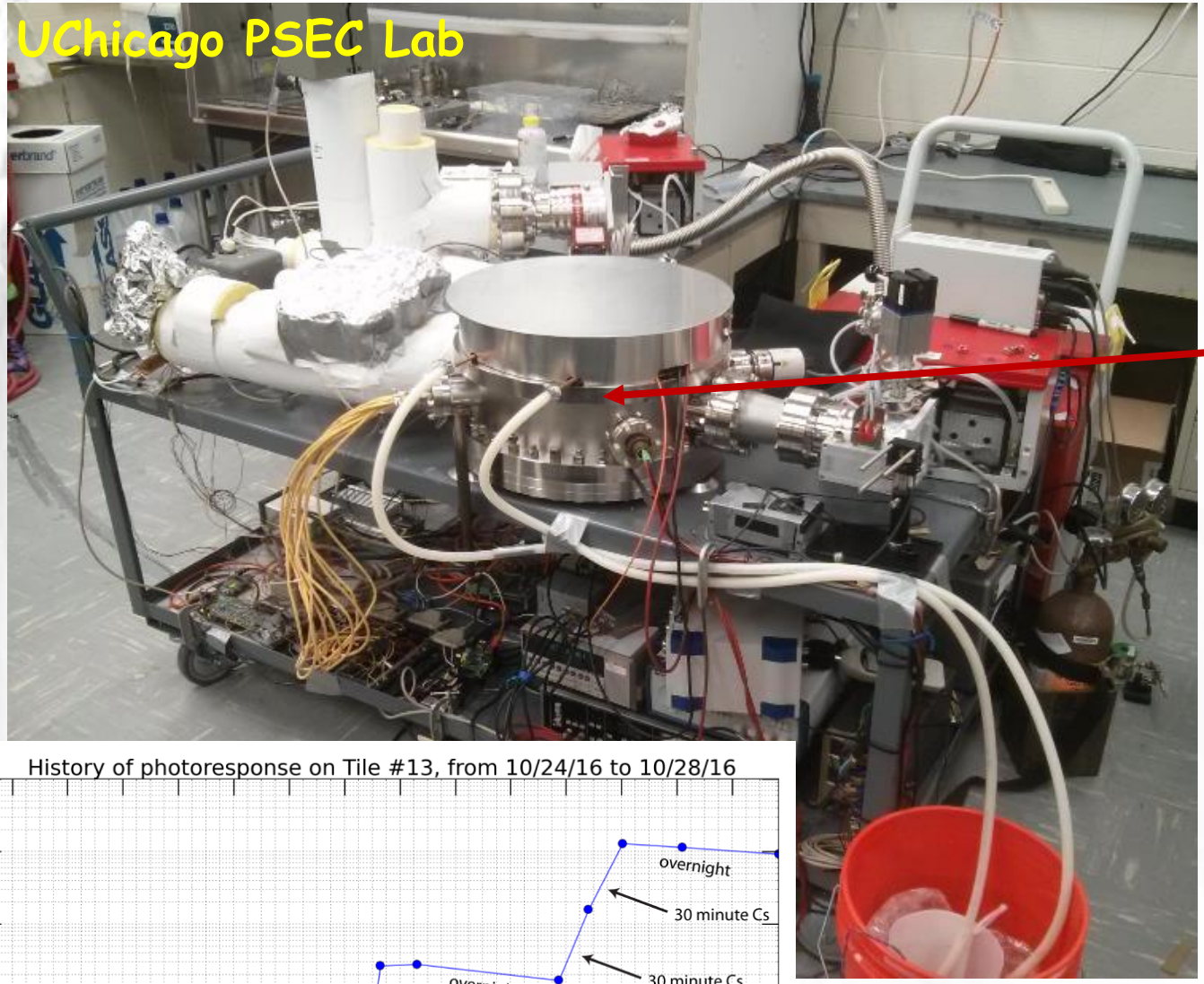


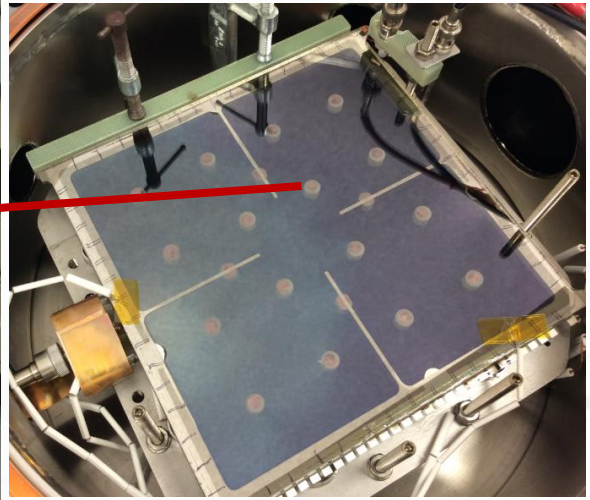
Step 1: pre-deposit Sb on the top window prior to assembly
Step 2: pre-assemble MCP stack in the tile-base
Step 3: do top seal and bake in the same heat cycle
using dual vacuum system
can vent the outer vacuum and access the detector
prior to PC synthesis
Step 4: bring alkali vapors inside the tile to make photo-cathode
Step 5: flame seal the glass tube or pinch the copper tube

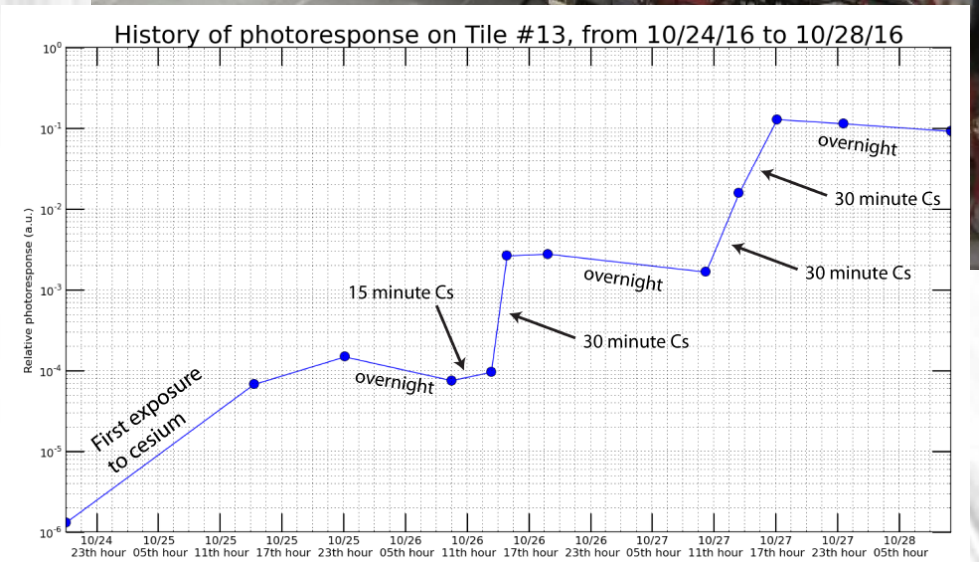
Heat Cycle


MG
3F6
6P6
9P2
8F5
300
250
200
150
100
50
°C
10/13
16:00
10/14
04:00
10/14
16:00
10/15
04:00
10/15
16:00
10/16
04:00

In-Situ LAPPD Fabrication







Heat only the tile not the vacuum vessel

Intended for parallelization

In-Situ Assembly Facility UChicago

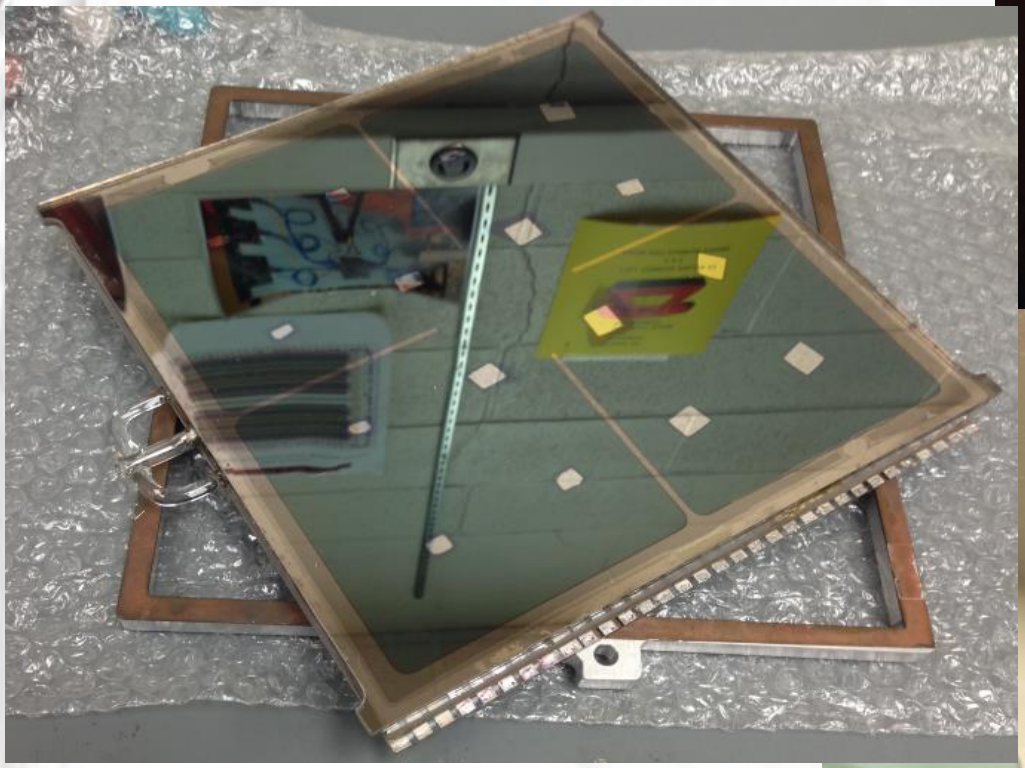
The idea is to achieve volume production by operating many small-size vacuum processing chambers at the same time
or/and make several tiles in bigger chambers

Looking forward towards transferring
the in-situ process to industry

First Sealed In-Situ Glass LAPPD

August 18, 2016

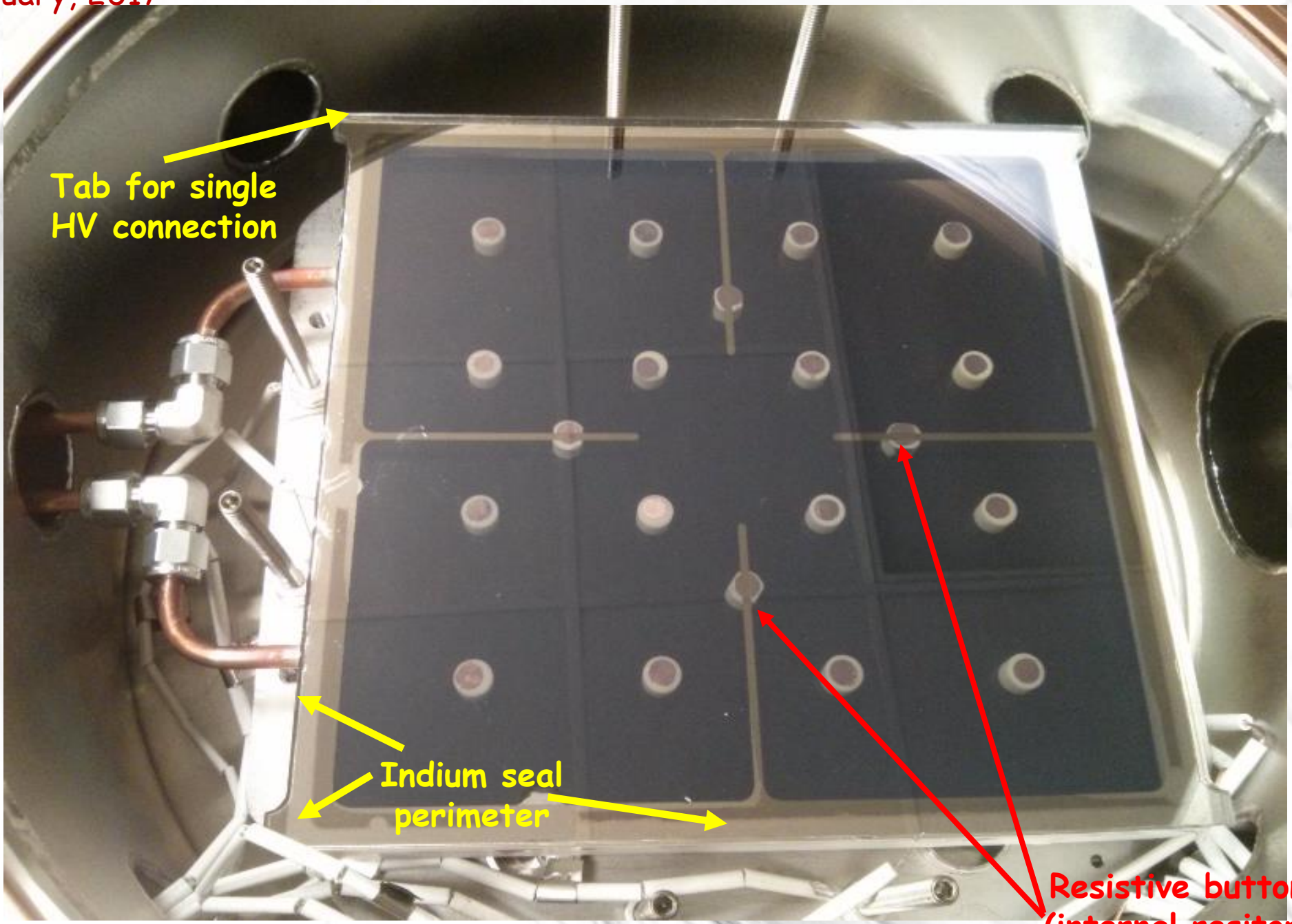
(Cs-Sb photo-cathode)



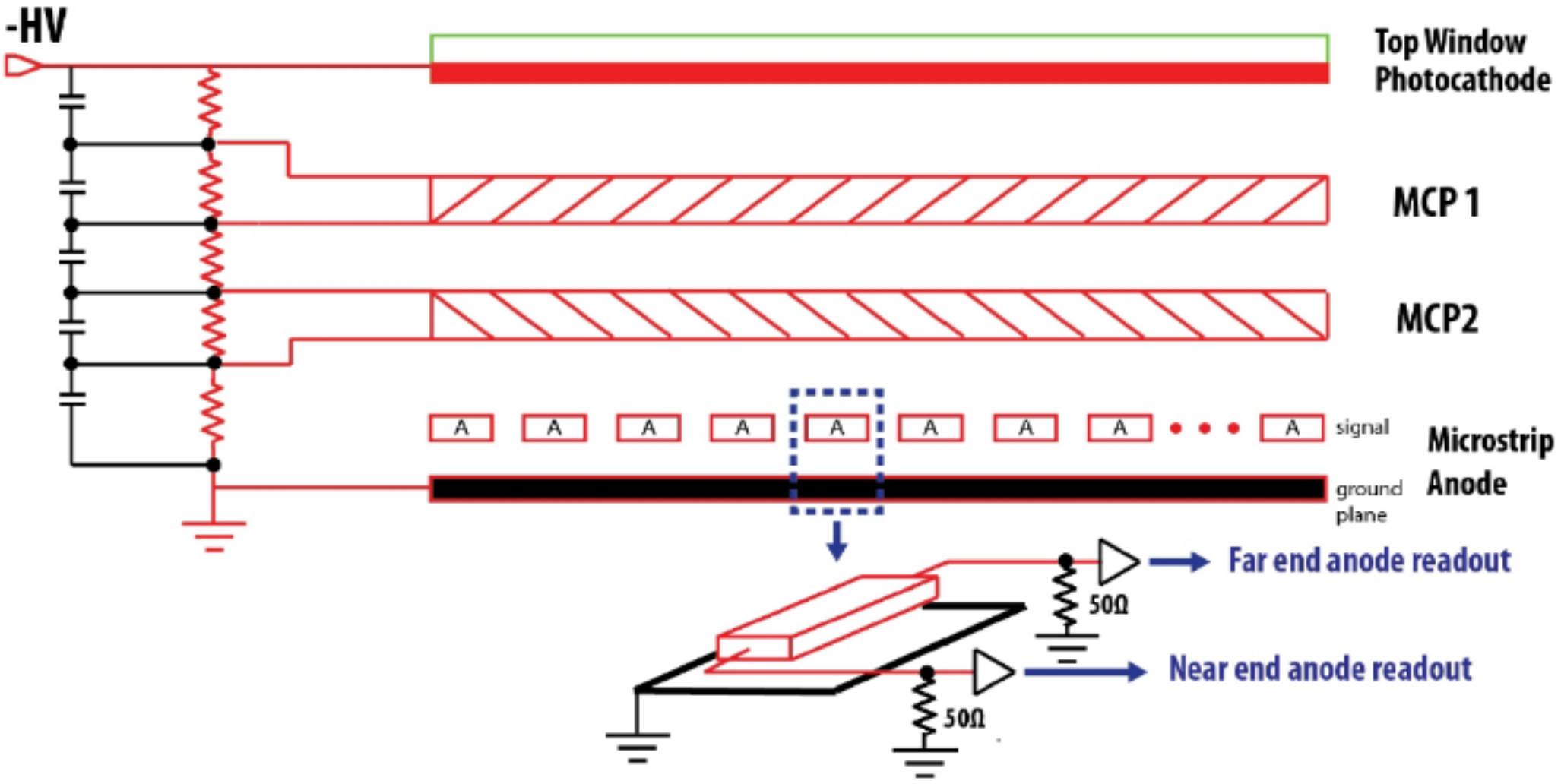
Flame seal by
J.Gregar, Argonne

Ceramic Gen-II LAPPD

January, 2017

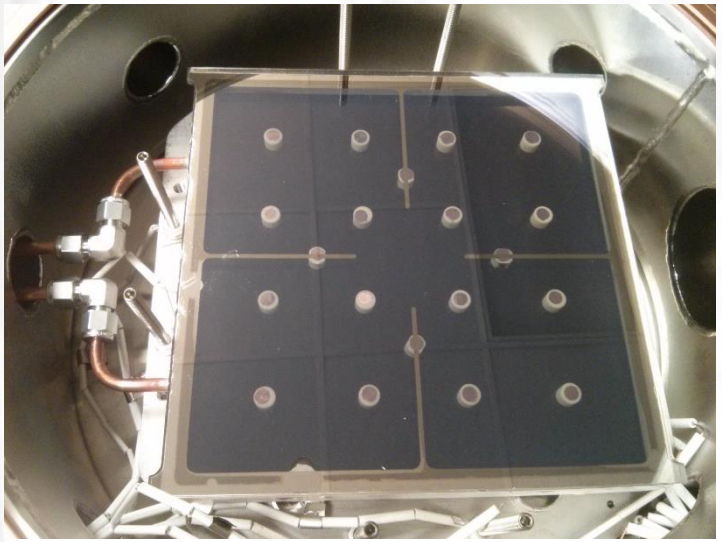


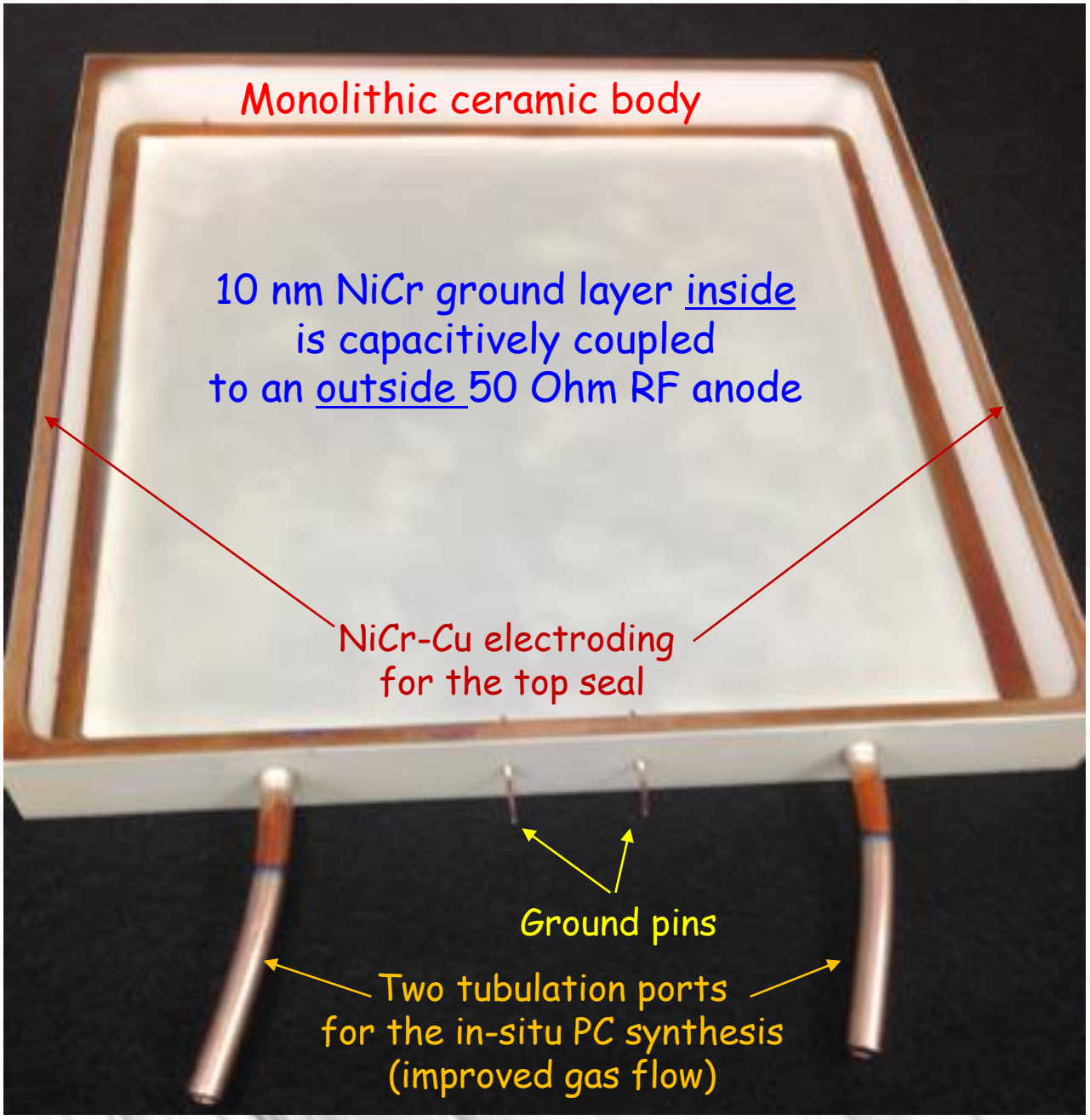
Internal HV Divider



Gen-II LAPPD

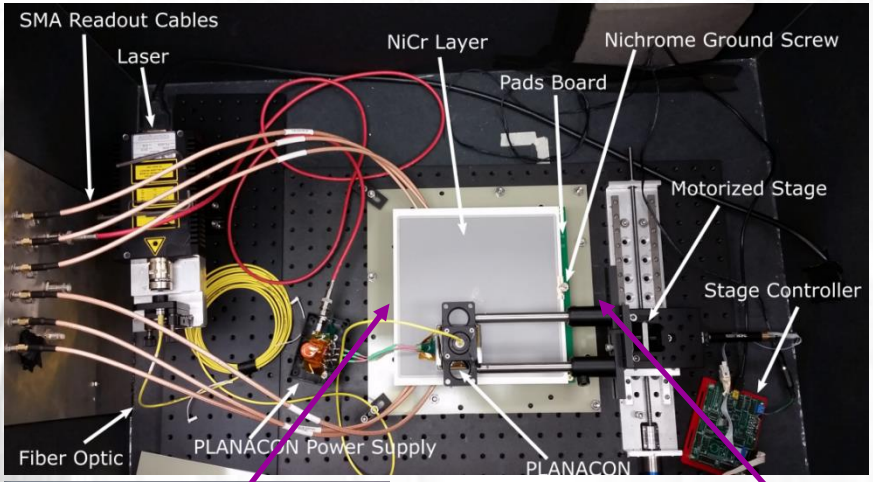
- Robust ceramic body
- Anode is not a part of the sealed detector package
- Enables fabrication of a generic tile for different applications
- Compatible with in-situ and vacuum transfer assembly processes

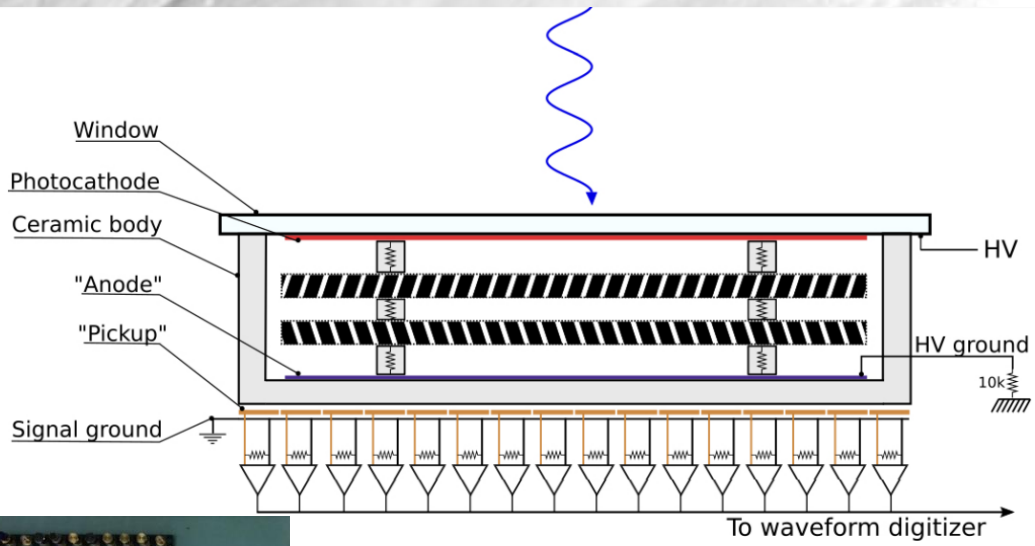


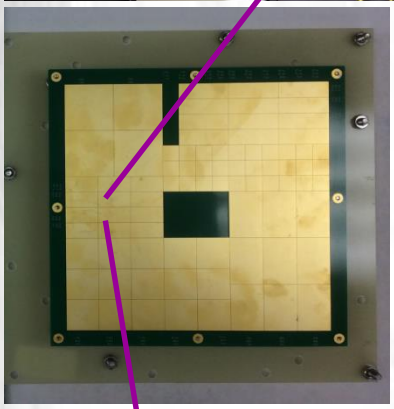


Joint effort with Incom Inc. via DOE SBIR

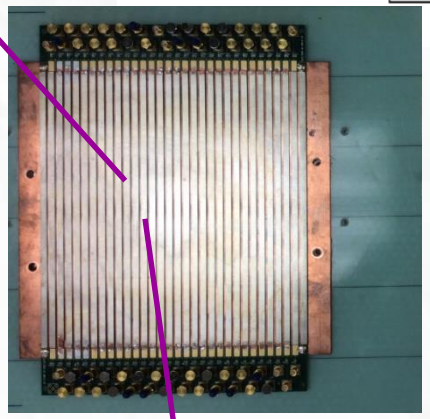
Gen-II LAPPD: "inside-out" anode



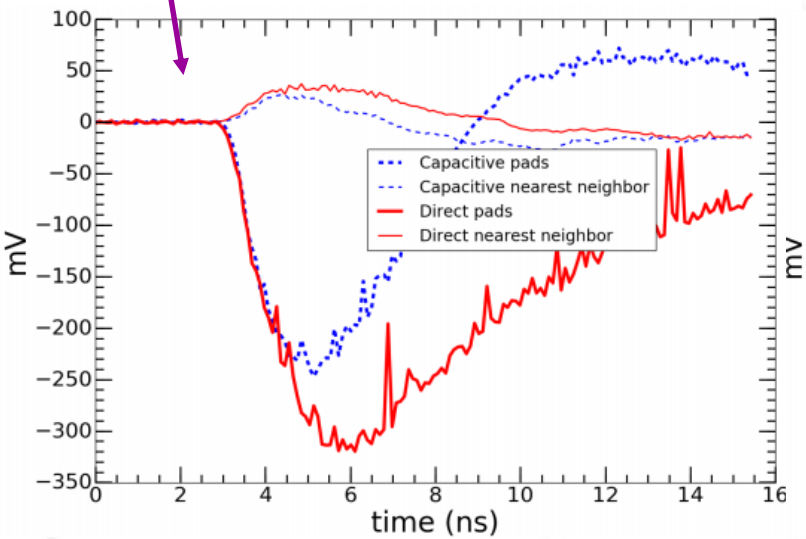


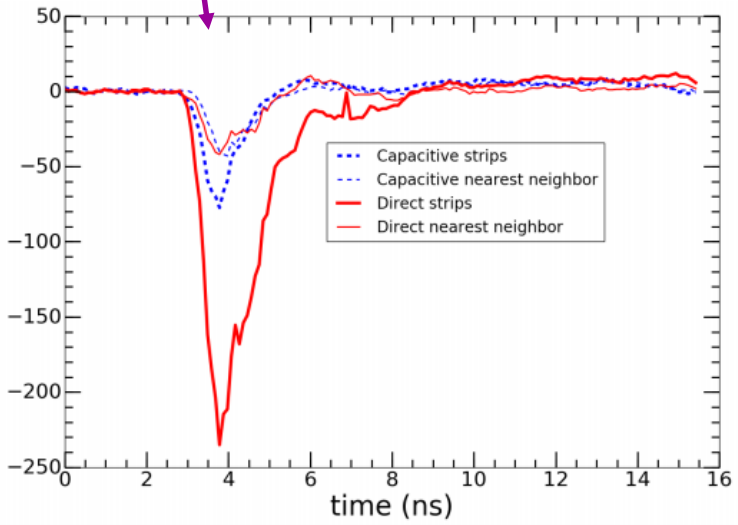


Chose your own readout pattern



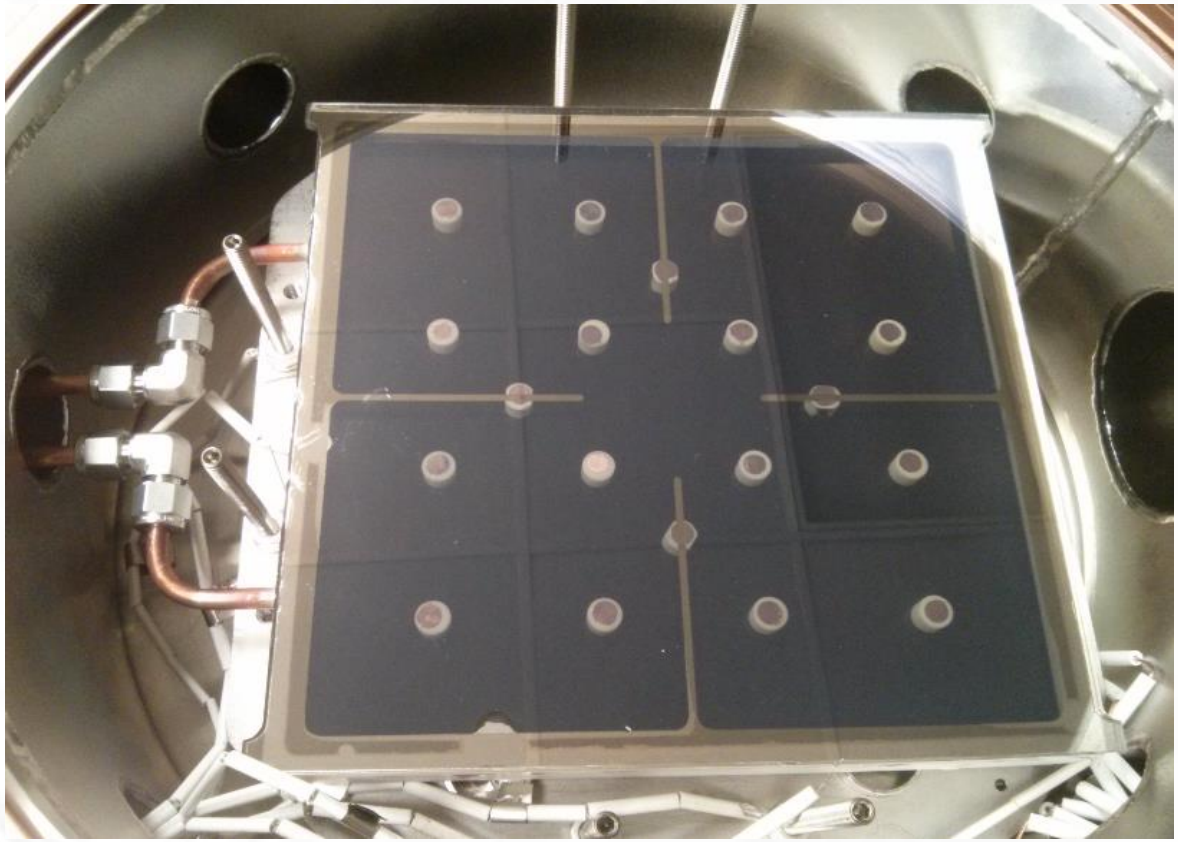
- Custom anode is outside
- Capacitively coupled
- Compatible with high rate applications





For details see NIMA 846 (2016) 75

In-Situ LAPPD: work in progress



LAPPD batch production milestones:

- Developed a robust metallurgy scheme for hermetic packaging
- Demonstrated Cs transport from a source outside of the detector package to the entire 20x20 cm^2 window surface in the presence of full size MCPs (we did made Cs-Sb photo-cathode)
- Showed that MCP initial resistance can be recovered after Cs-ation (MCPs are NOT permanently damaged or changed)

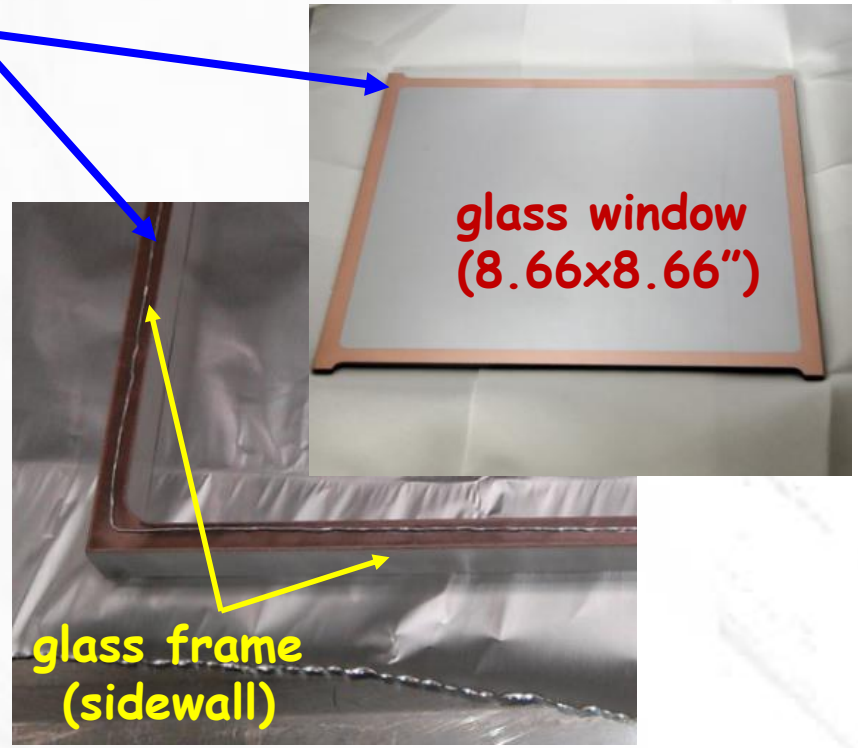
Indium Solder Flat Seal Recipe

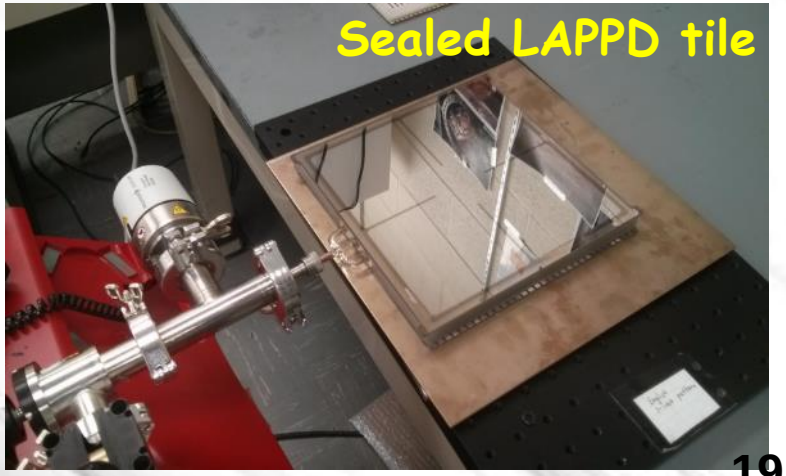
Input:

- Two glass parts with flat contact surfaces (also trying to seal ceramic + fused silica)

Process:

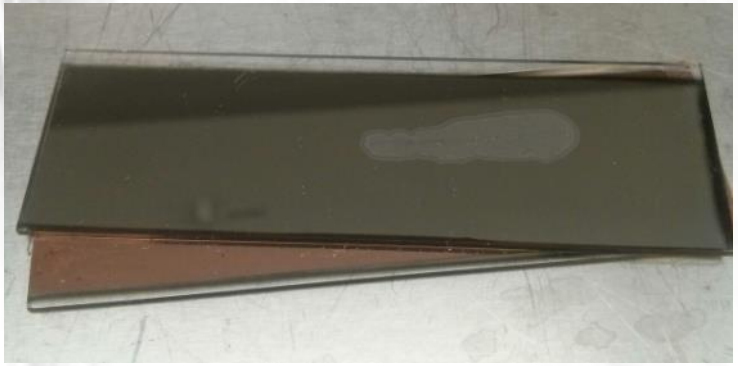
- Coat 200 nm of NiCr and 200 nm of Cu on each contact surface (no vacuum break in between NiCr and Cu depositions)
- Make a sandwich with 99.995% pure indium wire (etch the In wire 5% HCl just before assembly)
- Bake in vacuum at 250-300C for 24hrs (go significantly above melting – known as "superheat" in soldering industry)
- A good compression over the entire perimeter is needed to compensate for non-flatness and to ensure a good contact (no seal without a press on the edges!)





Metallization pattern is based on SSL seal by O. Siegmund et. al.

Understanding the Seal Recipe



Here is what we know about the seal:

(XPS with depth profile was used to characterize the seal)

- NiCr layer will provide tie layer
- Cu provides protection against oxide on NiCr
- Indium wire gets squished--oxide broken

(this principle is also used in cold seal by D. Walters at ANL)

- Cu diffuses into bulk Indium
- Ni and Cr diffuse into bulk Indium
- Indium bonds to the glass (presumably through a very thin layer of Cr – this is on the edge of sensitivity)

Many thanks to R. Jarrett at Indium Corp. for expert advice on indium metallurgy

Challenges for In-Situ Process

List of problems discovered so far:

- MCP plates go to lower resistance (recoverable in air)
- We had exposed Cu on the window- Indium wets it. Cs interacts with Indium to forms a flakes/powder inside the entire volume.
- Resistive buttons interact with Cs (new buttons last week)
- Measuring QE is made more difficult by our internal HV divider (can't get current across the PC-MCP gap directly).

Cs-In-(X?) Flakes/Powder Story

Ongoing investigation

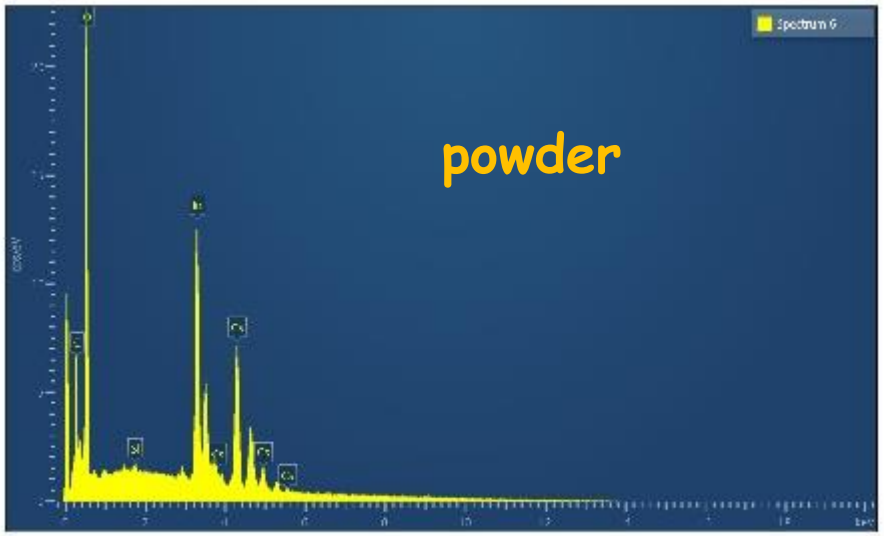


Figure 4: A spectrum from a **dust** fleck shown in the SEM picture above. The peaks indicate the existence of indium and Cs, and not their quantitative relative composition.

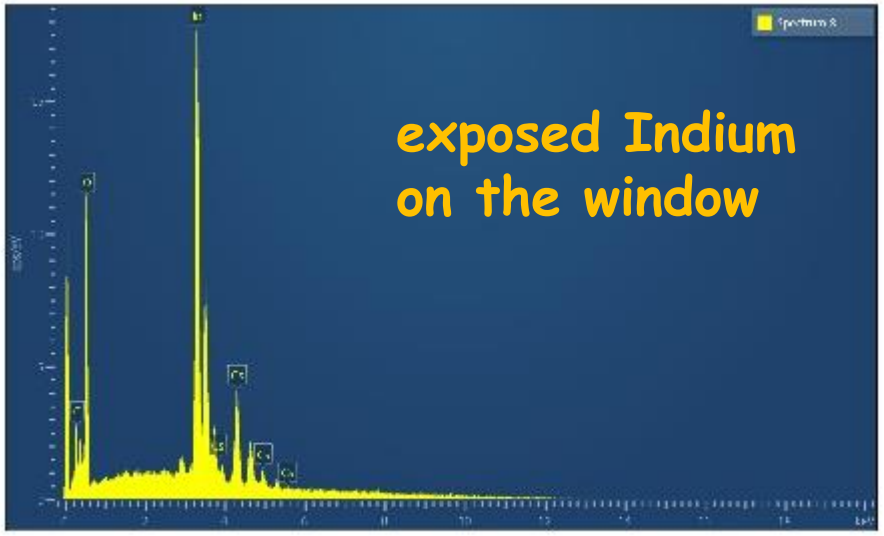
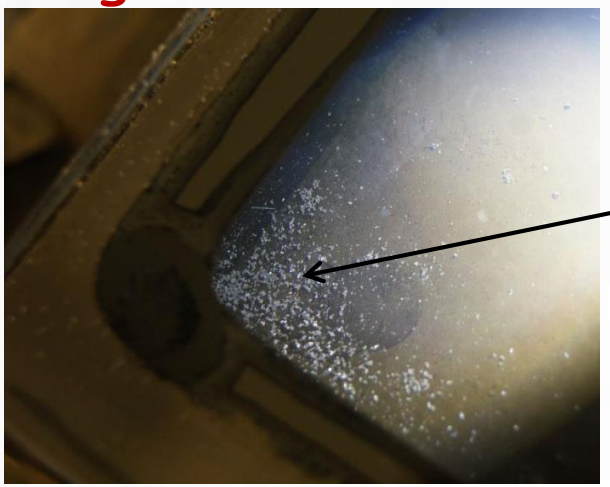


Figure 5: This spectrum is taken from the layer on the **window** that had turned black and flaky. The spectrum looks almost identical to that of the dust flecks.



Sealing surface
on top of sidewall

Powder after
exposure to air

In a few weeks we are getting new windows with improved metallization – avoid/limit In "seen" by Cs

Sb Story

We start with 10nm of Sb on the window –
this layer could be sitting in air for months before assembly

John Smedley and Klaus Attenkofer don't like this!
Sb oxidation is the main concern

Things to consider:

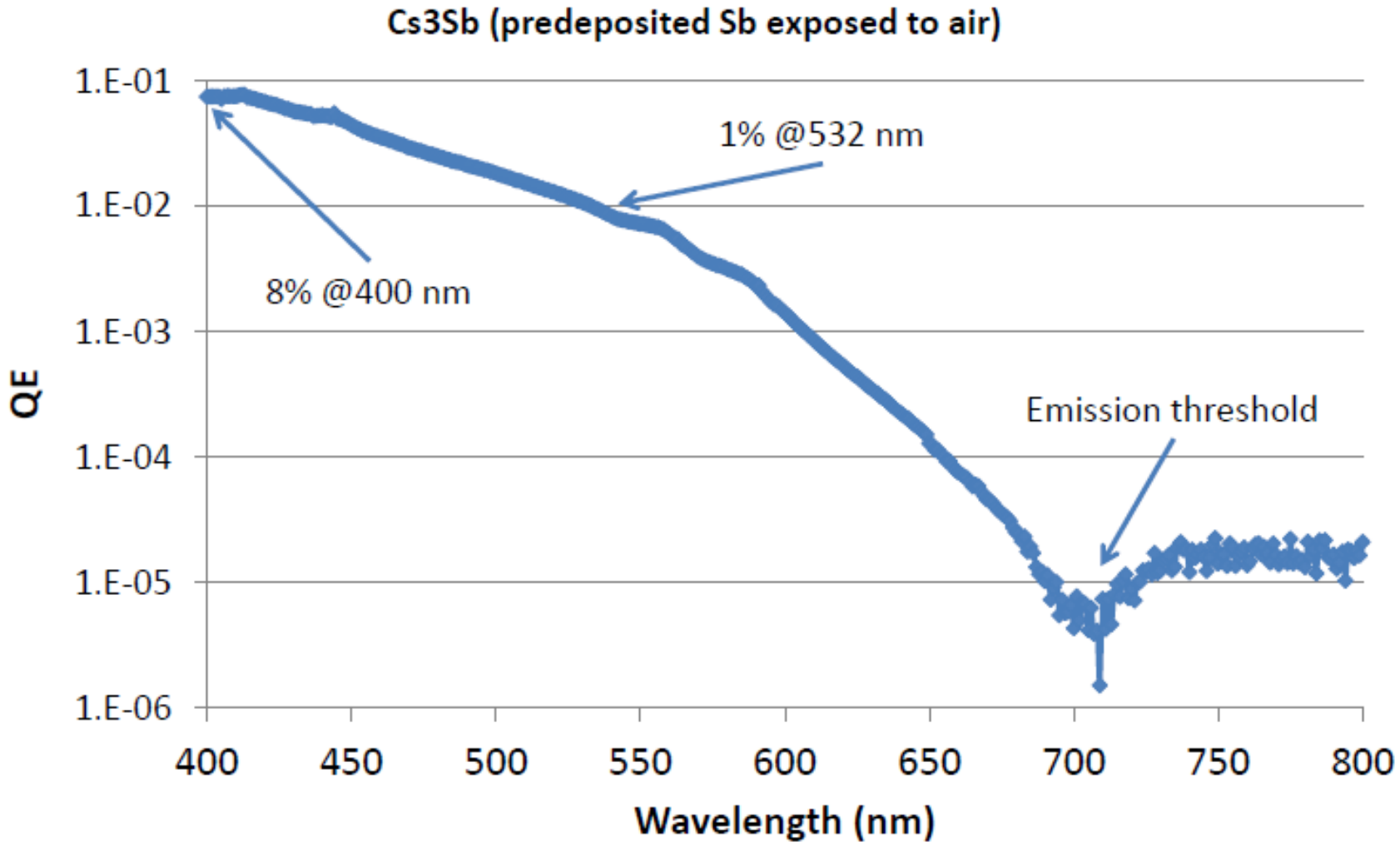
- We bake the whole detector including window at 300C for 16hrs and we do see reduction in the original Sb layer thickness (are we getting rid of oxide by long heating?)

- Eventually we have to characterize the Sb layer after the bake (may have to adjust original thickness or heat cycle)

- We have done XPS studies of the Sb layer as received from vendor (air exposed for 3 months)

Can we make PC after Sb was exposed to air?

Luca Cultrera at Cornell



Sb XPS Studies

Sb test coupon:
fused silica microscope slied with
200nm of NiCr + 200nm of Cu + 10nm of Sb

UChicago XPS details

(XPS expert support by Alexander Filatov at UChicago)

X-ray gun:

- 10 mA at 15 kV
- high resolution mode step size 0.1 eV
- area of the analyzed spot 300x700 mum

Ar ion beam (for depth profiling):

- beam size 6x6 mm
- beam energy 2 kV
- beam density 7.78 A/cm2

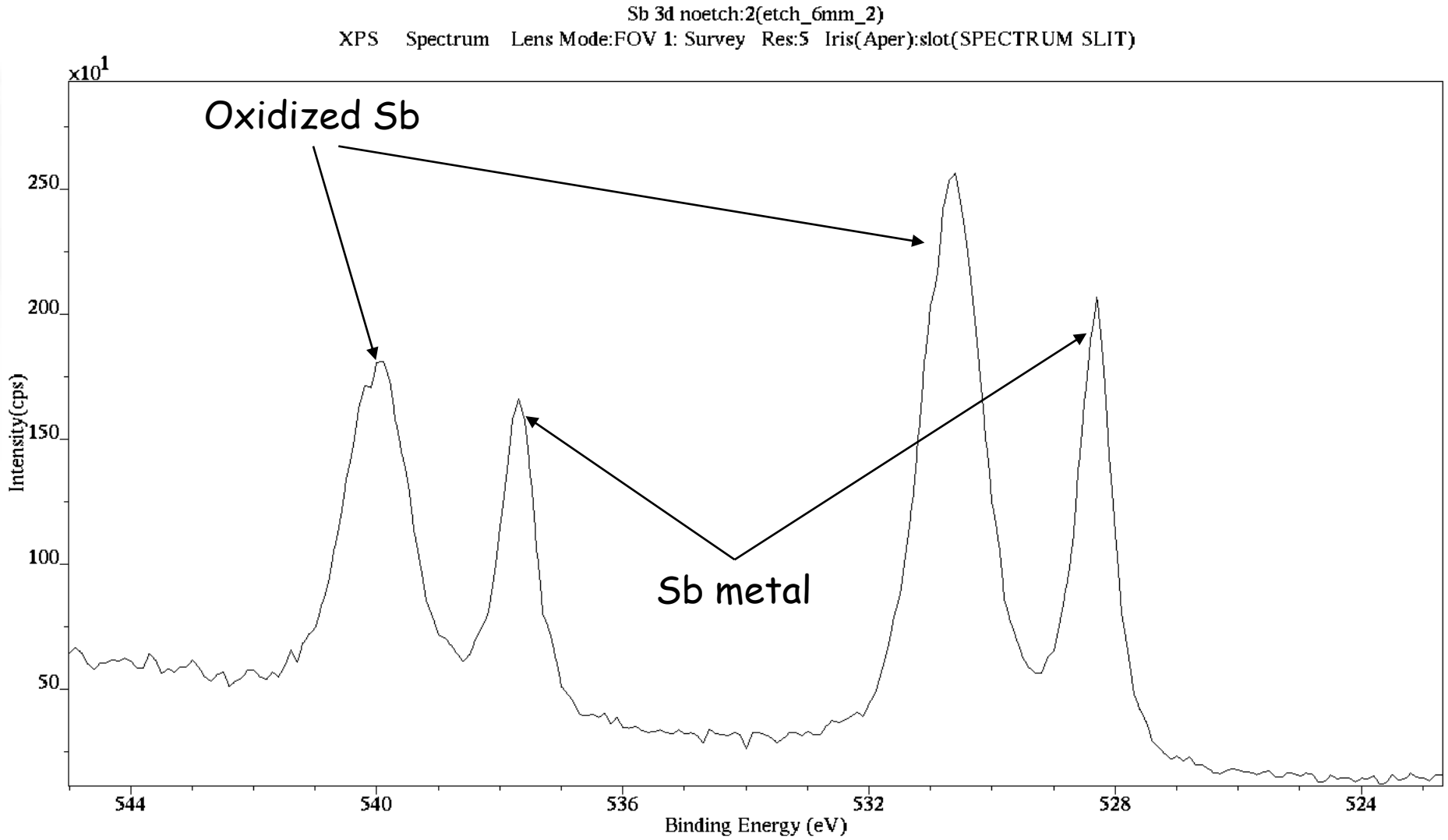
Side note on thin film coatings

- Good quality films are expert's territory
- Sb deposition in particular:
  - H.L. Clausing Inc.,
  - Bing Shi at the Argonne Thin Film Deposition Lab
- NiCr-Cu isn't easy, but we have one more commercial vendor for that

Depth profiling was performed using 5 sec etches by the Ar ion beam.
We estimated that a 5 sec etch removes on average 0.25 nm
of the surface material.

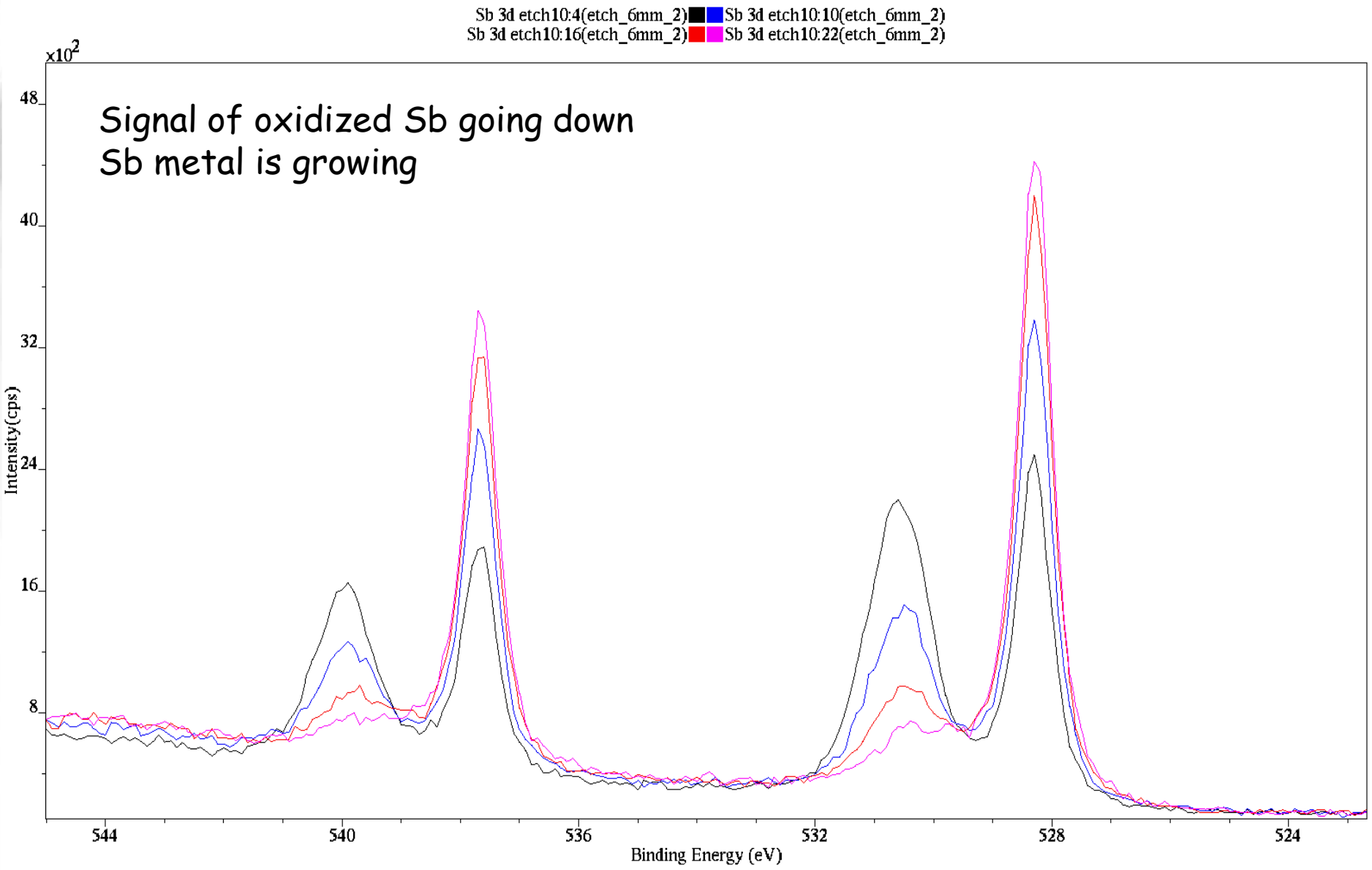
Sb XPS Studies

XPS scan before any ion etching



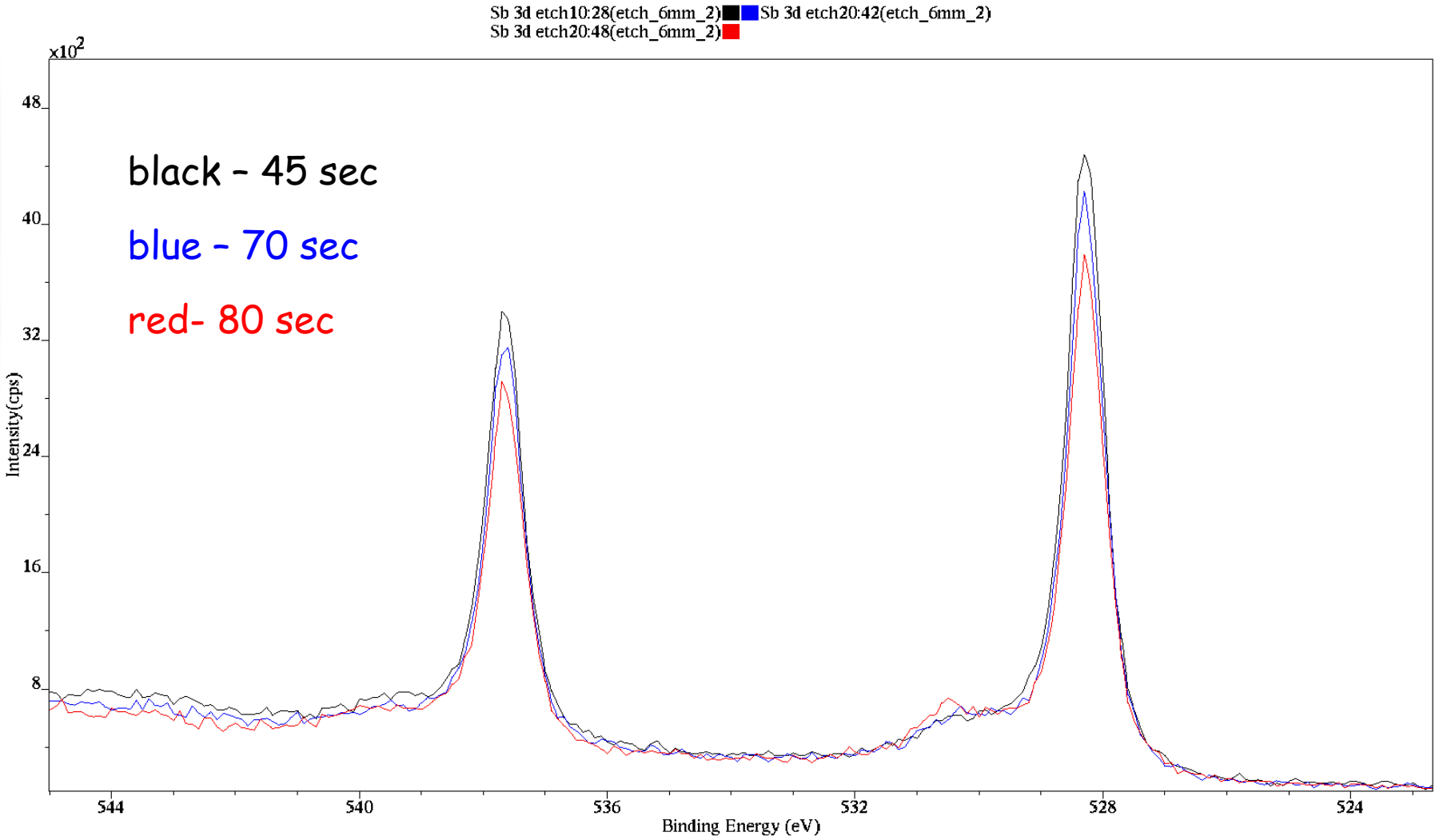
Sb XPS Studies

Intermediate scans within first 35 seconds of etching



Sb XPS Studies

After 40 seconds we see pure Sb metal (preferential sputtering of oxygen is not completely excluded, but it would have to be very strong)



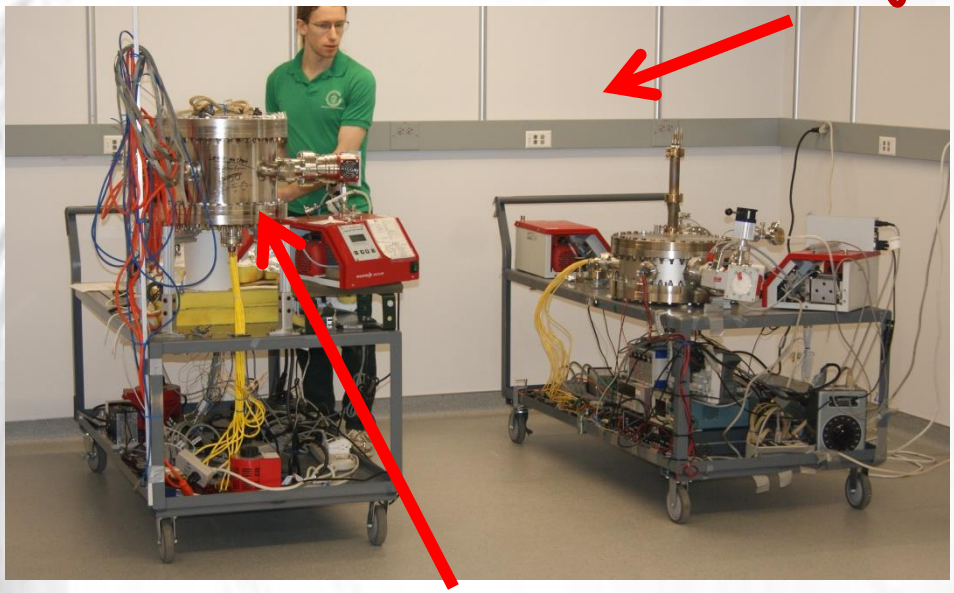
No Sb metal is seen after 200s

Assuming initial 10nm Sb thickness the average etch rate is 0.5A/sec

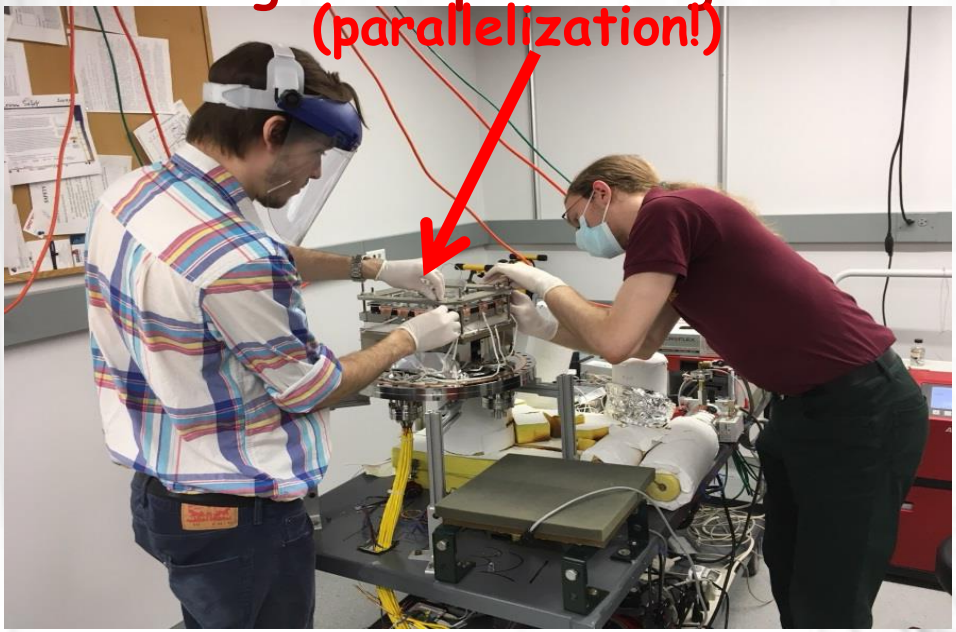
Therefore Sb-oxide thickness is ~40sec x 0.5A/sec = 2nm

What's Next?

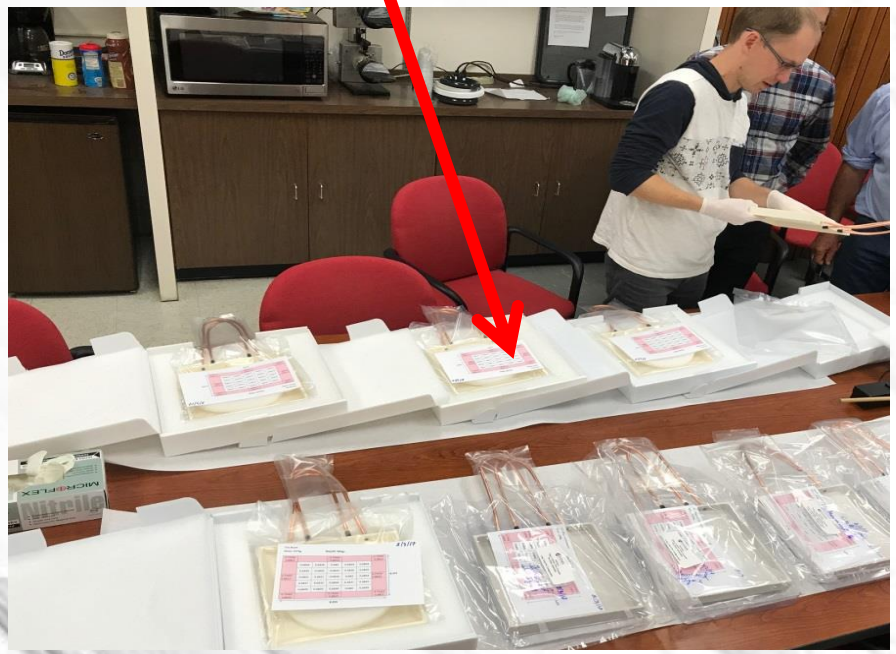
We've just got a new lab



We've got 2nd processing chamber (parallelization!)



We are getting lots of components



Conclusion

- We are exploring if an In-Situ, PMT-like, process can be used to manufacture LAPPDs without vacuum transfer of the window
- We consider this as a high risk R&D where success is not guaranteed but the pay-of is attractive enough to try
- So far we don't see obvious show-stoppers
- Lots of technical problems. So we value expert's advice and help

Questions to this expert audience:

1) What other measurements should we do to characterize pre-deposited Sb film?

2) Sb evaporates during seal and bake. What do you think is the optimal thickness at the start of Cs-ation to get good Cs3Sb photo-cathode?
2a) What is the best temperature to form Cs3Sb photo-cathode?
2b) What is the highest temperature Cs3Sb can withstand after it's formed?

3) What are pre-requisites to try to form bi-alkali PC by adding K?

4) What role does oxygen play in boosting QE of alkali photo-cathodes? Air exposure seems to recover MCPs resistance? How much dry air can we introduce into the system after Cs-ation without killing the photo-cathode?

5) Any experience in dealing with Cs-In powder? We will limit In seen by Cs, but what else can we do? What's the best way to distinguish between Cs-In and Cs-In-X?

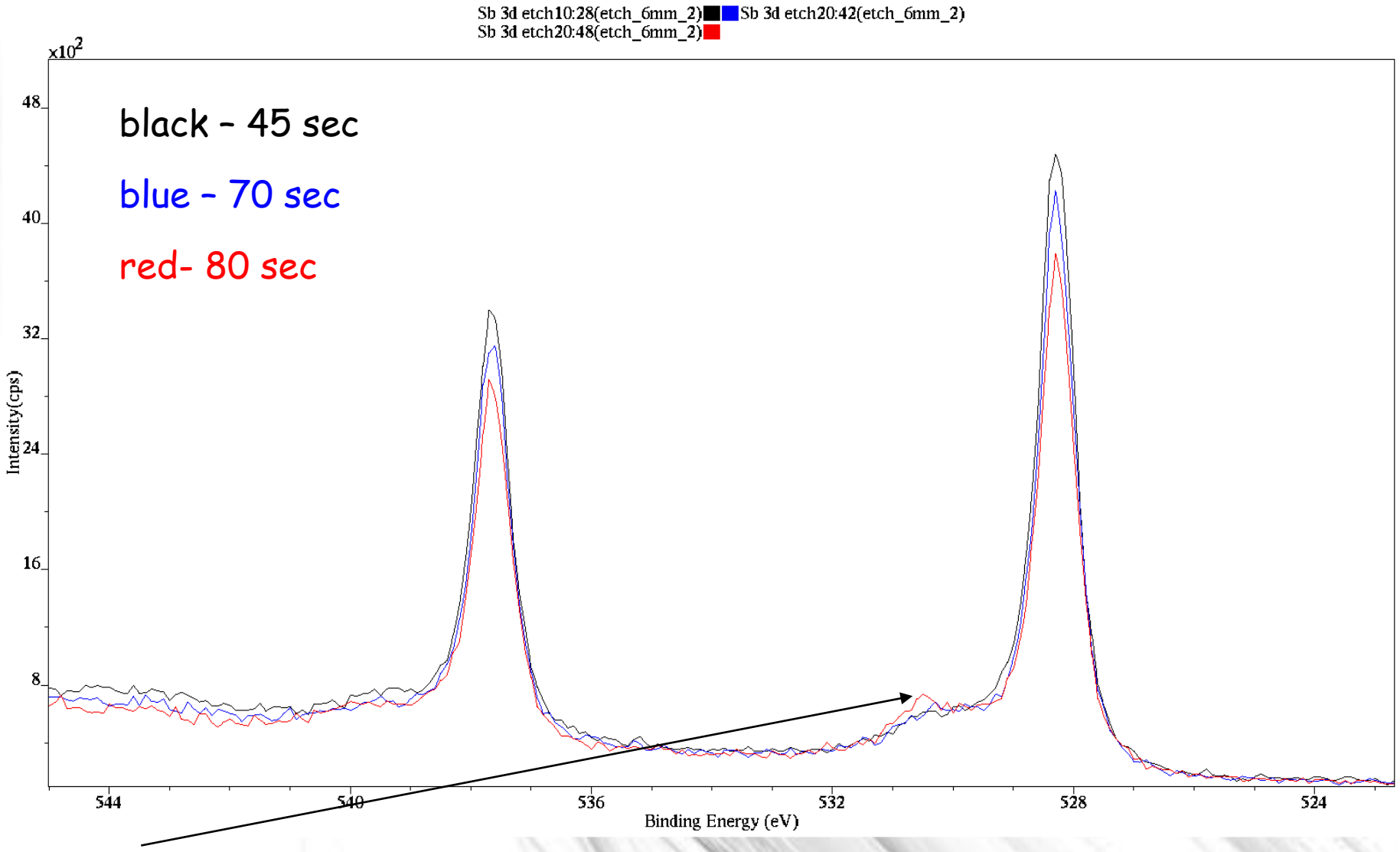
Acknowledgements

This work supported by U. S. Department of Energy, Office of Science, Office of Basic Energy Sciences and Offices of High Energy Physics and Nuclear Physics under contracts DE-SC0008172 and DE-SC0015367; the National Science Foundation under grant PHY-1066014; and the Physical Sciences Division of the University of Chicago.

Back-up

Sb XPS Studies

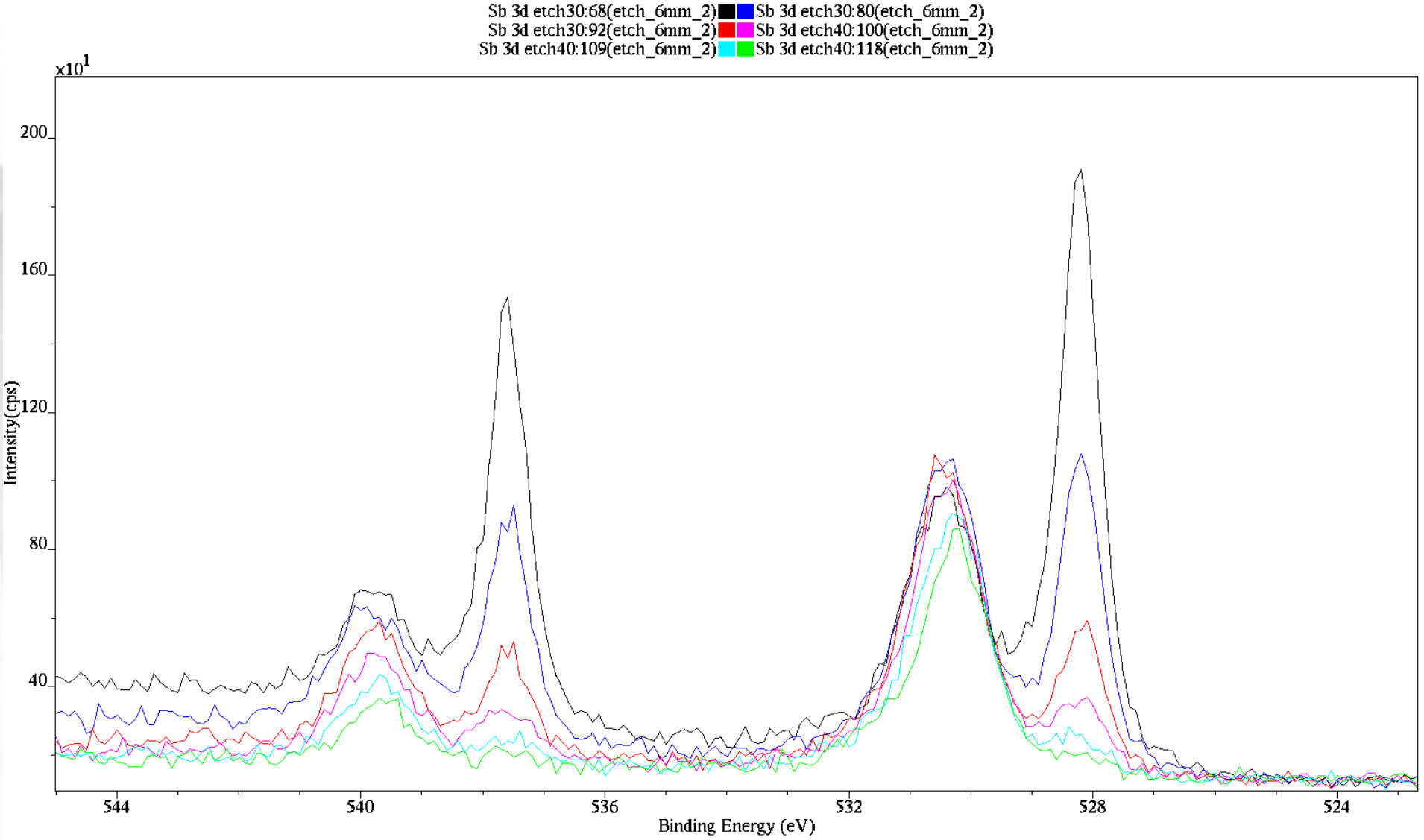
Between 45 seconds and 80 seconds we see pure Sb metal (preferential sputtering of oxygen is not completely excluded, but it has to be very strong)



Peak at 530.4 eV belongs to Auger signals of a Cu metal underlayer

Sb XPS Studies

Continue ion etch: Sb metal goes down, Auger Cu goes up

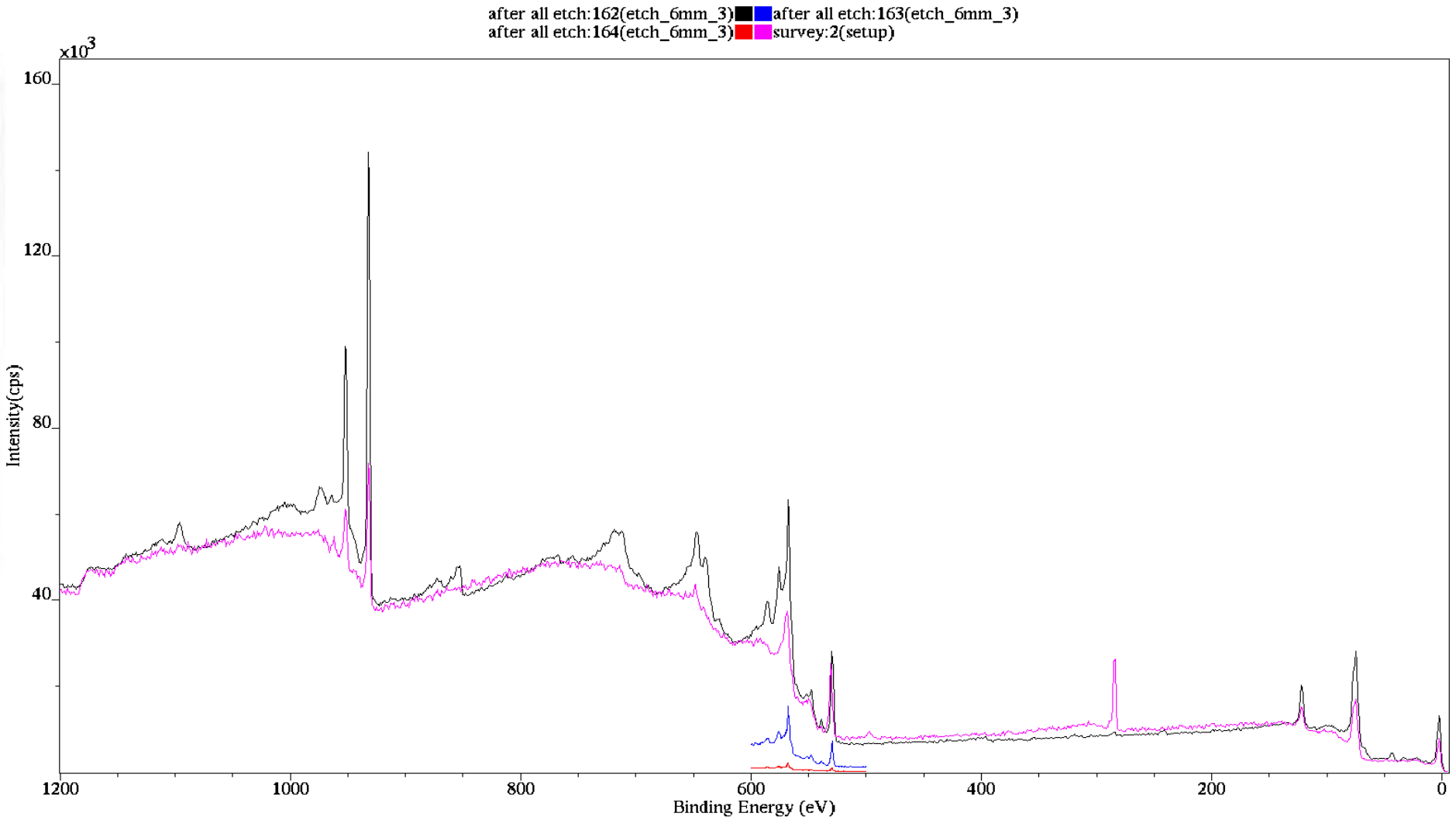


No Sb metal is seen after 200s

Assuming initial 10nm Sb thickness the average etch rate is 0.5A/sec

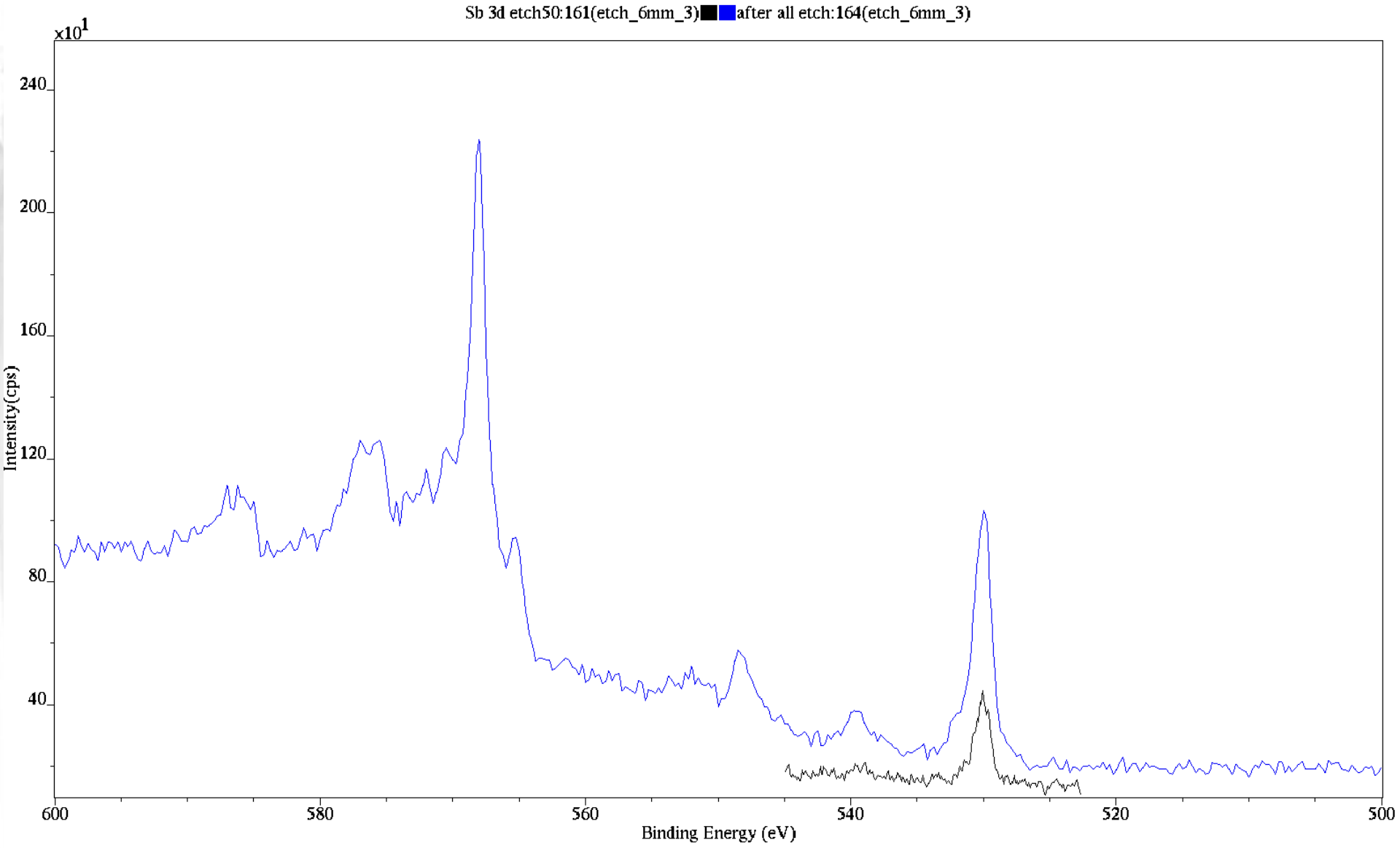
Sb XPS Studies

Assigning the ~530eV and 540eV peaks to Auger Cu



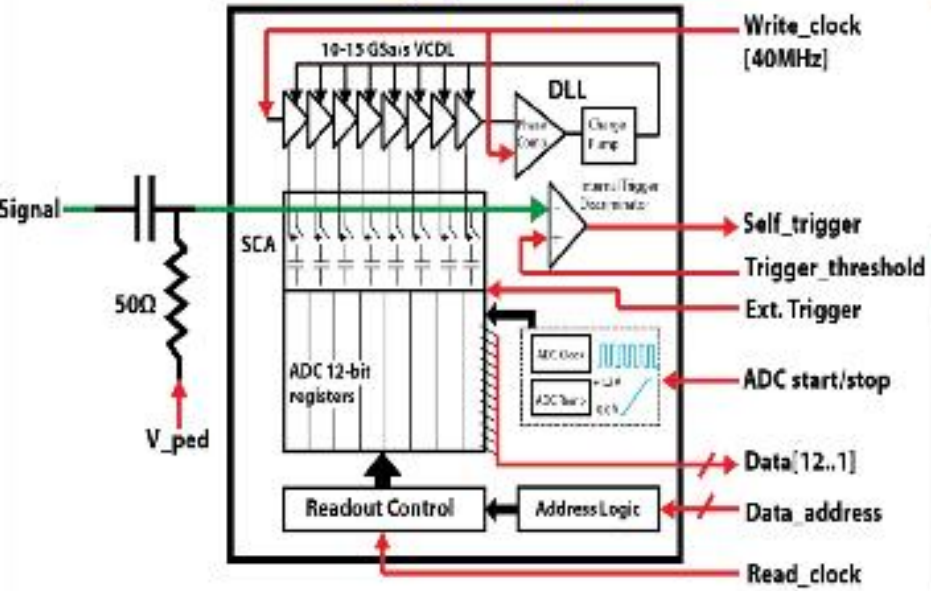
Sb XPS Studies

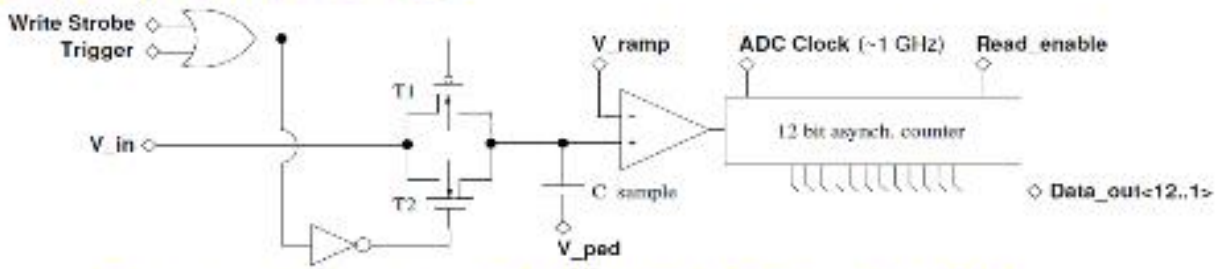
Assigning the ~530eV and 540eV peaks to Auger Cu



PSEC4 ASIC

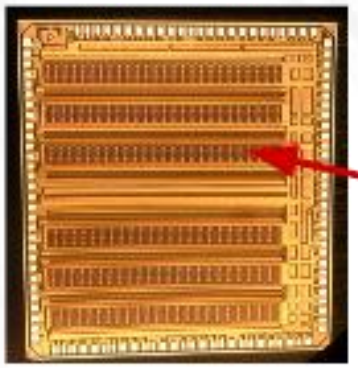
NIMA 735, (2014) 452-461





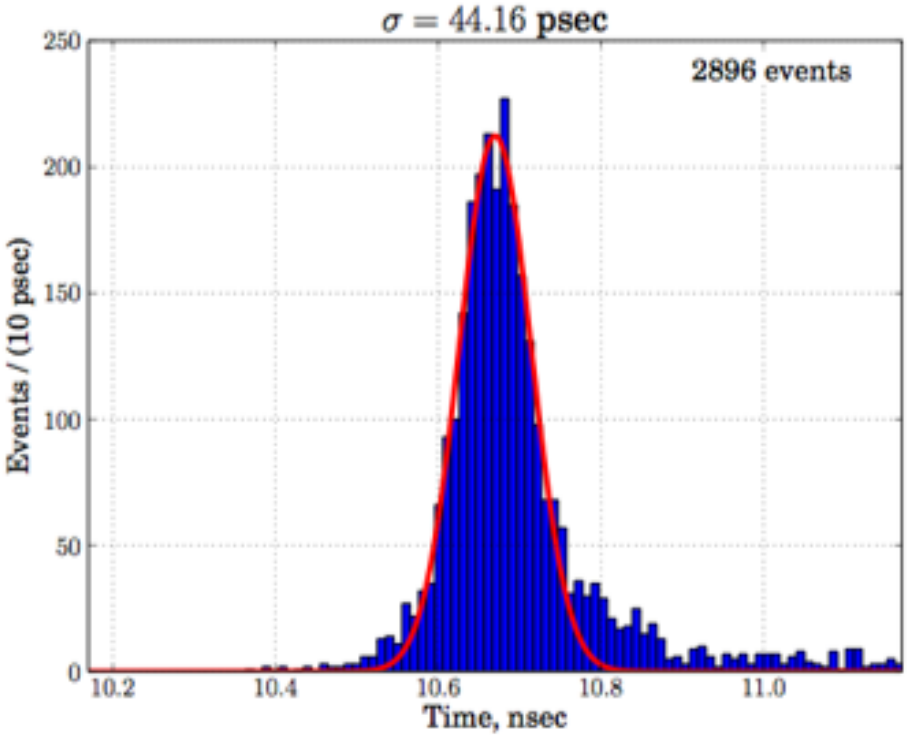
- Fabricated using IBM-8RF 130nm CMOS process
- Each of 6 channels is a switch capacitor array
  - 256 samples deep
  - on-chip ADC
  - sampled of 10's MHz clock using VCDL
- 10Gs/s, 1.5GHz
- Controlled by FPGA

PSEC4 die

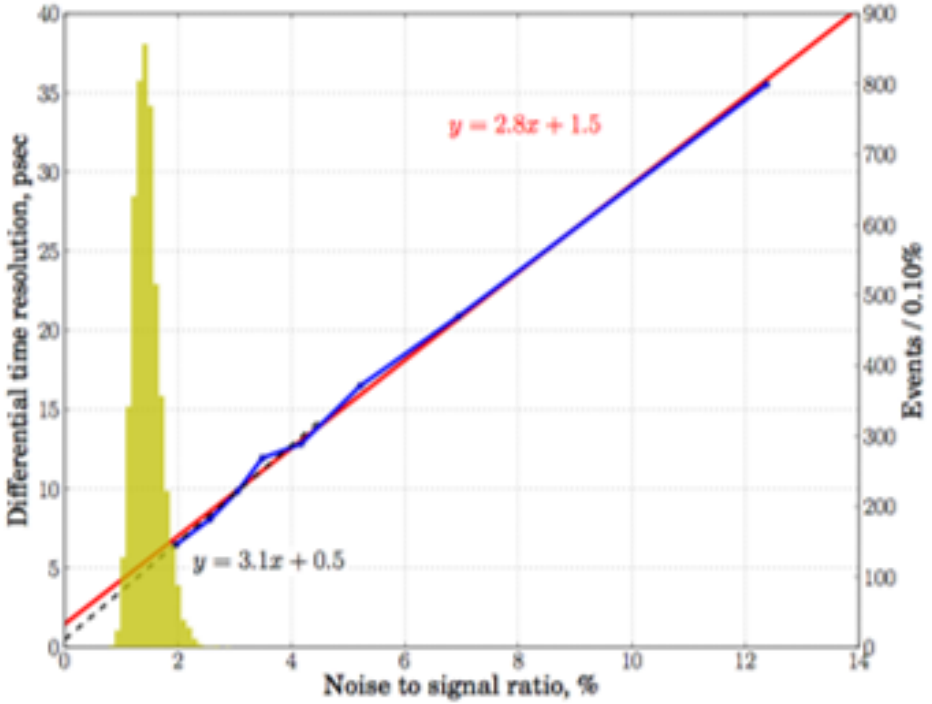


Evaluation board

Present (now old) Time Resolution



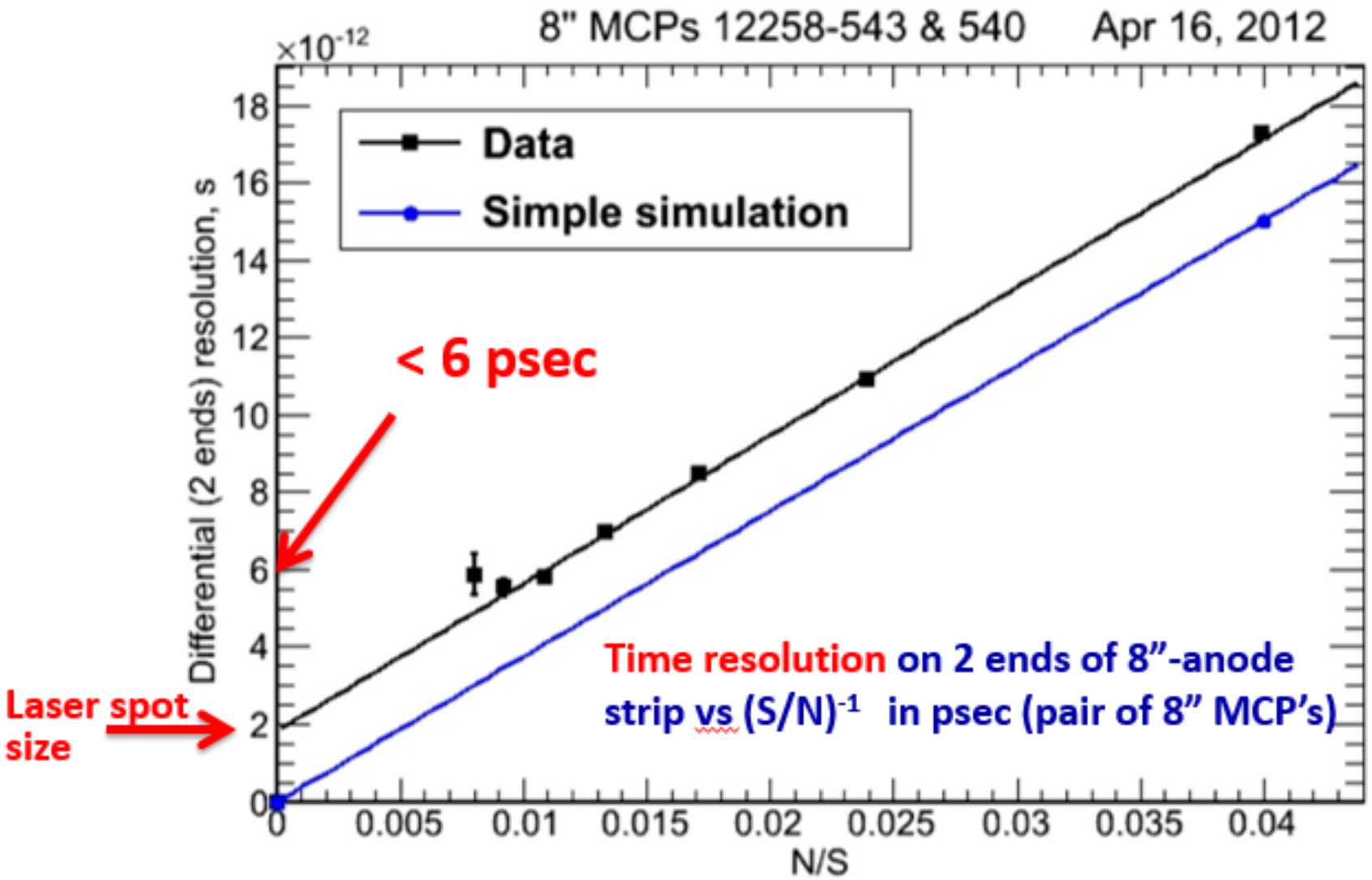
Single Photo-electron
PSEC4 Waveform sampling
Sigma=44 psec



Differential Time Resolution
Large signal Limit
Oscilloscope Readout
Black line is y=3.1x+0.5 (ps)
Red line is y=2.8x +1.5 (ps)
Where the constant term represents the large S/N limit (0.5-1.5 ps)

Highly non-optimized system (!)- could do much better

Timing res. agrees with MC



N = RMS of the noise; S = signal amplitude

M. Wetstein, B. Adams, A. Elagin, R. Obaid, A. Vostrikov, …

PSEC4

A B S T R A C T

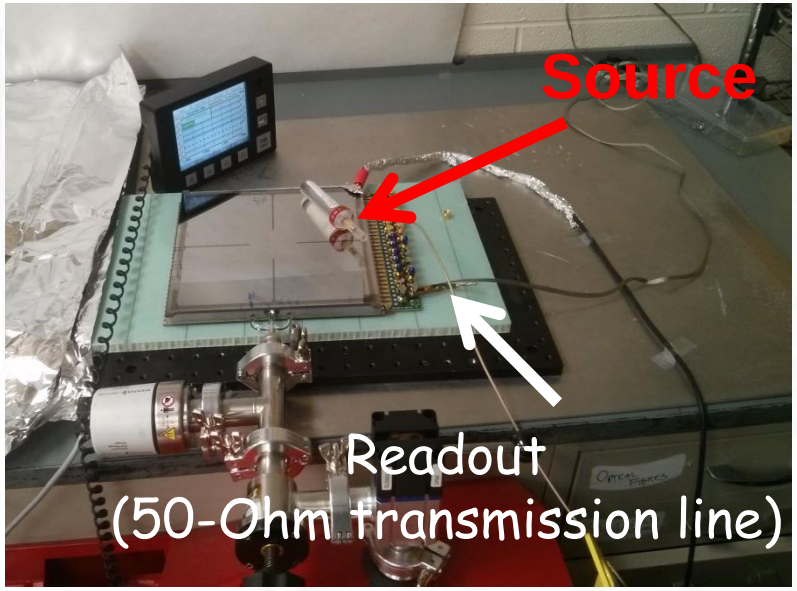
The PSEC4 custom integrated circuit was designed for the recording of fast waveforms for use in large-area time-of-flight detector systems. The ASIC has been fabricated using the IBM-8RF 0.13 μm CMOS process. On each of the six analog channels, PSEC4 employs a switched capacitor array (SCA) of 256 samples deep, a ramp-compare ADC with 10.5 bits of DC dynamic range, and a serial data readout with the capability of region-of-interest windowing to reduce dead time. The sampling rate can be adjusted between 4 and 15 Gigasamples/second (GSa/s) on all channels and is servo-controlled on-chip with a low-jitter delay-locked loop (DLL). The input signals are passively coupled on-chip with a −3 dB analog bandwidth of 1.5 GHz. The power consumption in quiescent sampling mode is less than 50 mW/chip; at a sustained trigger and a readout rate of 50 kHz the chip draws 100 mW. After fixed-pattern pedestal subtraction, the uncorrected integral non-linearity is 0.15% over a 750 mV dynamic range. With a linearity correction, a full 1 V signal voltage range is available. The sampling timebase has a fixed-pattern non-linearity with an RMS of 13%, which can be corrected for precision waveform feature extraction and timing.

First Signals from an In-Situ LAPPD

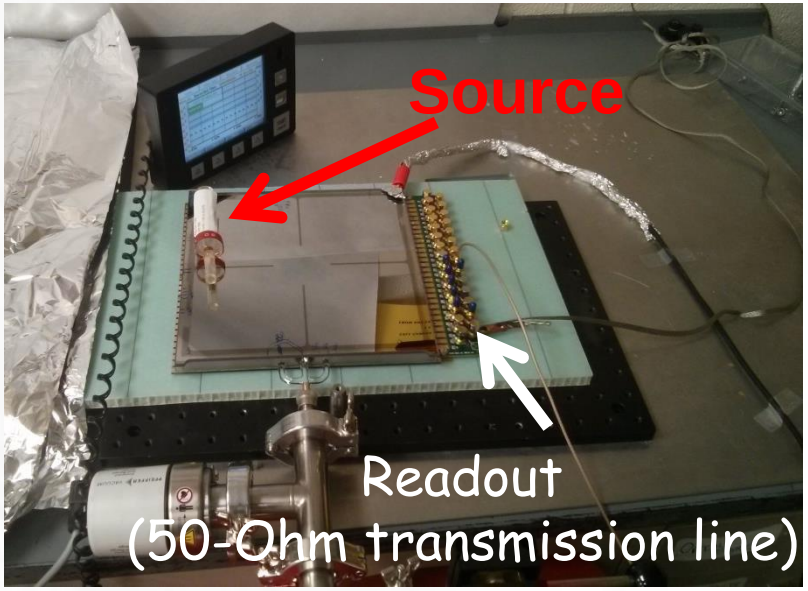
April, 2016

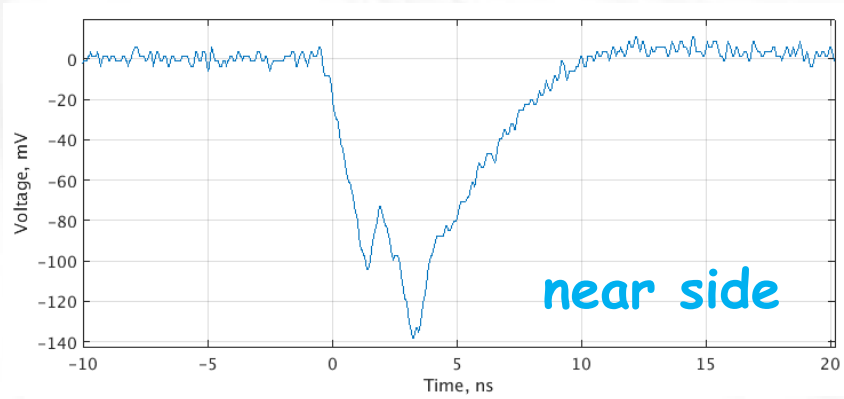
(Sb cathode)

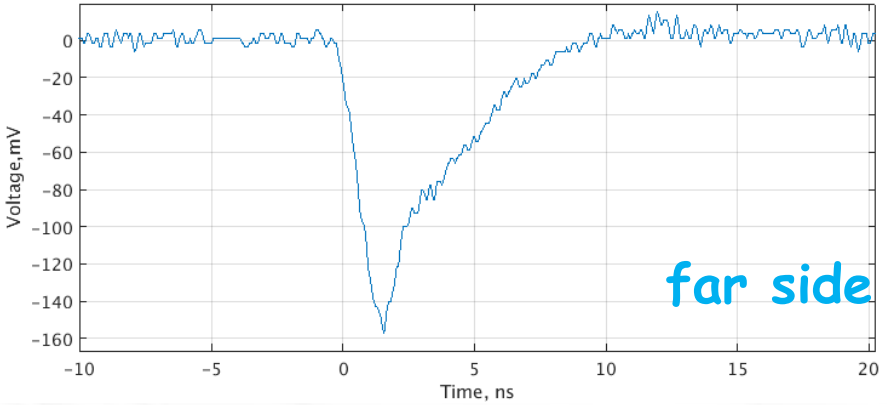
Near side: reflection from unterminated far end



Far side: reflection is superimposed on prompt







The tile is accessible for QC before photo-cathode shot
This is helpful for the production yield

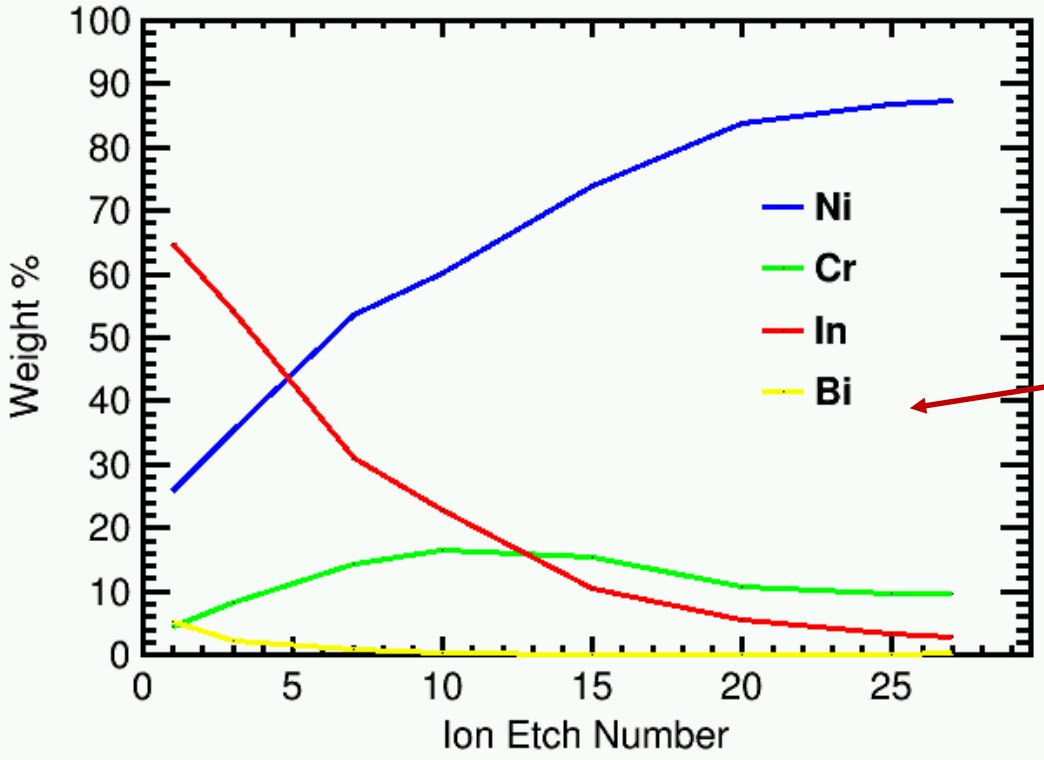
Metallurgy of the Seal

Moderate temperatures and short exposure time:

- A thin layer of copper quickly dissolves in molten indium
  - Indium diffuses into the NiCr layer

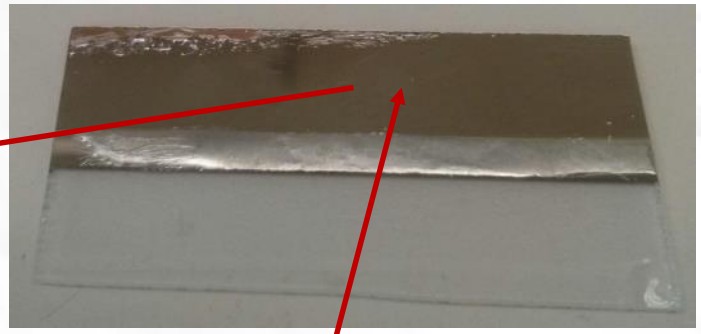
Low melting InBi alloy
allows to explore temperatures
below melting of pure In (157C)

Depth profile XPS



Layer depth (uncalibrated)

Glass with NiCr-Cu metallization
exposed to **InBi** at ~100C for <1hrs
(it seals at these conditions)



InBi was scraped when still
above melting (72C)

The ion etch number is a measure
for the depth of each XPS run

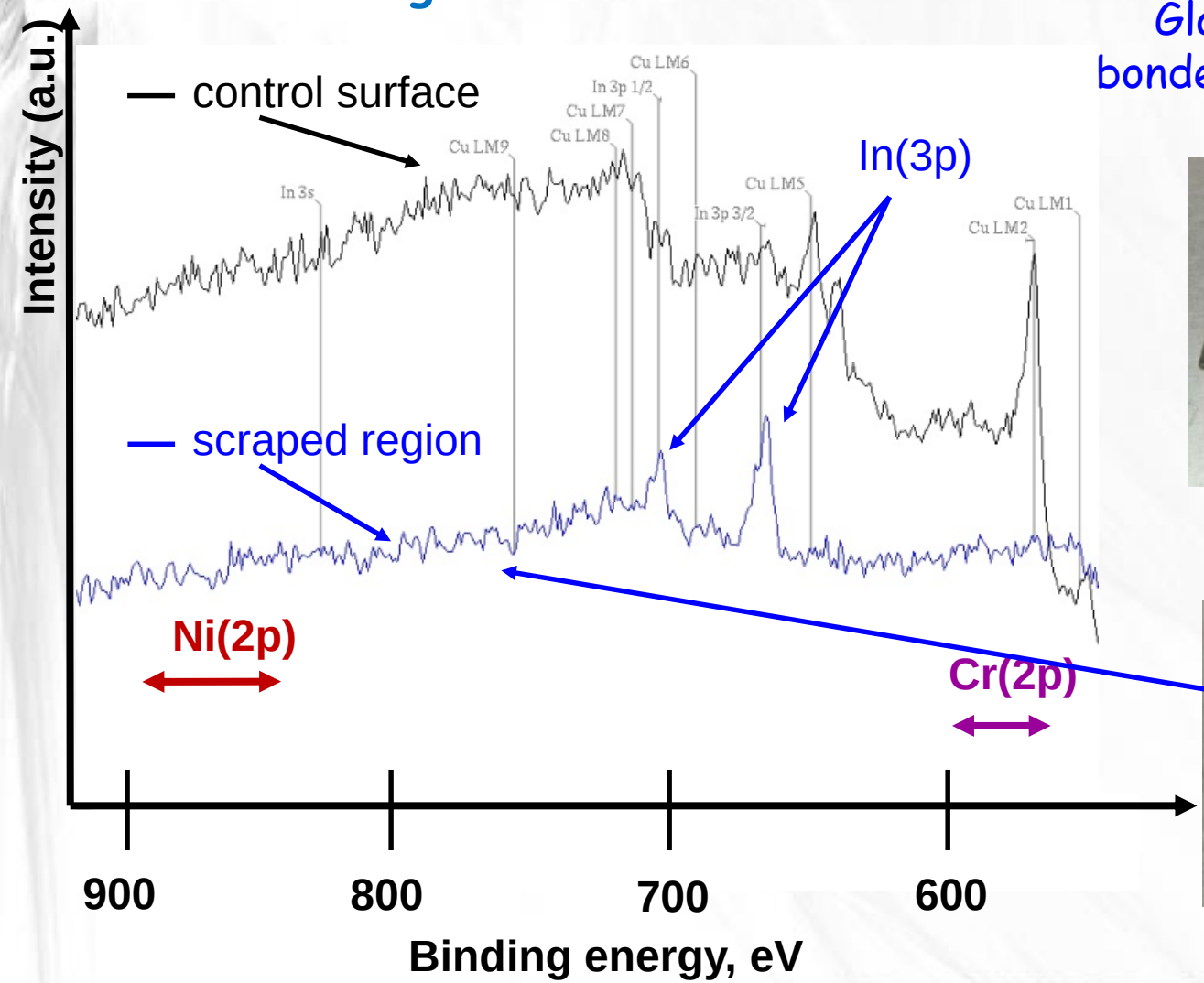
XPS access courtesy of
J. Kurley and A. Filatov at UChicago

Metallurgy of a Good Seal

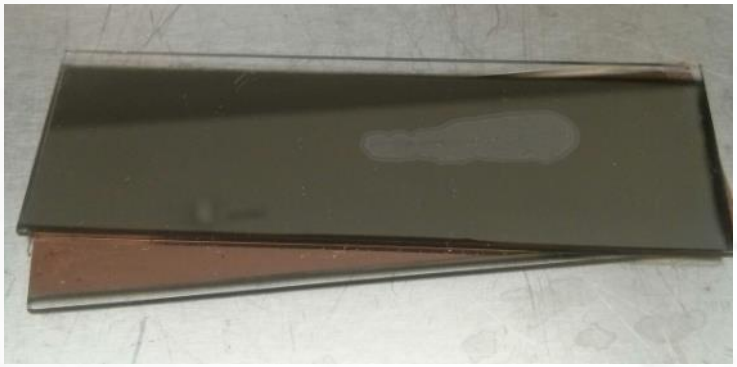
Higher temperatures and longer exposure time

- Indium penetrates through entire NiCr layer

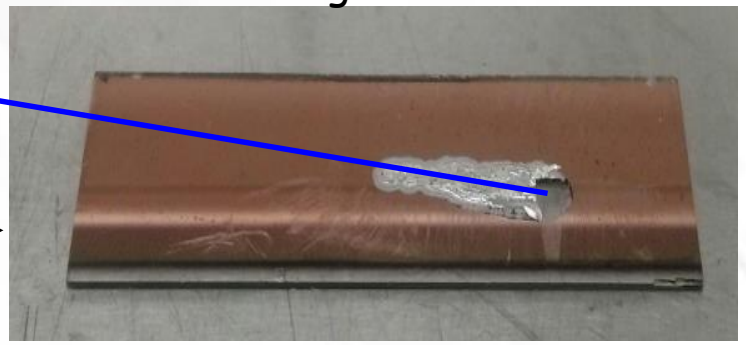
XPS of the glass side of the interface



Glass with NiCr-Cu metallization bonded by **pure In** at ~350C for 24hrs (it seals at these conditions)



Cut and scrape at the metal-glass interface



We now reliably seal at 250-300C for 12-24hrs

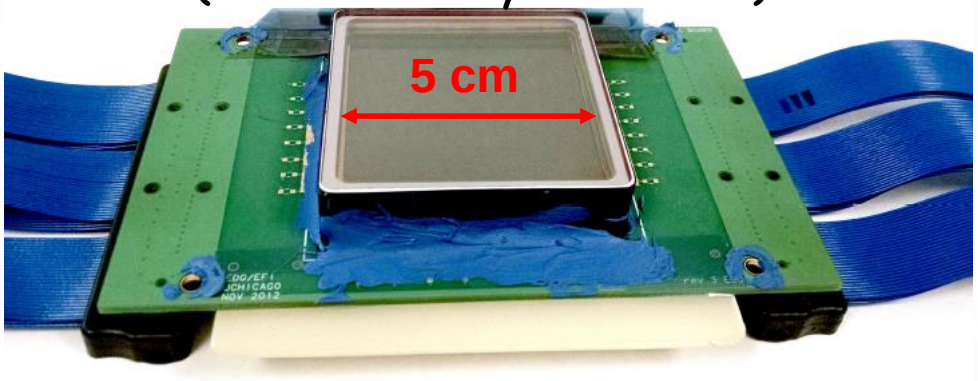
XPS data courtesy of A. Filatov at UChicago

Indium seal recipes exist for a long time

Why do we need another indium seal recipe?

PLANACON™

(MCP-PMT by Photonis)



Make larger photo-detectors

Our recipe scales well to large perimeter

Simplify the assembly process

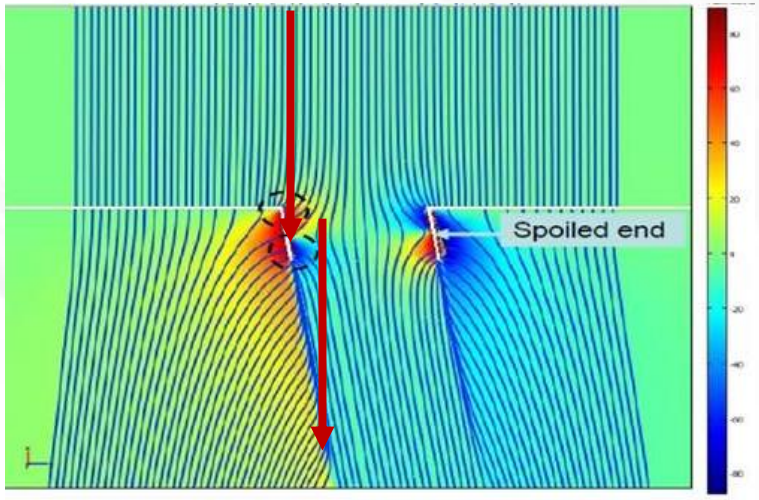
Our recipe is compatible with PMT-like batch production

Large-signal Limit Dependence

Does the time resolution go as 1/N or 1/root-N photo-electrons?

Hypothesis:

- In an MCP-PMT the time jitter is dominated by the 1st strike: path length to the 1st strike varies
- Smaller pores, increased bias angle are better
- "IF gain is such that a single photon shower makes the pulse (e.g. 10^7), time jitter is set by the probability that NO photon has arrived in interval δt" - H. Frisch
  This assumes that one fits the waveform to determine pulse T_0



E.g. if 50 photoelectrons (from Cherenkov light in a window) arrive within 50 psec, the probability that one goes for T psec with NO photon making a first strike goes as e^{-T}
=> a 1/N dependence