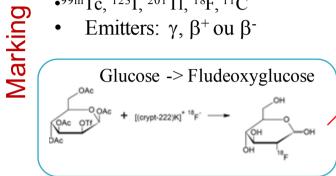
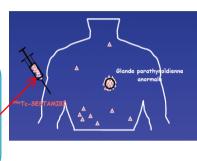
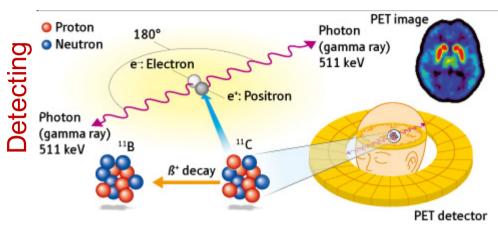
Nuclear medical imaging techniques: Principle:



Molecule + Radioactive isotope •^{99m}Tc, ¹²³I, ²⁰¹Tl, ¹⁸F, ¹¹C Emitters: γ , β^+ ou β^-



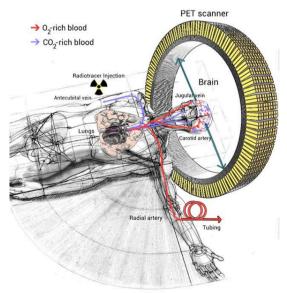




Nuclear imaging technology γ camera, tomographs

Technologies:

Cancer diagnostic



Cancer therapy

Gamma imaging camera



Beta probe

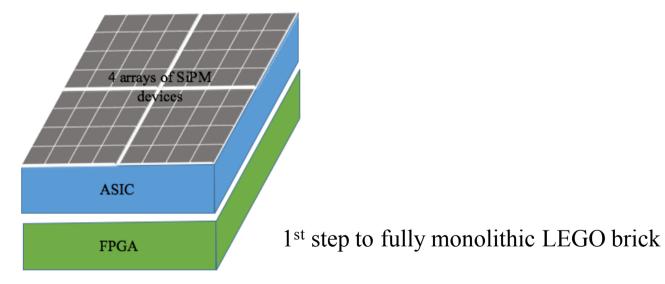


Beta-probe with active background rejection:

Active background rejection:

- reduction direct radioactive dose (to patient & medical personal)
- possibility to use it for tumors where gamma-ray background from the healthy organs prevent the application of traditional techniques

Detection module:



Proposal is submitted to FET-Launchpad; If any partner want to contribute \rightarrow you are welcome!



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SiPM`s failed to replace standard PMT`s in large detection surfaces experiments:

- Main limitations:
 - o Dark noise
 - Poor performance of large monolithic sensor or prohibitive cost due to large number of electronics channels if area covered by tiling small detection units
- Recent developments partially address these issues:
 - Recent developments (e.g. LVR from HPK) already partially tackle the noise issue, can still be improved
 - $\circ~$ Solution with anode in series (e.g. MEG, DarkSide) but requiring more complex bias stage or digital SiPM

Growing panel of sensors available

- Main limitation:
 - Optimization phase for electronics development (discrete) or ASIC tuning long and repetitive
 - Extended R&D phase
- Existing solution:
 - Electronic modeling of SiPM response





The D-LIGHT FET-OPEN program intended to propose the sensor that would tackle the surface and performance not require the user to develop custom analog readout. The research lines were:

- Improve the digital sensor from Philips to tackle the noise and speed issue
- Provide compact package with 3D integration of sensor and readout electronics
- Use a scalable approach where increasing size would not necessarily means increasing electronics channel

Recently we discovered that the sensor concept was realized by a group at the University of Sherbrook:

 A 2D Proof of Principle Towards a 3D Digital SiPM in HV CMOS With Low Output Capacitance (DOI: 10.1109/TNS.2016.2582686) More details in the next slides



A 2D Proof of Principle Towards a 3D Digital SiPM in HV CMOS With Low Output Capacitance (DOI: 10.1109/TNS.2016.2582686)

Every SPAD has (Exactly as planed in D-LIGHT):

- Active quenching
- Possibility to enable/disable SPAD
- Current source

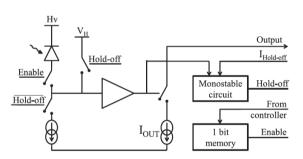
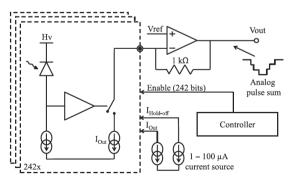


Fig. 2. Block diagram of the SPAD read-out.



If the goal is to implement the SPAD array and the readout in 3D fashion, the current implementation is performed with a monolithic approach (both approaches planed in D-LIGHT to) which offers poor filling factor

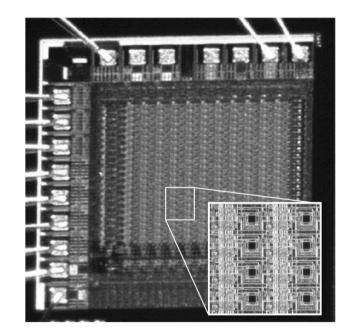


Fig. 5. Overview of the SiPM made in HV CMOS 0.8 μ m with a zoom on

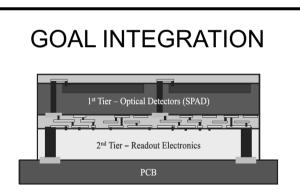


Fig. 1. Cross-section of the 3D digital SiPM. The $1^{\rm st}$ tier contains SPAD arrays with through silicon vias (TSV) and the $2^{\rm nd}$ tier contains quenching circuit arrays.



Fig. 3. Top level block diagram of the digital SiPM architecture, showing the analog sum of current pulse.

8 pixels of 50 \times 100 μ m².



A 2D Proof of Principle Towards a 3D Digital SiPM in HV CMOS With Low Output Capacitance (DOI: 10.1109/TNS.2016.2582686)

Advantages of the current source are:

- Fixed amplitude: lower fluctuation from avalanche to avalanche
- Variable duration: Reduction of dark count pile up, afterpulses
- Variable amplitude: Adaptable dynamic range

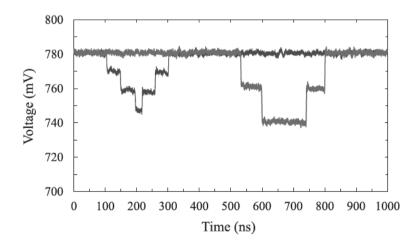


Fig. 10. Analog sum output for different current and hold-off values. In black, 3 SPADs triggered with an 11 mV response and 100 ns hold-off. In gray, 2 SPADs triggered with a 20 mV response and 200 ns hold-off.

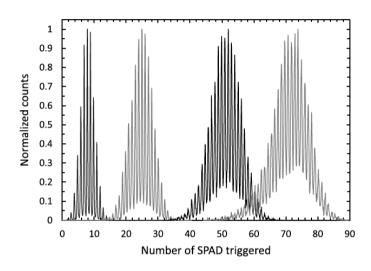


Fig. 11. Charge histogram for four different light intensities with clear steps of 0 to 90 SPADs triggered at the same time showing the single photon resolution capability of the digital SiPM.

Consequences:

- Photon counting capabilities up to high number of photons
- With the proper readout chip (e.g. SAMPIC) you can access the timing of all of them





If we follow this path, how can we contribute the current development:

- Improve SPAD performance:
 - DCR, XT
 - PDE:
 - Micro-lenses
 - Access to better CMOS technology (currently 0.8 µm HV CMOS)
- 3D integration:
 - Contact with companies:
 - <u>3D plus</u> for high yield 3D integration, e.g. <u>WDoD</u>
 - Silicon/Glass interposers (Planoptik, LPKF)
 - Access to machines:
 - Probe station (@ UniGe)
 - Flip-Chip machine (@ UniGe)
- Readout:
 - ASIC development
 - Interface to high performance ASICs (e.g. SAMPIC)
- Access to test facility

