ATLAS MDT ASD_V4

Design

May 29th, 2017

Federica Resta
Marcello De Matteis

andrea.baschirotto@sparklingic.com

ASDv4
Outline

- Channel Block Scheme ←←←
- Charge Sensitive Preamplifier
- Differential Amplifiers
- Wilkinson ADC
- Measurements Summary
- Conclusion

ASDv4
Channel Block Scheme

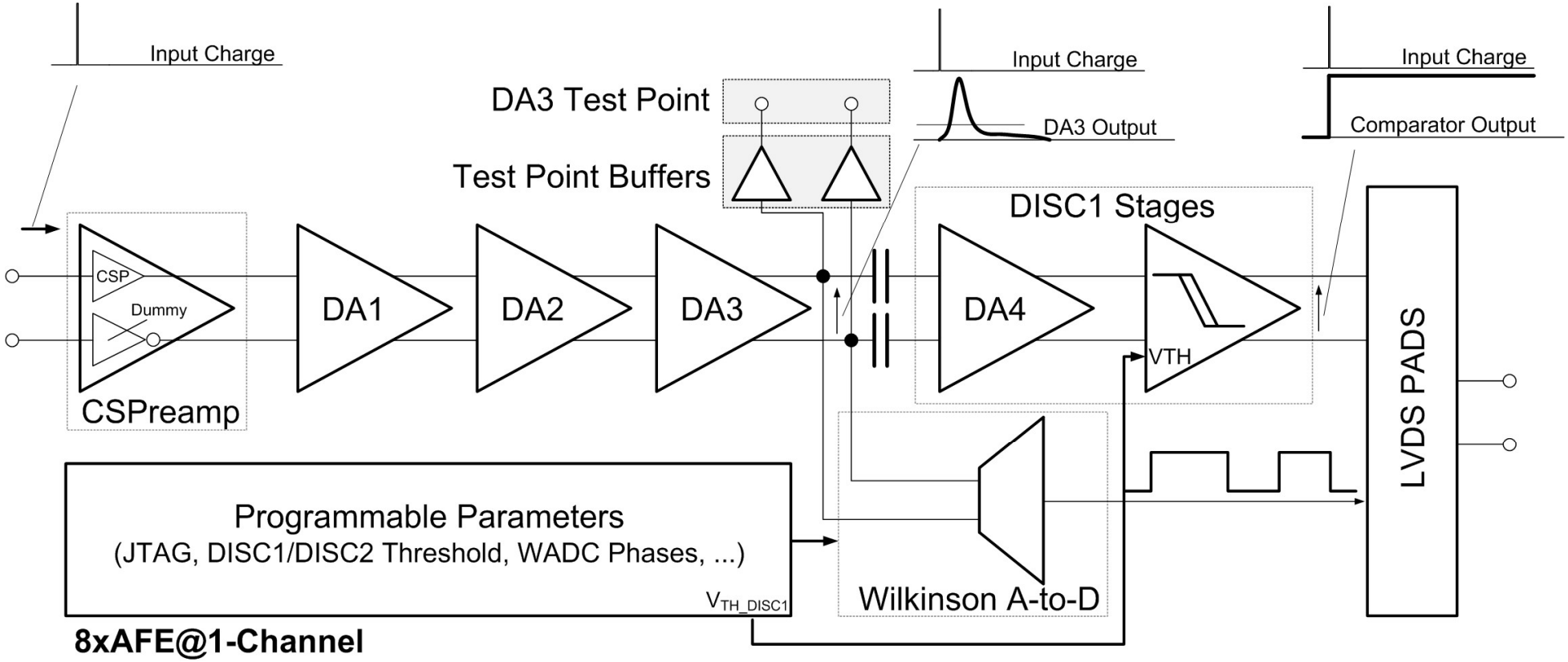

Fig. 1 – Channel Block Scheme.

ASDv4
Channel Critical Design Points (1/2)

- CMOS Technological Node
  - 130nm
  - 3.3V Supply Voltage
  - V_{TH} Reduction
    - 0.45V vs 0.75V
  - Sligth Reduction of intrinsic MOS gain
  - Smaller Signal
  - Substrate influenced by rail-to-rail digital signals
  - Smaller Area

- Detector Parasitic Capacitance
  - 60pF

Required a CAREFUL CSPreamp Design

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Channel Critical Design Points (1/2)

- CSPreamp
  - INPUT and KEY BLOCK
    - Charge to Voltage Conversion
  - Essential Matlab Model for performance optimization
    - Noise
    - Sensitivity
    - Peaking Time Delay

- Parasitic Capacitance at CSPremp Output
  - To guarantee a good conversion speed

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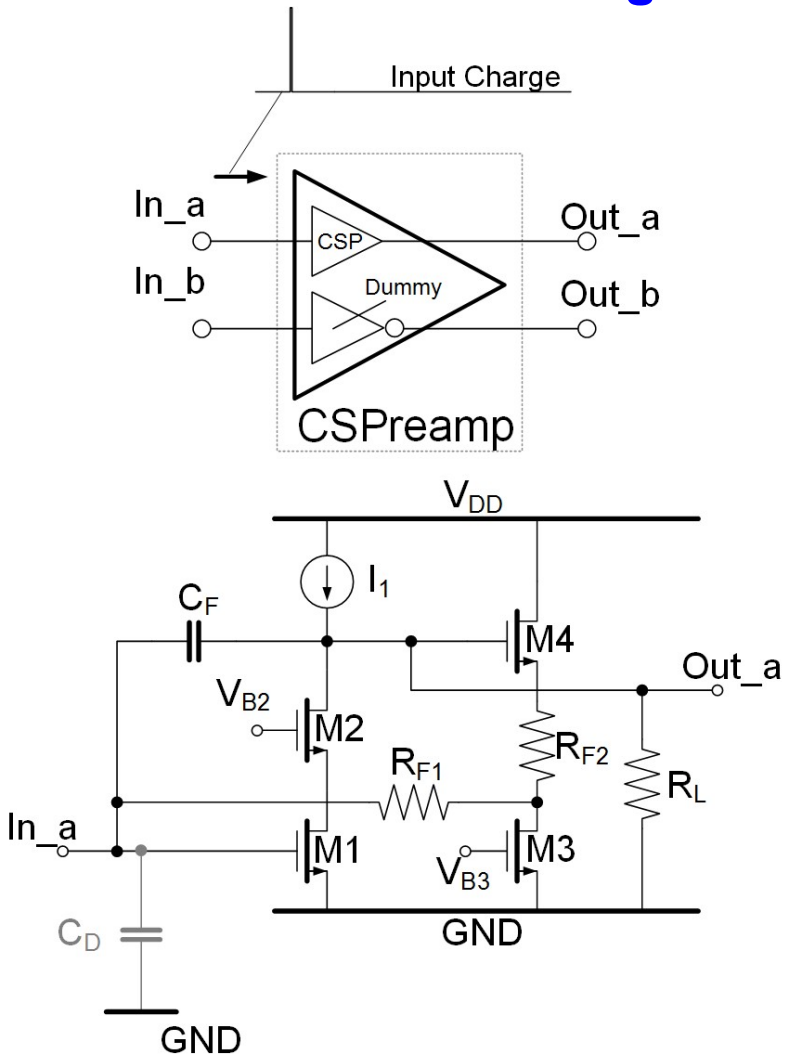
Charge Sensitive Preamplifier



- Pseudo-Differential Structure
  - 2 identical Charge Sensitive Amplifiers
    - CSPreamp
    - CSPreamp Dummy
- Feedback Components:
  - C_F
  - $R_F=R_{F1}+R_{F2}$

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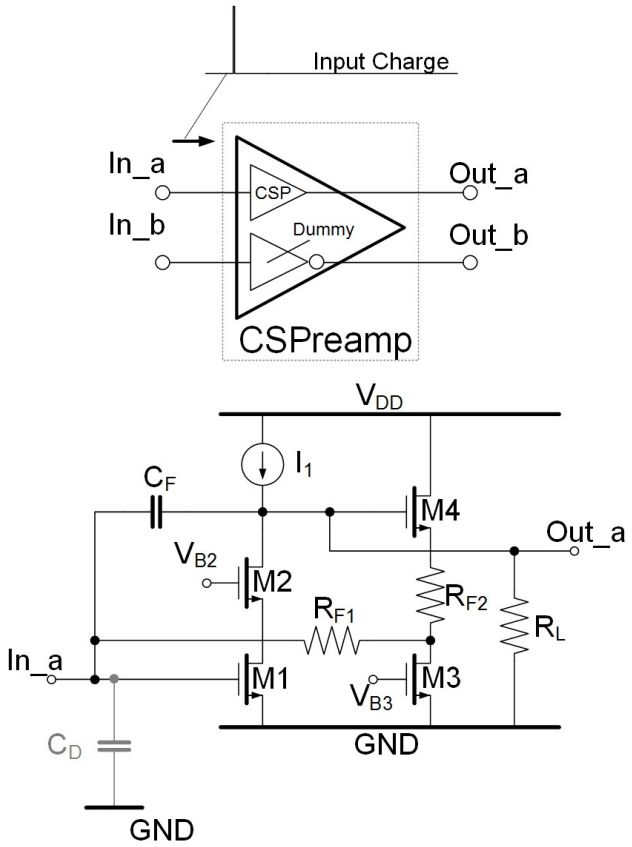
Charge Sensitive Preamplifier

$$T(s) \cong -R_F \cdot \frac{1-s\frac{C_F}{g_{m1}}}{\left(1+sC_FR_F\cdot\left(1+\frac{C_D}{C_F}\left(1+\frac{R_L}{R_F}\right)\frac{1}{1+g_{m1}R_L}\right)\right)\cdot\left(1+s\frac{C_D}{g_{m1}}\right)}$$

- With
  - Detector Capacitance (C_D)
  - Feedback Capacitance (C_F)
  - Feedback Resistor ($R_F=R_{F1}+R_{F2}$)
  - Load Resistor (R_L)
  - DC Loop Gain ($g_{m1}\cdot R_L\approx400$)
  - $C_D/C_F\approx88$



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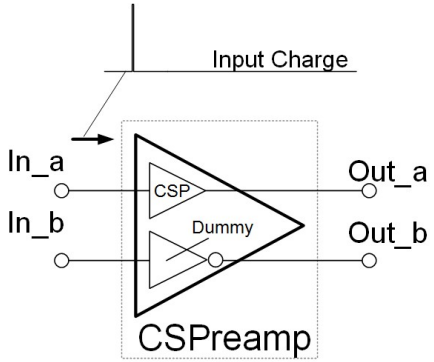
Charge Sensitive Preamplifier

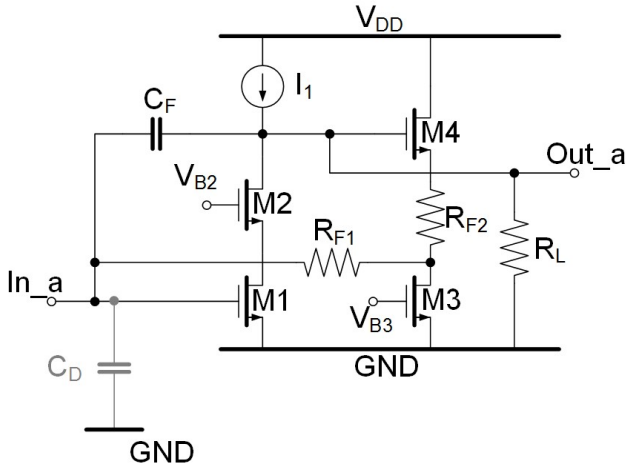
$$T(s) \cong -R_F \cdot \frac{1-s\frac{C_F}{g_{m1}}}{\left(1+sC_FR_F\cdot\left(1+\frac{C_D}{C_F}\left(1+\frac{R_L}{R_F}\right)\frac{1}{1+g_{m1}R_L}\right)\right)\cdot\left(1+s\frac{C_D}{g_{m1}}\right)}$$

- Choosing
  - $R_L=R_F$
  - $g_{m1}>>1/R_F$

- High Frequency Zero (≈5GHz)
- CSPreamp Transfer Function can be approximated to:

$$T(s) \cong -R_F \cdot \frac{1}{\left(1+sC_FR_F\cdot\left(1+2\cdot\frac{C_D}{C_F}\cdot\frac{1}{1+g_{m1}R_L}\right)\right)\cdot\left(1+s\frac{C_D}{g_{m1}}\right)}$$





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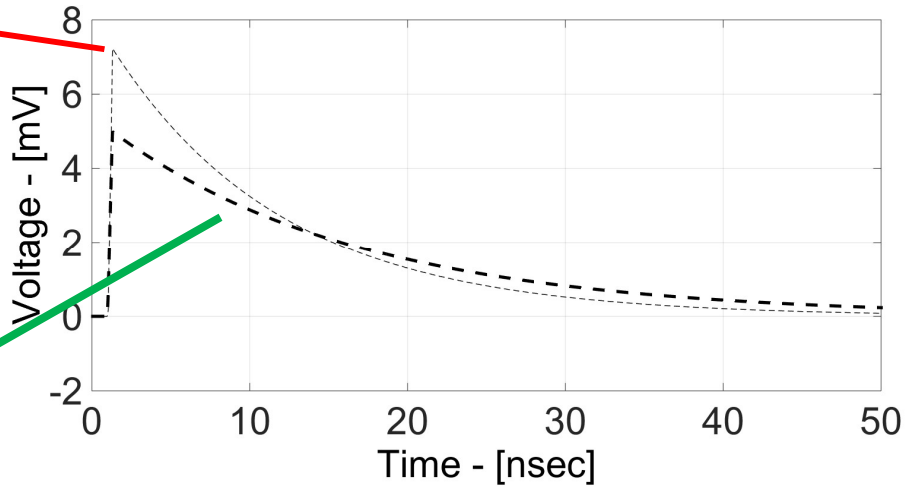
CSPreamp Dominant Pole

- Ideal Case:
  - Open Loop Amplifier has
    - Infinitive gain
    - Infinitive bandwidth
  - Ideal Dominant Pole Constant → $C_F R_F$
  - Ideal Sensitivity → $S_{CSP,IDEAL} \cong \left(\frac{1}{C_F}\right)$



- Finite DC Gain ($g_{m1} \cdot R_L \approx 400$)
  - Dominant Pole Constant → $\approx C_F R_F \cdot \left(1 + 2 \cdot \frac{C_D}{C_F} \cdot \frac{1}{g_{m1} R_L}\right)$
  - Sensitivity → $S_{CSP} \cong S_{CSP,IDEAL} \cdot \left(\frac{1}{1+2 \cdot \frac{C_D}{C_F} \cdot \frac{1}{g_{m1} \cdot R_L}}\right) = 0.68 \cdot S_{CSP,IDEAL}$

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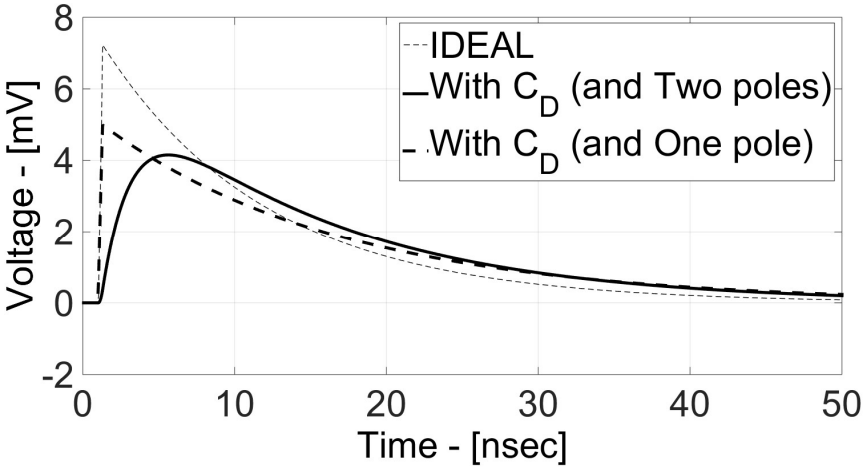
CSPreamp Second Pole Effect

- Ideal Case:
  - Open Loop Amplifier has
    - Infinitive gain
    - Infinitive bandwidth
  - Ideal Dominant Pole Constant → $C_F R_F$
  - Ideal Sensitivity → $S_{CSP,IDEAL} \cong \left(\frac{1}{C_F}\right)$



- Finite DC Gain ($g_{m1} \cdot R_L \approx 400$)
  - Dominant Pole Constant → $\approx C_F R_F \cdot \left(1 + 2 \cdot \frac{C_D}{C_F} \cdot \frac{1}{g_{m1} R_L}\right)$
  - Second Pole Constant → $\approx \frac{g_{m1}}{C_D}$
  - Sensitivity → $S_{CSP} \cong S_{CSP,IDEAL} \cdot \left(\frac{1}{1+2 \cdot \frac{C_D}{C_F} \cdot \frac{1}{g_{m1} \cdot R_L}}\right) = 0.68 \cdot S_{CSP,IDEAL}$

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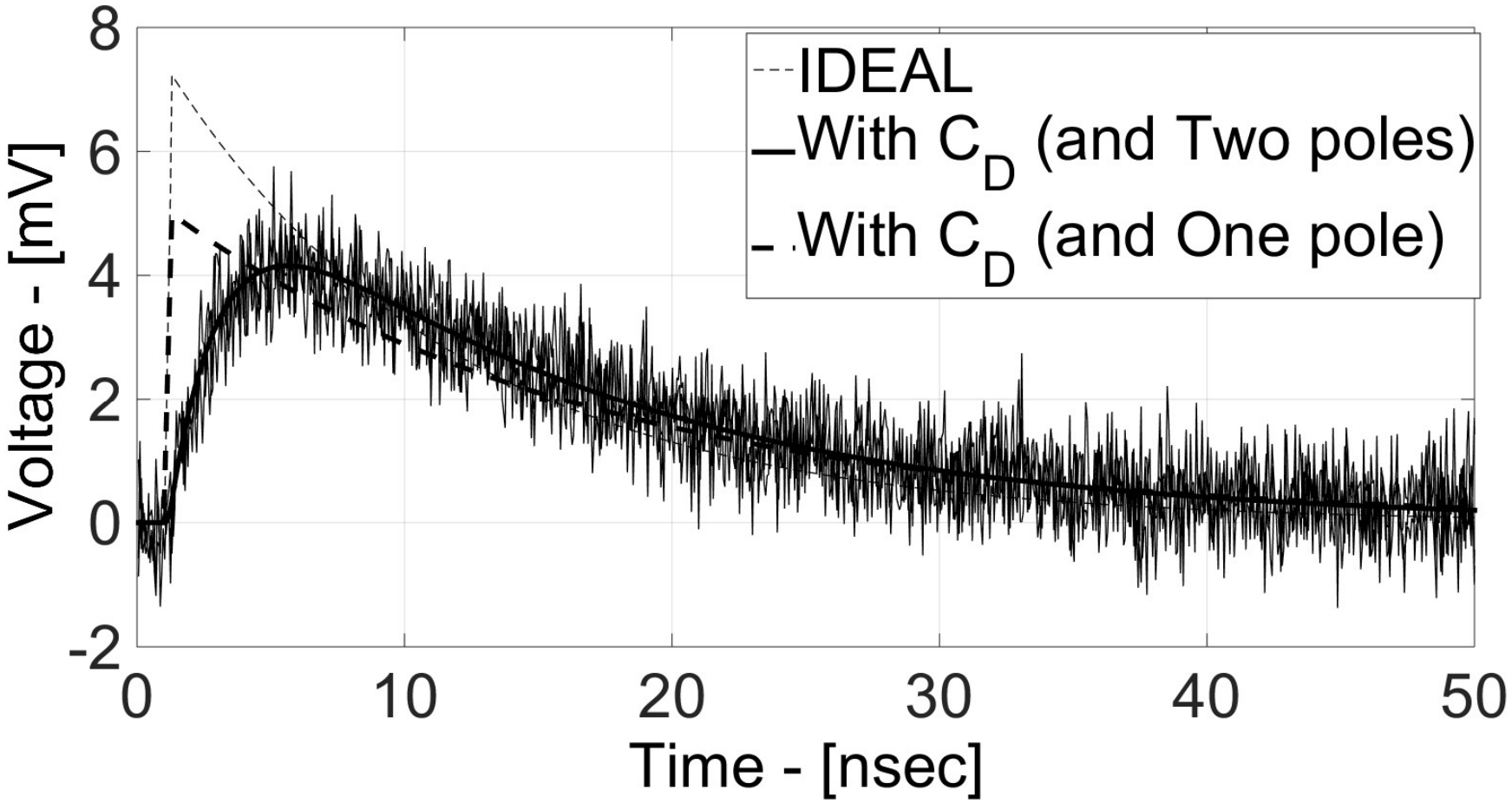
CSPreamp Transient Noise Model



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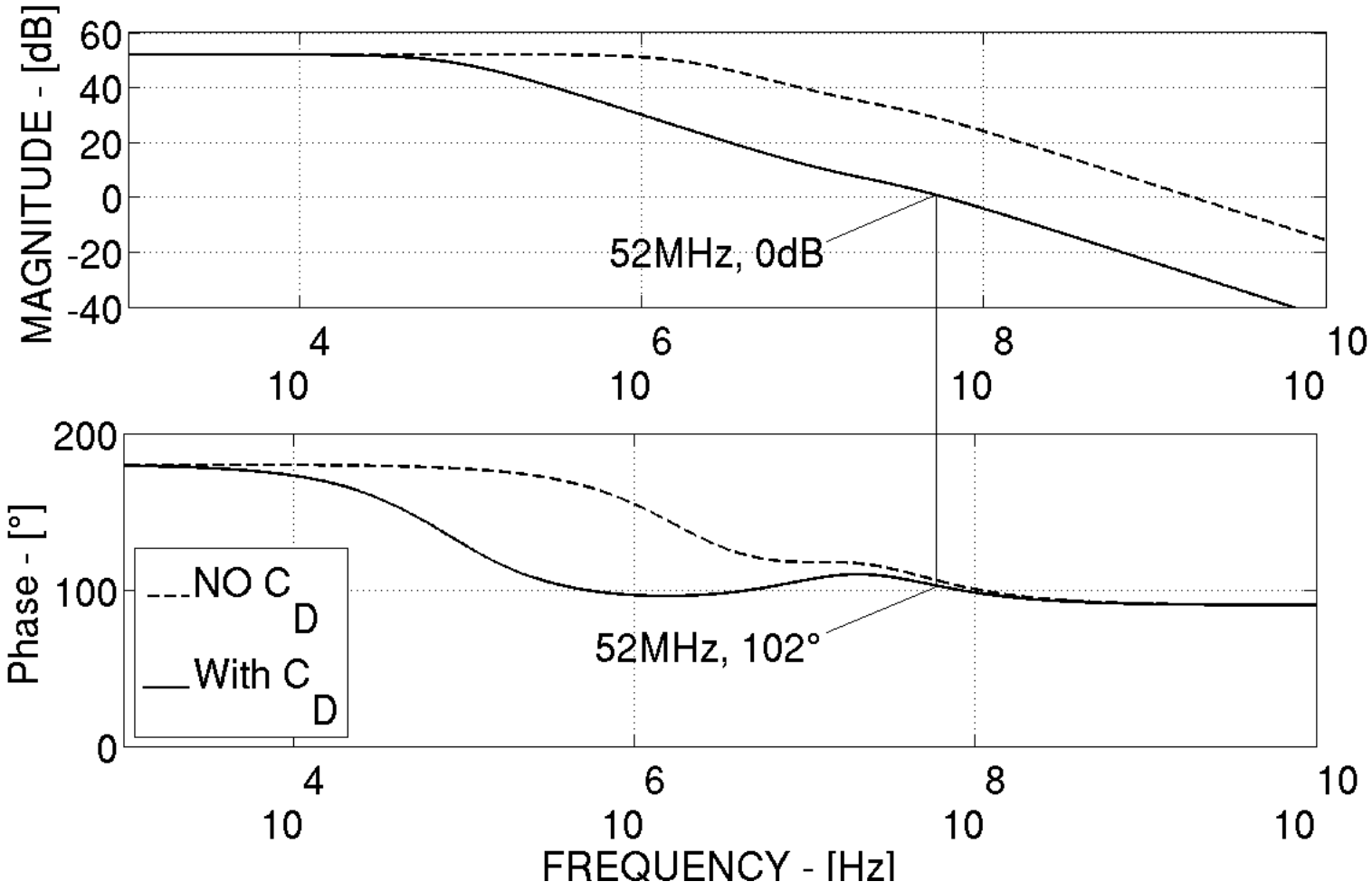
CSPreamp Loop Gain



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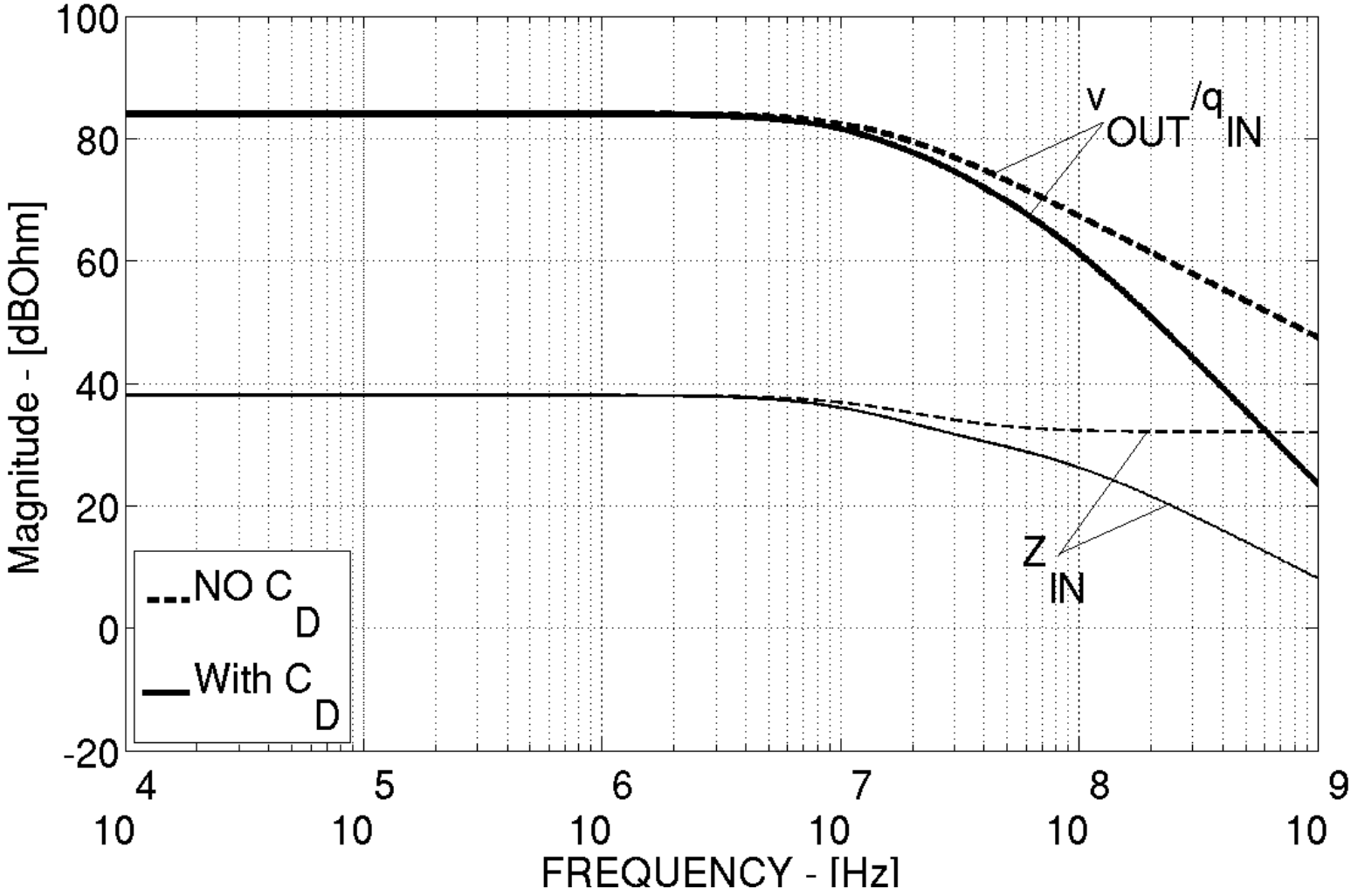
CSPreamp Frequency Responses



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CSPreamp Design Parameters Summary

Parameter	Min	Nominal	Max
Current Consumption	1.8mA	2.1mA	2.6mA
Supply-Voltage	3.3V	3.3V	3.3V
Peaking Time Delay (PTD)	8ns	7ns	6.2ns
DC-Gain	78dBΩ	82dBΩ	85dBΩ
-3dB Bandwidth	9MHz	11MHz	13.2MHz
Loop-Gain PM	90°	102°	103°
Output Noise	0.63mV$_{RMS}$	0.55mV$_{RMS}$	0.47mV$_{RMS}$
In-Band IRN PSD	5.8nV/√Hz	5nV/√Hz	4nV/√Hz

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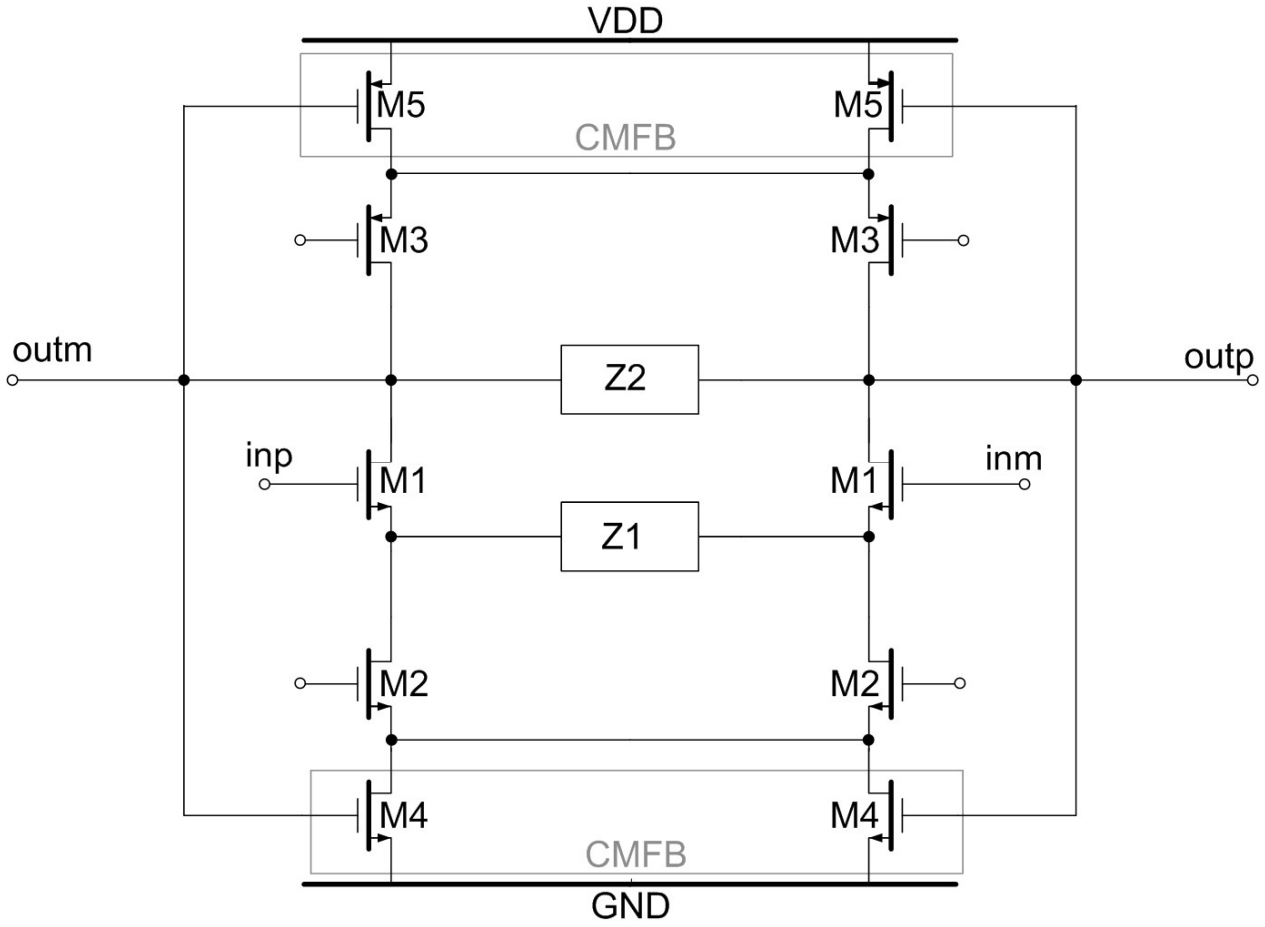
Differential Amplifiers



Stage	Z1	Z2
DA_1	1.35kΩ	6.26kΩ
DA_2	2.45kΩ // (2.45kΩ + 1/(s·47pF))	6.26kΩ
DA_3	2.45kΩ + 1/(s·47pF)	9.77kΩ

Smaller CMFB MOS:

- Reduce CSPreamp Parasitic Capacitance Load
- Manage Peaking Time Delay

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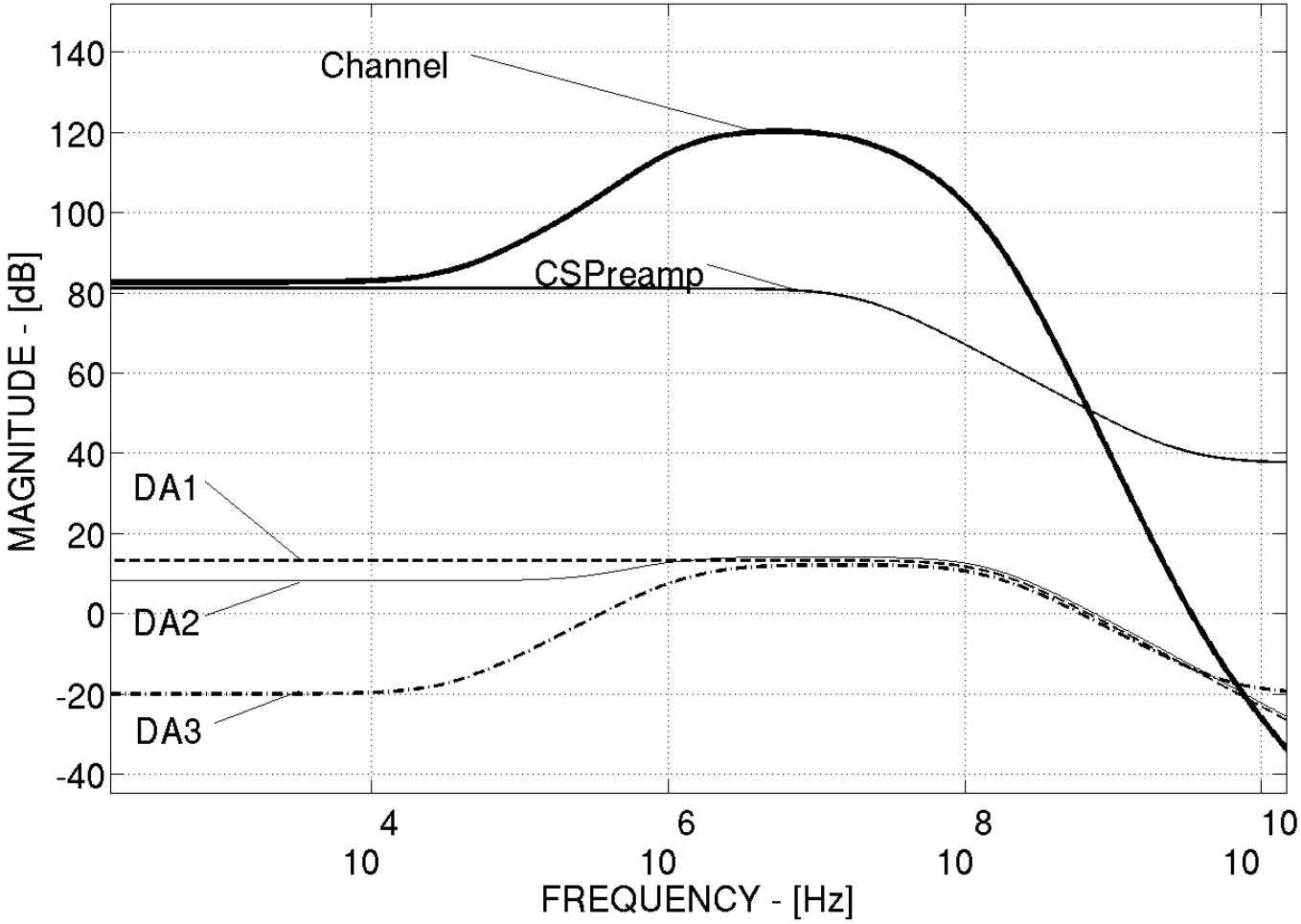
Differential Amplifiers



- 5MHz center frequency
- 30kHz high-pass frequency
- +6dB/octave slope

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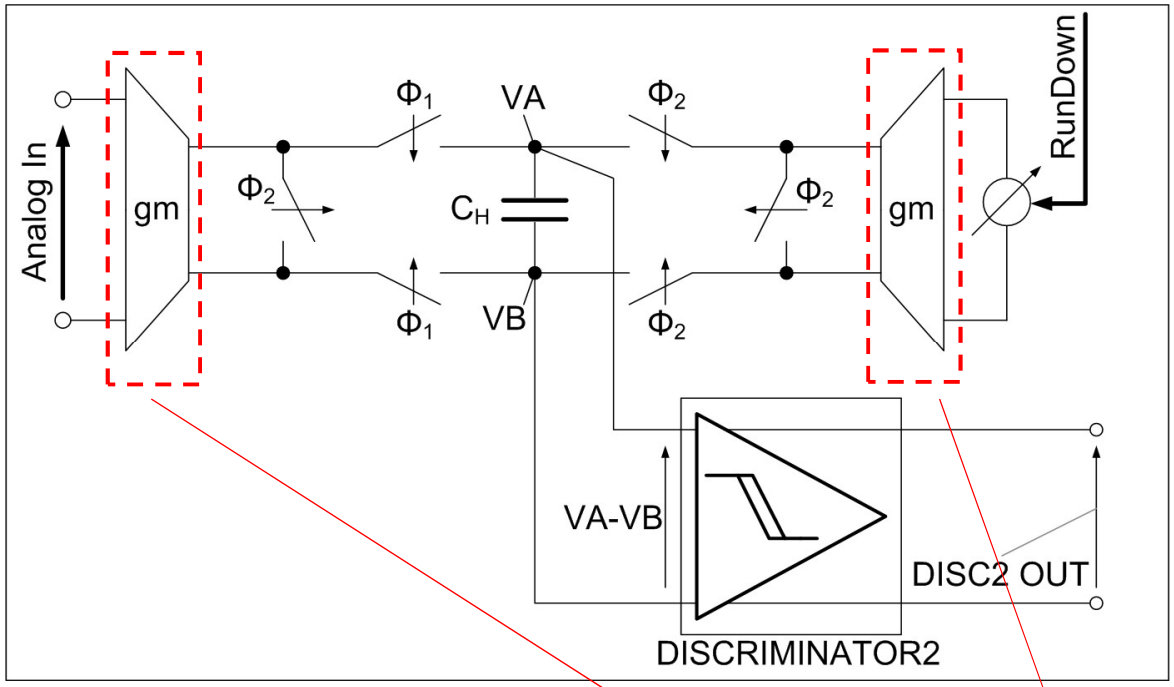
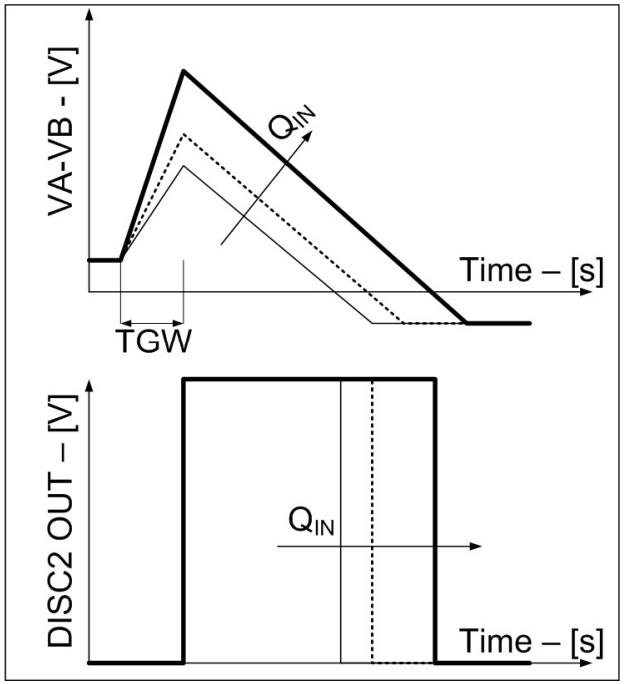
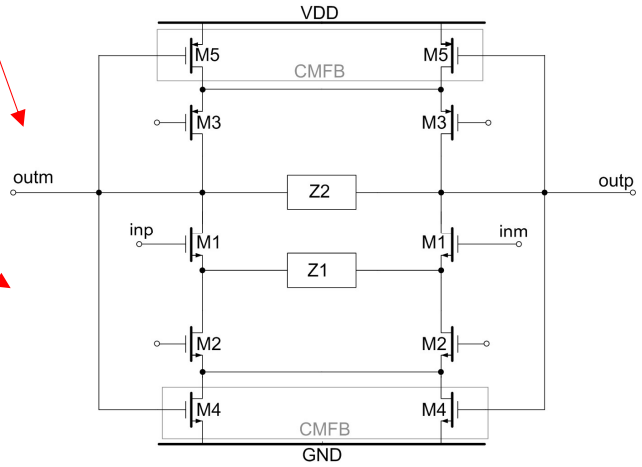
Wilkinson ADC





- Gain Stages Optimization
  - Reduction Parasitic Capacitance
  - Symmetrical Layout



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Measurements Summary (1/2)

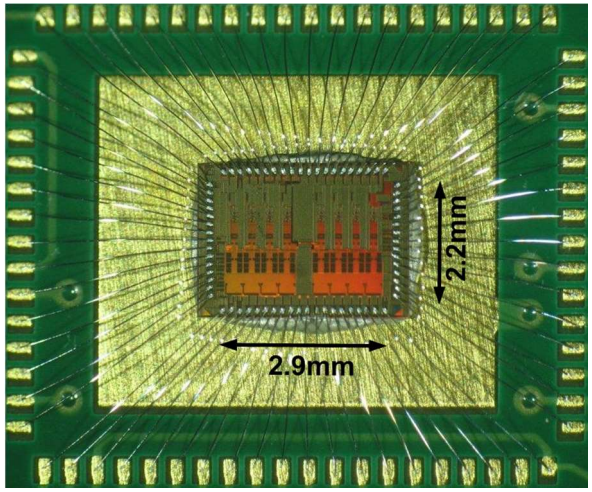

Fig. 2 – MDT-ASDv4 Chip Photo.

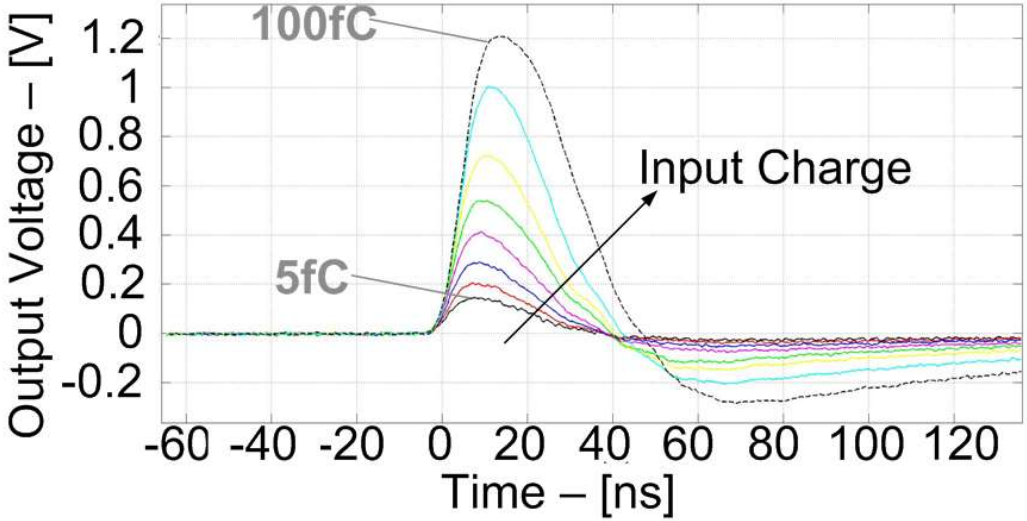

Fig. 3 – DA_3 Output Signal vs. Input Charge.

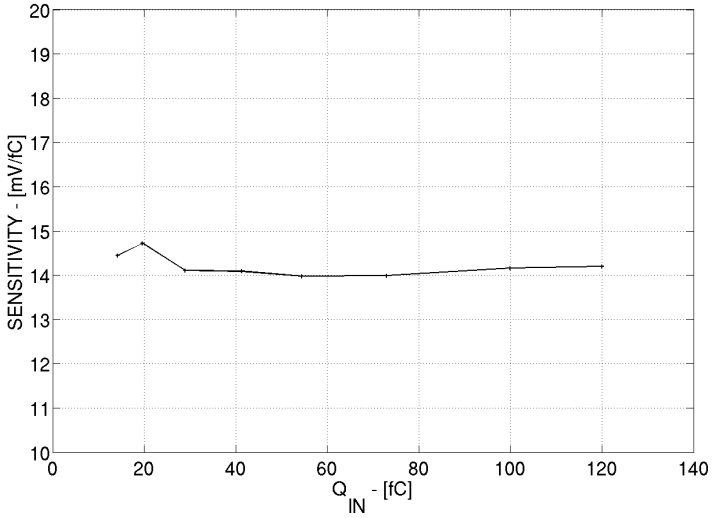

Fig. 4 – Channel Sensitivity vs. Input Charge.

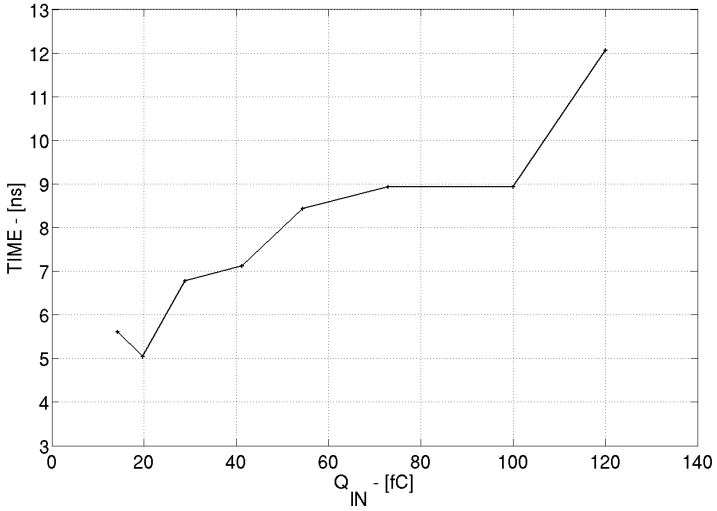

Fig. 5 – Peaking Time Delay vs. Input Charge.

ASDv4
Measurements Summary (2/2)

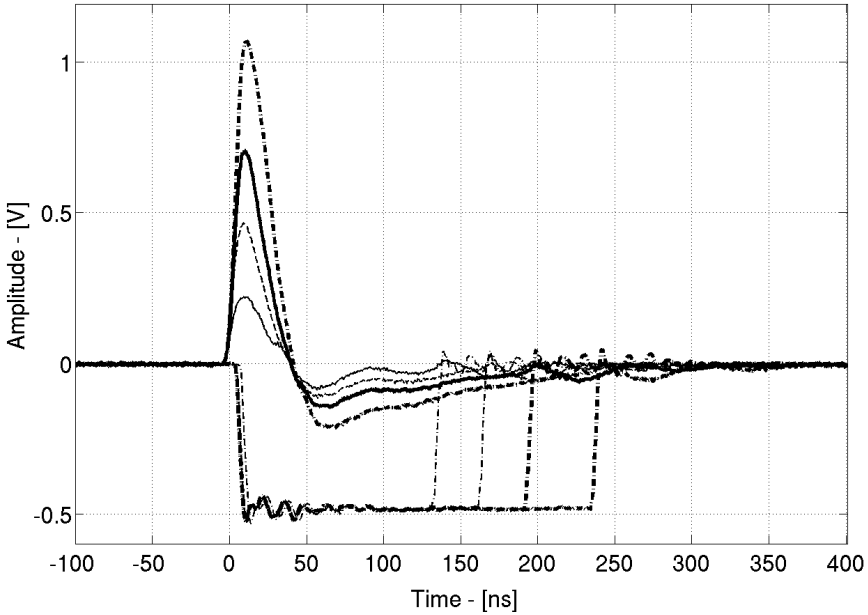

Fig. 6 – W-ADC, DA_3 Output Signals vs. Input Charge.

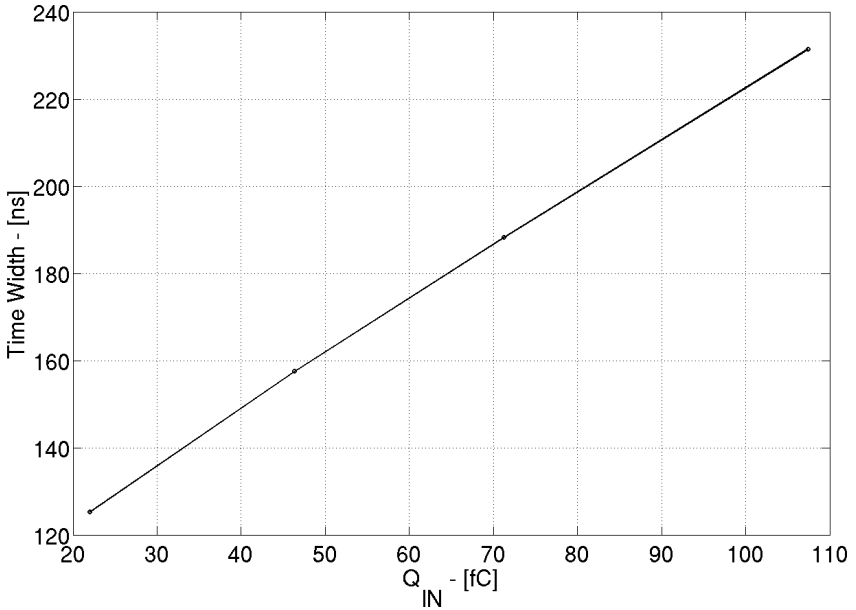

Fig. 7 – W-ADC Output Pulse Width vs. Input Charge.

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ASDv4
Conclusion

- MDT-ASDv4
  - Management of 60pF-C_D
  - Accurate q_{IN}-to-V conversion
  - Maximum Peaking Time Delay → 12ns
  - Linear V-to-T conversion
  - Area of 6.38mm^2

Total Current Consumption	162mA
Channel[1] Current Consumption	18.7mA*
Channel[2] Current Consumption	12.56mA
Total Power Consumption @3.3V of Supply Voltage	535mW
Channel[1] Power Consumption @3.3V of Supply Voltage	61.9mW
Channel[2] Power Consumption @3.3V of Supply Voltage	41.44mW

* 32.7% LVDS
21% CSP
20.2% Wilkinson ADC
16% $DAi_{i=1,2,3,4}$ chain
6.5% DISC1

BLOCK	PIN NAME	DESCRIPTION	TYPE	#	I/O INTERFACE
JTAG Serial Interface 6 PADs	SCLK	Clock Line	Digital In	1	Vpulse Generator
	SIN	Load Control Line	Digital In	1	Vbit Generator
	SDOWN	Down Control Line	Digital In	1	Vpulse Generator
	SHIFT	Shift Control Line	Digital In	1	Vpulse Generator
	SLOAD	Data Line	Digital In	1	Vpulse Generator
	SOUT	Data Line	Digital Out	1	noConn Istance
MDT-ASD V4 Channel 32 PADs	<ina0:ina7>	Positive Channel Input	Analog In	8	1 nF Cap or Current Generator in parallel with 60 pF Cap
	<inb0:inb7>	Negative Channel Input	Analog In	8	470 pF Cap
	<outa0:outa7>	Positive Channel Output	Analog Out	8	Input 'A' LVDS Termination
	<outb0:outb7>	Negative Channel Output	Analog Out	8	Input 'B' LVDS Termination
Channel#7 Buffer 2 PADs	anaa	DA_{3oa} of Channel#7	Analog Out	1	1 pF Cap
	anab	DA_{3ob} of Channel#7	Analog Out	1	1 pF Cap
Current Channels Generator 1 PAD	IBIAS_10 µA	Current Generator	Analog In	1	Current Generator of 10 µA ± 5 %
Supplies 29 PADs	<vdd1:vddq>	Supply Voltage	Analog In	10	DC-Voltage Generator of 3.3 V ± 5 %
	<sub1:subq>	Ground Voltage	Analog In	7	DC-Voltage Generator of 0 V
	<gnd1:gndq>	Ground Voltage	Analog In	12	DC-Voltage Generator of 0 V

Fig. 8 – MDT-ASDv4 Pin Table (70 Pins).

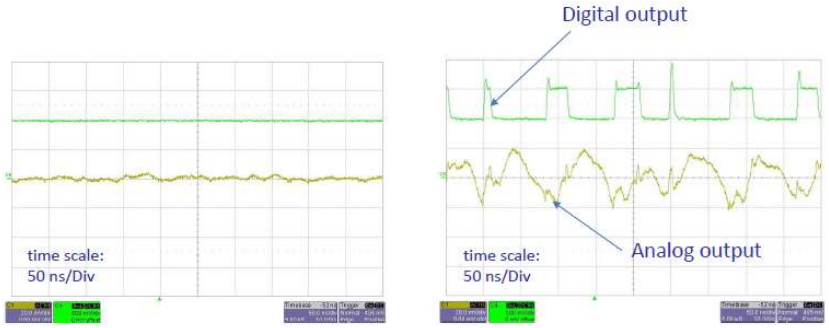
[1] Including CSP+DA1+DA2+DA3+DA4+DISC1+WILKINSON ADC+MUX+LVDS
[2] Including CSP+DA1+DA2+DA3+DA4+DISC1+WILKINSON ADC

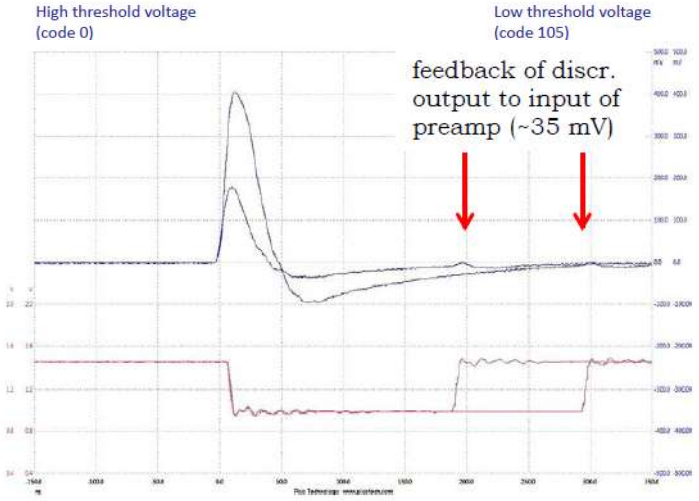
ASDv4

Conclusion – Measurements Issues

1. Substrate Noise
2. Channel Mismatch
3. Smaller Deadtime Range

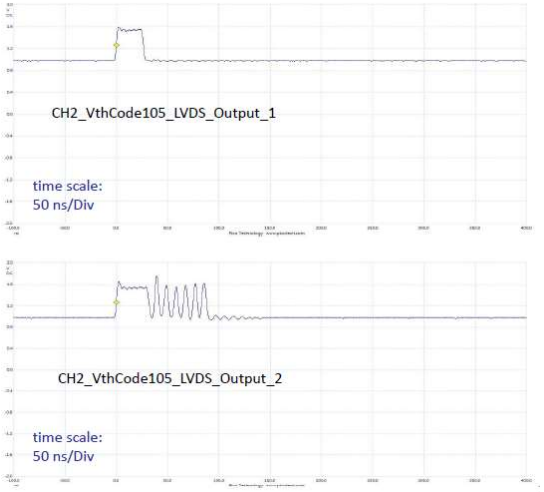
- No input signal, programmable board connected to set different threshold voltage values
- Baseline noise impact, which should have only influenced the comparison result at the output of DISC1, now seems to also affect the previous stages – the amplifier chain, and the corresponding effect can be observed at the analog buffer's output
- Possible backward coupling from DISC1 to the analog chain is one reasonable explanation

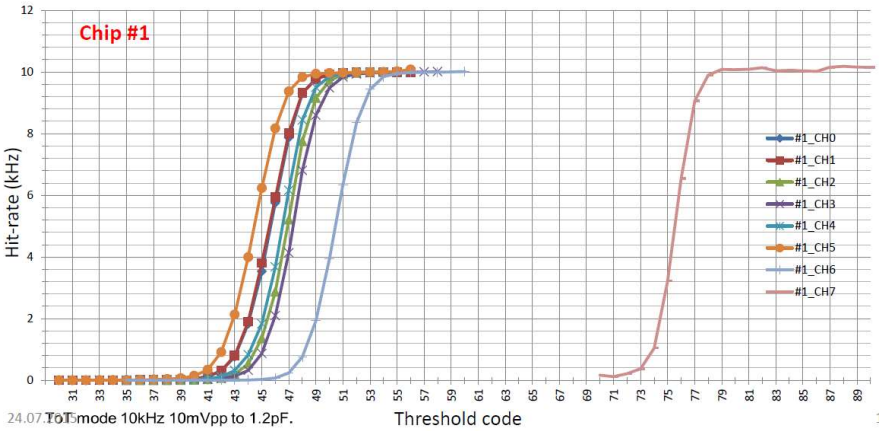




- Input: 10mV voltage step to 1.2pF → 12fC input charge.
- The two screen shots show the LVDS output of a CH2 in ToT mode, HystCode=0, VthCode=105 (-43mV), it may cause oscillations.
- There is a kind of "stable oscillating" threshold. After reaching this threshold, the output starts to oscillate (here around code 107-108). Interesting thing is that to stop oscillation the threshold has to be pulled back very far, far more from a level when it start to happen.

25.07.2015





24.07.2015 ToT mode 10kHz 10mVpp to 1.2pF.