# ATLAS MDT ASD_V6

## Report no. 7
## Design Review – ASDv4 – ASDv5

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# DESIGN REVIEW

## Outline

- ASDv4 Fixing Activities
  - Substrate Noise
  - Channel Mismatch
  - Deadtime
- ASDv5 Issues
  - Jtag Serial Data Interface
  - Integration Gate
- New CSPreamp

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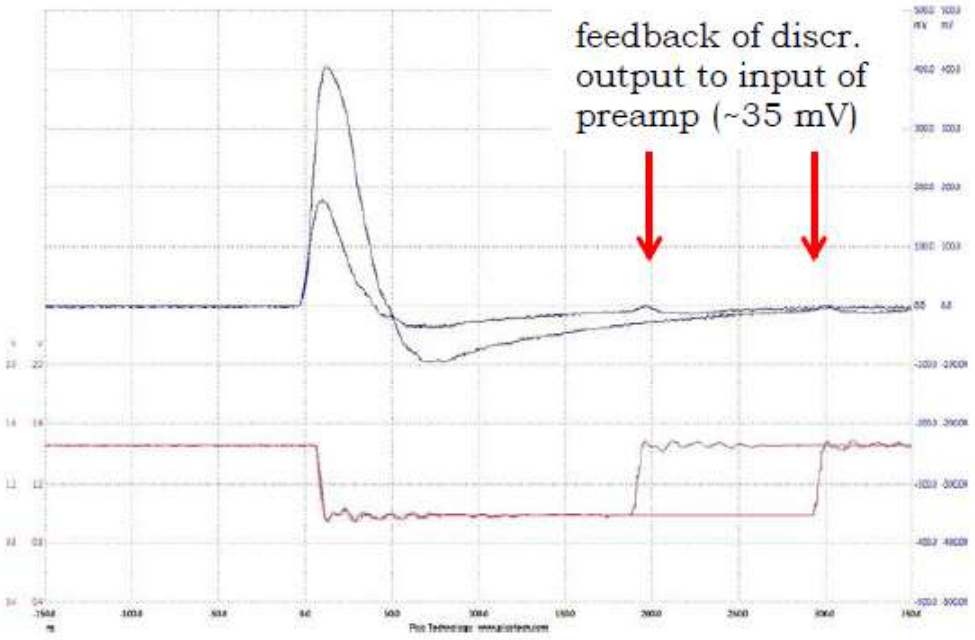
# Substrate Noise

## Introduction

- Digital signals reach 3.3V
  - Substrate more sensible
    - Difficult SE structures optimization to improve noise rejection



# Substrate Noise
## Adopted Approaches

- Schematic Level
  - Replace SE CSPreamp (as in MDT-ASD User Manual 2002-03)

    with FD CSPreamp

- Layout Level
  - Supplies/Grounds Isolation
  - Routing Improvement

# Substrate Noise
## Schematic Approach

- Schematic Level
  - Replace SE CSPreamp with FD CSPreamp

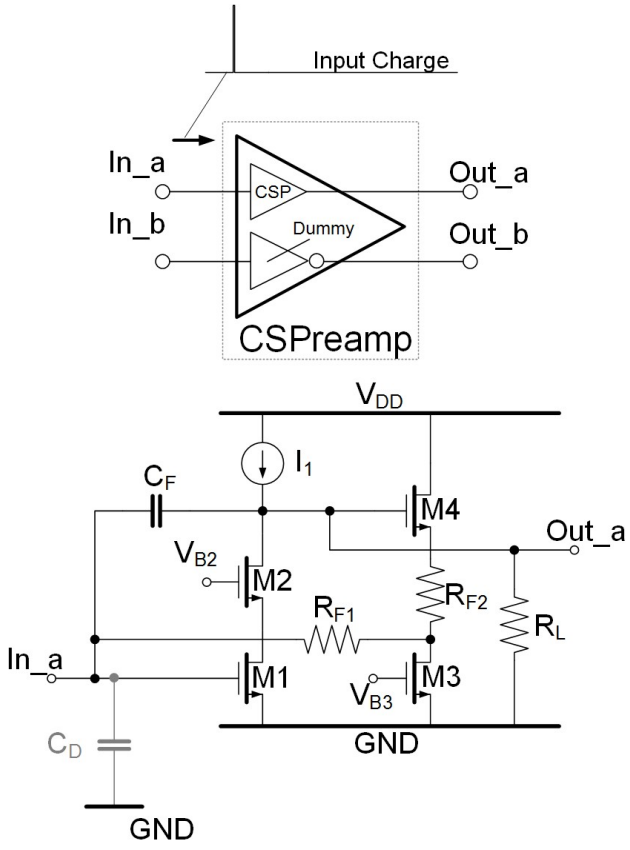



Fig. 1 – SE CSPreamp (up to ASDv4)

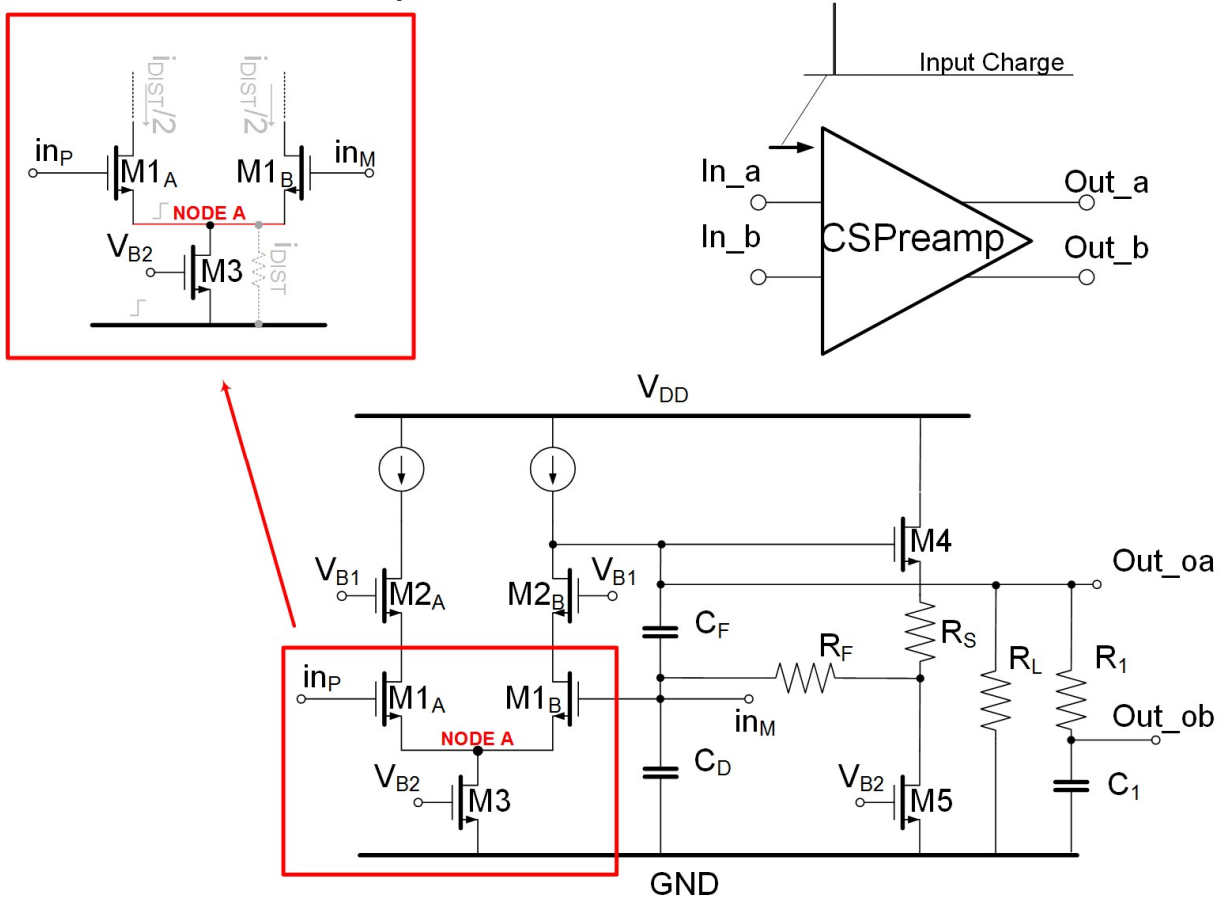



Fig. 2 - FD CSPreamp (from ASDv5)

# Substrate Noise

## Supply Noise Rejection

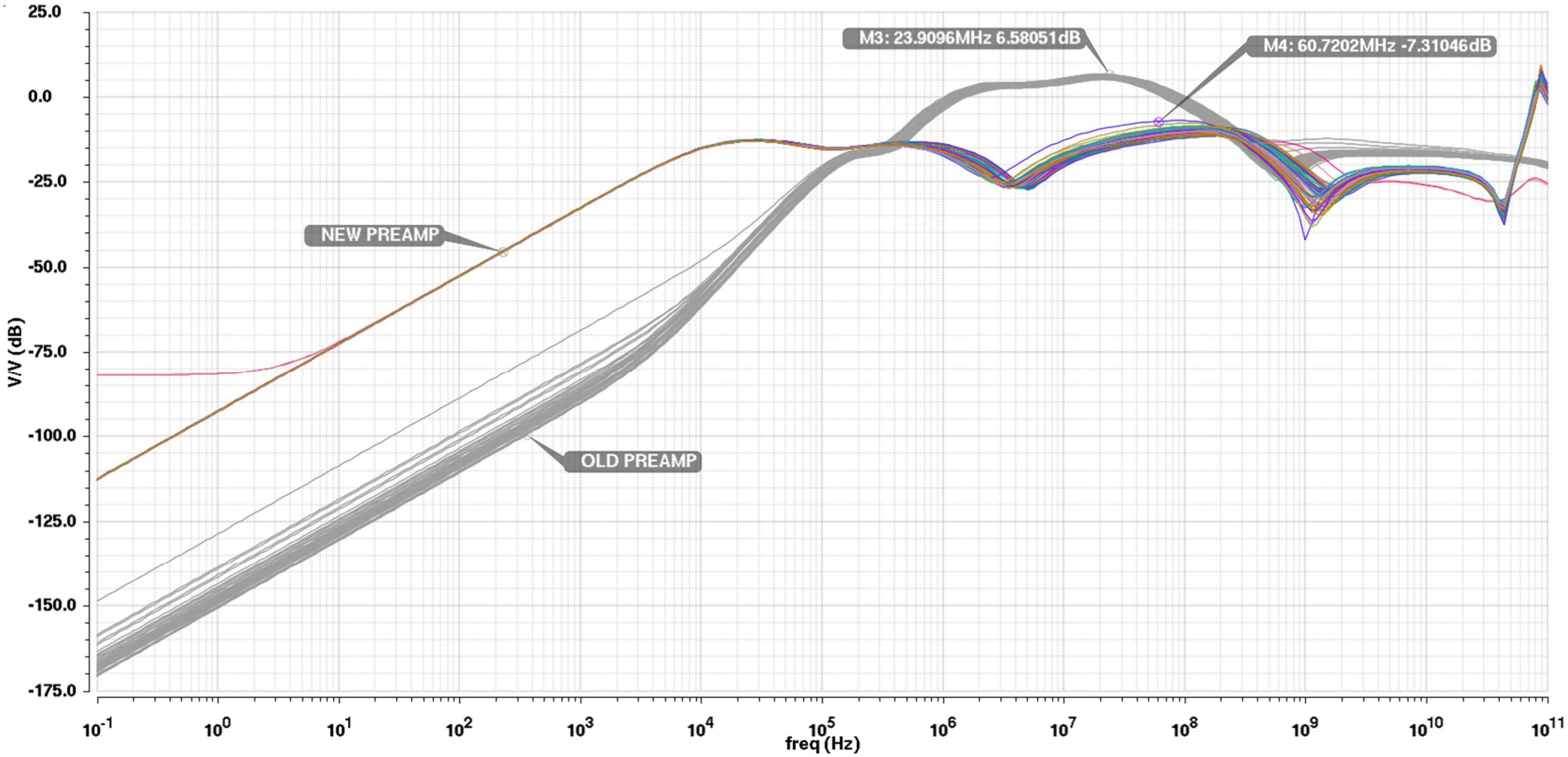



**Fig. 3 – Comparison of $v_{OUT,CSPreamp}/v_{DD}$ Frequency Responses.**

# Substrate Noise
## Layout Approach (1/2)

- Layout Level
  - Supplies/Grounds Isolation
    - *Guard Rings* and *BFMOAT*

Foundry Application Note
**Substrate Isolation in IBM BiCMOS and CMOS RF Technologies**

*Figure 5. Cross Section of Substrate with a BFMOAT Region (BiCMOS 7HP Technology)*

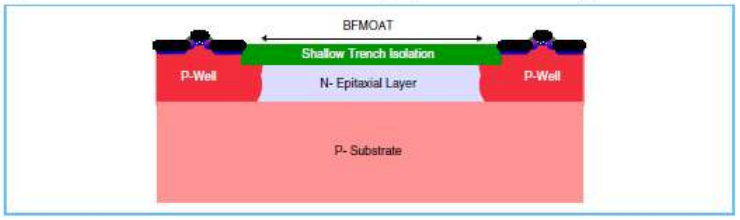
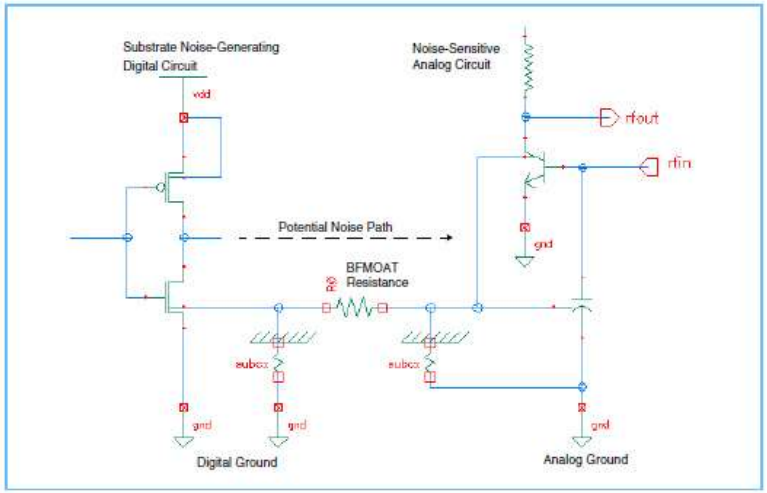



*Figure 17. Circuit Simulation with Isolation Impedance and Separate Grounds between Noise-Generating and Noise-Sensitive Circuits*




Foundry Application Note
**Substrate Isolation in IBM BiCMOS and CMOS RF Technologies**

*Figure 18. Ideal Layout of Circuit Blocks with an Isolation Moat and Separate Grounds*

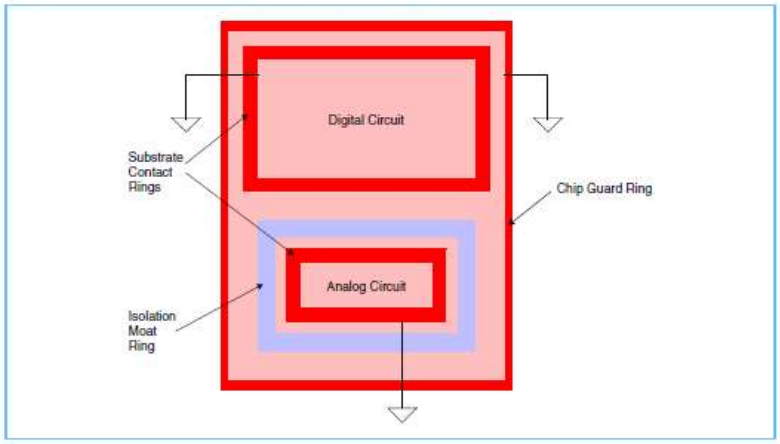
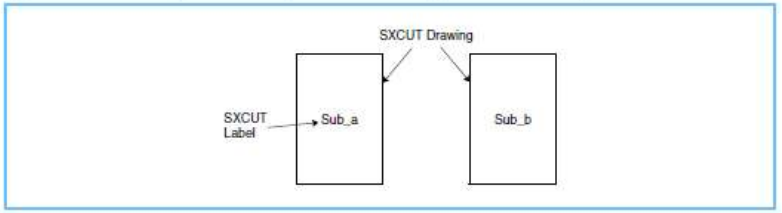
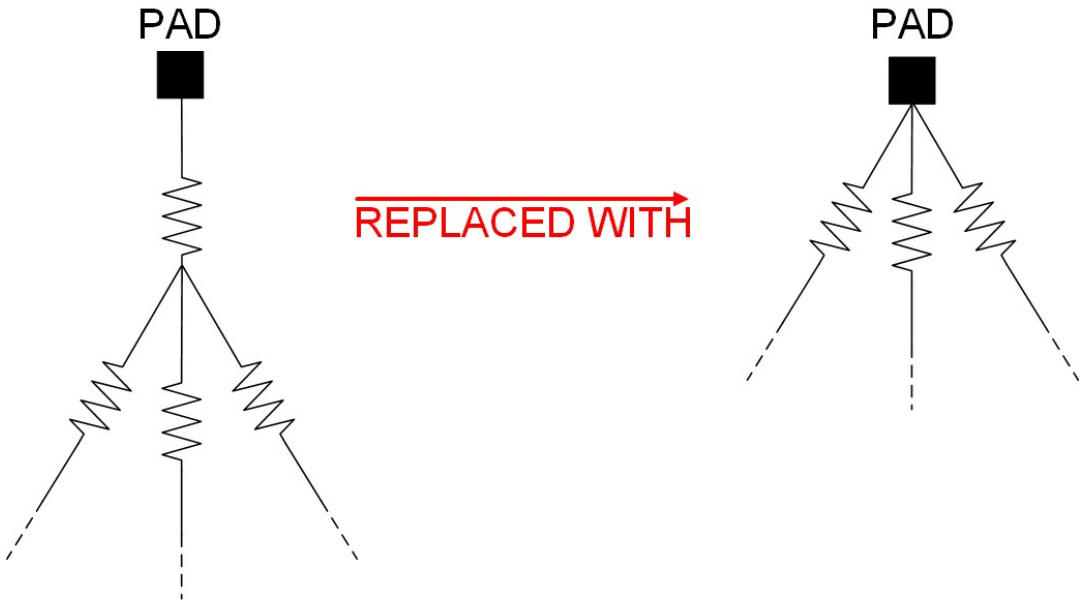



*Figure 19. Substrate Regions Defined by the SXCUT Drawing Level and Named by the SXCUT Label*



# Substrate Noise
## Layout Approach (2/2)

- Layout Level
  - Supplies/Grounds Isolation
    - *Guard Rings* and *BFMOAT*
  - Routing Improvement



# Substrate Noise

## Intermediate Result

- PEX Transient Simulation with an improved version of the new CSPreamp
  - Better sensitivity (~0.94mV/fC) and ENC (~0.85fC)

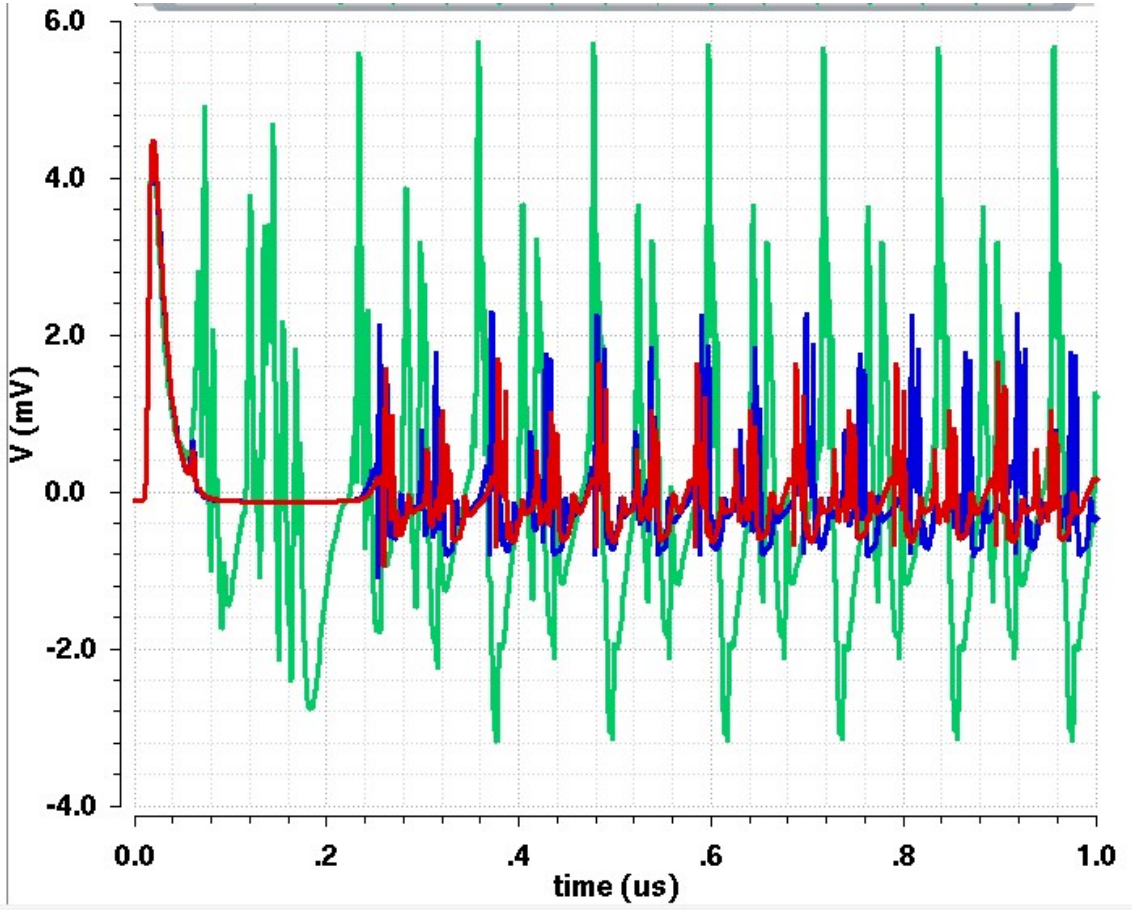



Fig. 4 - CSPreamp Output @ $Q_{IN}$=5fC

# Substrate Noise

## PEX Transient Noise Simulation Results

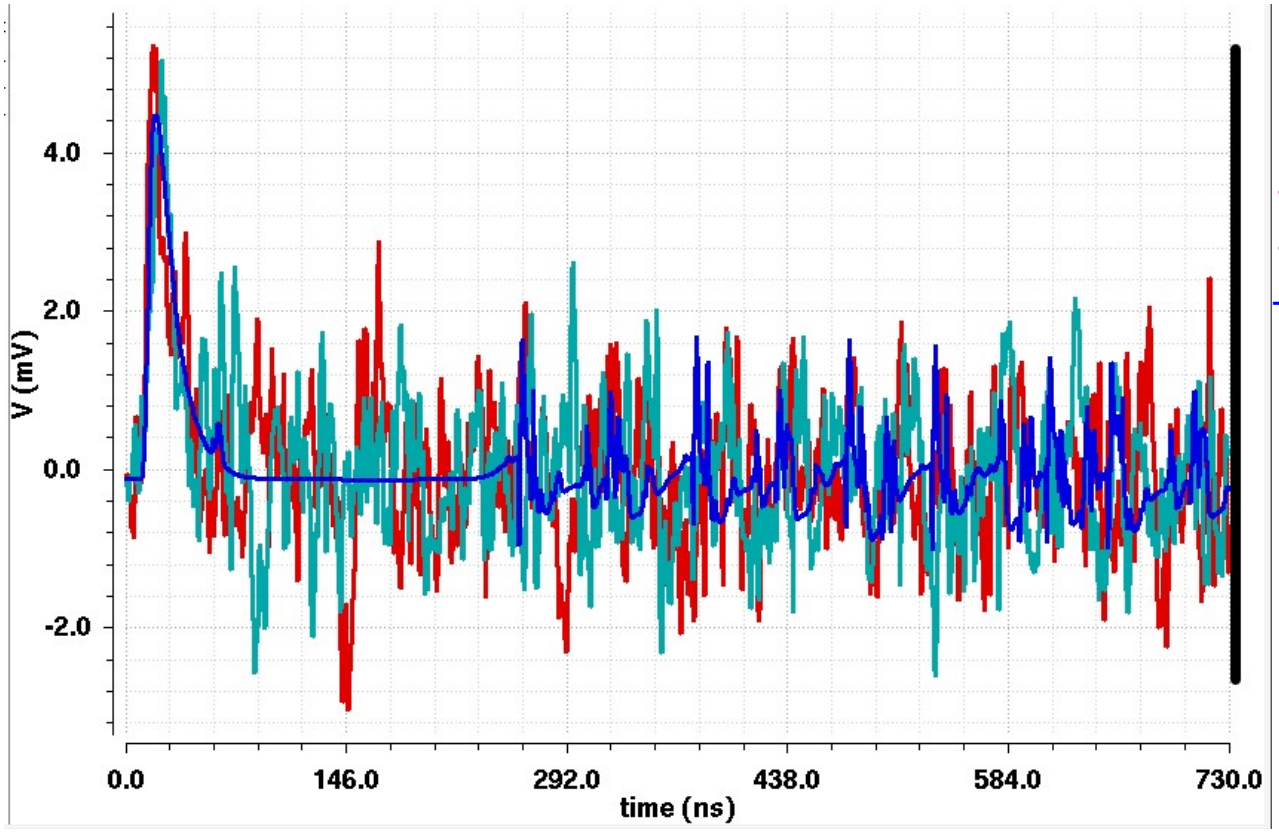


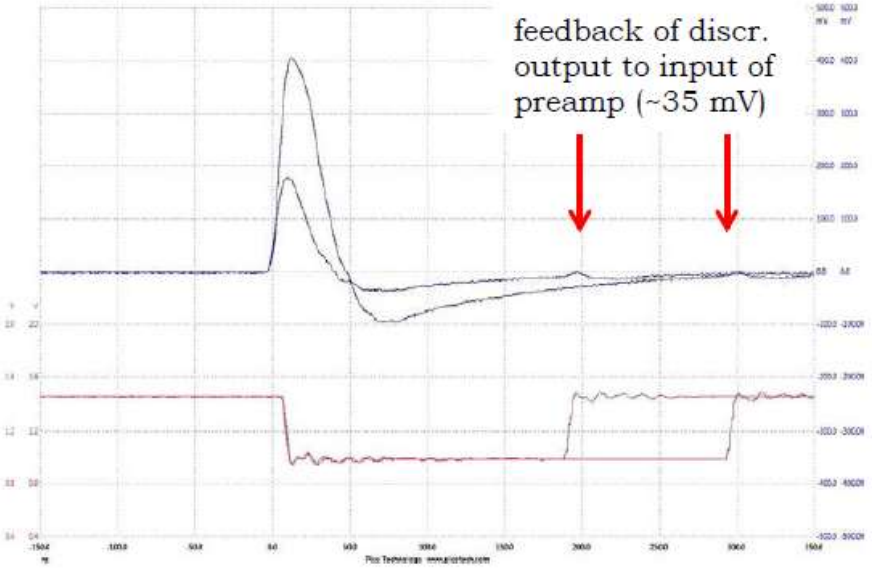

Fig. 5 - CSPreamp Output @ $Q_{IN}$=5fC

- The effort for disturbance mitigation is vanished by noise presence

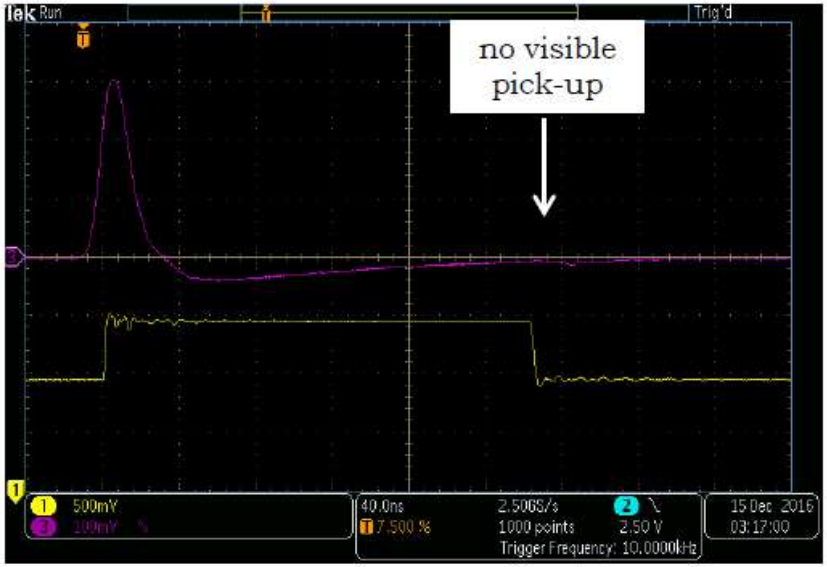
# Substrate Noise

## CSPreamp Performance Summary

| Specification@CSPreamp Output | MDT-ASD User Manual 2002-03 | ASD_V4 | ASD_V5 |
|---|---|---|---|
| Sensitivity | 0.93mV/fC | 0.74mV/fC | 0.94mV/fC |
| ENC | 6000 $e^-_{rms}$ → 0.96fC | 0.86fC | 0.85fC |
| RMS noise | 0.89$mV_{RMS}$ | 0.64$mV_{RMS}$ | 0.8$mV_{RMS}$ |
| Peaking Time Delay @ CSPreamp Output | - | 8.8ns | 8.7ns |
| CSPreamp Voltage Peak @$Q_{IN}$=5fC | 4.65mV | 3.7mV | 4.7mV |
| -3dB Bandwidth | 11.94MHz | 11MHz | 16.7MHz |




ASD_Vs_4




peak amplitude 300 mV, peaking time ~ 12 ns

ASD_Vs_5

**Fig. 6 - MPI Measurements Comparison.**

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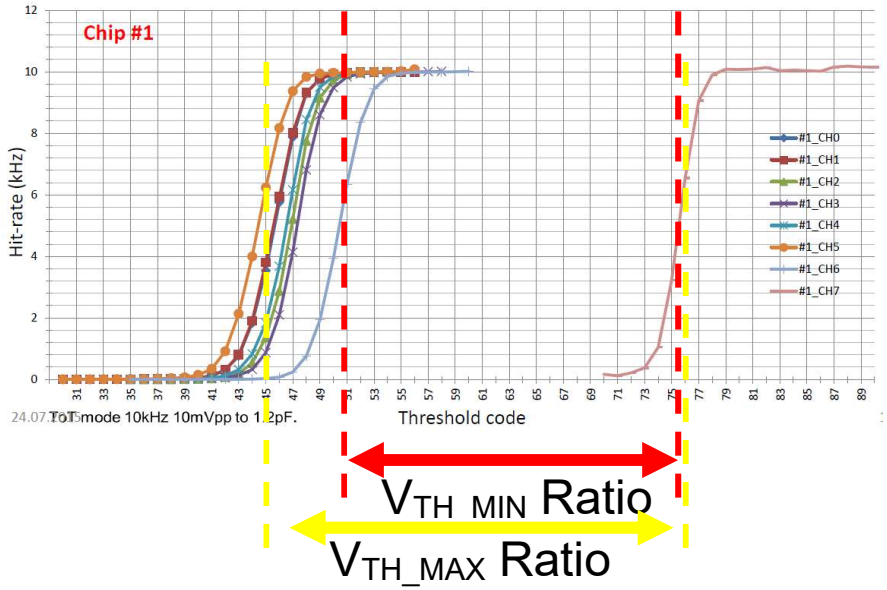
# CHANNEL Mismatch
## Introduction

- CH7 affected by buffer connection
  - Longer and more thick wires
  - Parasitic capacitances (≈1.5pF) greater than gate capacitances

- DA3 output:
  - Amplitude reduction of 1.7 factor
  - Peaking Time Delay increment of 1.3 factor
  - Noise reduction of 1.47 factor

- Measurements
  - $V_{TH\_MIN}$ ratio → around 1.4
  - $V_{TH\_MAX}$ ratio → around 1.65



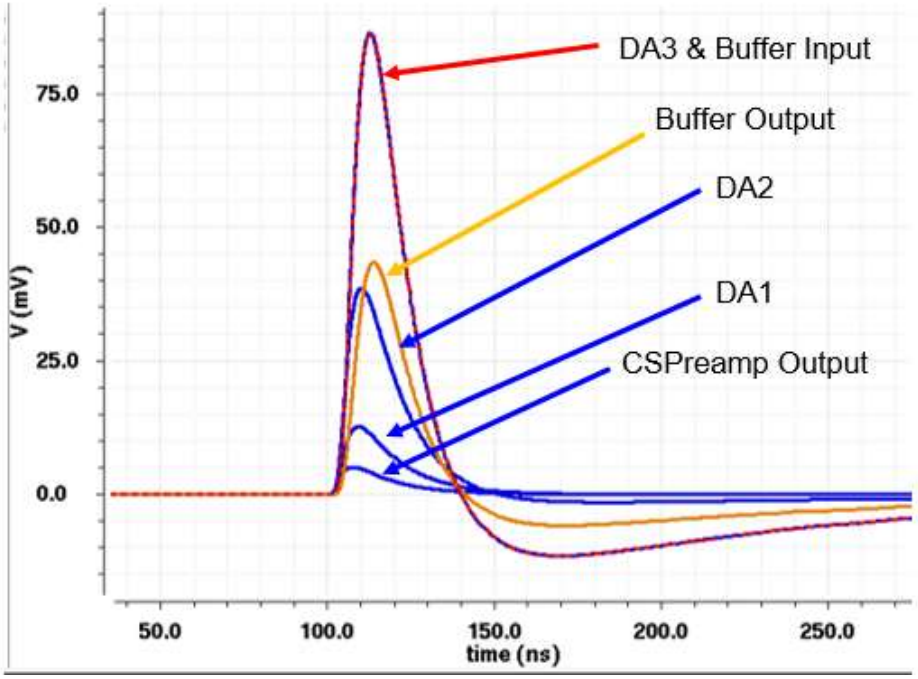
# CHANNEL Mismatch

## Solution

- Layout Modification
  - Parasitic capacitances decrement
    - Closer DA3 and Buffer
    - Shorter wires
    - Less width wires

- **Switches** to disconnect the buffer

- Schematic Transient simulations



# CHANNEL Mismatch

## PVT Schematic Transient Results

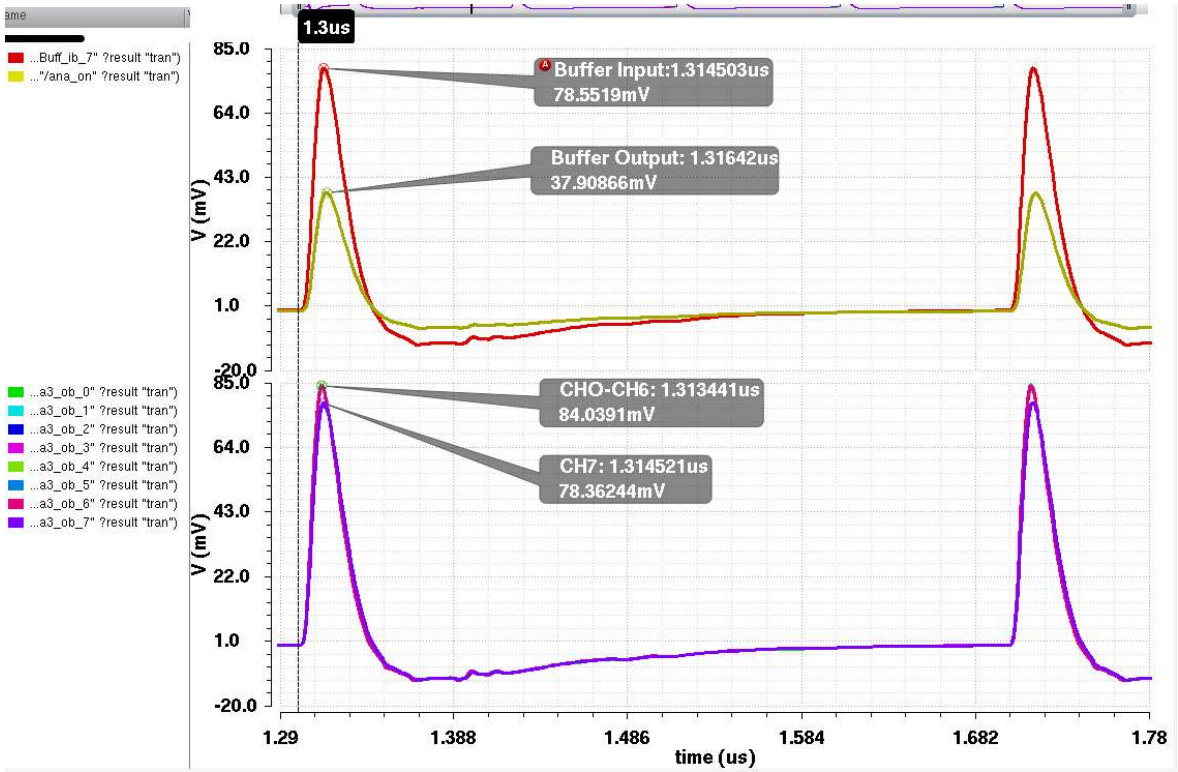
| Parameters | Units | CHANNEL V5 | | |
|---|---|---|---|---|
| | | Nominal | PVT | |
| | | | min | max |
| Peak Voltage Preamp | mV | 5.042 | 4.43 | 5.291 |
| Peaking Time Preamp | ns | 7.68 | 6.448 | 9.945 |
| Peak Voltage DA1 | mV | 12.66 | 9.936 | 15.17 |
| Peaking Time DA1 | ns | 9.252 | 7.905 | 11.61 |
| Peak Voltage DA2 | mV | 38.57 | 27.61 | 49.4 |
| Peaking Time DA2 | ns | 10.18 | 8.751 | 12.64 |
| Peak Voltage DA3 | mV | 86.3 | 58.23 | 116.1 |
| Peaking Time DA3 | ns | 12.79 | 11.13 | 15.24 |
| Peak Voltage Buffer Input | mV | 86.57 | 58.53 | 116.3 |
| Peaking Time Buffer Input | ns | 12.79 | 11.13 | 15.41 |
| Peak Voltage Buffer Output | mV | 43.42 | 21.48 | 64.79 |
| Peaking Time Buffer Output | ns | 13.89 | 11.84 | 16.71 |

- Including switches to disconnect the buffer

# CHANNEL Mismatch

## Buffer ON – DA3 Signal

- Transient Simulations
  - With Buffer
  - Without Buffer
- Buffer ON
- Minimum Input Charge
- Calibre Extracted
- DA3 Output Signals

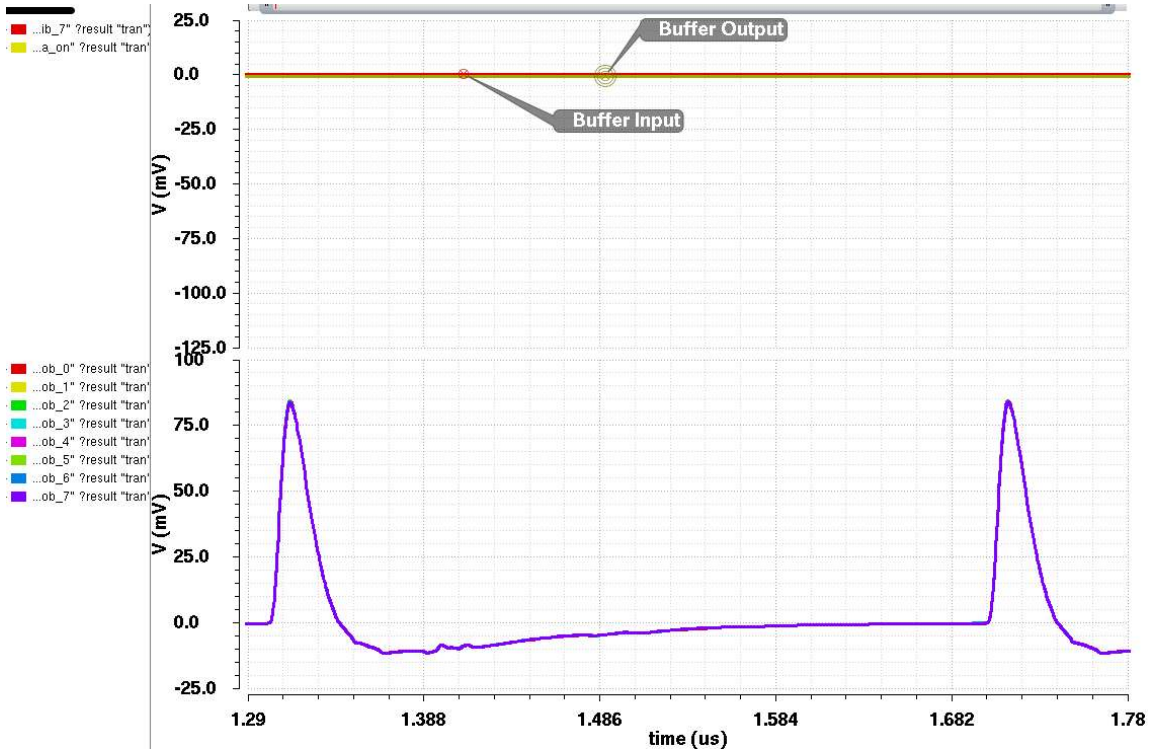



| | Peak Voltage | Peaking Time |
|---|---|---|
| DA3 Output of CH0-CH6 | 84mV | 13.4ns |
| DA3 Output of CH7 | 78.36mV | 14.5ns |
| Buffer Input | 78.55mV | 14.5ns |
| Buffer Output | 37.9mV | 16.4ns |

# CHANNEL Mismatch

## Buffer OFF – DA3 Signal

- Transient Simulations
  - With Buffer
  - Without Buffer
- Buffer OFF
- Minimum Input Charge
- Calibre Extracted
- DA3 Output Signals

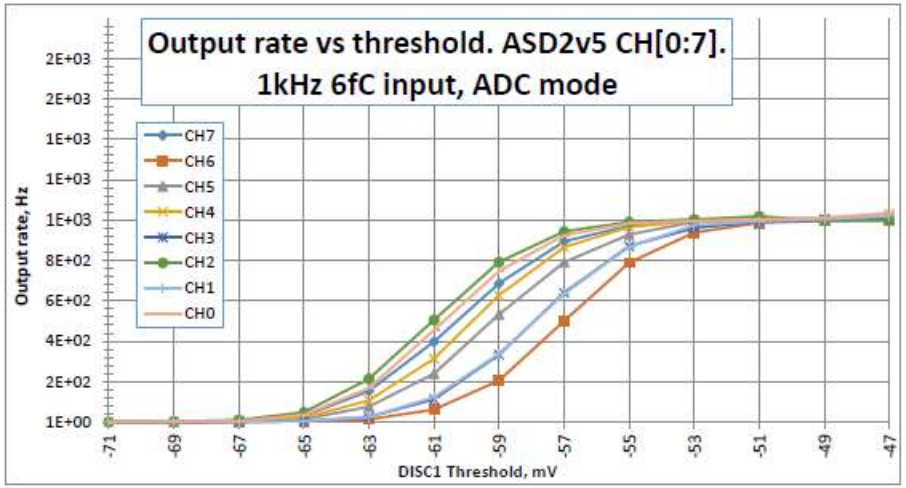



| | Peak Voltage | Peaking Time |
|---|---|---|
| DA3 Output of CH0-CH7 | 84 mV | 13.4 ns |
| Buffer Input | 0 mV | - |
| Buffer Output | 0 mV | - |

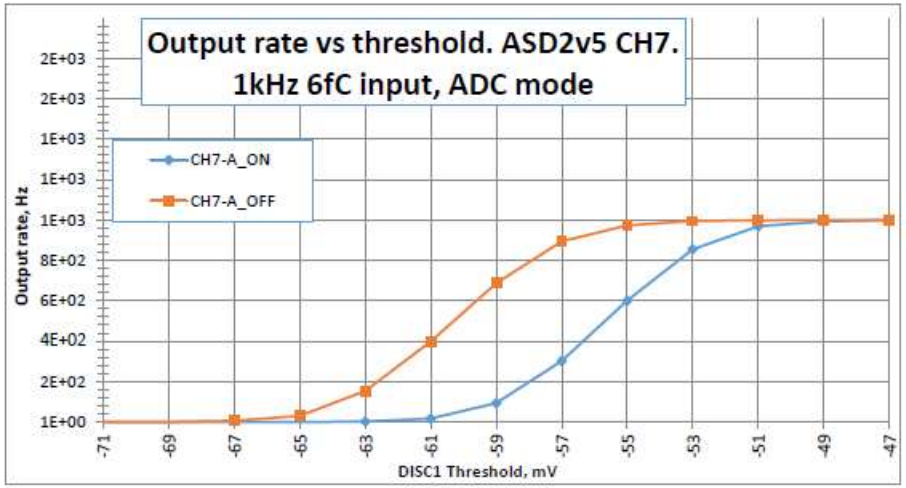
# CHANNEL Mismatch

## MPI Measurements

2. The spread of internal offset of channels is extremely low – 4mV. Channel 7 is in range with other channels.




3. Enabling analog output on channel 7 adds very little load – effectively shifting threshold by 5mV



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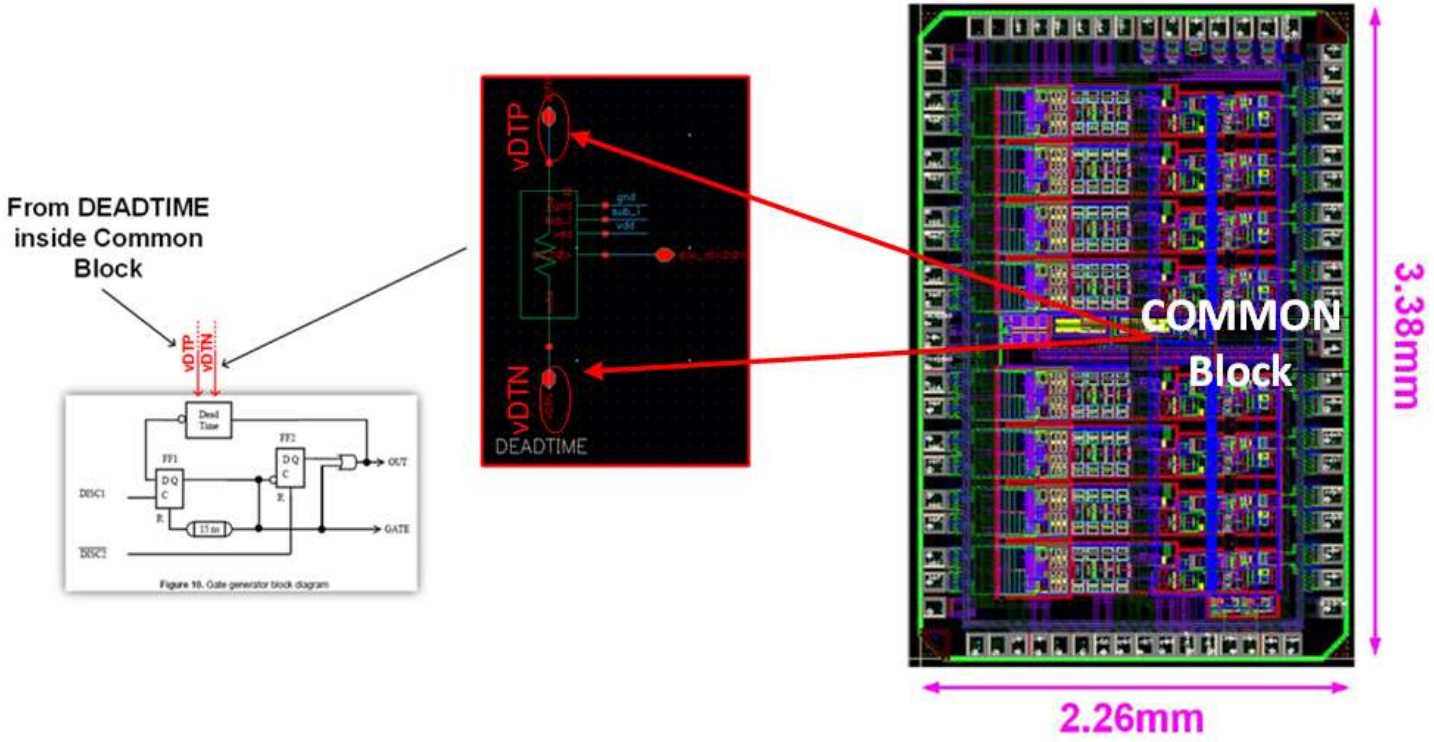
# DeadTime Issue

## Introduction




- DeadTime is proportional to ΔV=vDTP-vDTN=R•I
  - → proportional to a current (I)
- Each Channel has a Phase Generator Block with 2 voltages coming from Common Block (vDTP and vDTN)
- The Distance between each Channel and Common Block is variable
  - Mismatch between two different channels in terms of
    - Current
    - DeadTime

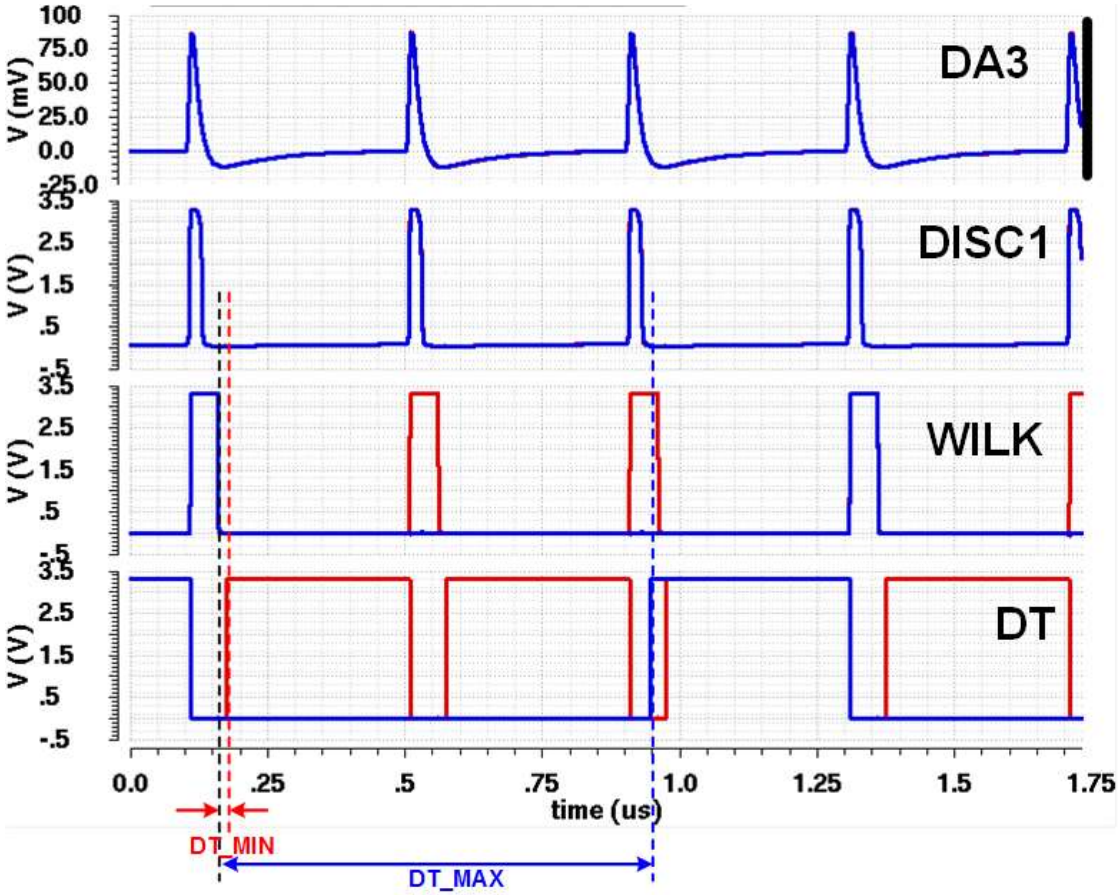
# DeadTime Issue

## Solution – SCH. Simulation

- LOCAL DeadTime Generation

| PARAMETER | VALUES |
|---|---|
| Hysteresys | 0 |
| Threshold2 | 7 |
| Threshold1 | 118 → -19mV |
| Integration Gate | 8 |
| Rundown Code | 4 |
| DeadTime | 0 - 7 |
| Input Charge | 5fC |
| Period Input Charge | 400ns |

| Word Codes | Values |
|---|---|
| **0** | **13.77ns** |
| 1 | 148.1ns |
| 2 | 263.4ns |
| 3 | 372.8ns |
| 4 | 479ns |
| 5 | 582.7ns |
| 6 | 684.5ns |
| **7** | **784.9ns** |



# DeadTime Issue

## PT Simulations

PT simulations with

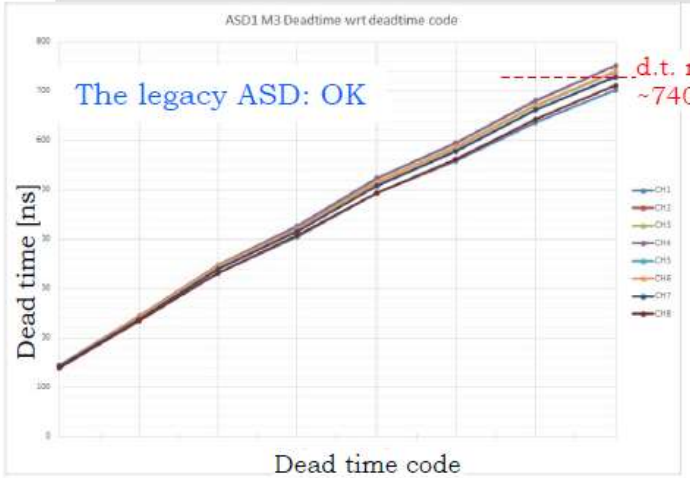
- Process variation (ss, sf, fs, ff, tt)
- Temperature variation (-40°, 27°, 120°)
- Maximum and Minimum DeadTime Codes

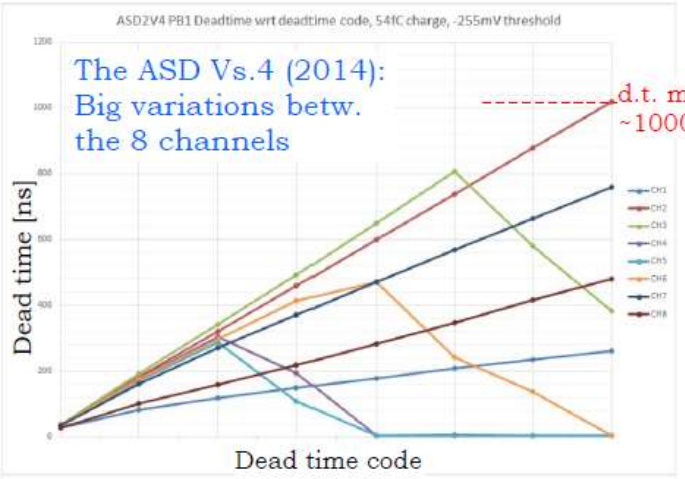
| Word Codes | Nominal Values | Process / Temperature | |
|---|---|---|---|
| | | Min. Values | Max. Values |
| 0 | 13.77ns | 9.609ns | 20.19ns |
| 1 | 148.1ns | - | - |
| 2 | 263.4ns | - | - |
| 3 | 372.8ns | - | - |
| 4 | 479ns | - | - |
| 5 | 582.7ns | - | - |
| 6 | 684.5ns | - | - |
| 7 | 784.9ns | 732.3ns | 839.2ns |

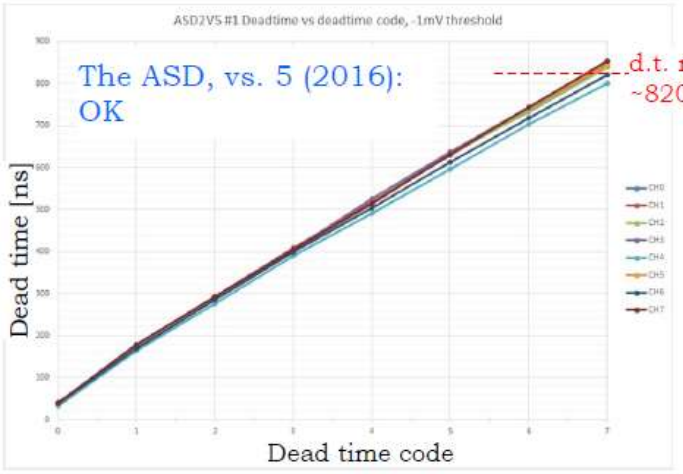
# DeadTime Issue

## MPI Measurements

### Dead time vs. dead time code: fixed




Similar behaviour of the ADC reading (trailing-leading edge) vs. run-down current code

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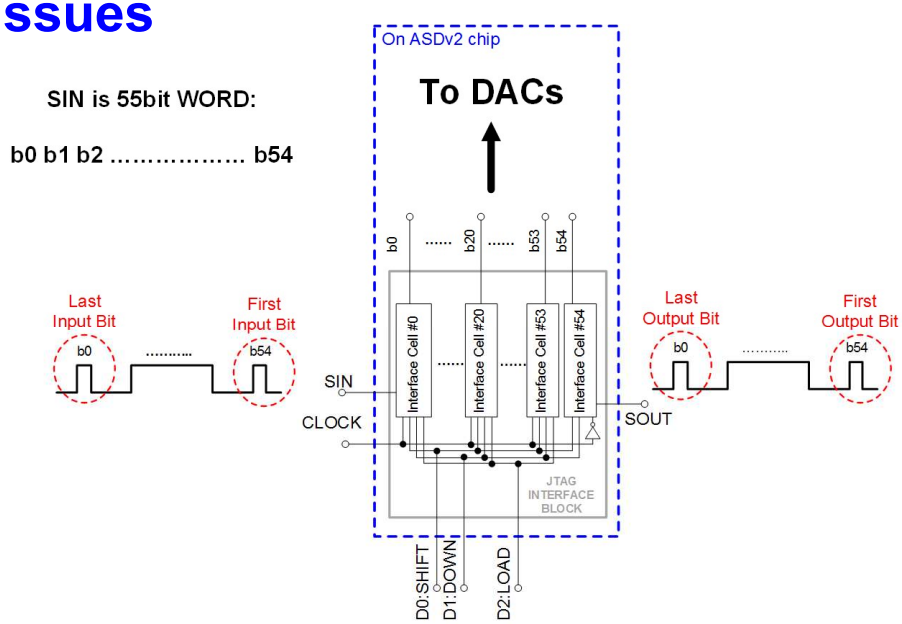
# JTAG Serial Data Interface

## Version5 Issues

- Hysteresis bit setting
  - Once ‘1111’ word code is set
    - Problem with the reset to ‘0000’
    - Chip Switch OFF is necessary

- ASD2v6 JTAG Interface:
  - Same Interface Cells for each Bit
  - DACs interface optimization

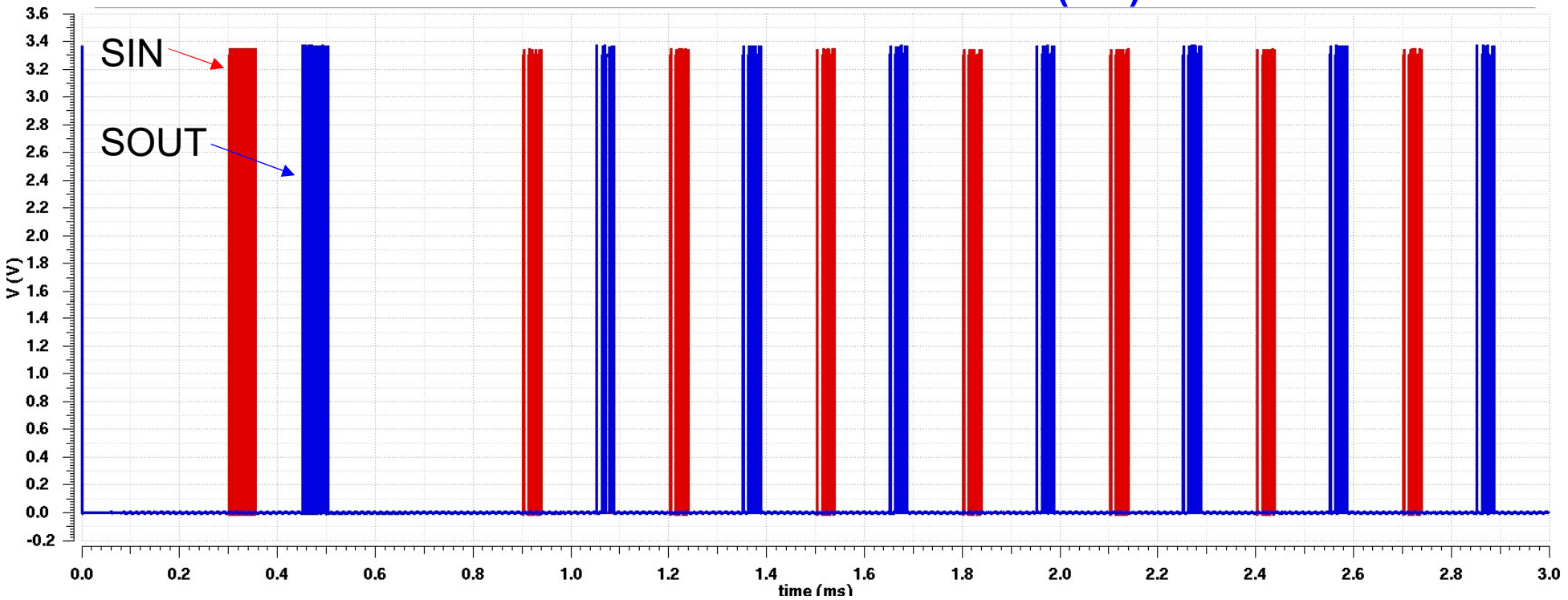



| CASE1 | |
|---|---|
| INPUT WORD CODE | OUTPUT WORD CODE |
| 1111 | 1111 ☺ |
| 0000 | 1111 ☹ |
| 0110 | 1111 ☹ |
| 1111 | 1111 ☺ |
| 0000 | 1111 ☹ |
| 0110 | 1111 ☹ |

| CASE2 | |
|---|---|
| INPUT WORD CODE | OUTPUT WORD CODE |
| 0000 | 0000 ☺ |
| 0000 | 0001 ☹ |
| 0110 | 0111 ☹ |
| 1111 | 1111 ☺ |
| 0000 | 1111 ☹ |
| 0110 | 1111 ☹ |

# JTAG Serial Data Interface

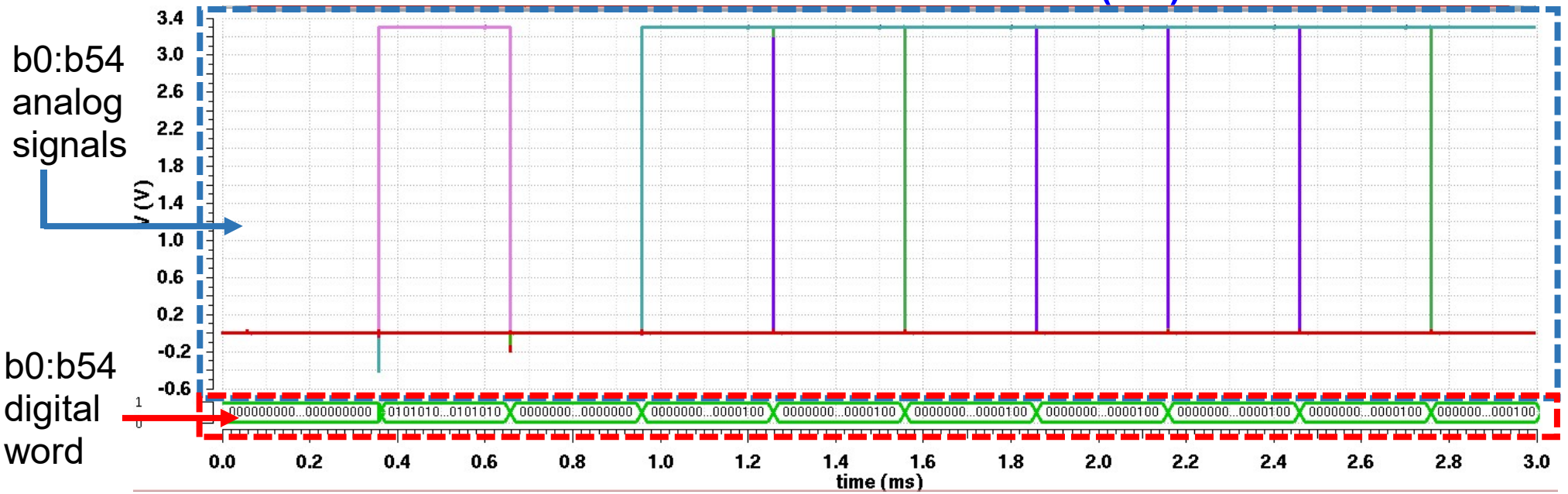
## Schematic Simulation Results (1/2)




- JTAG Interface V6
  - SOUT signal is delayed SIN one
  - Input and Ouput signals are the same ☺

# JTAG Serial Data Interface

## Schematic Simulation Results (2/2)




- 10 different word codes (shown in next slide) have been used as input
  - All words are correct
  - All words are received correctly by DACs
  - Fan-out problem for hysteresis bits have been solved
    - Problem resulting in the replacement of the custom interfaces with standard ones
      - → Input of hysteresis block has been optimitazed

# JTAG Serial Data Interface

## Transmitted Word Codes

| # | [b0:b15] | [b16] | [b17:b19] | [b20:b23] | [b24:b26] | [b27:b30] | [b31:b33] | [b34:b41] | [b42:b54] |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0000000000000000 | 0 | 000 | 0000 | 000 | 0000 | 000 | 00000000 | 0000000000000 |
| 2 | 0101010101010101 | 0 | 101 | 0101 | 010 | 1010 | 101 | 01010101 | 0101010101010 |
| 3 | 0000000000000000 | 0 | 000 | 0000 | 000 | 0000 | 000 | 00000000 | 0000000000000 |
| 4 | 0000000000000000 | 0 | 111 | 0111 | 110 | 1111 | 111 | 01111011 | 0000000000100 |
| 5 | 0000000000000000 | 0 | 111 | 0111 | 110 | 1001 | 111 | 01111011 | 0000000000100 |
| 6 | 0000000000000000 | 0 | 111 | 0111 | 110 | 0110 | 111 | 01111011 | 0000000000100 |
| 7 | 0000000000000000 | 0 | 111 | 0111 | 110 | 0000 | 111 | 01111011 | 0000000000100 |
| 8 | 0000000000000000 | 0 | 111 | 0111 | 110 | 1010 | 111 | 01111011 | 0000000000100 |
| 9 | 0000000000000000 | 0 | 111 | 0111 | 110 | 1000 | 111 | 01111011 | 0000000000100 |
| 10 | 0000000000000000 | 0 | 111 | 0111 | 110 | 0001 | 111 | 01111011 | 0000000000100 |
| | ↓ Channel Mode (CH0-CH7) | ↓ Chip Mode | ↓ DeadTime | ↓ Wilkinson ADC Integration Gate | ↓ Wilkinson ADC Rundown Current | ↓ Hysteresis DAC (DISC1) | ↓ Wilkinson ADC Threshold DAC (DISC2) | ↓ Main Threshold DAC (DISC1) | ↓ No Used |

- Correct trasmission of all the word codes
- Hysteresis bits NOT AFFECT by ‘1111’ setting

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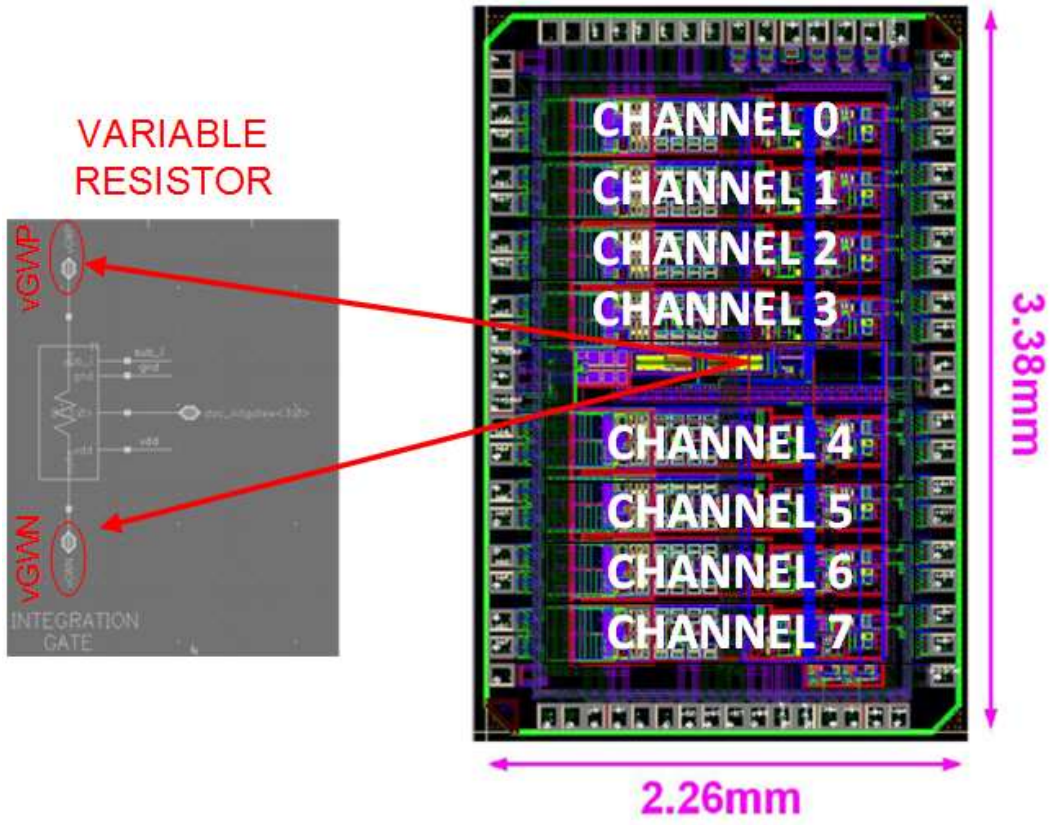
# IntegrationGate Uniformity

## Version5 Issue

- One variable resistor shared between the 8 Channels
- Integration gate width generation through a current $I_{INT\_GATE}$

$$I_{INT\_GATE} = \frac{vGWP - vGWN}{R_{INT\_GATE}}$$



# IntegrationGate Uniformity
## Version5 Solution

- One variable resistor for each channel has been inserted
  - ***Local*** Integration Gate ***generation***

- Integration gate width generation through a current $I_{INT\_GATE}$

$$I_{INT\_GATE} = \frac{vGWP - vGWN}{R_{INT\_GATE}}$$

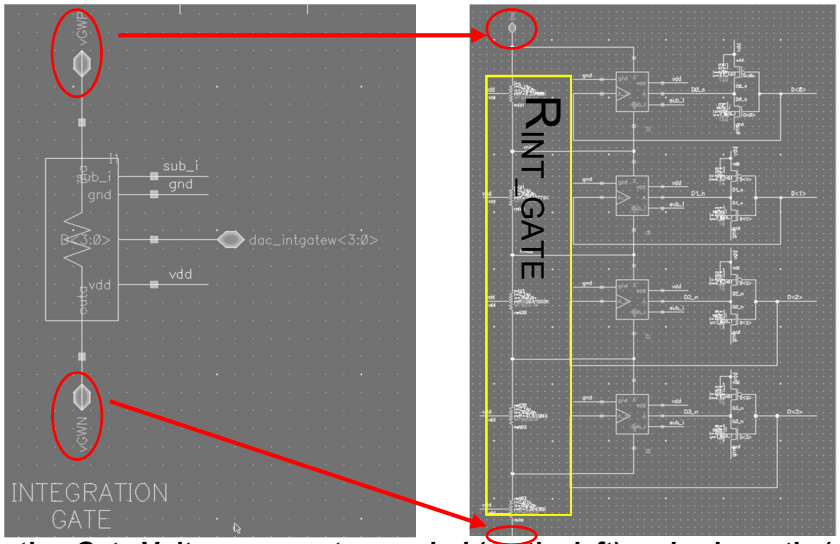
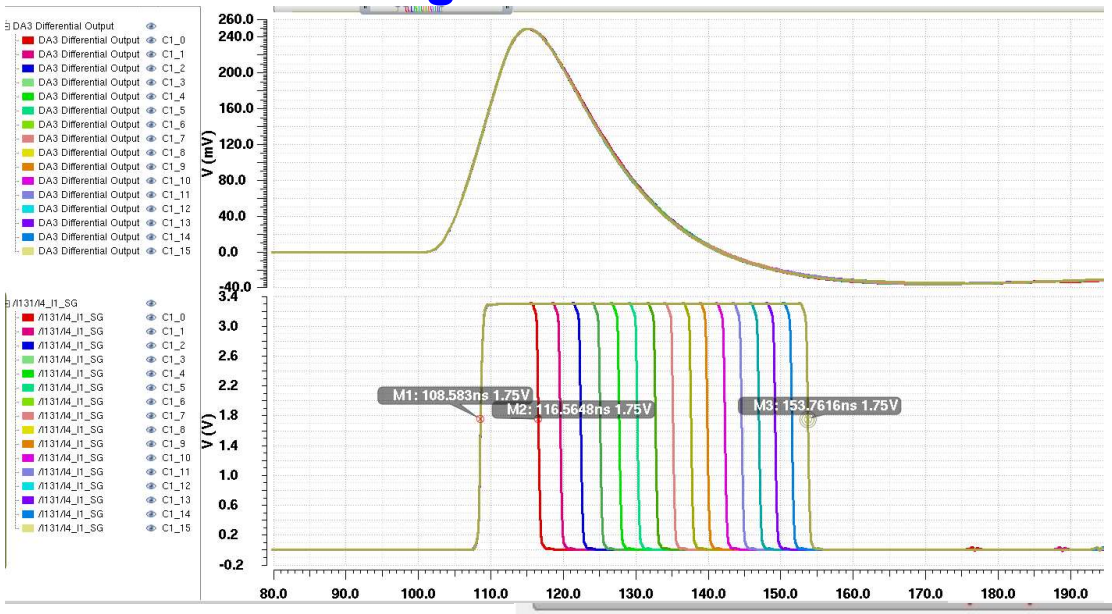



**Fig. 7 - Integration Gate Voltage generator symbol (on the left) and schematic (on the rigth).**

# IntegrationGate Uniformity

## PEX Integration Gate Width




- 16 transient post-layout simulations
- User MDT Manual specification:
  - Range:  8ns – 45ns
  - LSB: ~2.5ns
  - Resolution: 4 bits

| Corner | dintgate0 | dintgate1 | dintgate2 | dintgate3 | PEX_integration_width |
|---|---|---|---|---|---|
| C1_0 | 0 | 0 | 0 | 0 | 8.015n |
| C1_1 | 1 | 0 | 0 | 0 | 11.03n |
| C1_2 | 0 | 1 | 0 | 0 | 13.86n |
| C1_3 | 1 | 1 | 0 | 0 | 16.53n |
| C1_4 | 0 | 0 | 1 | 0 | 19.17n |
| C1_5 | 1 | 0 | 1 | 0 | 21.67n |
| C1_6 | 0 | 1 | 1 | 0 | 24.17n |
| C1_7 | 1 | 1 | 1 | 0 | 26.59n |
| C1_8 | 0 | 0 | 0 | 1 | 29.08n |
| C1_9 | 1 | 0 | 0 | 1 | 31.32n |
| C1_10 | 0 | 1 | 0 | 1 | 33.75n |
| C1_11 | 1 | 1 | 0 | 1 | 36.06n |
| C1_12 | 0 | 0 | 1 | 1 | 38.45n |
| C1_13 | 1 | 0 | 1 | 1 | 40.69n |
| C1_14 | 0 | 1 | 1 | 1 | 42.99n |
| C1_15 | 1 | 1 | 1 | 1 | 45.21n |

# DESIGN REVIEW

## Outline

- ASDv4 Fixing Activities
  - Substrate Noise
  - Channel Mismatch
  - Deadtime
- ASDv5 Issues
  - Jtag Serial Data Interface
  - Integration Gate ←←←
- New CSPreamp

# New CSPreamp

## CSPreamp_V5 Cadence Scheme

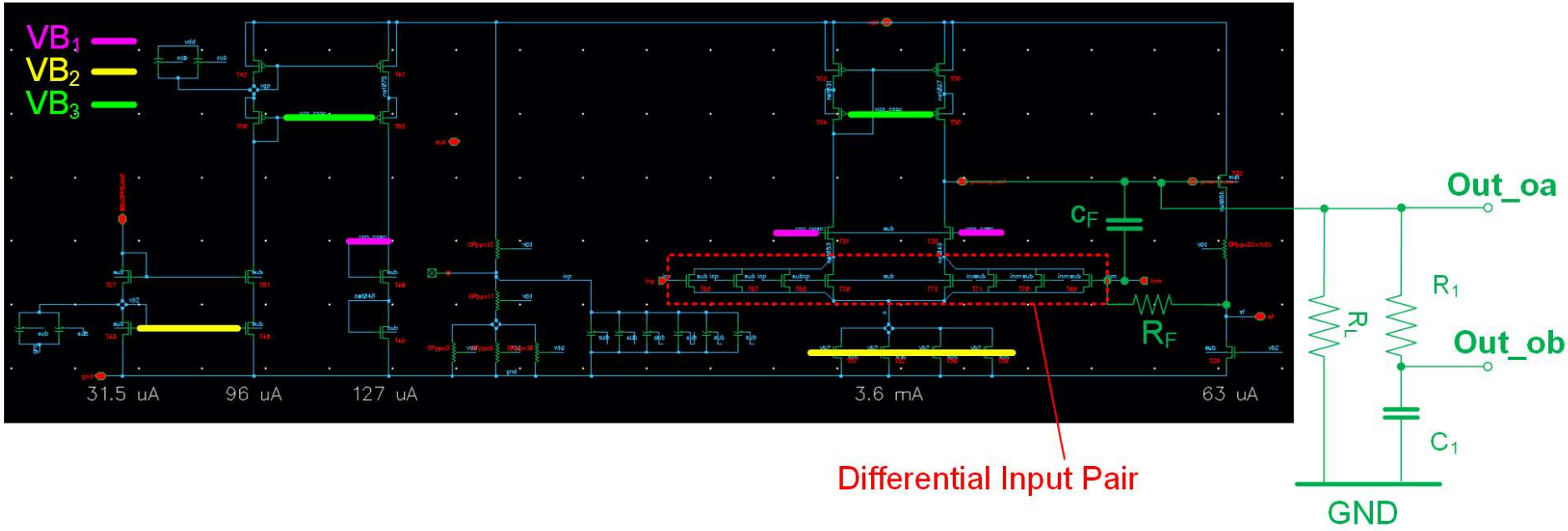



**Fig. 8 – CSPreamp Cadence Scheme.**

# New CSPreamp

## CSPreamp_V5 Scheme (1/2)

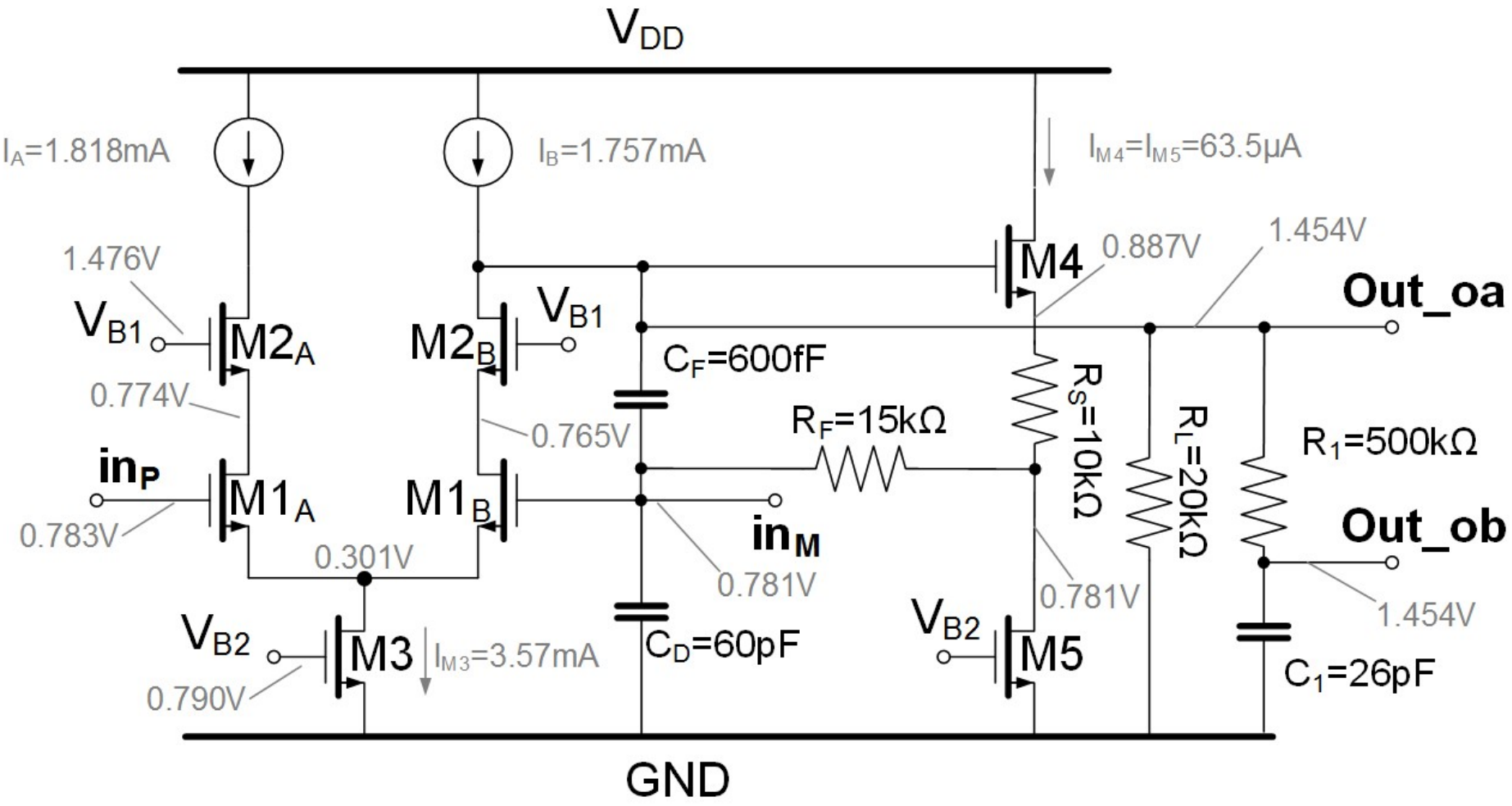



**Fig. 9 – CSPreamp Fully Differential Transistor Level Scheme.**

# New CSPreamp

## CSPreamp_V5 Scheme (2/2)

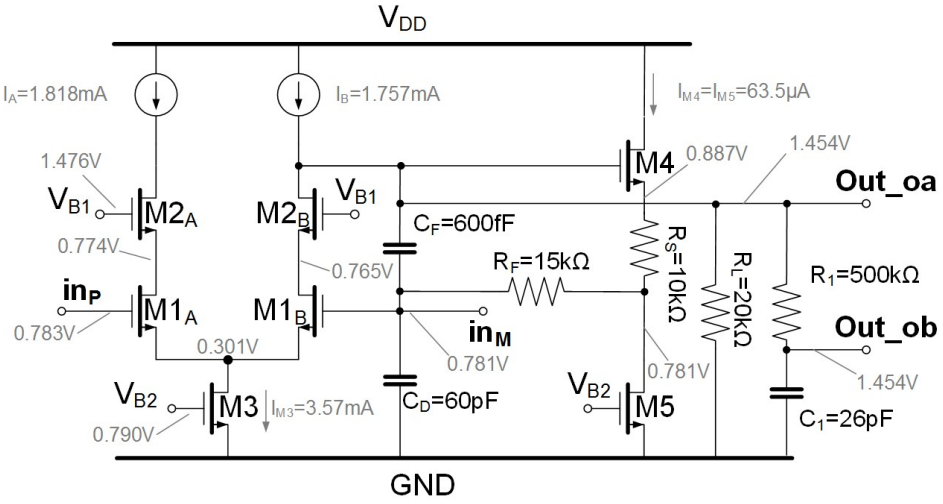



Fig. 10 – CSPreamp Transistor Level Scheme.

| MOS | W/L | $g_m$ [mA/V] | $r_{DS}$ [kΩ] |
|---|---|---|---|
| $M1_A$ | 2mm/400nm | 34.36 | 1.03 |
| $M1_B$ | 2mm/400nm | 33.36 | 0.978 |
| $M2_A$ | 150µm/400nm | 17.38 | 3.14 |
| $M2_B$ | 150µm/400nm | 16.74 | 2 |
| M3 | 928µm/3µm | 18.41 | 505.7 |
| M4 | 80µm/500nm | 1.187 | 118 |
| M5 | 16µm/3µm | 0.348 | 1.22 |

- Current Consumption → 3.94mA
- **Power Consumption** @ 3.3V of Supply Voltage → **13mW**
- DC Open Loop *Gain*
  - $20 \cdot log_{10}\left(gm_{M1_B} \cdot R_{OUT}\right) = 20 \cdot log_{10}\left(gm_{M1_B} \cdot \left(R_L \parallel R_{M2_B - M1_B} \parallel R_{I_B}\right)\right) \cong 50dB$
  - With
    - $R_L = 20k\Omega$
    - $R_{M2_B - M1_B} = gm_{M2_B} \cdot r_{DS_{M2B}} \cdot r_{DS_{M1B}} \cong 32.7k\Omega$
    - $R_{I_B} \cong 46.3\text{k}\Omega$

# New CSPreamp

## CSPreamp_V5 Responses

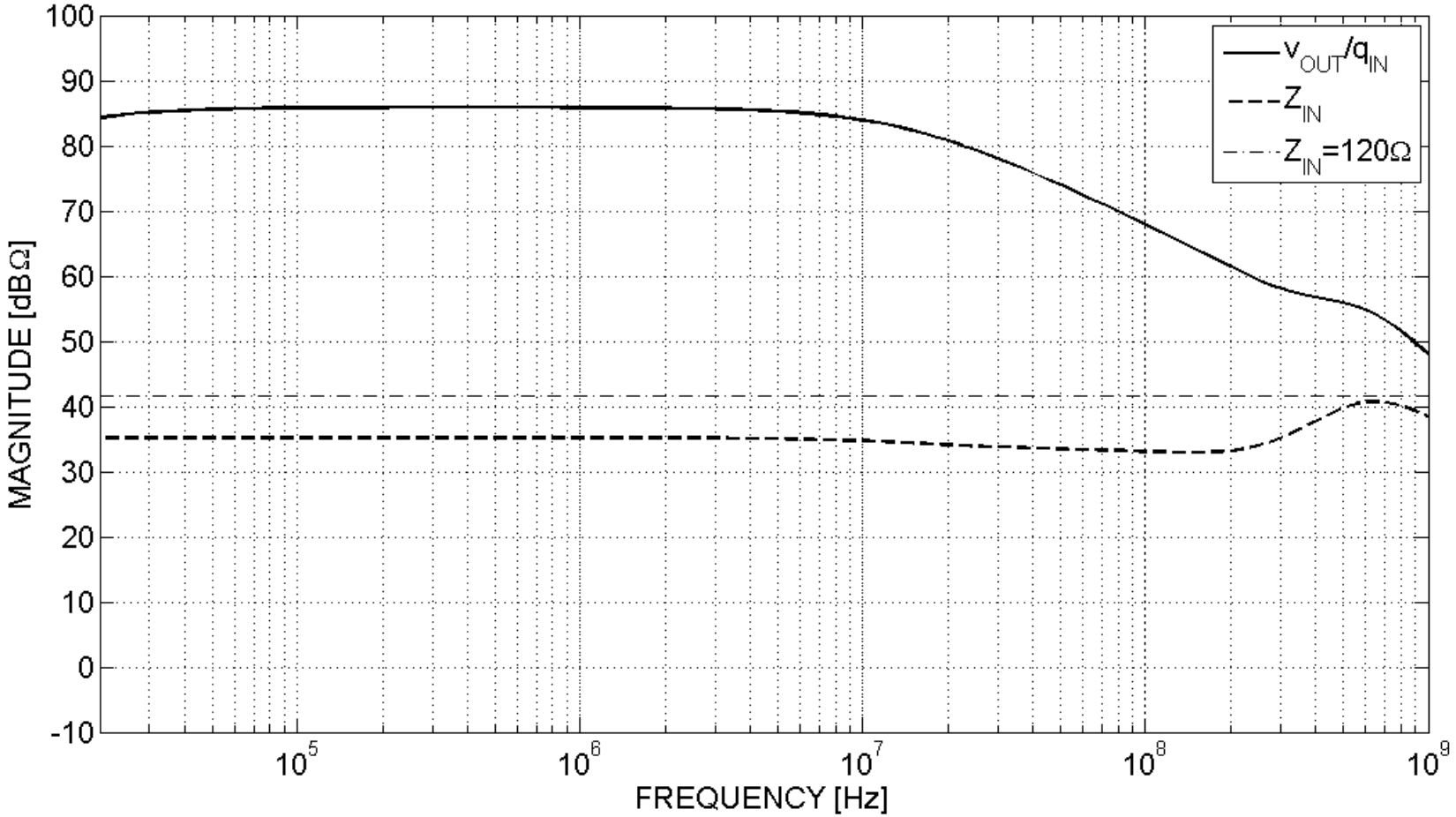



**Fig. 11 – $v_{OUT}/q_{IN}$ and $Z_{IN}$ (Input Impedance) Frequency Responses.**

# New CSPreamp

## CSPreamp_V5 Loop Gain Frequency Response

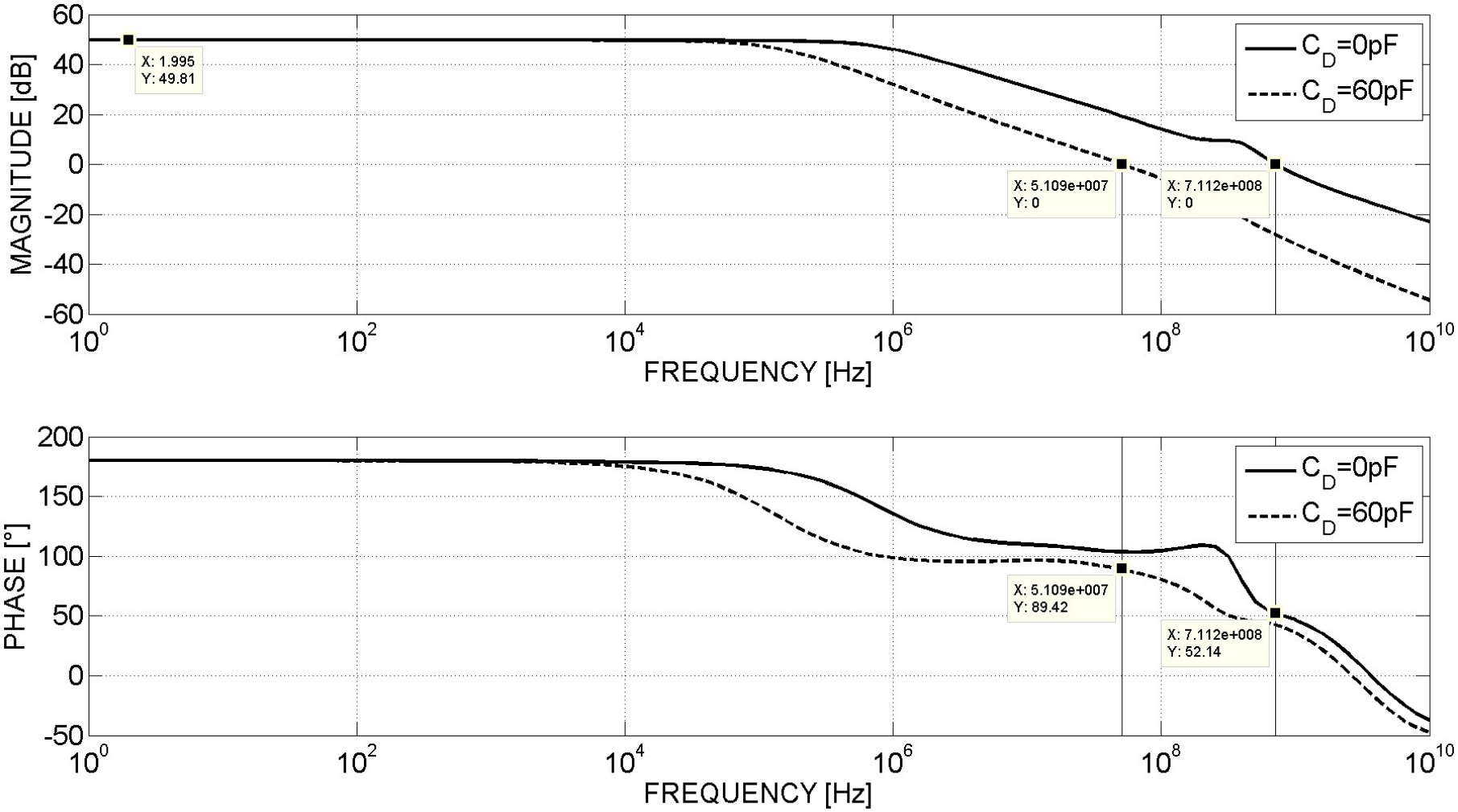



**Fig. 12 – CSPreamp Loop Gain Frequency Response.**

# New CSPreamp

## CSPreamp_V5 PSRR

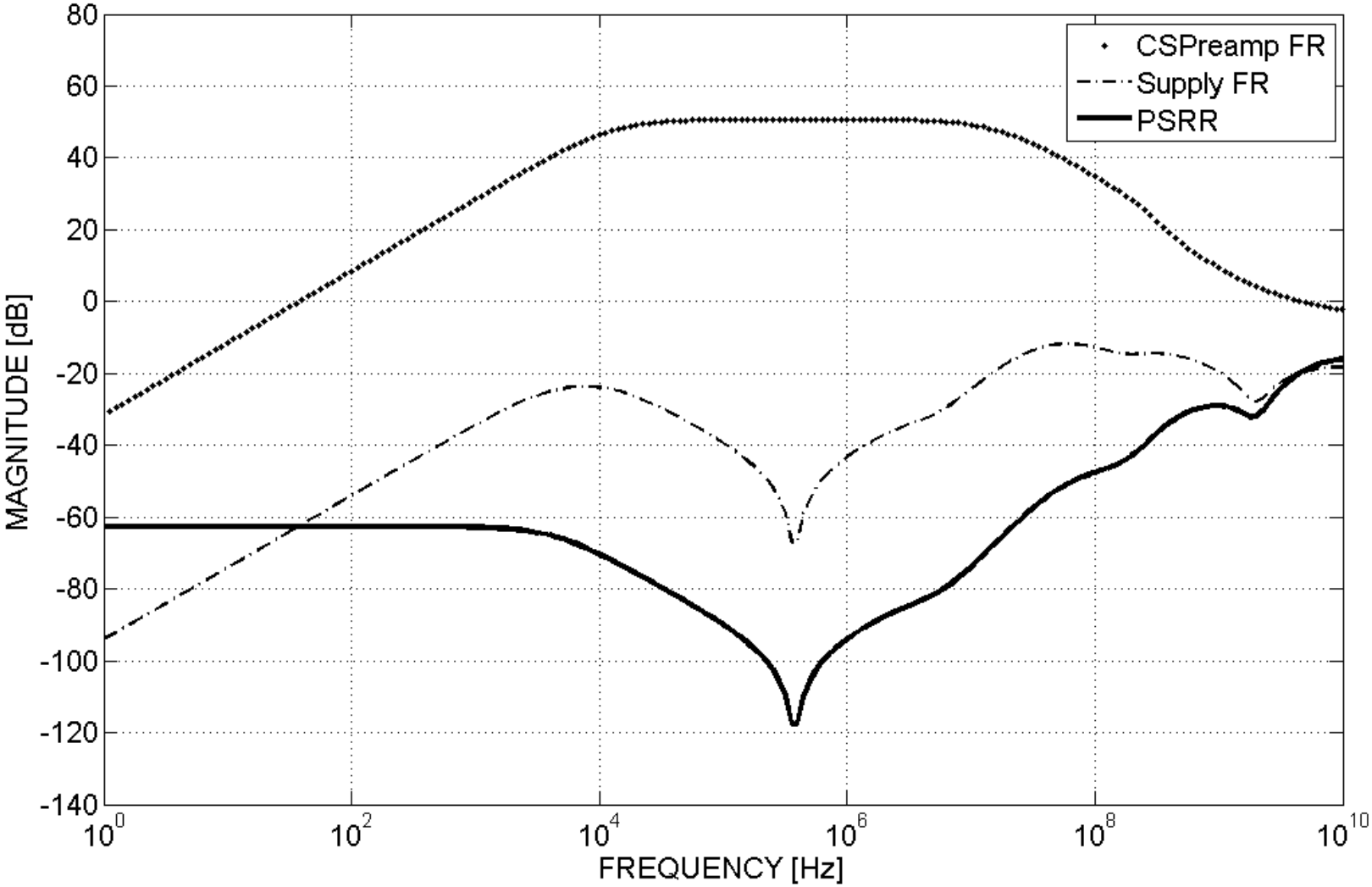
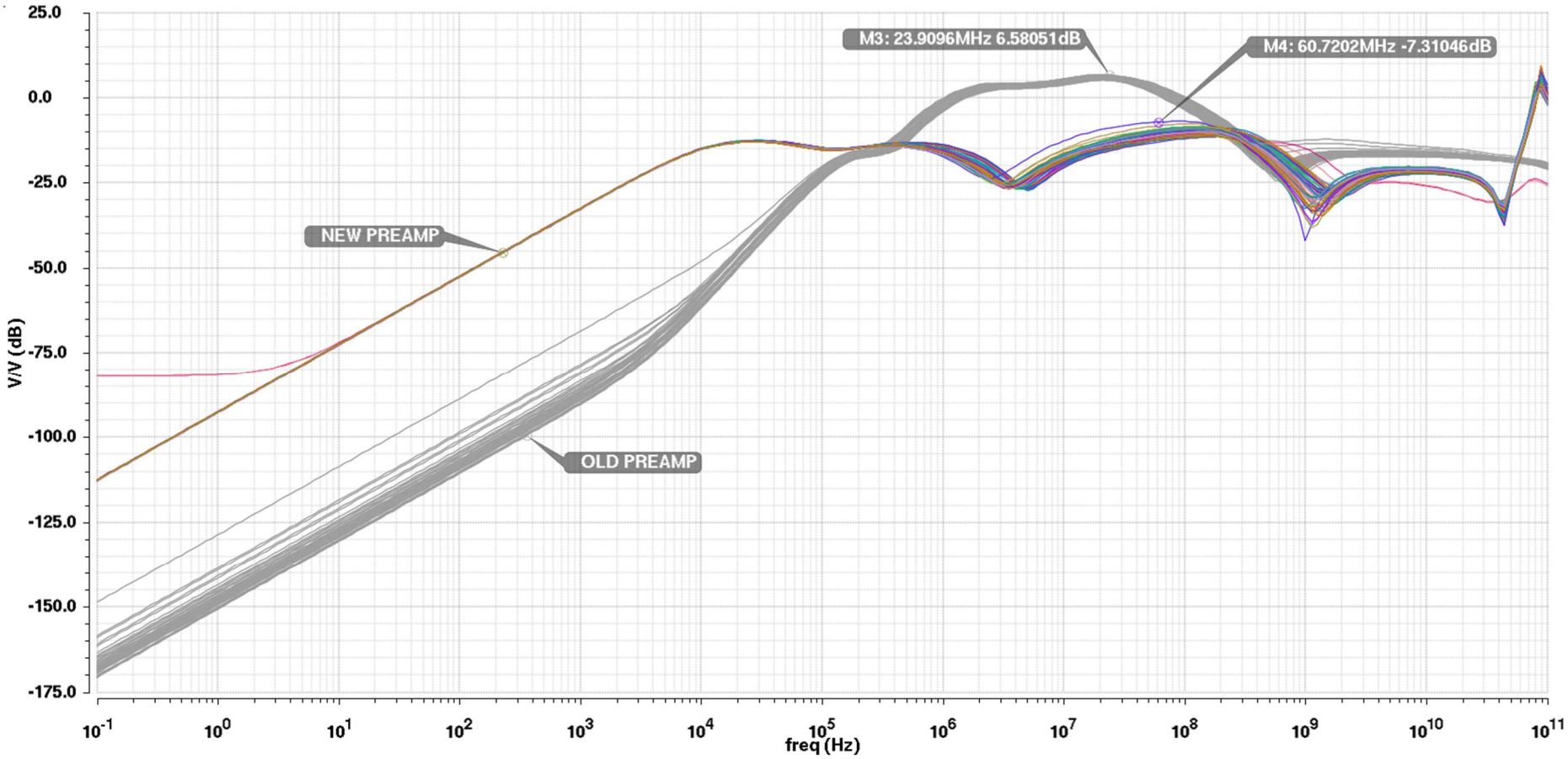



**Fig. 13 – CSPreamp and Supply Frequency Responses, Power Supply Rejection Ratio.**

# New CSPreamp

## Frequency Response of Supply Signal Comparison



# THANKS FOR THE ATTENTION!

# BACK-UP SLIDES

## Outline

- Differential Amplifiers ←←←
  - Generic Scheme
  - DA1
  - DA2
  - DA3
  - Chain Frequency Responses
  - Transient Signals
  - Noise Performance
- ToT Mode (DISC1 Output)
- ADC Mode (DISC2 Output)
- Layout Comparison
- Power Consumption Comparison

# DIFFERENTIAL AMPLIFIERS

## Generic Differential Amplifiers Scheme

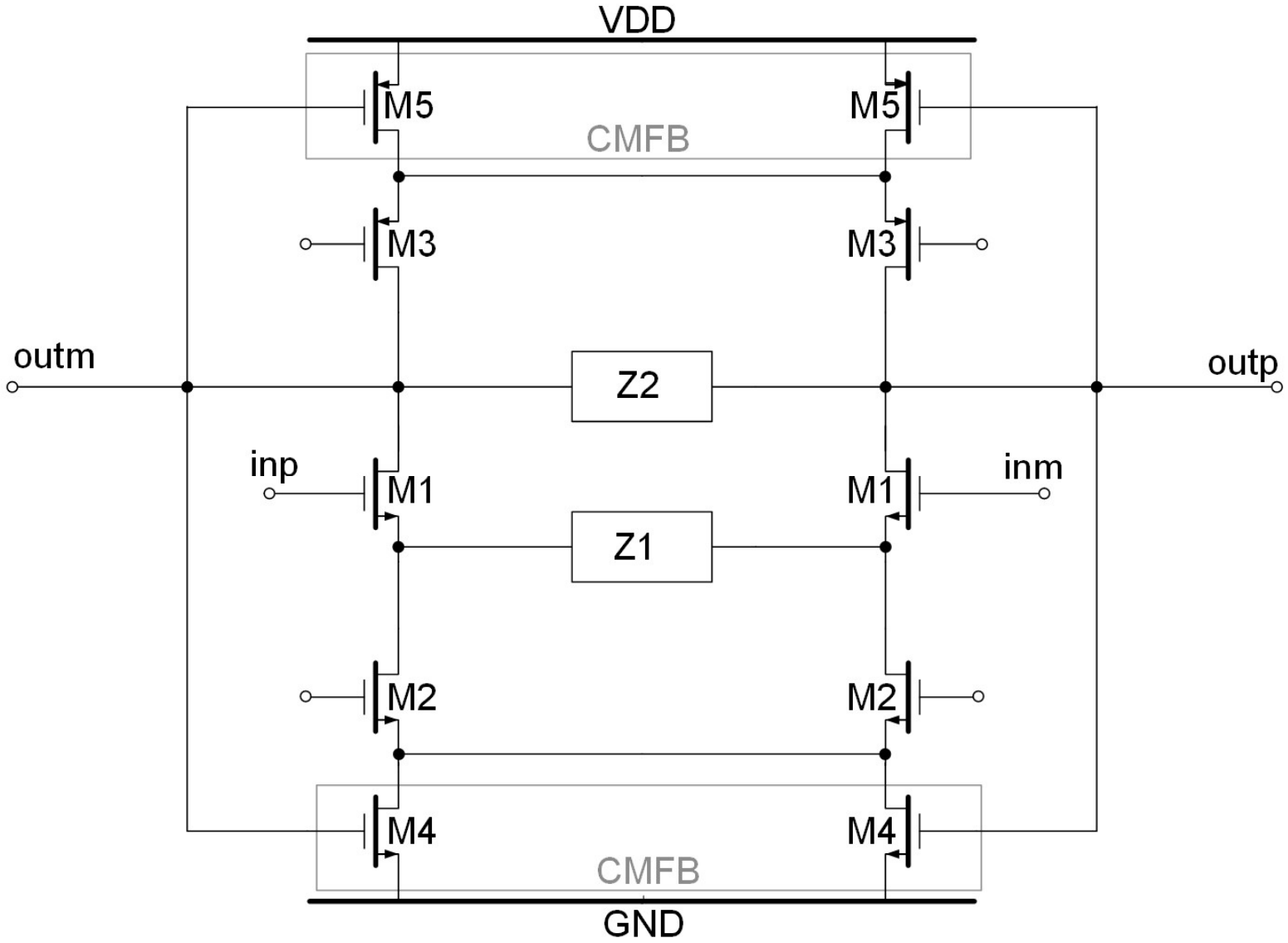



**Fig. 14 – DAi Transistor Level Scheme.**

# DIFFERENTIAL AMPLIFIERS

## $DA_1$ Scheme

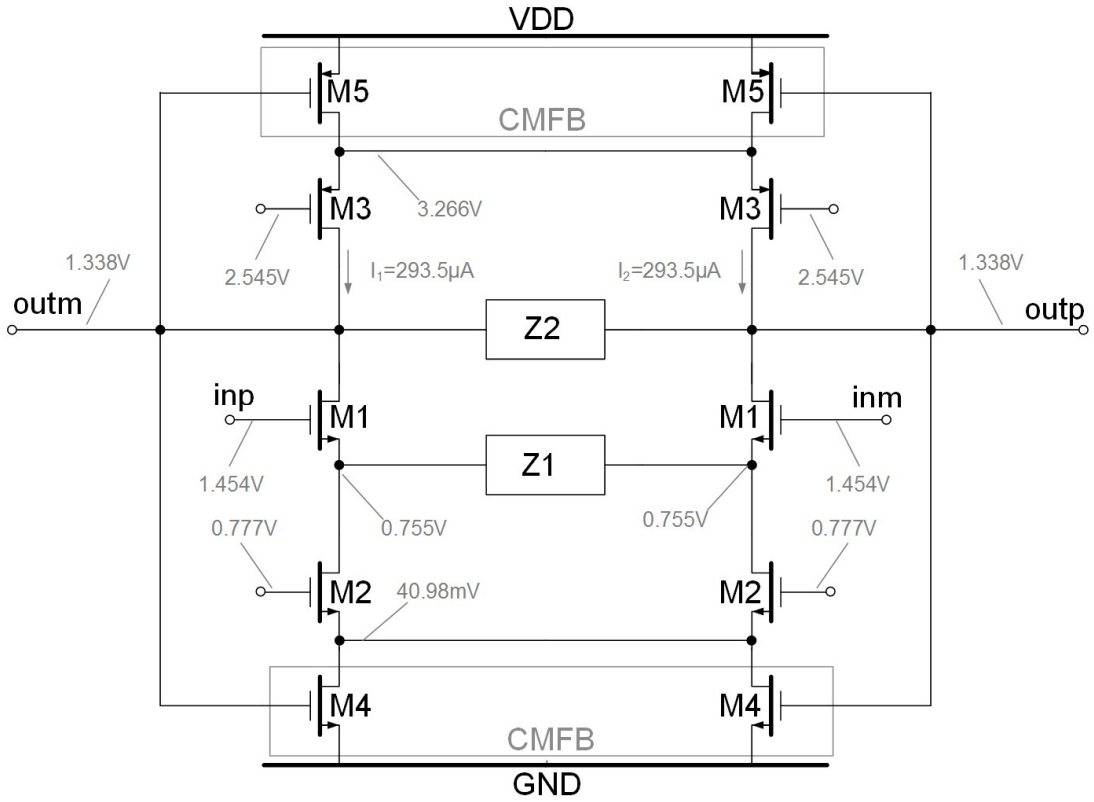



**Fig. 15 – $DA_1$ Transistor Level Scheme.**

| MOS | W/L | $g_m$ [mA/V] | $r_{DS}$ [kΩ] |
|---|---|---|---|
| M1 | 30µm/400nm | 2.987 | 10.58 |
| M2 | 30µm/900nm | 1.897 | 41.74 |
| M3 | 90µm/900nm | 1.657 | 174.33 |
| M4 | 15µm/400nm | 0.296 | 0.133 |
| M5 | 45µm/400nm | 0.108 | 0.114 |

| IMPEDANCEs | VALUEs |
|---|---|
| Z1 | 1.34kΩ |
| Z2 | 6.26kΩ |

| CURRENTs | VALUEs |
|---|---|
| $I_1=I_2$ | 293.5µA |

- Current Consumption → 0.746mA
- **Power Consumption** @ 3.3V of Supply Voltage → **2.46mW**

# DIFFERENTIAL AMPLIFIERS

## $DA_2$ Scheme

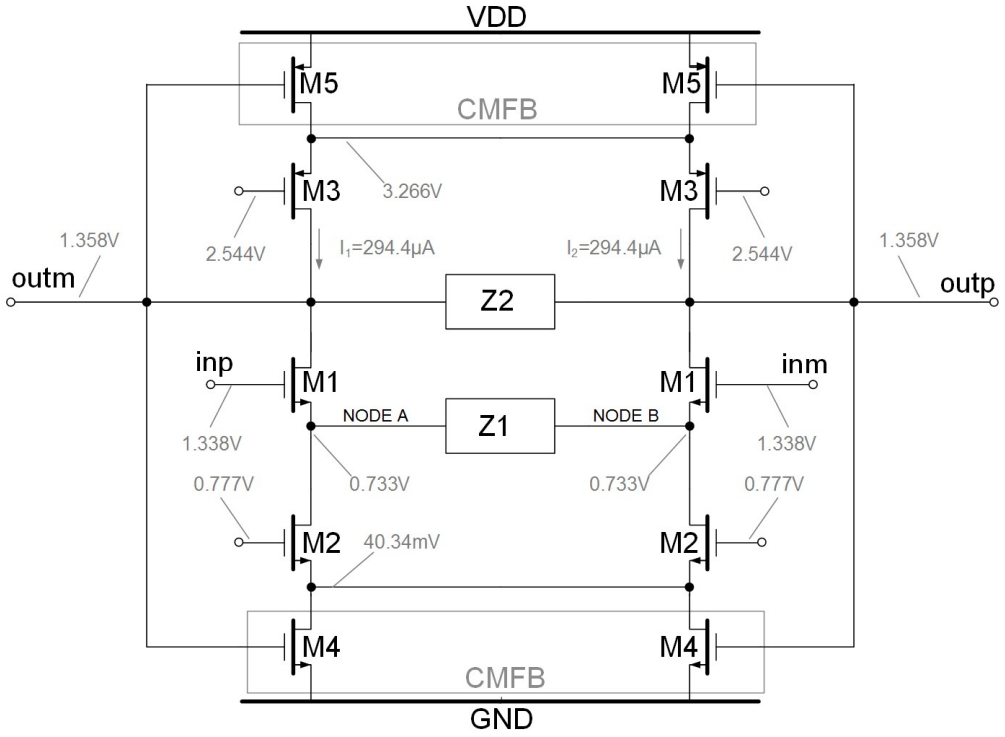



**Fig. 16 – $DA_2$ Transistor Level Scheme.**

| MOS | W/L | $g_m$ [mA/V] | $r_{DS}$ [kΩ] |
|---|---|---|---|
| M1 | 90µm/400nm | 4.477 | 8.772 |
| M2 | 30µm/900nm | 1.898 | 40.13 |
| M3 | 90µm/900nm | 1.659 | 173 |
| M4 | 15µm/400nm | 0.288 | 0.130 |
| M5 | 45µm/400nm | 0.111 | 0.114 |

| IMPEDANCEs | VALUEs |
|---|---|
| Z1 | See Fig. 17 |
| Z2 | 6.26kΩ |

| CURRENTs | VALUEs |
|---|---|
| $I_1=I_2$ | 294.4µA |

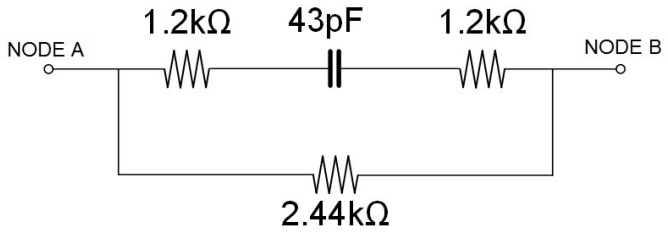



**Fig. 17 – Z1 Impedance Scheme of DA2 Block.**

- Current Consumption → 0.748mA
- **Power Consumption** @ 3.3V of Supply Voltage → **2.47mW**

# DIFFERENTIAL AMPLIFIERS

## $DA_3$ Scheme

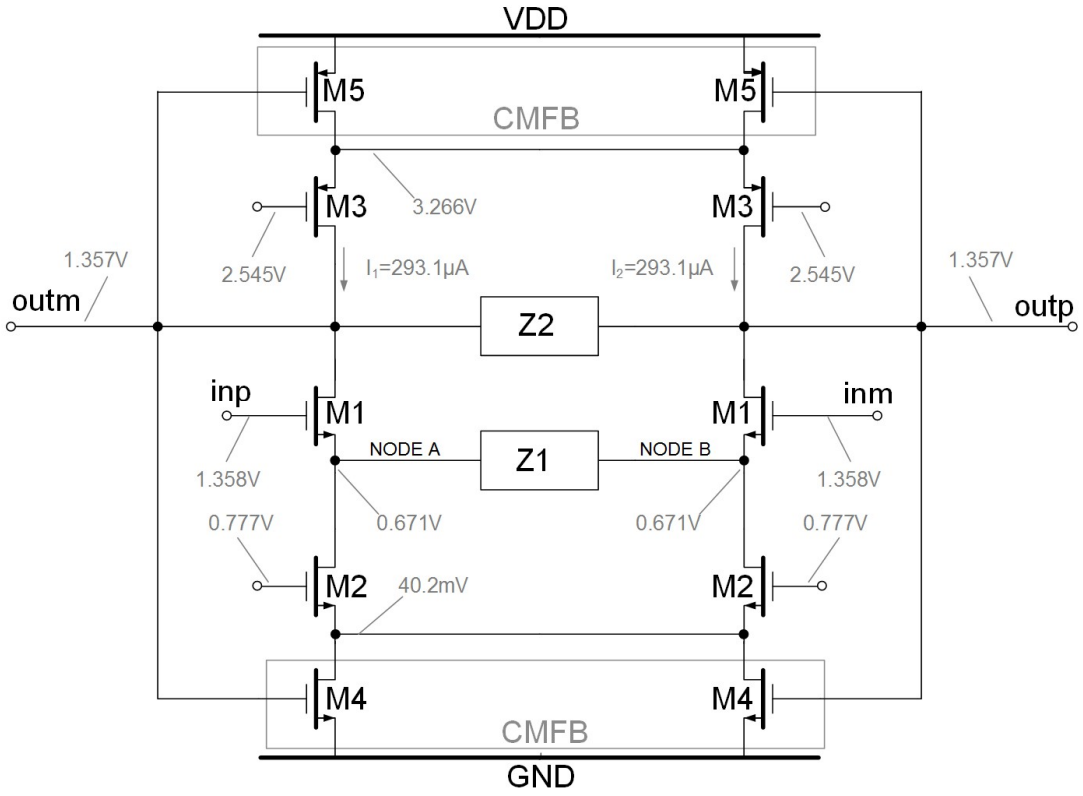



**Fig. 18 – $DA_3$ Transistor Level Scheme.**

| MOS | W/L | $g_m$ [mA/V] | $r_{DS}$ [kΩ] |
|---|---|---|---|
| M1 | 30µm/400nm | 2.995 | 12.13 |
| M2 | 30µm/900nm | 1.89 | 35.93 |
| M3 | 90µm/900nm | 1.655 | 174.3 |
| M4 | 15µm/400nm | 0.288 | 0.130 |
| M5 | 45µm/400nm | 0.110 | 0.115 |

| IMPEDANCEs | VALUEs |
|---|---|
| Z1 | See Fig. 19 |
| Z2 | 9.47kΩ |

| CURRENTs | VALUEs |
|---|---|
| $I_1=I_2$ | 293.1µA |


**Fig. 19 – Z1 Impedance Scheme of DA3 Block.**

- Current Consumption → 0.745mA
- **Power Consumption** @ 3.3V of Supply Voltage → **2.45mW**

# DIFFERENTIAL AMPLIFIERS

## Chain Frequency Responses

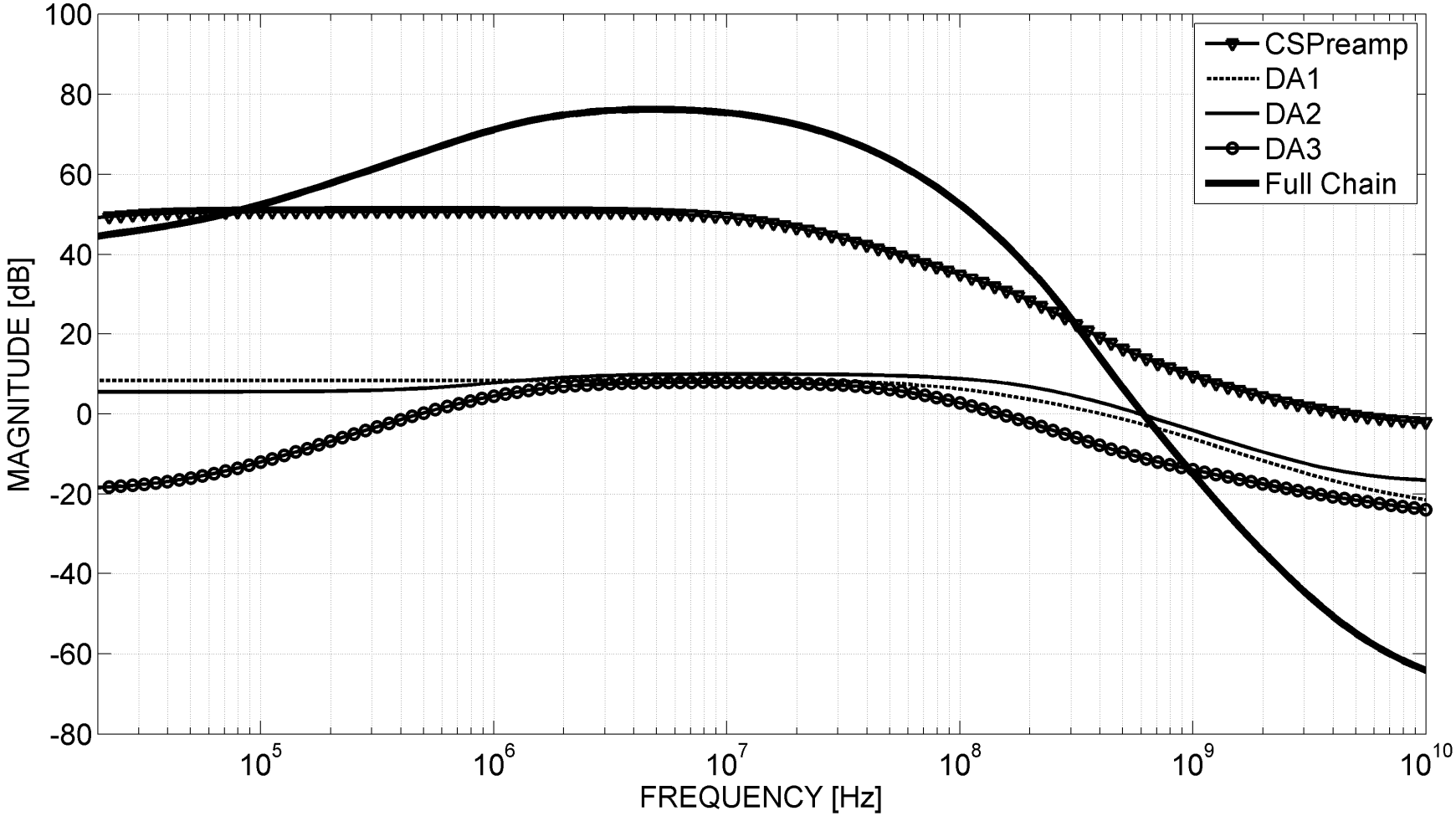



**Fig. 20 – Channel Frequency Responses.**

- Full Chain Frequency Response:
  - Peak of 76dB @ 5MHz
  - Bandwidth from 1.4MHz to 17.4MHz

# DIFFERENTIAL AMPLIFIERS

## Transient Signals

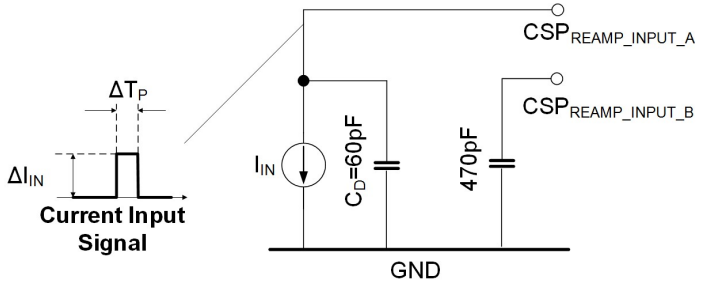



Fig. 22 – Input Nets used in Design.

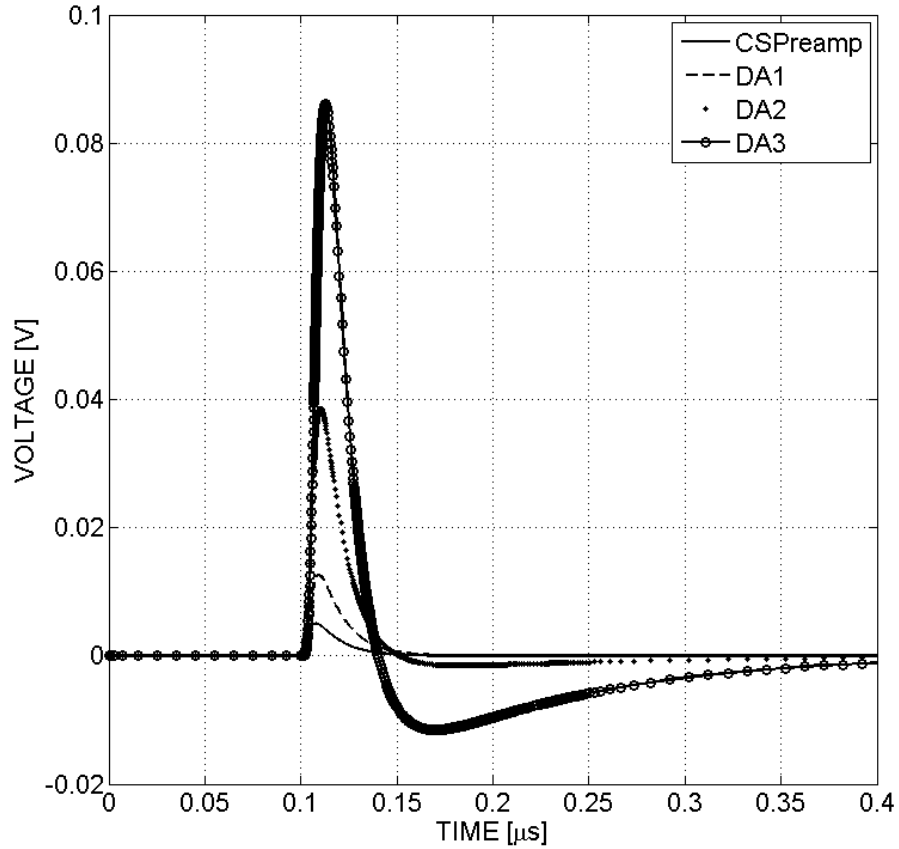



Fig. 21 – Output Signals from Transient Simulation.

| Input Signal Features: | |
|---|---|
| $C_D$ | 60pF |
| $\Delta T_P$ | 3ns |
| $\Delta I_{IN}$ | 1.67μA |
| $q_{IN}$ | 5fC |
| $q_{in}$ Arrival Time | 100ns |

| Output Signal Features: | | |
|---|---|---|
| STAGE | $V_{PEAK}$ [mV] | Peaking Time [ns] |
| CSPreamp | 5.04 | 7.6 |
| DA1 | 12.66 | 9.2 |
| DA2 | 38.57 | 10.16 |
| DA3 | 86.03 | 12.8 |

# DIFFERENTIAL AMPLIFIERS

## $DA_3$ Output for Different Input Charges

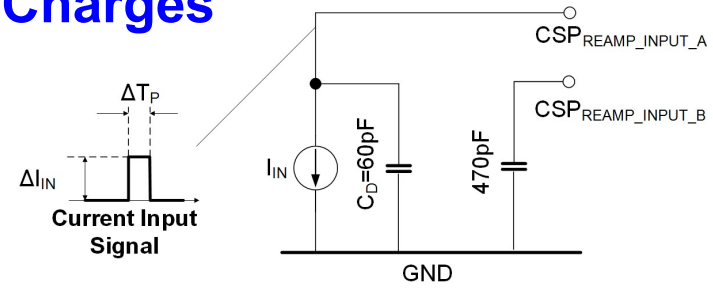



**Fig. 23 – Input Nets used in Design.**

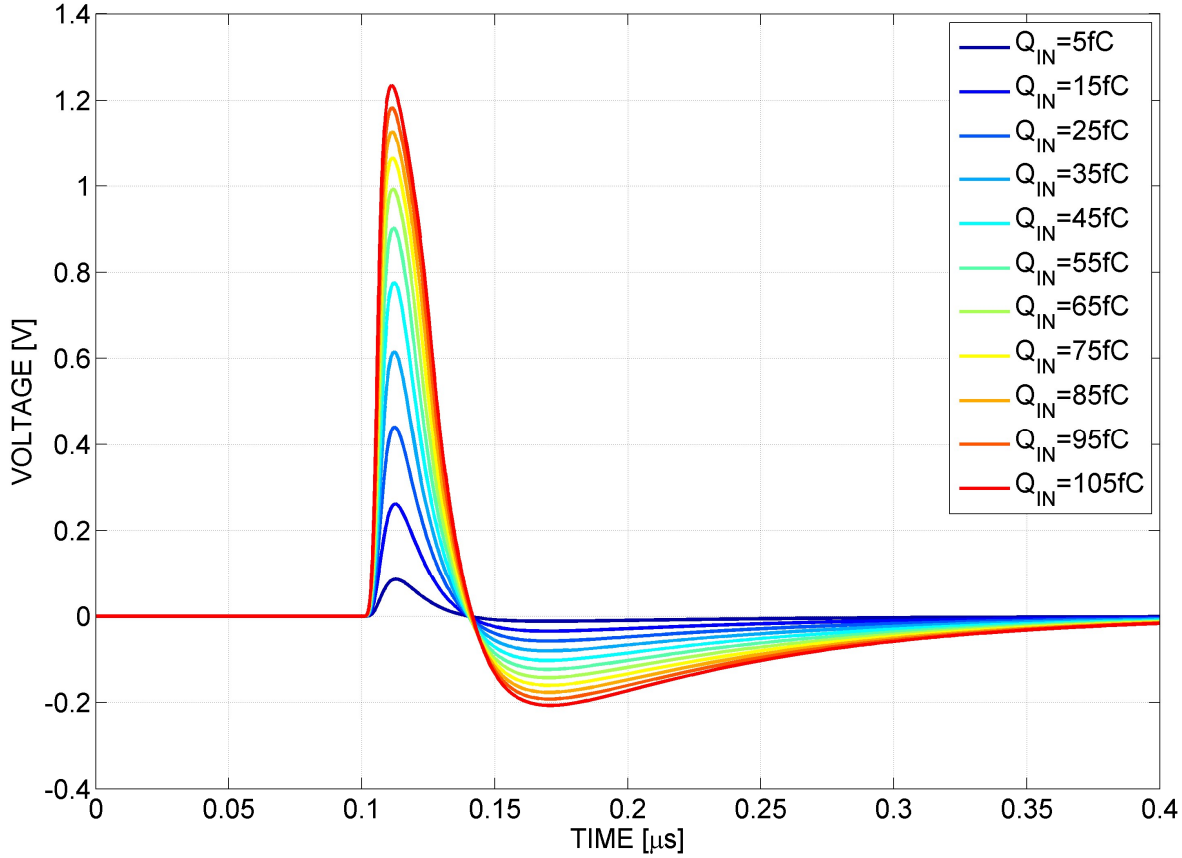



**Fig. 24 – Output Signals from Transient Simulation.**

| Input Signal Features: | |
|---|---|
| $C_D$ | 60pF |
| $\Delta T_P$ | 3ns |
| $\Delta I_{IN\_MIN}$ | 1.67μA |
| $\Delta I_{IN\_MIN}$ | 35μA |
| $q_{IN\_MIN}$ | 5fC |
| $q_{IN\_MAX}$ | 105fC |
| $q_{in}$ Arrival Time | 100ns |

# DIFFERENTIAL AMPLIFIERS

## $DA_3$ Peak Voltage

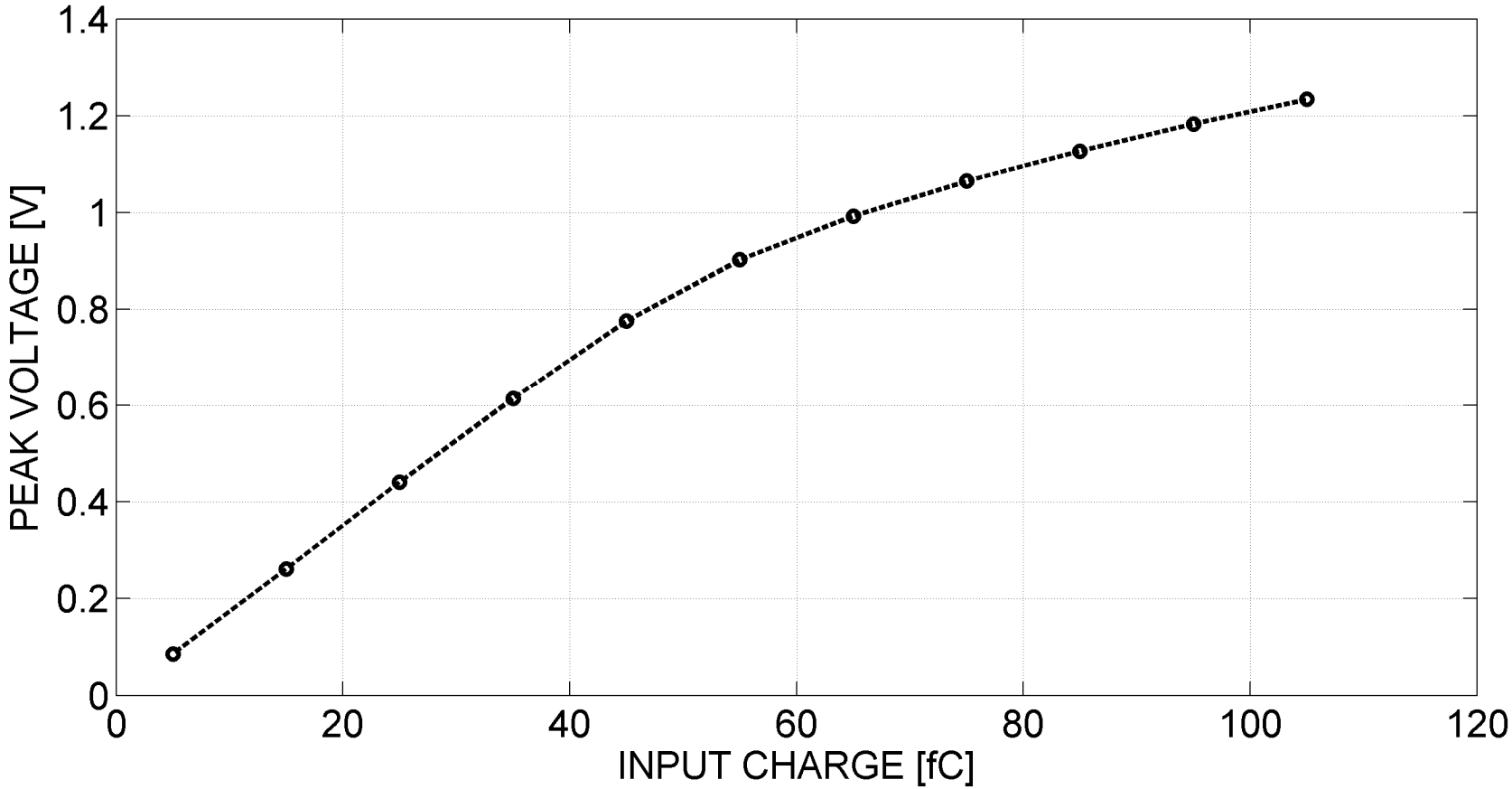
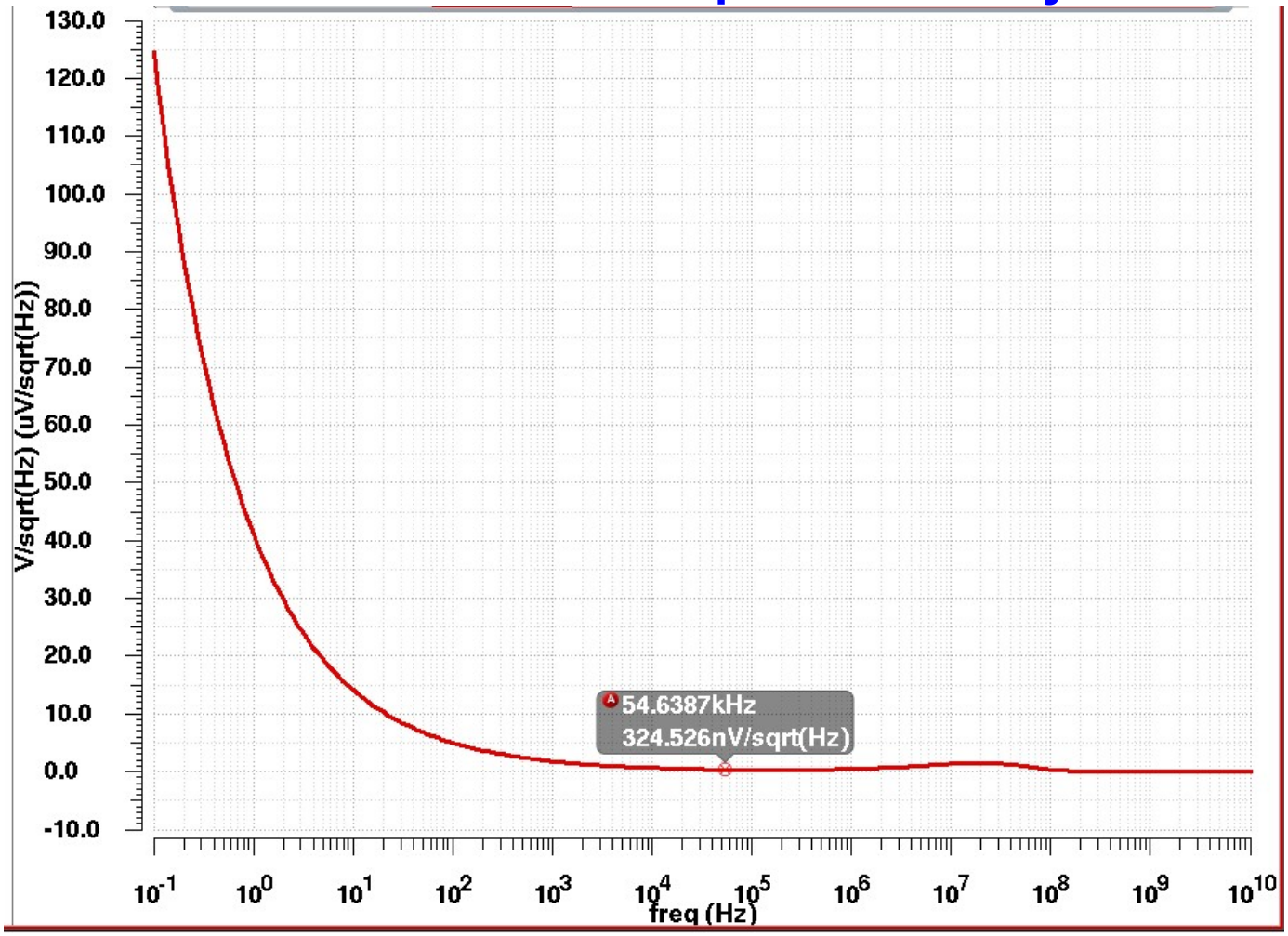



**Fig. 25 – $DA_3$ Peak Voltage with Different Input Charges (up to 105fC)**

- Sensitivity @ DA3 Output → about 14mV/fC
- Peaking Time Delay → ≤13ns

# DIFFERENTIAL AMPLIFIERS

## Chain Noise Power Spectral Density




- Noise at DA3 Output
- Integrated Noise → 10.5mV$_{RMS}$

# BACK-UP SLIDES

## Outline

- Differential Amplifiers
  - Generic Scheme
  - DA1
  - DA2
  - DA3
  - Chain Frequency Responses
  - Transient Signals
  - Noise Performance
- ToT Mode (DISC1 Output) ←←←
- ADC Mode (DISC2 Output)
- Layout Comparison
- Power Consumption Comparison

# ToT MODE

## DISC1

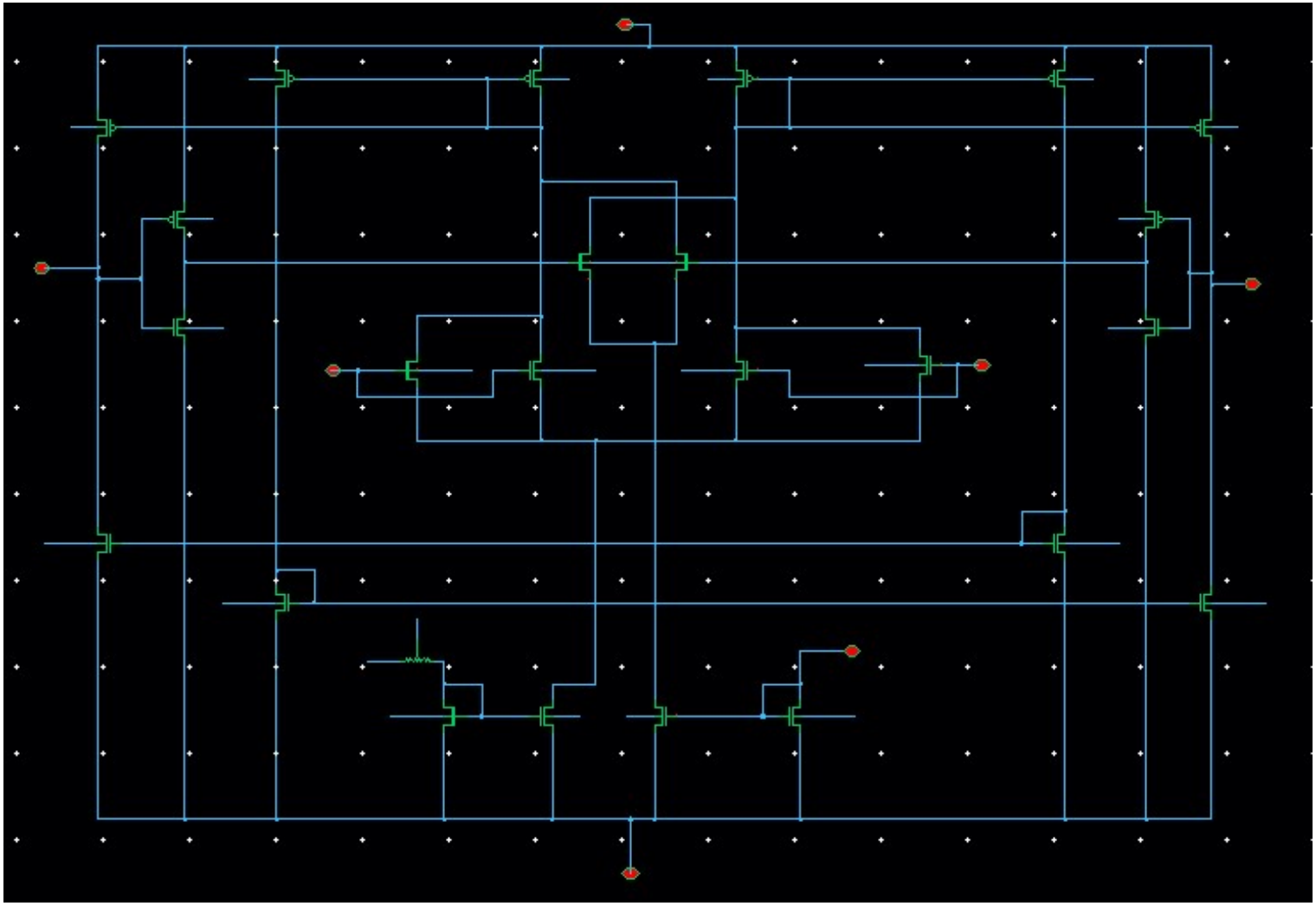


**Fig. 26 - Dicriminator1 Cadence Scheme.**

# ToT MODE

## DISC1 Output

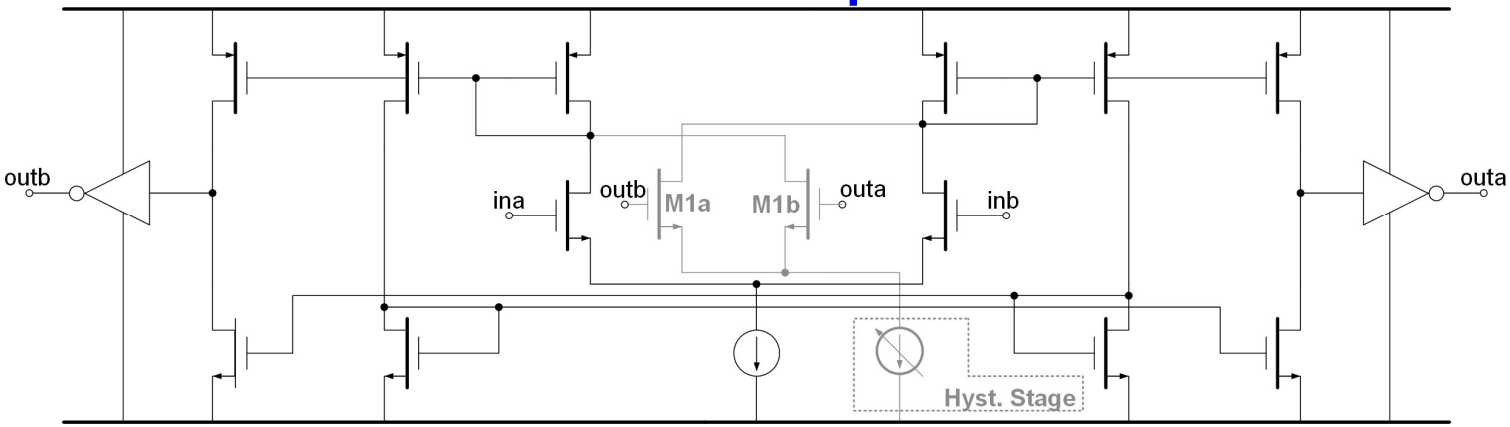
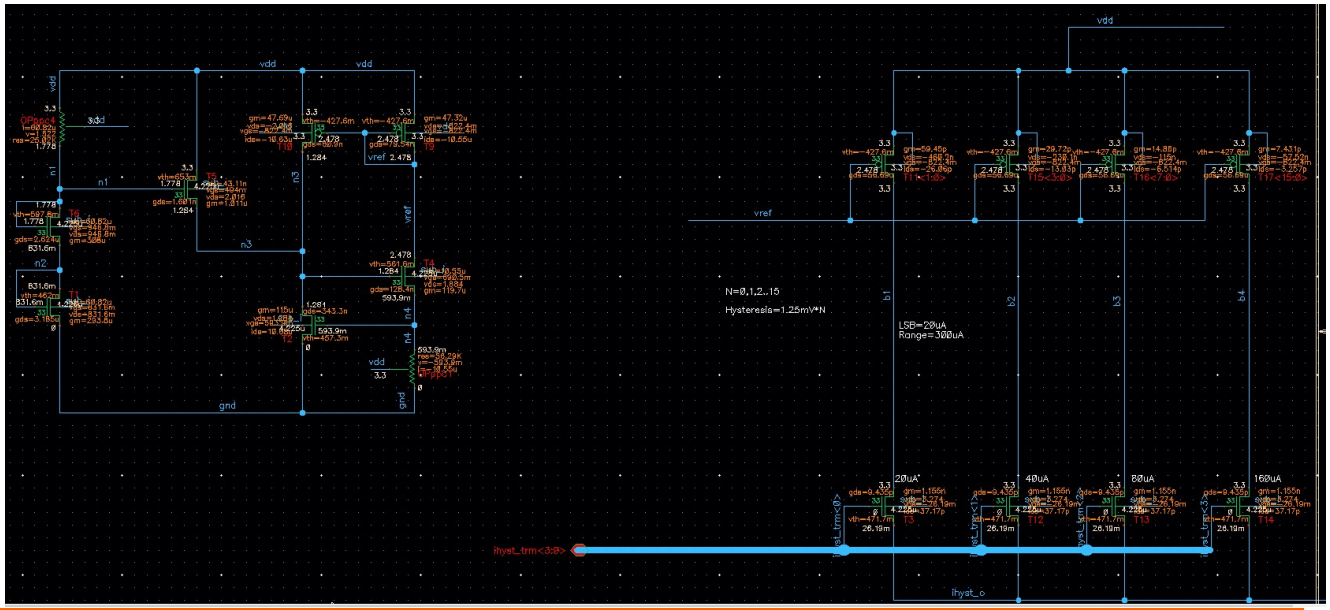


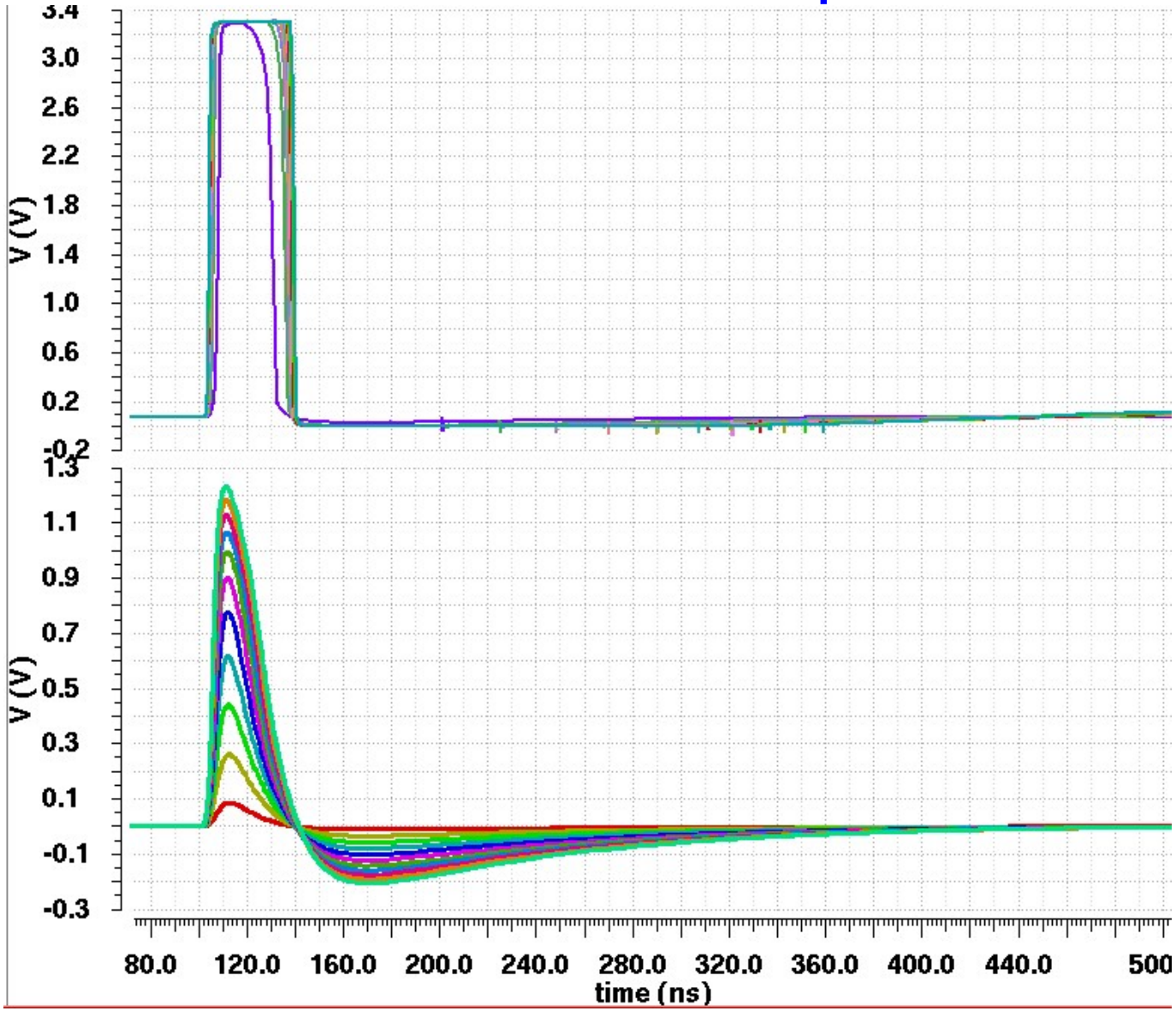

**Fig. 27 - Dicriminator1 Transistor Level Scheme.**

- Mirror Input Stage
- Static Current Consumption → about 1.4mA
- Local Hysteresis Generation:
  - 20µA of LSB
  - 300µA of Range
  - 4bit Resolution



# ToT MODE

## DISC1 Output




DISC1 Output

$DA_3$ Output

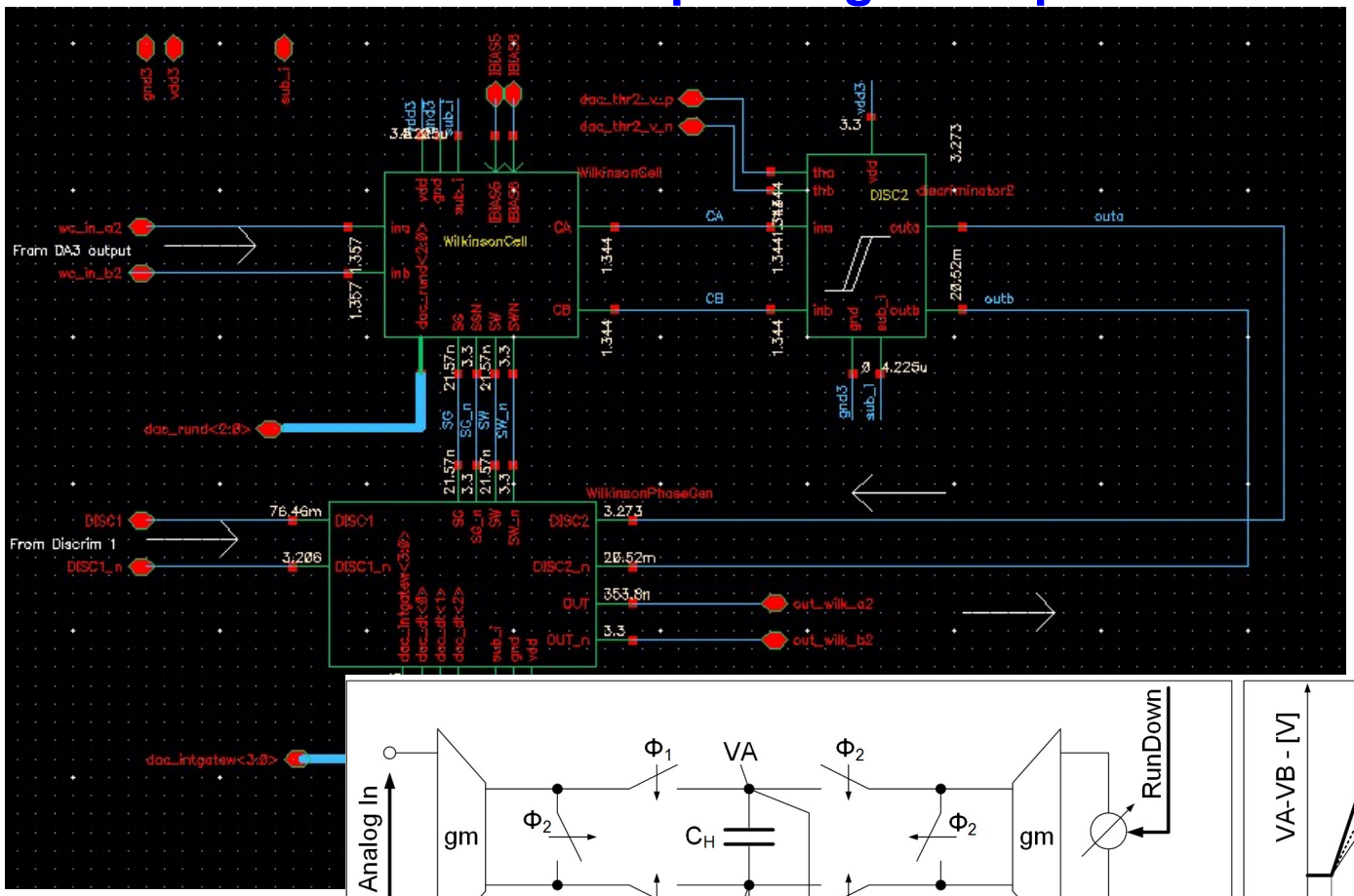
# BACK-UP SLIDES

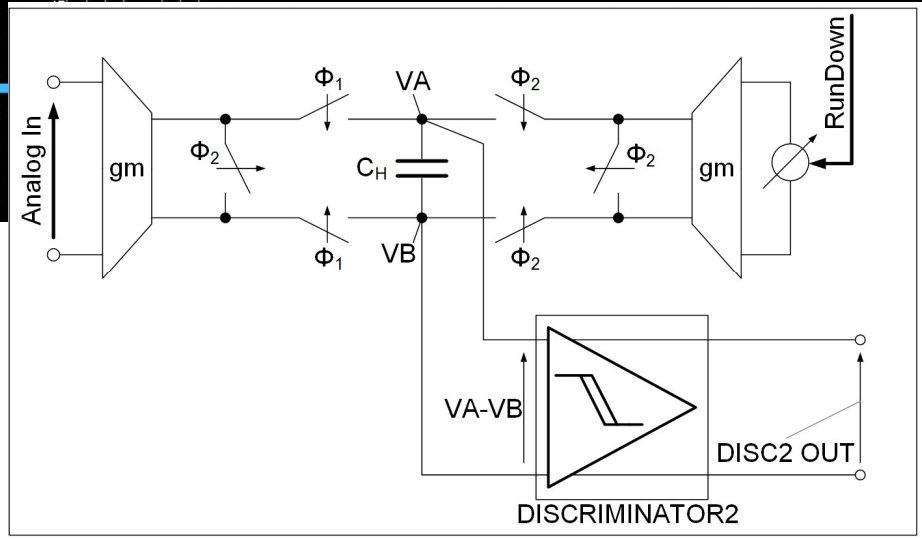
## Outline

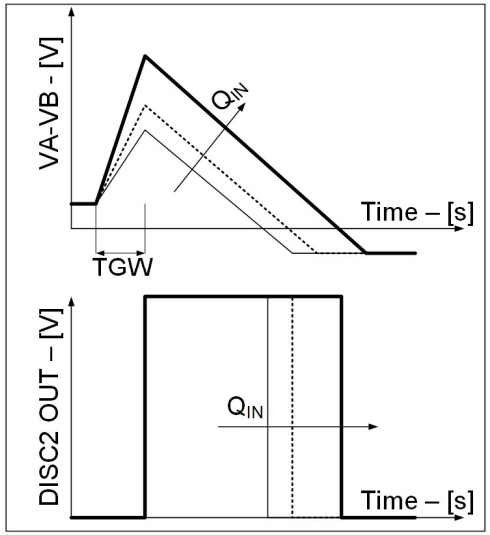
- Differential Amplifiers
  - Generic Scheme
  - DA1
  - DA2
  - DA3
  - Chain Frequency Responses
  - Transient Signals
  - Noise Performance
- ToT Mode (DISC1 Output)
- ADC Mode (DISC2 Output) ←←←
- Layout Comparison

# Power Consumption ComparisonADC MODE

## Wilkinson ADC Operating Principle

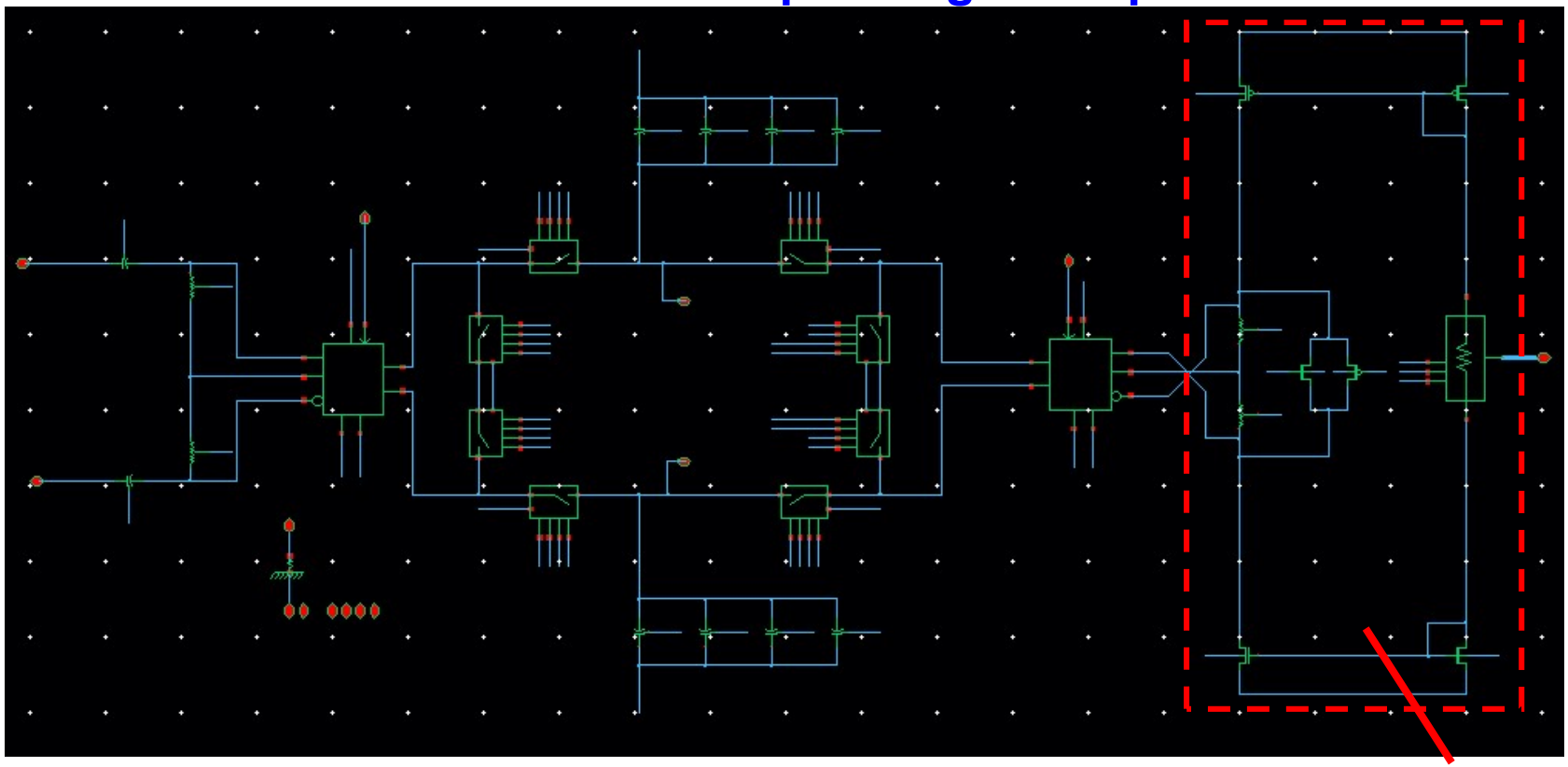


# ADC MODE

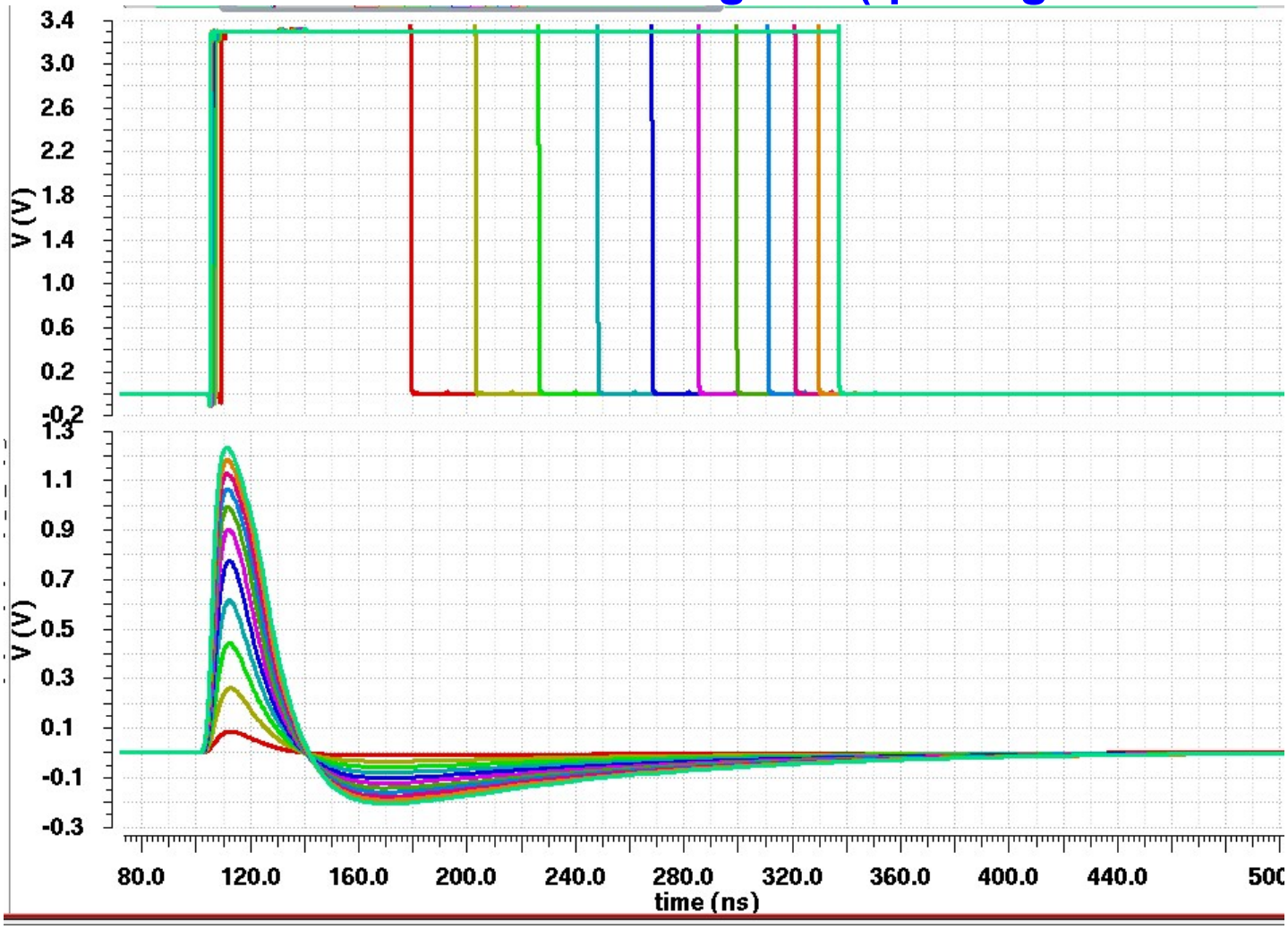
## Wilkinson ADC Operating Principle




- Local Generation of Programmable Parameters:
  - Rundown Current (in Wilkinson Cell→ASDv4)
  - Integration Gate Width (in Wilkinson Phase Gen→ASDv6)
  - DeadTime (in Wilkinson Phase Gen→ASDv5)
- Channel Matching Improvement

# ADC MODE

## Wilkinson ADC Signals ($q_{IN}$ range = 5fC – 105fC)



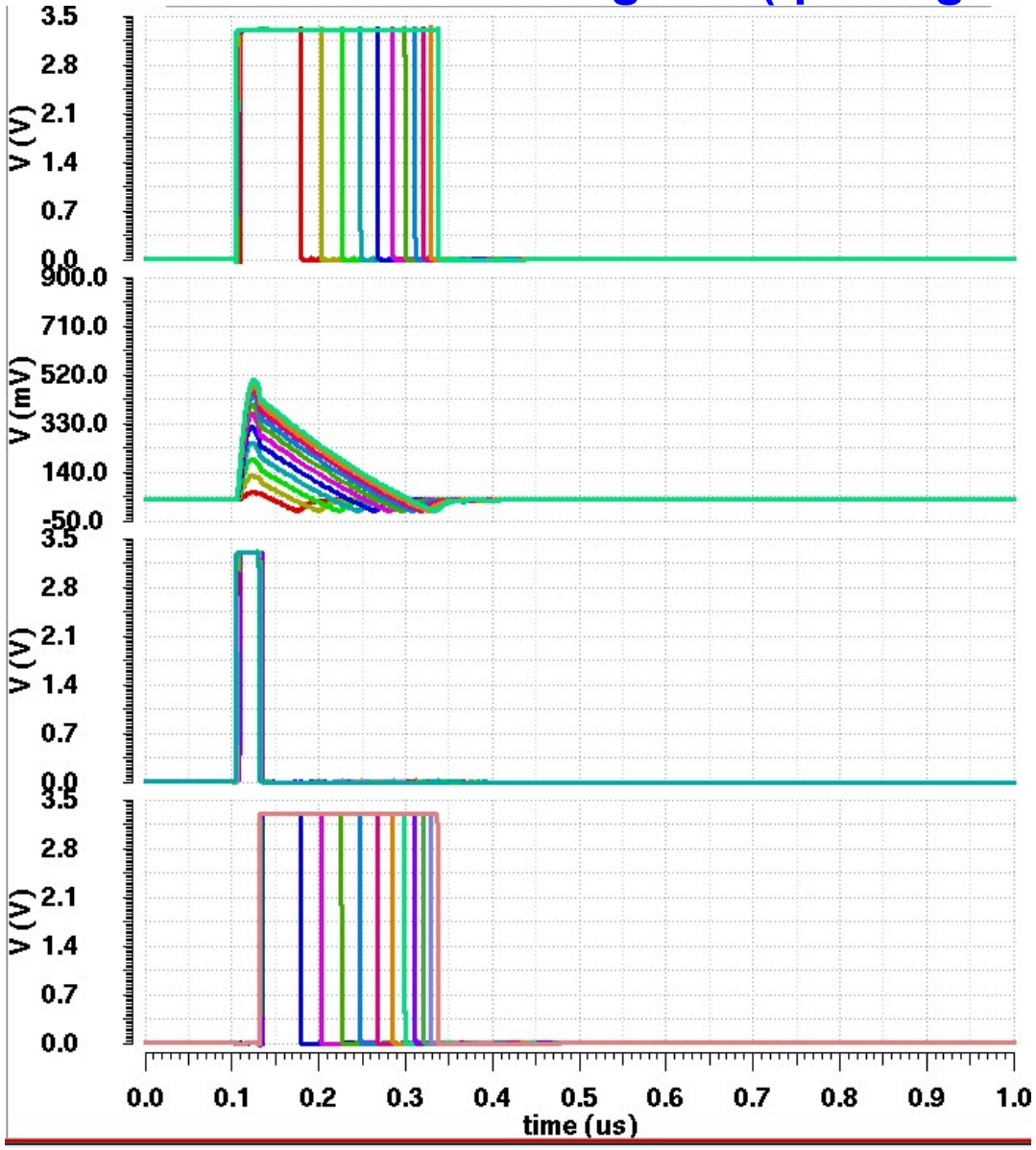

Wilkinson ADC Output

DA3 Output

- $q_{IN}$ range: 5fC – 105fC
- Step Size:10fC

# ADC MODE

## Wilkinson ADC Signals ($q_{IN}$ range = 5fC – 105fC)




Wilkinson Outputs

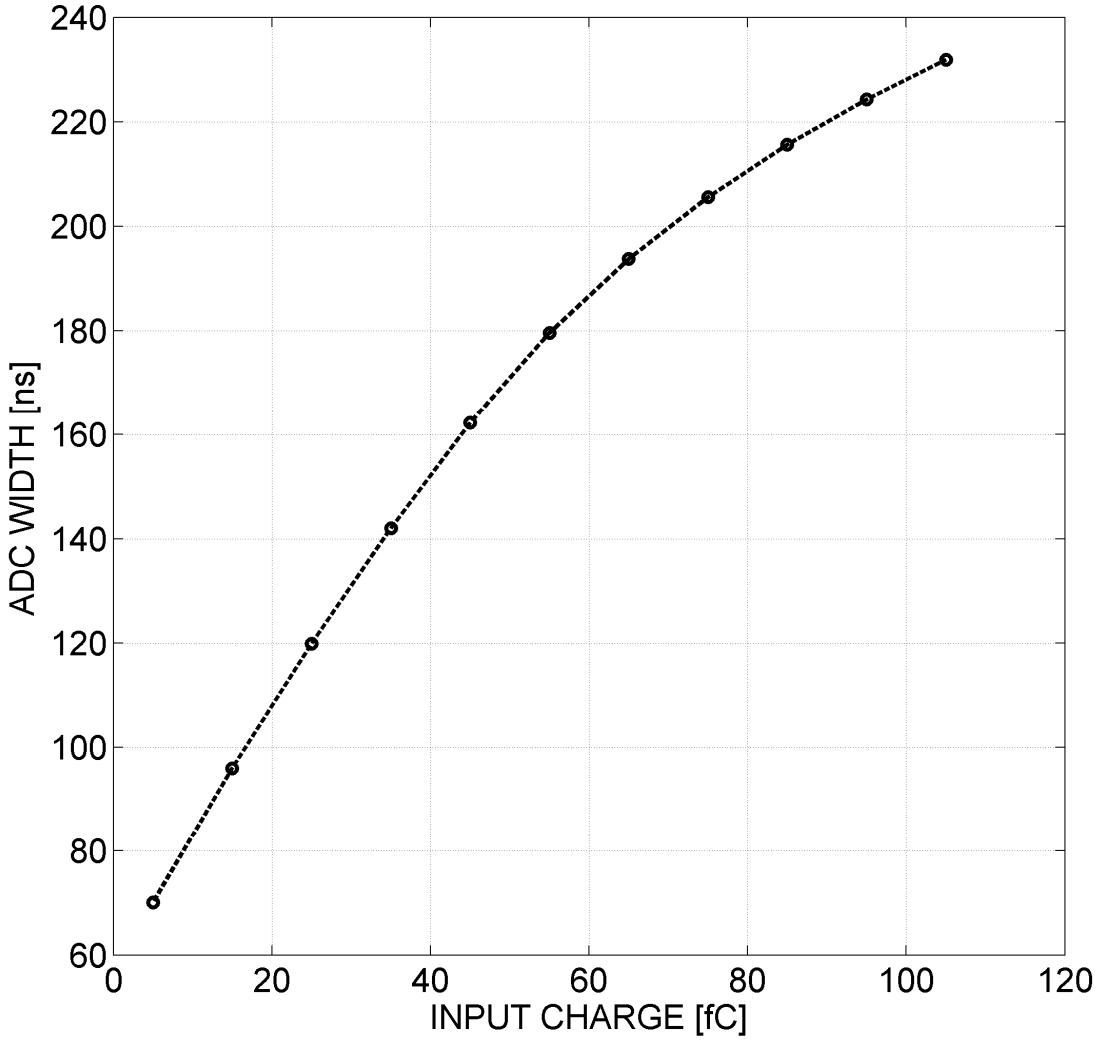
$C_H$ Charge/Discharge

Integration Impulses

Rundown Impulses

# ADC MODE

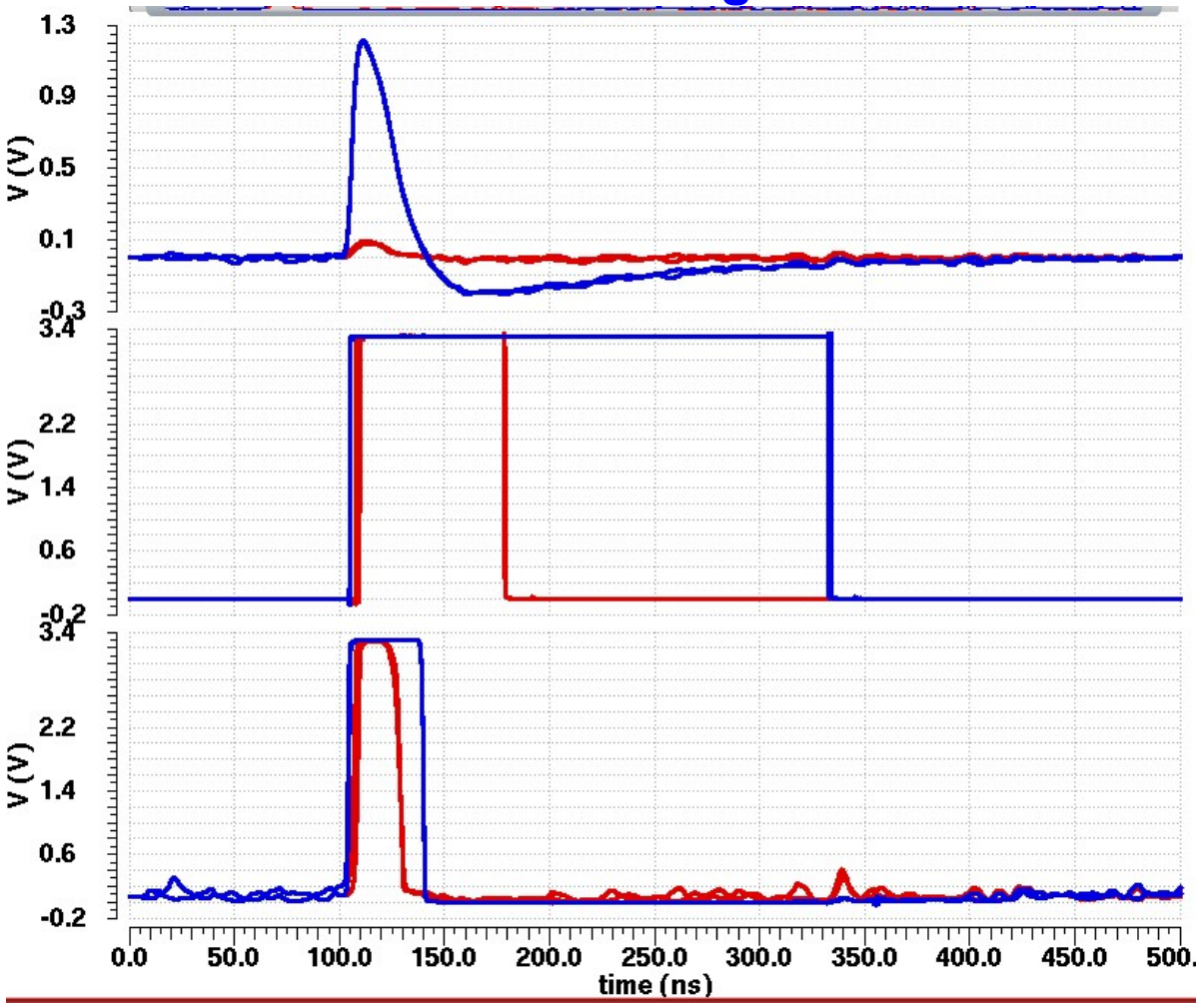
## Wilkinson ADC Characteristic




| Parameter | Value |
|---|---|
| $q_{IN}$ Range | 5fC – 105fC |
| $q_{IN}$ Step Size | 10fC |
| ADC Width Range | 70ns – 230ns |

# ADC MODE

## Wilkinson ADC Signals –Transient Noise




DA3 Output

Wilkinson ADC

DISC1 Output

- $q_{IN\_MIN}$=5fC, $q_{IN\_MAX}$=100fC
- Threshold1 Voltage → 19mV
- Threshold2 Voltage → -31mV

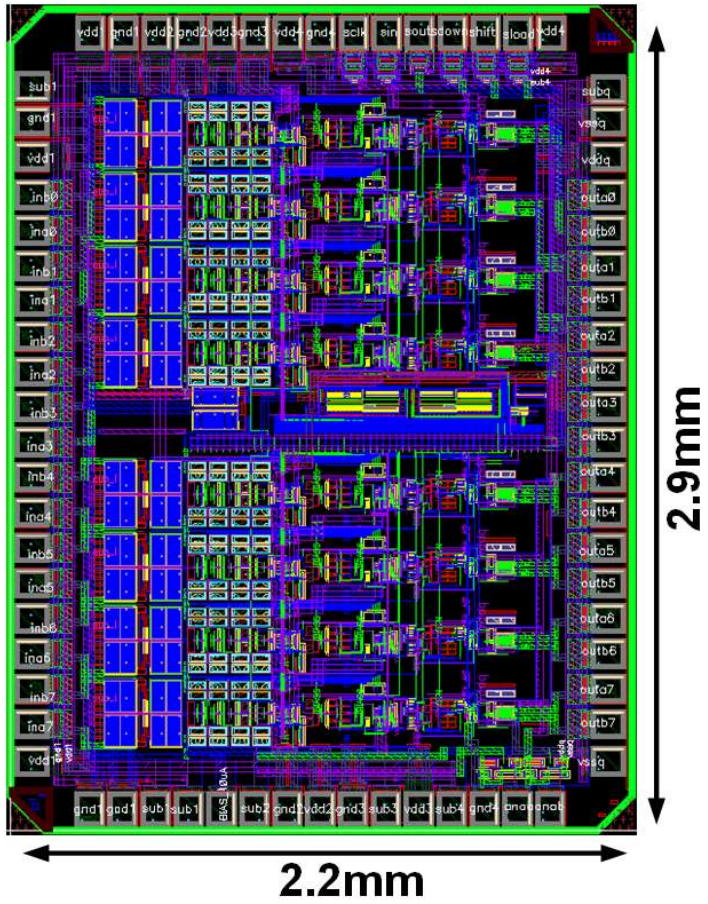
# BACK-UP SLIDES

## Outline

- Differential Amplifiers
  - Generic Scheme
  - DA1
  - DA2
  - DA3
  - Chain Frequency Responses
  - Transient Signals
  - Noise Performance
- ToT Mode (DISC1 Output)
- ADC Mode (DISC2 Output)
- Layout Comparison ←←←
- Power Consumption Comparison

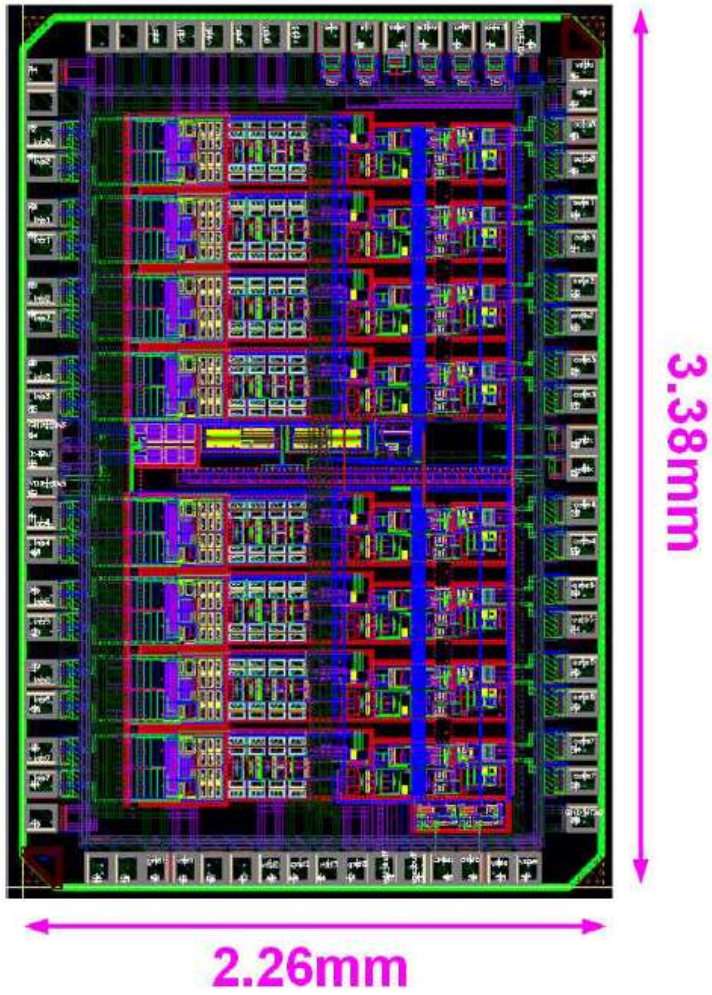
# LAYOUT

## Version4




- Area → 6.38mm$^2$

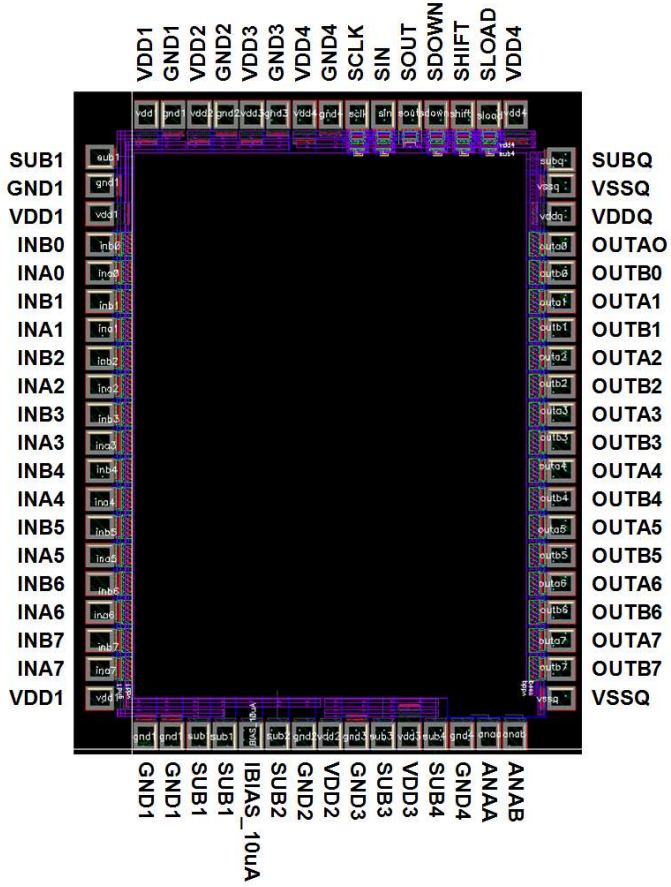
## Version5




- Area → 7.64mm$^2$
- +19.7% due to BFMOAT introduction and supplies separation

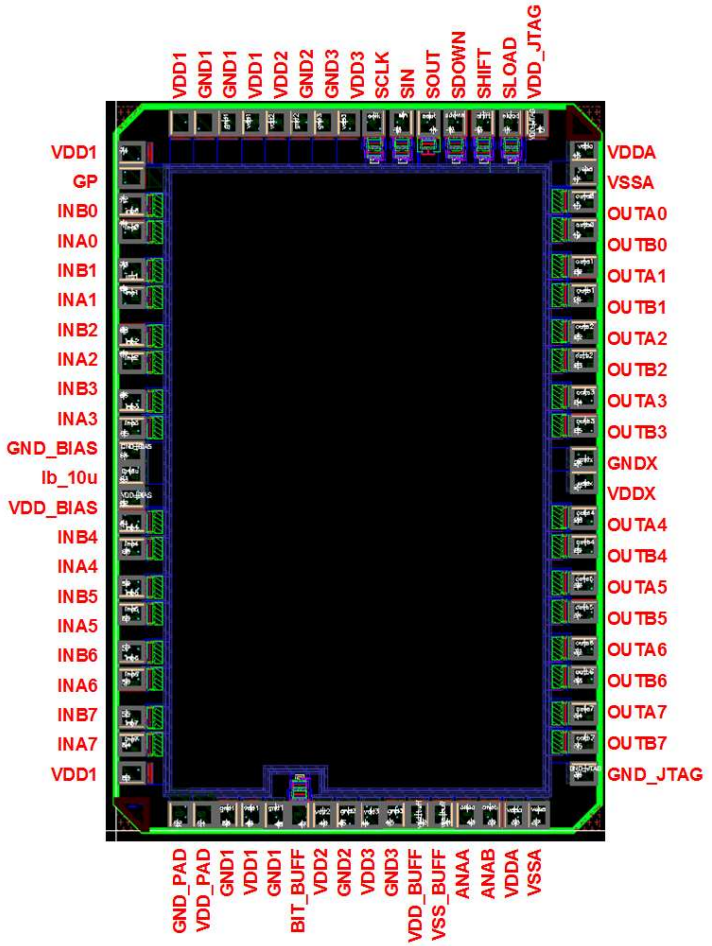
# LAYOUT

## PADRING V4




70 Pads

## PADRING V5




74 Pads

# LAYOUT

## Pin List V4 – 70 Pins

| BLOCK | PIN NAME | DESCRIPTION | TYPE | # | I/O INTERFACE |
|---|---|---|---|---|---|
| JTAG Serial Interface 6 PADs | SCLK | Clock Line | Digital In | 1 | Vpulse Generator |
| | SIN | Load Control Line | Digital In | 1 | Vbit Generator |
| | SDOWN | Down Control Line | Digital In | 1 | Vpulse Generator |
| | SHIFT | Shift Control Line | Digital In | 1 | Vpulse Generator |
| | SLOAD | Data Line | Digital In | 1 | Vpulse Generator |
| | SOUT | Data Line | Digital Out | 1 | noConn Istance |
| MDT-ASD V4 Channel 32 PADs | <ina0:ina7> | Positive Channel Input | Analog In | 8 | 1 nF Cap or Current Generator in parallel with 60 pF Cap |
| | <inb0:inb7> | Negative Channel Input | Analog In | 8 | 470 pF Cap |
| | <outa0:outa7> | Positive Channel Output | Analog Out | 8 | Input 'A' LVDS Termination |
| | <outb0:outb7> | Negative Channel Output | Analog Out | 8 | Input 'B' LVDS Termination |
| Channel#7 Buffer 2 PADs | anaa | $DA_{3oa}$ of Channel#7 | Analog Out | 1 | 1 pF Cap |
| | anab | $DA_{3ob}$ of Channel#7 | Analog Out | 1 | 1 pF Cap |
| Current Channels Generator 1 PAD | IBIAS_10 µA | Current Generator | Analog In | 1 | Current Generator of 10 µA ± 5 % |
| Supplies 29 PADs | <vdd1:vddq> | Supply Voltage | Analog In | 10 | DC-Voltage Generator of 3.3 V ± 5 % |
| | <sub1:subq> | Ground Voltage | Analog In | 7 | DC-Voltage Generator of 0 V |
| | <gnd1:gndq> | Ground Voltage | Analog In | 12 | DC-Voltage Generator of 0 V |

## Pin List V5 – 74 Pins

| BLOCK | PIN NAME | DESCRIPTION | TYPE | # | I/O INTERFACE |
|---|---|---|---|---|---|
| JTAG Serial Interface 8 PADs | SCLK | Clock Line | Digital In | 1 | Vpulse Generator |
| | SIN | Load Control Line | Digital In | 1 | Vbit Generator |
| | SDOWN | Down Control Line | Digital In | 1 | Vpulse Generator |
| | SHIFT | Shift Control Line | Digital In | 1 | Vpulse Generator |
| | SLOAD | Data Line | Digital In | 1 | Vpulse Generator |
| | SOUT | Data Line | Digital Out | 1 | noConn Istance |
| | VDD_JTAG | JTAG Supply Voltage | Analog In | 1 | DC-Voltage Generator of 3.3 V ± 5 % |
| | GND_JTAG | JTAG Ground Voltage | Analog In | 1 | DC-Voltage Generator of 0 V |
| MDT-ASD V4 Channel 55 PADs | <ina0:ina7> | Positive Channel Input | Analog In | 8 | 1 nF Cap or Current Generator in parallel with 60 pF Cap |
| | <inb0:inb7> | Negative Channel Input | Analog In | 8 | 470 pF Cap |
| | <outa0:outa7> | Positive Channel Output | Analog Out | 8 | Input 'A' LVDS Termination |
| | <outb0:outb7> | Negative Channel Output | Analog Out | 8 | Input 'B' LVDS Termination |
| | VDD_1 | CSPreamp Supply Voltage | Analog In | 5 | DC-Voltage Generator of 3.3 V ± 5 % |
| | GND_1 | CSPreamp Ground Voltage | Analog In | 4 | DC-Voltage Generator of 0 V |
| | VDD_2 | Analog Section Supply Voltage | Analog In | 2 | DC-Voltage Generator of 3.3 V ± 5 % |
| | GND_2 | Analog Section Ground Voltage | Analog In | 2 | DC-Voltage Generator of 0 V |
| | VDD_3 | Digital Supply Voltage | Analog In | 2 | DC-Voltage Generator of 3.3 V ± 5 % |
| | GND_3 | Digital Ground Voltage | Analog In | 2 | DC-Voltage Generator of 0 V |
| | VDD_A | MUX-LVDS Supply Voltage | Analog In | 2 | DC-Voltage Generator of 3.3 V ± 5 % |
| | VSS_A | MUX-LVDS Ground Voltage | Analog In | 2 | DC-Voltage Generator of 0 V |
| | VDD_X | Common Block Supply Voltage | Analog In | 1 | DC-Voltage Generator of 3.3 V ± 5 % |
| | GND_X | Common Block Ground Voltage | Analog In | 1 | DC-Voltage Generator of 0 V |
| Channel#7 Buffer 2 PADs | anaa | $DA_{3oa}$ of Channel#7 | Analog Out | 1 | 1 pF Cap |
| | anab | $DA_{3ob}$ of Channel#7 | Analog Out | 1 | 1 pF Cap |
| | VDD_BUFF | Buffer Supply Voltage | Analog In | 1 | DC-Voltage Generator of 3.3 V ± 5 % |
| | VDD_BUFF | Buffer Ground Voltage | Analog In | 1 | DC-Voltage Generator of 0 V |
| | BIT_BUFF | Buffer Power ON bit | Digital In | 1 | Vpulse Generator |
| External Bias 3 PADs | Ib_10 u | Current Generator | Analog In | 1 | Current Generator of 10 µA ± 5 % |
| | VDD_BIAS | External Bias Supply Voltage | Analog In | 1 | DC-Voltage Generator of 3.3 V ± 5 % |
| | GND_BIAS | External Bias Ground Voltage | Analog In | 1 | DC-Voltage Generator of 0 V |
| Supplies 3 PADs | VDD_PAD | Padring Supply Voltage | Analog In | 1 | DC-Voltage Generator of 3.3 V ± 5 % |
| | GND_PAD | Padring Ground Voltage | Analog In | 1 | DC-Voltage Generator of 0 V |
| | GP | Padring Ground Plane | Analog In | 1 | DC-Voltage Generator of 0 V |

# BACK-UP SLIDES

## Outline

- Differential Amplifiers
  - Generic Scheme
  - DA1
  - DA2
  - DA3
  - Chain Frequency Responses
  - Transient Signals
  - Noise Performance
- ToT Mode (DISC1 Output)
- ADC Mode (DISC2 Output)
- Layout Comparison
- Power Consumption Comparison ←←←

# POWER CONSUMPTION

## Version 4

| Name | Description | Value | |
|---|---|---|---|
| $I_{VDD1}$ | CSP<br>External Bias | 8x3.9mA=31.2mA<br>90.77µA | 31.3mA |
| $I_{VDD2}$ | Channel Bias<br>Hysteresis Block<br>DA1<br>DA2<br>DA3<br>DA4<br>Wilkinson | 8x0.653mA=5.22mA<br>8x82.05µA=0.656mA<br>8x0.744mA=5.95mA<br>8x0.746mA=5.97mA<br>8x0.743mA=5.94mA<br>8x0.739mA=5.91mA<br>8x1.57mA=12.56mA | 42.2mA |
| $I_{VDD3}$ | DISC1<br>DISC2<br>Wilkinson Phase Gen | 8x1.22mA=9.76mA<br>8x1.56mA=12.48mA<br>8x0.66mA=5.28mA | 27.5mA |
| $I_{VDD4}$ | Common Block<br>Jtag<br>MUX | 1.11mA<br>45.94nA<br>8x1.06nA | 1.1mA |
| $I_{VDDQ}$ | CH7 Buffer<br>LVDS | 11.21mA<br>8x6.14mA=49.12mA | 60.3mA |

- Total Current Consumption: 162mA → 535mW @ 3.3V Supply Voltage
- Termination: 100Ω
- Channel Current Consumption ≈ $(I_{VDD1}+I_{VDD2}+I_{VDD3})/8+I_{MUX}+I_{LVDS}$≈18.76mA
  →→→ 61.9mW/channel

# POWER CONSUMPTION

## Version 5

| Name | Description | Value |
|---|---|---|
| $I_{VDD1}$ | CSP | 31.5mA |
| $I_{VDD2}$ | Channel Bias<br>DA1<br>DA2<br>DA3<br>DA4 | 28.7mA |
| $I_{VDD3}$ | Hysteresis Block<br>DISC1<br>DISC2<br>Wilkinson<br>Wilkinson Phase Gen | 42mA |
| $I_{VDDA}$ | MUX - LVDS | 49.1mA |
| $I_{VDDX}$ | Common Block | 1.11mA |
| $I_{VDD\_BUFF}$ | CH7 Buffer | 10.57mA |
| $I_{VDD\_JTAG}$ | Jtag Interface | 45.9nA |
| $I_{VDD\_BIAS}$ | External Bias | 90.8µA |
| $I_{VDD\_PAD}$ | Padring | 303.3nA |

- Total Current Consumption: 163mA → 538mW @ 3.3V Supply Voltage
- Termination: 100Ω
- Channel Current Consumption = $(I_{VDD1}+I_{VDD2}+I_{VDD3}+I_{VDDA})/8$=18.9mA
  →→→ 62mW/channel

# POWER CONSUMPTION

## Comparison

| | Values | | |
|---|---|---|---|
| | **ASD2_V4** | **ASD2_V5** | **ASD_V6** |
| Total Current Consumption | 162mA | 163mA | 164mA |
| Channel[1] Current Consumption | 18.7mA* | 18.9mA* | 19.05mA* |
| Channel[2] Current Consumption | 12.56mA | 12.76mA | 12.91mA |
| Total Power Consumption @3.3V of Supply Voltage | 535mW | 538mW | 541mW |
| Channel[1] Power Consumption @3.3V of Supply Voltage | 61.9mW | 62mW | 62.86mW |
| Channel[2] Power Consumption @3.3V of Supply Voltage | 41.44mW | 42.10mW | 42.6mW |

ASD1 Channel Power Connsumption → ~35mA @3.3V of Supply Voltage

* 32.7% LVDS
21% CSP
20.2% Wilkinson ADC
16% $DAi_{i=1,2,3,4}$ chain
6.5% DISC

[1] Including CSP+DA1+DA2+DA3+DA4+DISC1+WILKINSON ADC+MUX+LVDS
[2] Including CSP+DA1+DA2+DA3+DA4+DISC1+WILKINSON ADC