MDT-ASD ("Legacy ASD")
History, design choices, and motivations

John Oliver

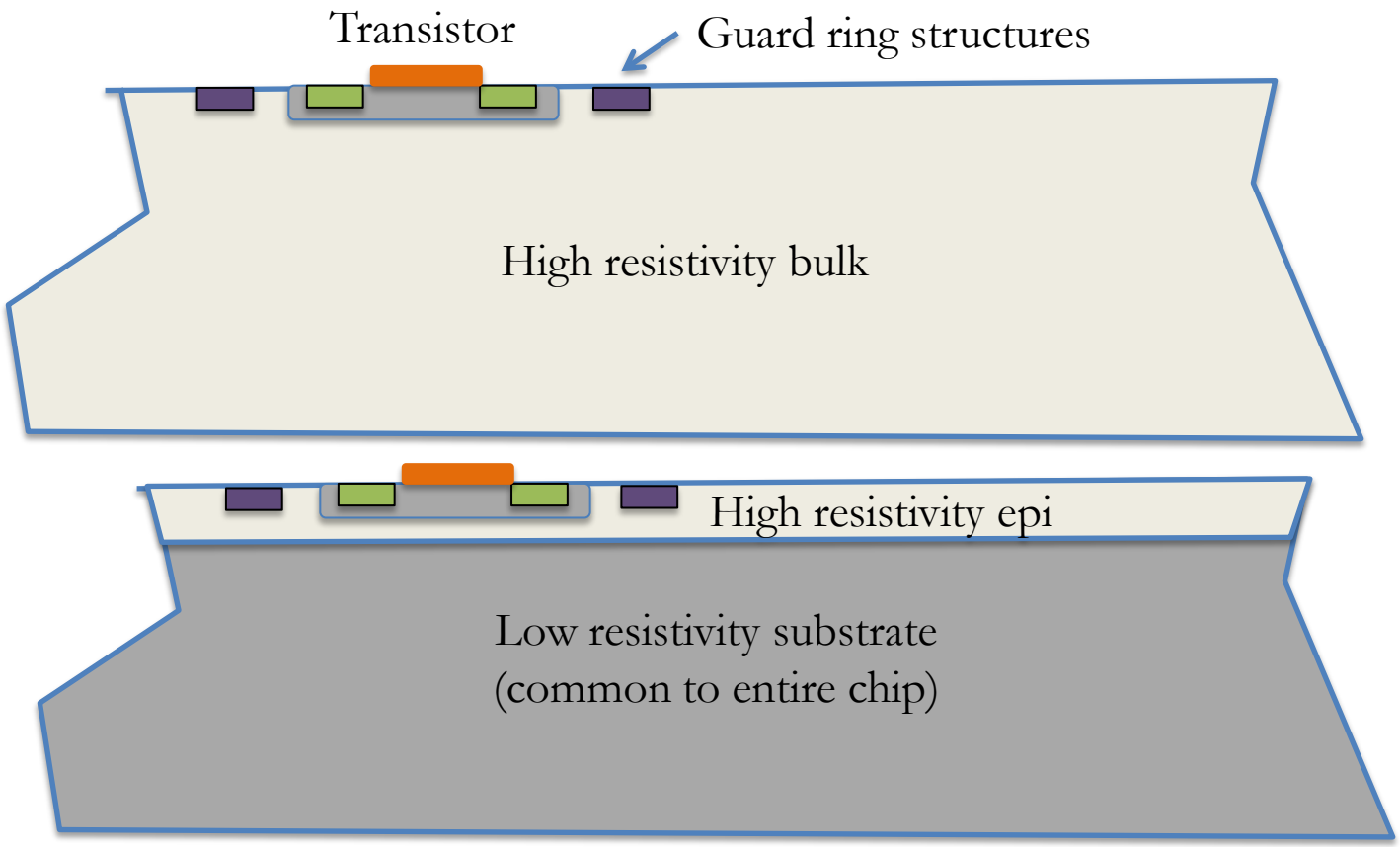
- Major design work done ~ 1998 – 2001
  - John Oliver – Harvard University
  - Eric Hazen, Christophe Posch – Boston University
- For complete description, see
  "ATL-MUON 2002-2003
  Rev 2.1 10-Sep-2007

ASIC Processes for Muons – A Brief History

- Until 1993, we worked on Muon Spectrometer for SDC (Solenoidal Detector Collaboration) at the Supercollider.
- Worked on bipolar processes with U. Penn – Transision Radiation Detector (or was it Straw Tube Tracker?)
- First discussions with ATLAS started in ~ 1995 after demise of SSC
- At the time, HEP community was experimenting with bipolar, biCMOS[1], and CMOS for detector front ends
- CMOS processes were available in US through MOSIS and prototypes (MPWs) were cheap….very cheap!
- One could build prototype preamps for ~$5k
- Scale (gate length) was getting smaller by the year 3u → 1u → 0.5u
- We started building & testing preamp/shapers using 1u then headed to 0.5u ~ 1997 or so
- Settled on HP 0.5u CMOS through MOSIS
- Process was *epitaxial,* not by our choice, but that's what was available (see following slide)
- Process yielded peaking times ~ 15ns deemed "good enough" for MDT shaping

[1] eg "DMILL"

Bulk vs Epitaxial CMOS



Transient electric field lines generated in transistors tend to terminate on

- Guard ring structures in bulk processes
- Guard ring structures **and** substrate in epi processes →Dangerous!
- Epi processes were used commercially to prevent transistor "latchup" in inverter and other structures
- Note that these CMOS structures were "simple" at the time, not sophisticated as today's processes → no "trenches" or other fancy stuff!

Table 3. HP 0.5µ CMOS process parameters

Parameter	n-channel	p-channel	either	Units
Minimum gate length			0.5	µm
Threshold voltage (typ)	0.76	0.88		V
Kprime	92	26		$\mu A/V^2$
N+ diffusion sheet resistance	2.2	2.2		Ω/sq
Poly sheet resistance (silicided)			2.0	Ω/sq
Poly sheet resistance (silicide blocked)			130	Ω/sq
Gate oxide thickness			100	Å
Gate capacitance			3.5	$fF/\mu m^2$
Linear capacitor			2.3	$fF/\mu m^2$
Vbkd	11.3	-9.6		V

Passive components

a) Resistors: Silicide blocked poly → ~ 12kΩ easy
b) Capacitors: "Linear" or MIM up to 10pf or more
c) Capacitors built in two vertically opposite halves to equalize bottom plate strays

Table 2. ASD analog specifications

Input impedance	$Z_{IN} = 120\ \Omega$
Noise	ENC = 6000 e^- rms or ~ 5 primary electrons (pe^-)
Shaping function	bipolar
Shaper peaking time	$t_p = 15$ ns
Sensitivity at discriminator input	1.65 mV/pe (gas gain 2×10^4) or 8.9 mV/fC (delta pulse into terminated MDT)
Linear range	1.5 V or 900 pe^-
Nominal threshold setting	40 mV or 24 pe^- (~ 5 σ_{noise})

Notes

a) Zin (120 Ω) small compared with Z0 of tube (380 Ω)

b) Noise dominated by termination

Circuit Architecture
&
Motivation

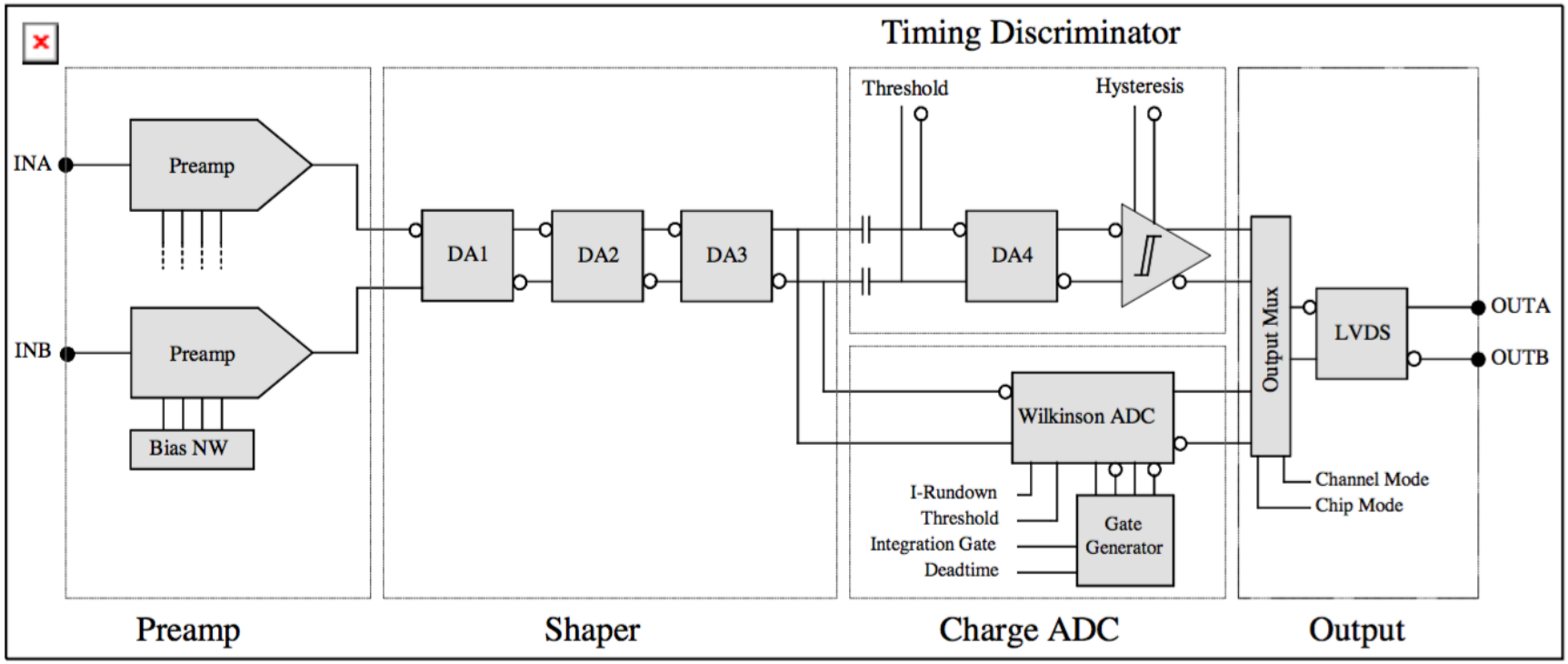


Figure 2. MDT-ASD channel block diagram

Circuit Architecture
&
Motivation

- Concern that epitaxial process (low resistivity substrate) can lead to substrate coupling if one is not careful
- Any transients coupled into substrate anywhere can couple back into high gain input stages.
- Guard rings will not prevent this.
- Decided on fully differential architecture all the way through.
- Two independent low input impedance transimpedance preamplifiers (Idea comes from **Mitch Newcomer** who used this configuration for Straw Tube Tracker [I think?] in bipolar process)
- Motivation for this configuration was to render any input pickup differential, and thus cancelled by subsequent stages.
- This feature works "sort of" but less effective than one might think. To be fully effective, input external (R & C) loads on both preamps would have to be the same. Actually, they are very different.
- Differential feature makes for easy DC balance after preamps

Circuit Architecture
&
Motivation (continued)

- < 15ns peaking time, fast fall time → Transimpedance amplifier ie **not** a charge integrator
- Multiple gain/shaping stages with pole/zero networks to yield final bipolar shaping
- All control logic (real time) is hand built and fully differential.
- All real time logic traces (differential) sit over bypassed well to further isolate from substrate.
- Result was that no digital substrate coupling was ever observed.