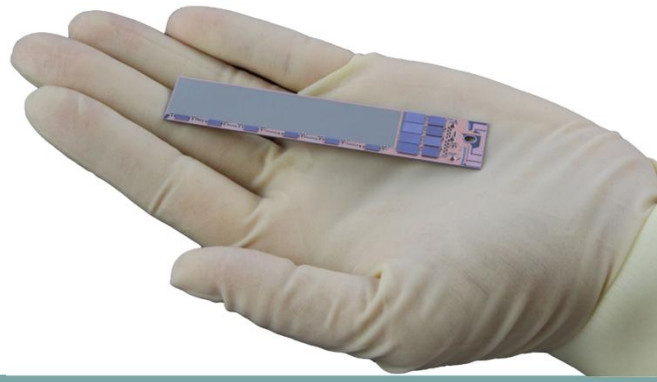
Phase 2 Module W37_IF

Gated Mode with Final Chip Set
August 2nd 2017

C. Koffmane



PXD9 Sensor Yield

Combined	PXD9-6 (3 wafers)			PXD9-7 (4 wafers)				PXD9-8 (9 wafers)								
Wafer arrangement	W30	W35	W36	W31	W37	W38	W40	W32	W33	W41	W42	W43	W44	W45	W46	W47
Inner Forward	G58.4	G98.4	G99	G98.9	G98.4	B98.8	G100	G100	B98.4	G99.5	G99.3	G100	G99	M99.5	G99.5	G99.5
Outer Forward 1	G99.9	G98.4	G99	G98.4	G98.1	B98.4	G99.5	G99.5	G100	G99.5	M100	G100	G100	G99.5	G100	G98.1
Outer Forward 2	G99.5	M99	G99.5	G99	B98.4	B98.4	M99.5	G100	G100	B99.5	M100	B99.5	G100	G100	G99.9	B98.4
Outer Backward 1	G97.5	G88	G98.4	G99.4	G98.4	G97.9	M100	B99	G99.5	B98.4	G99.5	B38.4	G99	B99.5	G99.5	B98.4
Outer Backward 2	G98.6	G96.9	G98.6	G99.5	G99.5	B98.1	G99.9	G100	B99	B98.4	G100	M99.9	G100	G100	G100	B98.4
Inner Backward	G97.9	M100	G99.5	G100	G98.4	G98.4	G100	G100	B98.4	G100	G100	G100	G100	G100	G99.5	G99.5

Combined	PXD9-9 (6 wafers)						PXD9-10 (6 wafers)						
Wafer arrangement	W01	W02	W03	W04	W05	W06	W07	W08	W09	W10	W11	W12	W13
Inner Forward	B95	G99	G99	G99	G99.3	G98.8	B17.9	G99.5	G99.4	G99	G99.3	B100	G99.5
Outer Forward 1	G99.6	G99	B99.2	G99.3	G99.5	G98.9	B37.9	B99	G99	G98.4	G99	G99	G97.9
Outer Forward 2	B98.2	B99	G99.4	B98	G99.3	G97.9	B37.9	G99.5	G99.5	G98.4	G99	M98.9	B98.2
Outer Backward 1	G100	B98.9	G99	M99	G99	G99	B37.9	G99	G99	G98.4	B95.5	G99.5	B98.2
Outer Backward 2	B99	B98.9	B99.4	B99.5	B98.9	B99	B37.9	G99	M99.5	B97.6	B98.8	G99	G98.4
Inner Backward	G94.4	M99	G100	M99.5	G98.4	M99.5	B17.9	B99.5	G100	B99	M98.7	B99	G99

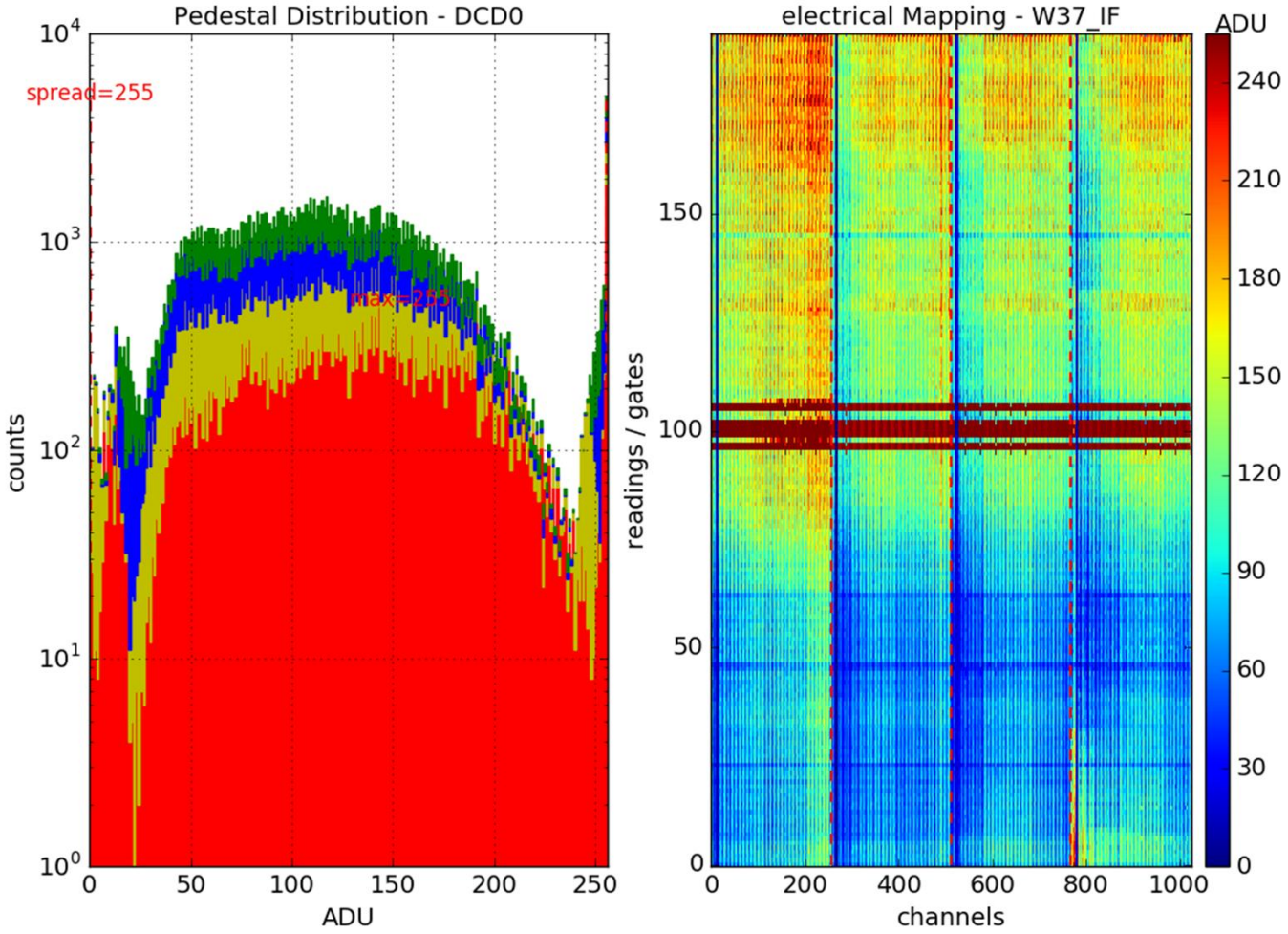
	REQ	G99	G98	G95	M99	M98	M95
Inner Forward	8	17	3	0	1	0	0
Outer Forward	12	26	6	2	3	1	0
Outer Backward	12	22	3	1	4	0	0
Inner Backward	8	13	3	0	3	1	0

G: good
M: medium
B: bad
The number behind gives the minimal percentage of live pixels on the sensor

Almost 2x prime grade sensors available

C. Kiesling, 27th B2GM, Plenary Session, KEK, Japan, June 19-23, 2017

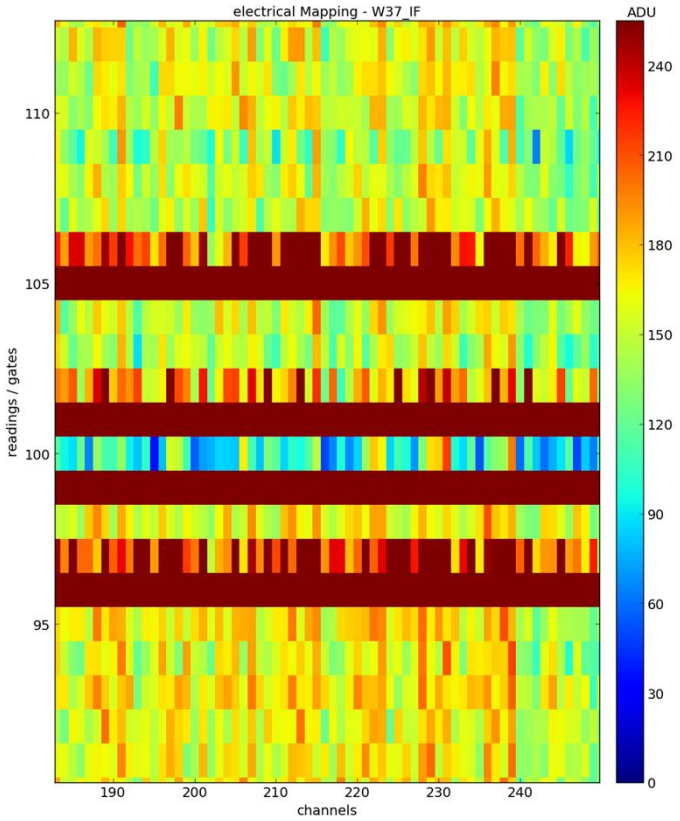
Pedestal Distribution



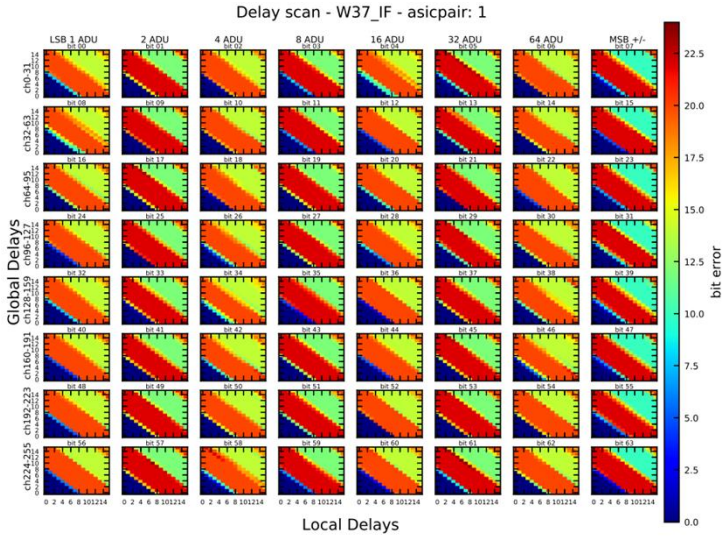
- Sanity check at MPP
  - 9 pedestals show ~8 gates w/ high ADU values (probably no clear)

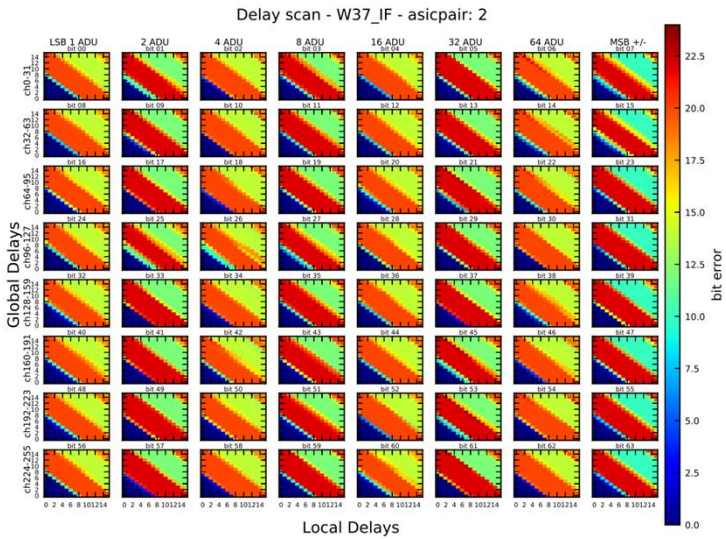
Pedestal Distribution

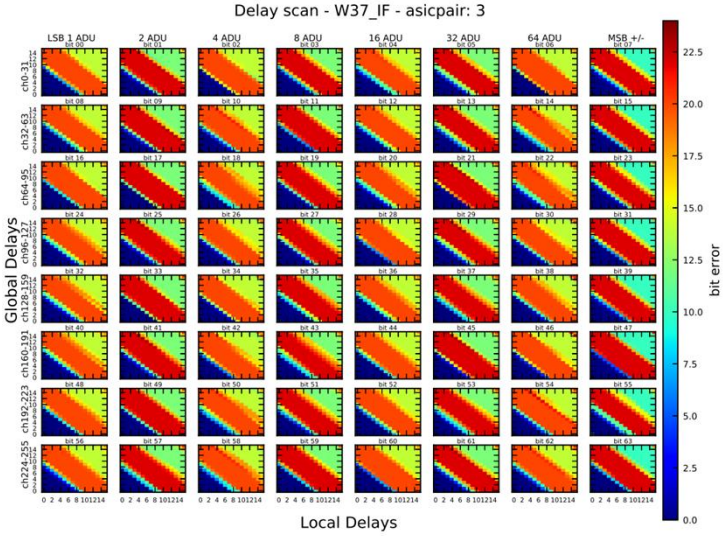
- Using different VNSubIn
- 4 gates seem to be broken
  - 2.1% of the pixels
- The next gate in the rolling shutter mode is affected as well
  - 4.2% of the pixels can not be used

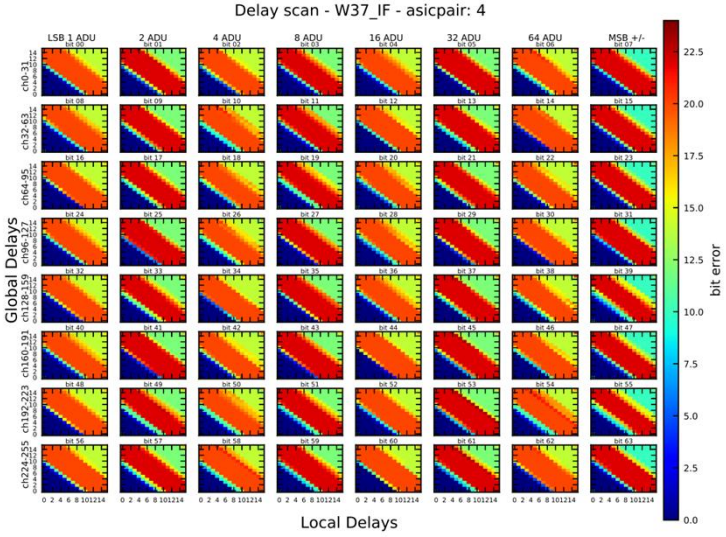


W37_IF Delays @ 76.33 MHz

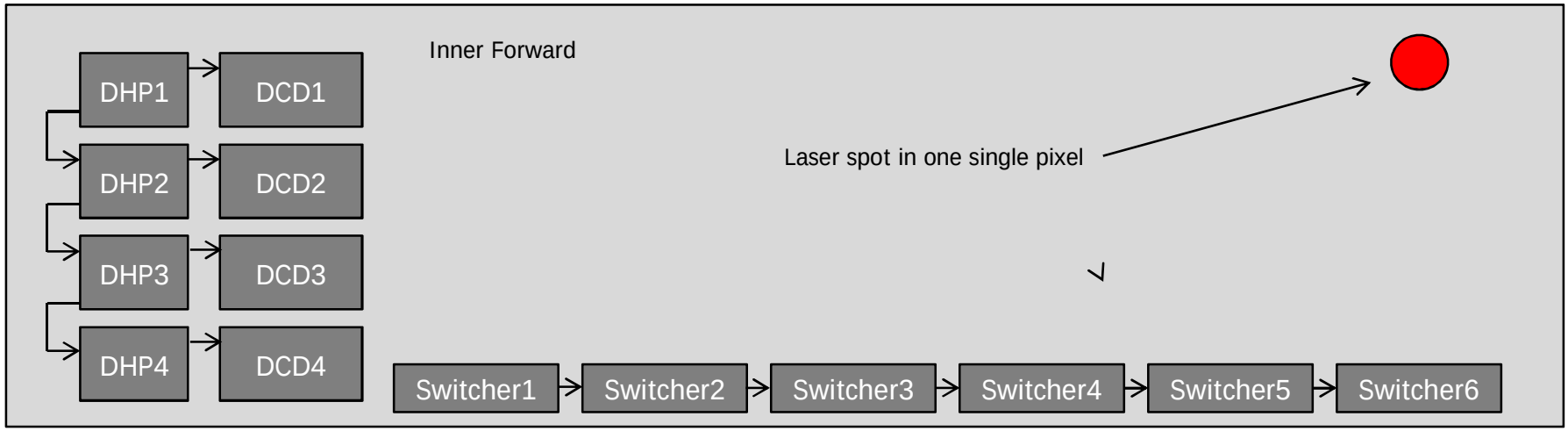


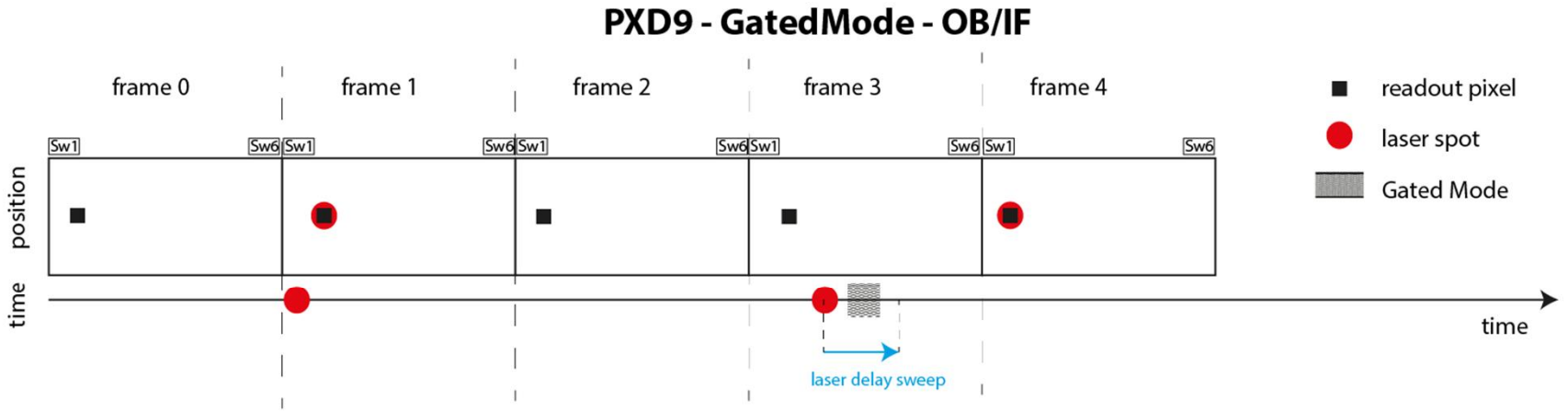






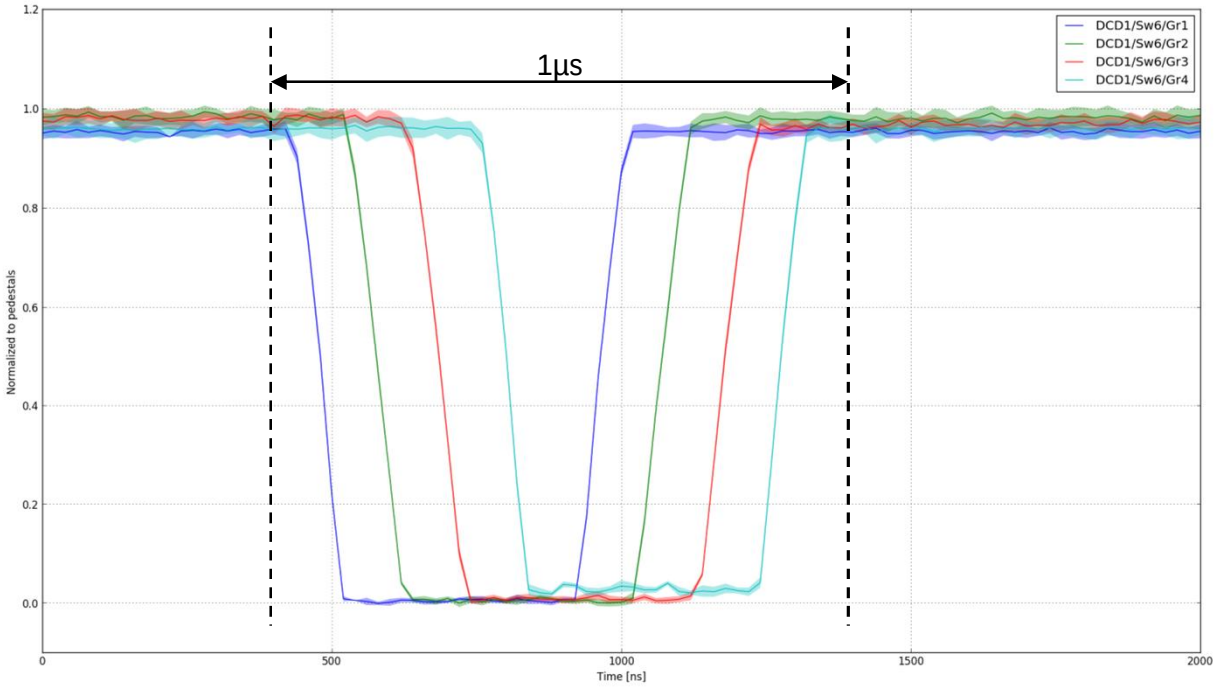
Gated Mode Laser Tests





frame 0: pedestals
frame 1: pixel shows signal of the laser impinging in frame 1 (right before the pixel is read)
frame 2: pixel shows Clear efficiency
frame 3: pixel shows pedestal value; gated mode is switched on ; laser is impinging
frame 4: pixel shows signal (charge conservation & junk charge prevention), depending on timing of laser

Gated Mode Laser Tests

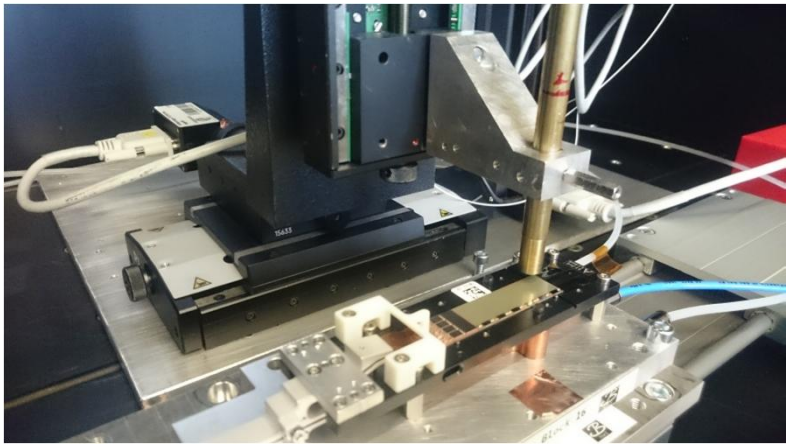


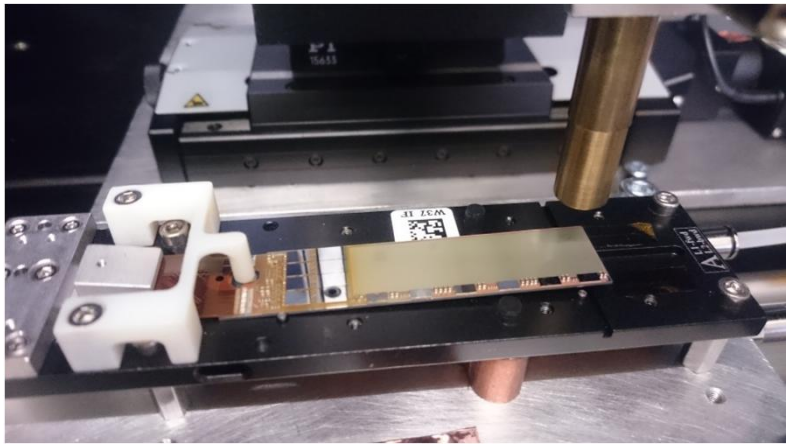
Plot shows the normalized signal charge which is created by the laser before, during and after the Gated Mode.
X-axis shows the timing of the laser.

- New gated mode sequence (since DHPT1.2b does not execute memory address 512 twice)
- Gated Mode with Read-out shields the four tested regions (last switcher, all channel groups)
- Basic verification of the Gated Mode with final ASICs and at nominal frequency: ok
- Detailed investigation on the pedestal oscillation after GM still necessary

Back-up

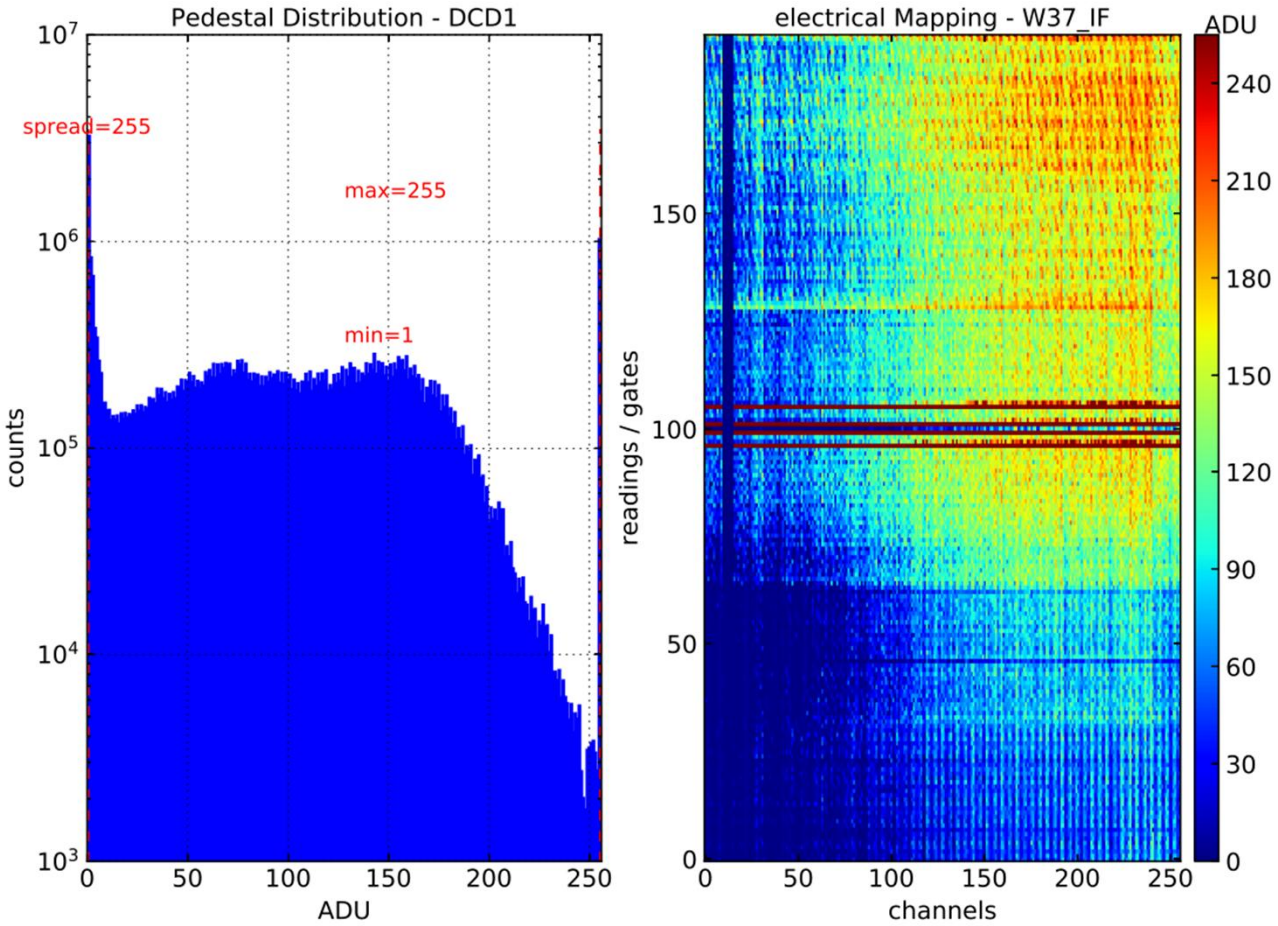
Module Installation at HLL



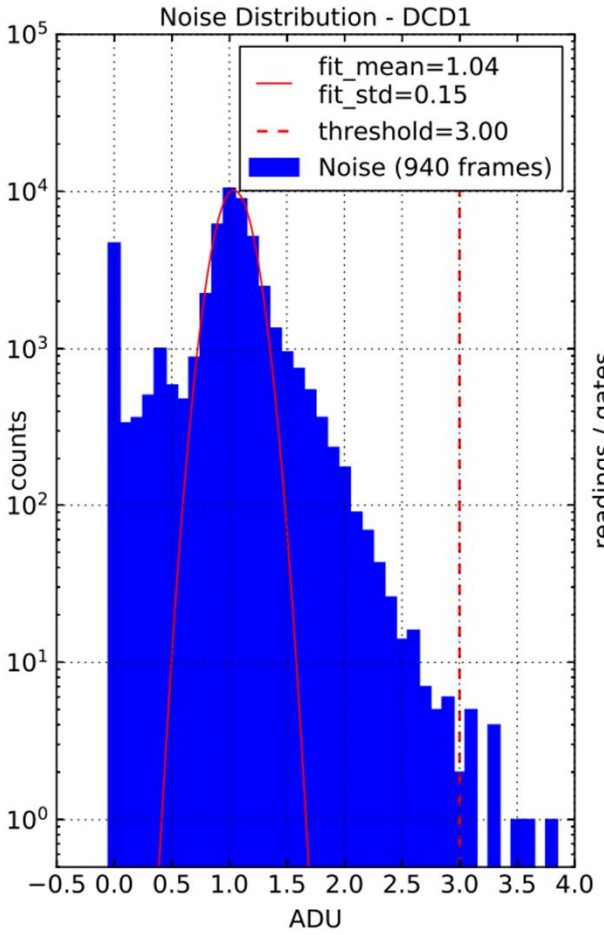


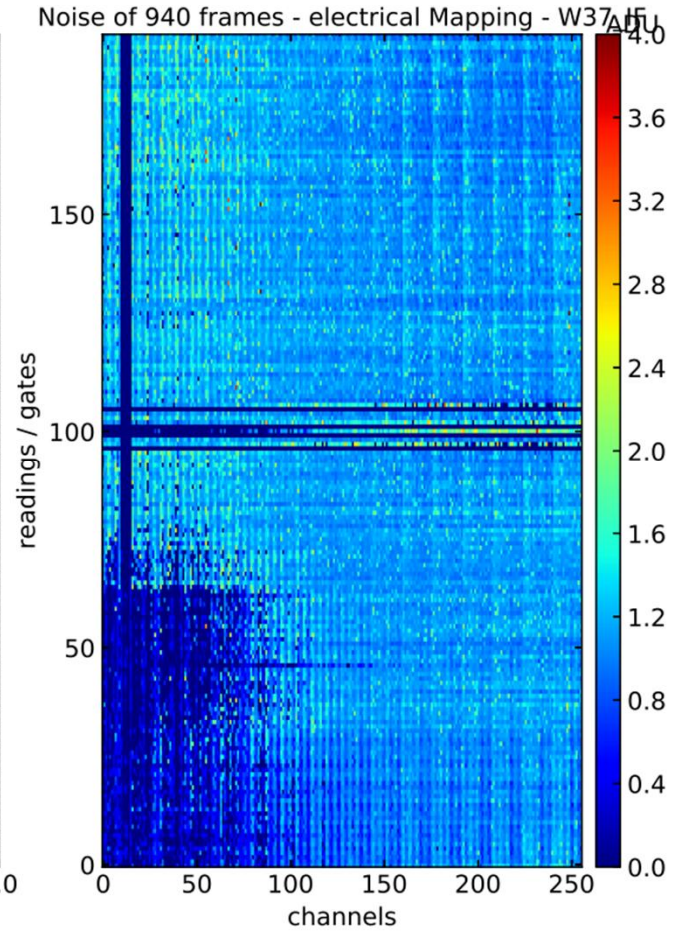
w Clamp alone does not guarantee good thermal contact to the transport jig

W37_IF different VNSubIn DCD1

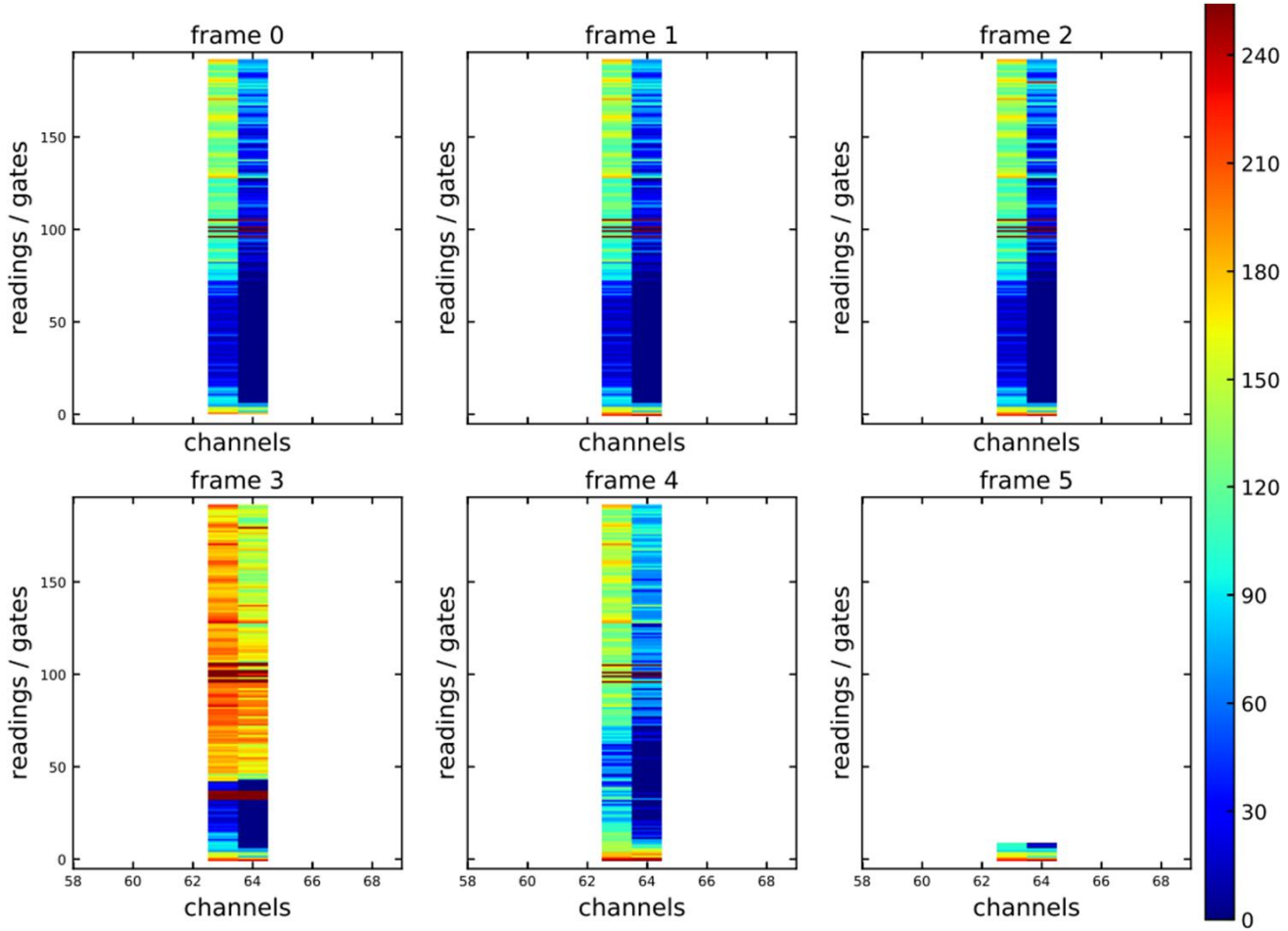


W37_IF Noise DCD1



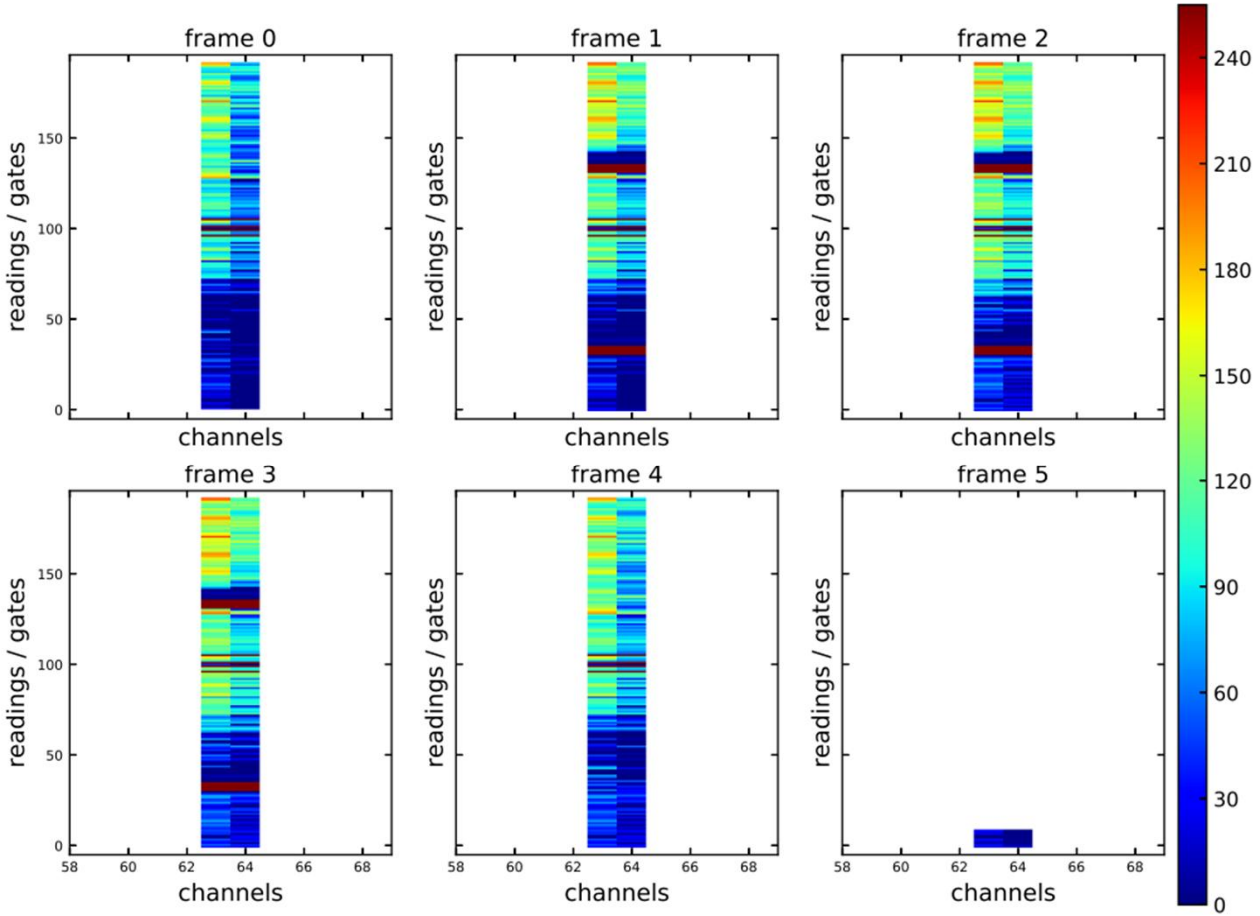


W37_IF Gated Mode during Frame 3



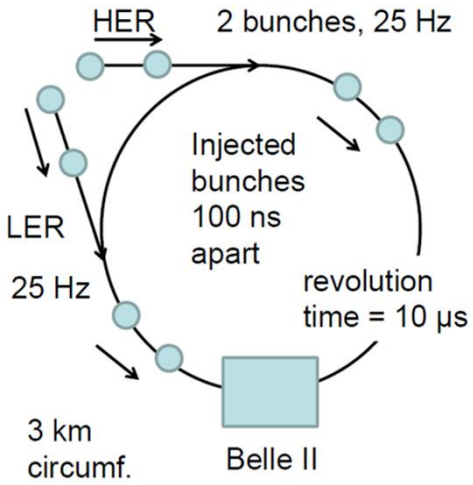
- Ø Long Gated mode timing (Frame3)
- Ø Different pedestals during GM frame

2 x GM in Frames 1, Frame 2 and Frame 3

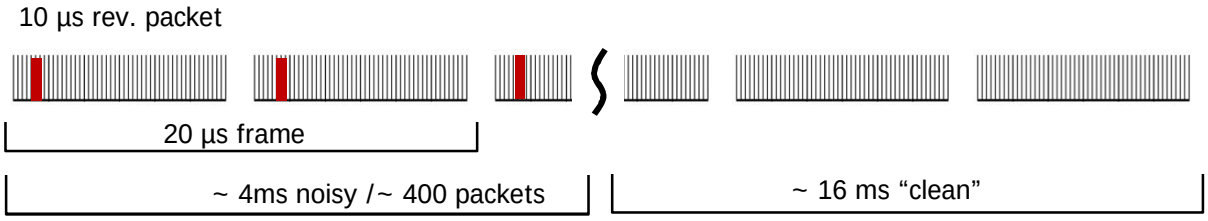


No analog common mode correction

SuperKEKB Injection Scheme – Need of Electronic Shutter



10µs packets with 2503 bunches , 200 ns gap in-between (TDR)



§ continuous injection à ~ 400 revolutions with two noisy bunches (100ns apart) every 20 ms
§ DEPFET integrates two trains, these noisy bunches would blank the frames à 20% loss of data

§ the best solution: gate the DEPFET during the passage of the noisy bunches
§ ~100ns gate, with some rise and fall times, twice per frame à 2x2µs of 20 µs blind
§ assuming 4 ms relaxation time (not clear), ~200 consecutive frames with gate cycles

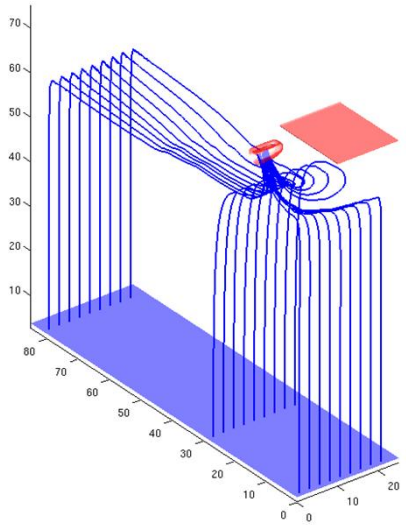
§ DEPFET operation mode during gating: DEPFET off, Clear active (Vgs=3 .. 5V, Vclear=16 .. 20V)

DEPFET Gated Mode Operation

Switching to gated mode:

» DHE receives signal from acc., sends “veto” à DHPT switches to gated sequence à controls Switcher

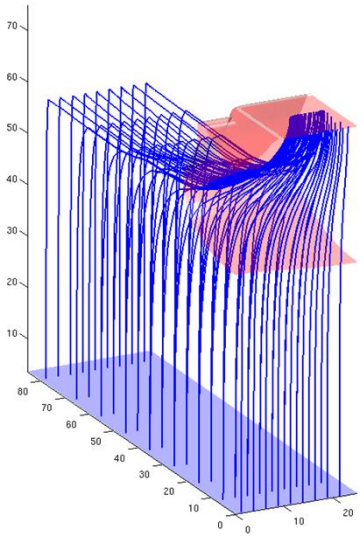
» DCD operation mode remains untouched



Normal charge collection

» Vgs=4V, Vclear=5V

» all signal charge collected in internal gate



Gated mode

» Vgs=4V, Vclear=20V

» all signal charge dumped to *Clear*

Challenge: switch all *Clear* contacts in the matrix from ~5V à ~20V
shown on small matrix, but as expected, it‘s more difficult on large modules

W31_OF1 (PXD9 Pilot Run)