W37_OF1

Summary

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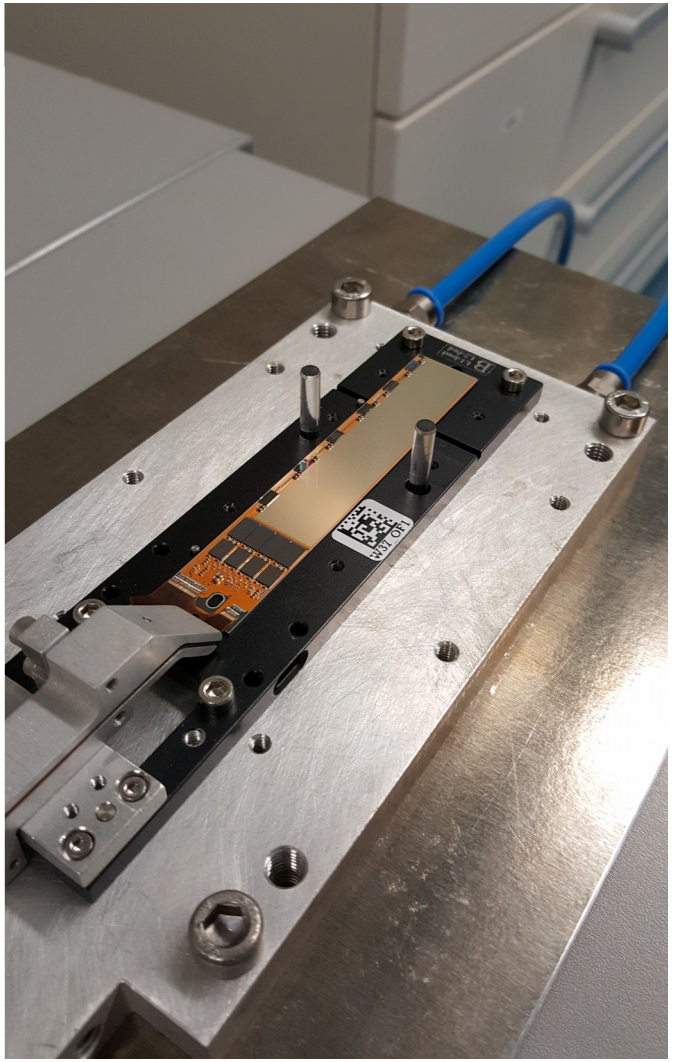
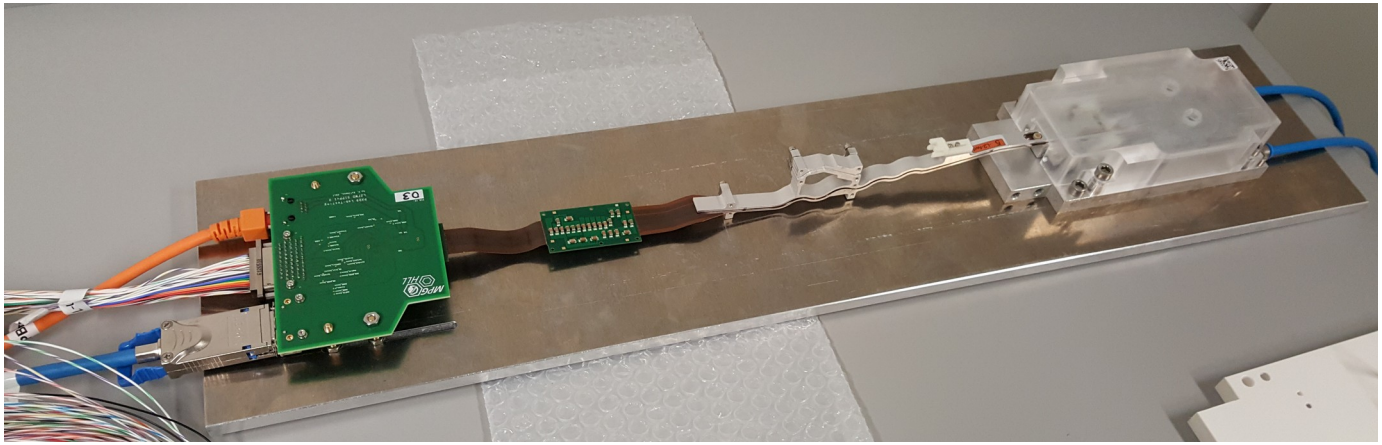
Module Setup

- clamp attached
- inner and outer cover in place
- cooling with chiller at 20°C
- no vacuum





Module Setup

- configDB entry generated from templates
  - file ‘W37_OF1_Goettingen’
- first power up and configuration manually
  - full JTAG chain functional
  - currents at expected levels
  - all HS links up
- now using the automatic power up sequence
- most recent commit: 513 (includes offsets)

Module Parameters

- HS Links:
  - Bias = 210
  - Biasd = 110
  - Delay = 0
- DCD:
  - Amplow = 275 mV
  - RefIn = 725 mV
  - Ipsource = 70
  - Ipsource_middle = 67
  - Ipsource2 = 70
  - IFBPBias = 70
  - Gain = En90
- DCD data delays:
  - Global = 0
  - Local = 4,5
- DCD offset delays:
  - offset_frame_sync_dly = 0
  - offset_des_dly = 8
  - offset_dcd_dlys = [3,4]
- Voltages:
  - Clear-On = 19 V
  - Clear-Off = 5 V
  - Gate-Off = 5 V
  - Source = 6 V
  - CCG = 0 V
  - Guard = -5 V
  - Bulk = 10 V
  - HV = -70 V
  - Drift = -5 V
  - Gate-On = [-1.5V, -1.7V]

Module Temperatures

- measured via DHP temperature diode
- all covers, with clamp, chiller @ 18°C
    - only DHPs powered
        - 25-30
    - DHPs and DCD powered, but DCD analog OFF
        - 30-35

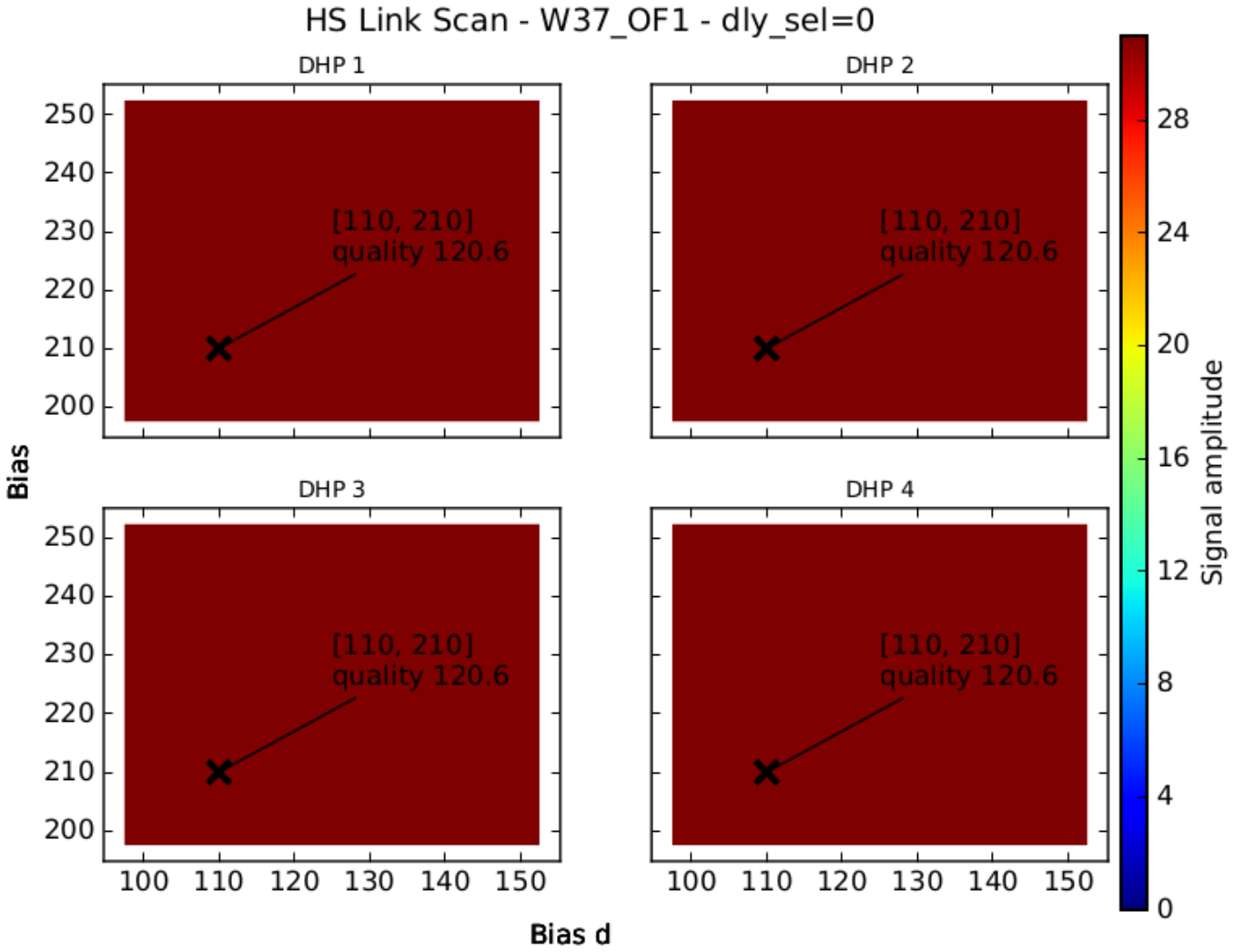
--> for both W37_OF1 and EMCM

- DHPs and DCDs powered and DCD analog ON
    - 50-58
- all powered (DCDs analog ON and matrix)
    - 55-60

- calibration?
    - even with only DHPs powered: 5-10 spread between DHP temperatures

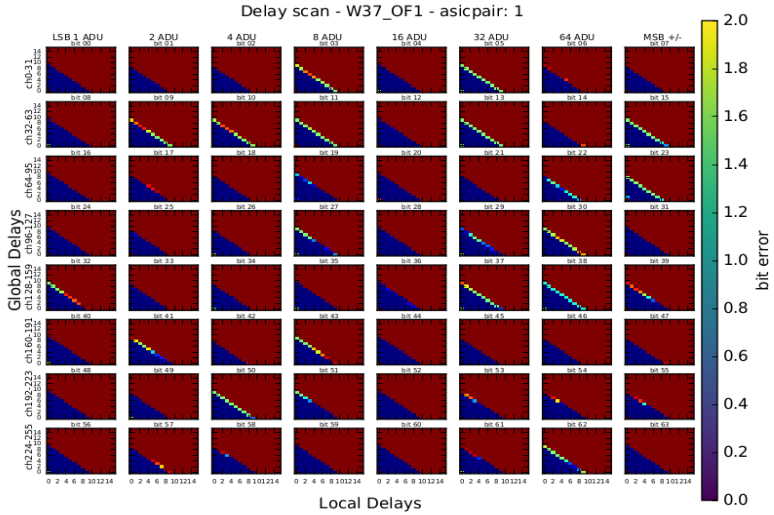
HS Link Optimization

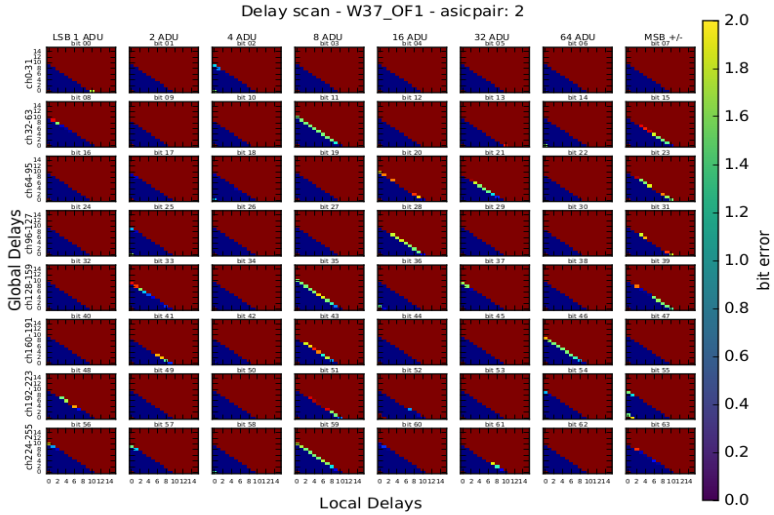
- Scan: https://elog.belle2.org/elog/PXD-Mass-Testing/170
- Analysis: https://elog.belle2.org/elog/PXD-Mass-Testing/171

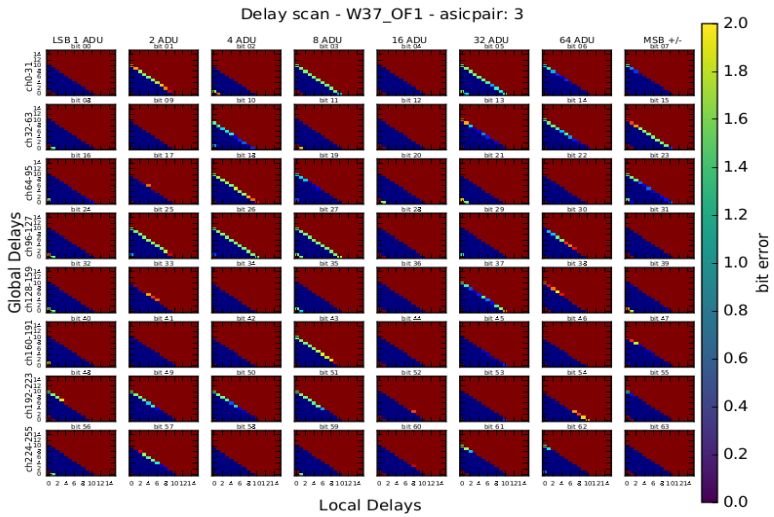


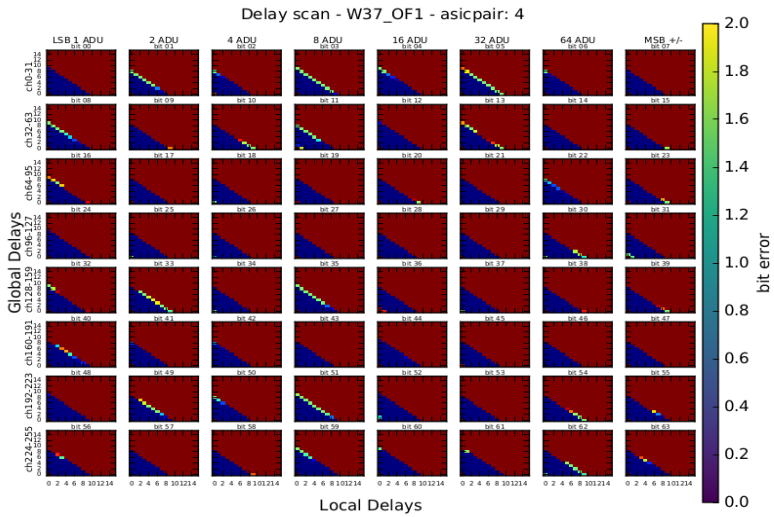
Delay Optimization

- Scan: https://elog.belle2.org/elog/PXD-Mass-Testing/147
- Analysis: https://elog.belle2.org/elog/PXD-Mass-Testing/148

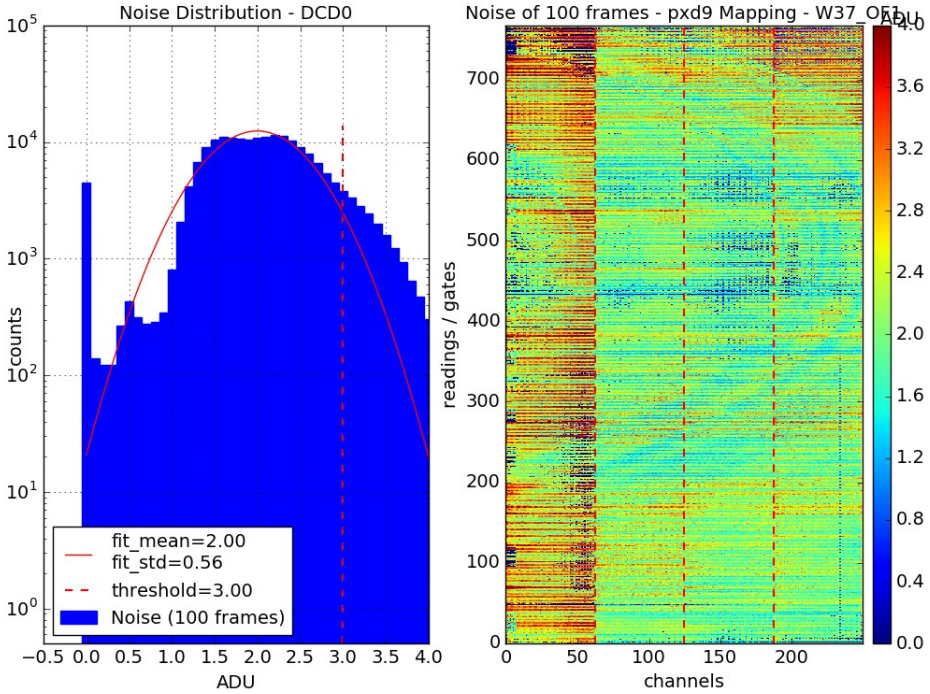


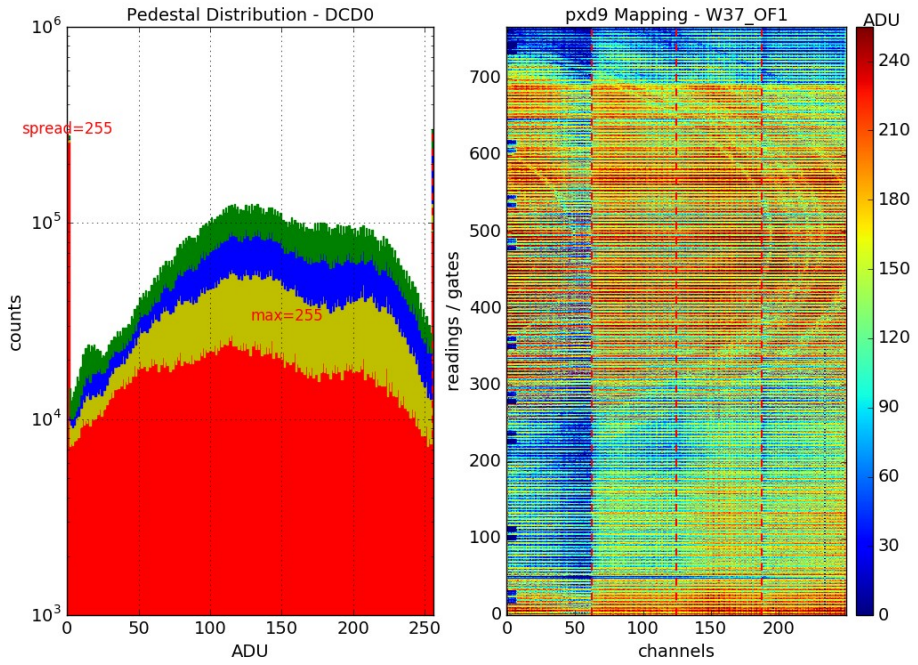






Pedestal and Noise

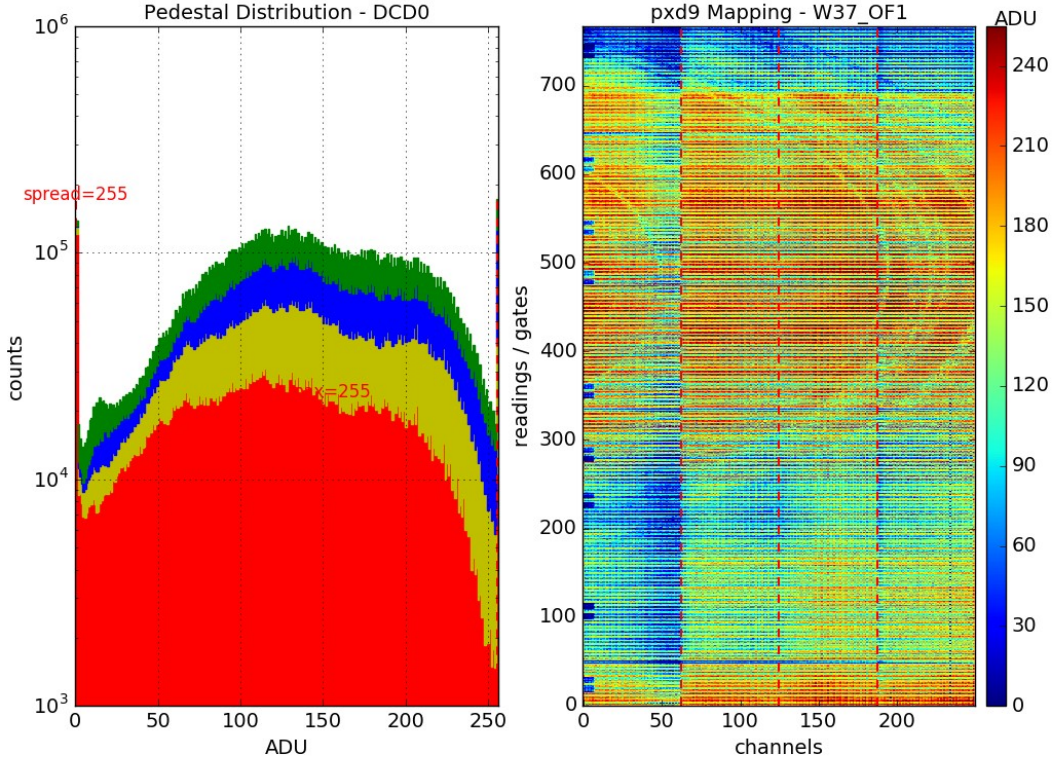




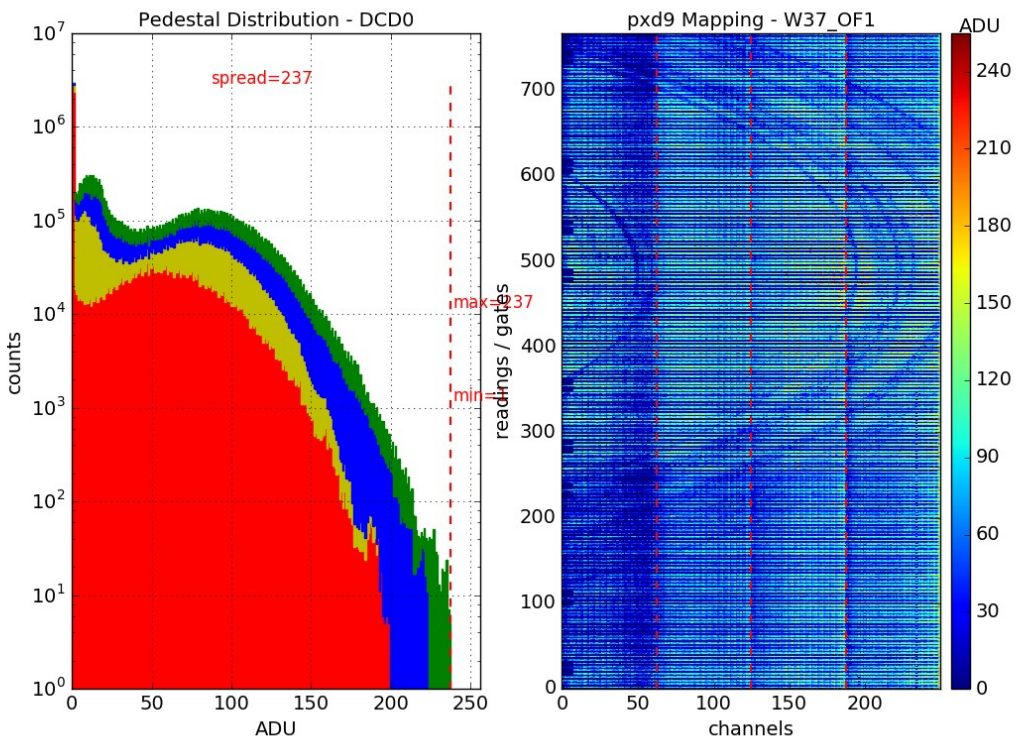
Pedestals with optimized VNSubIn (22 – 22 – 24 – 24) and GateOn voltages (-1500mV, -1600mV, -1700mV)

ACMC

- ACMC off: https://elog.belle2.org/elog/PXD-Mass-Testing/229
- ACMC on: https://elog.belle2.org/elog/PXD-Mass-Testing/228



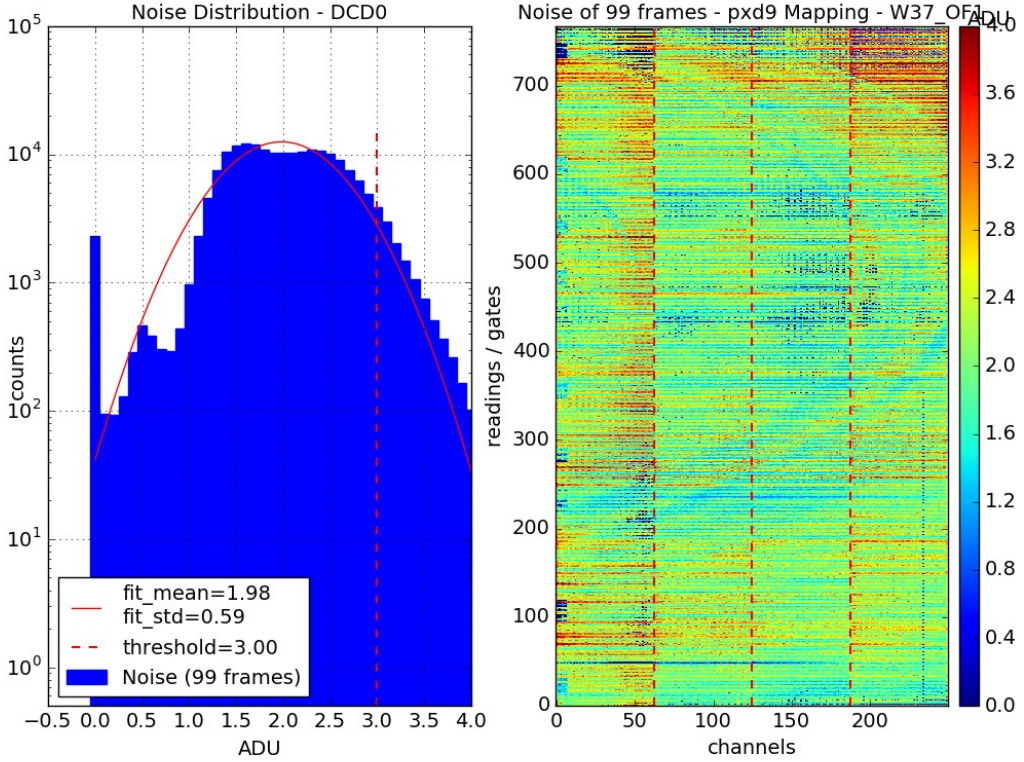
ACMC off



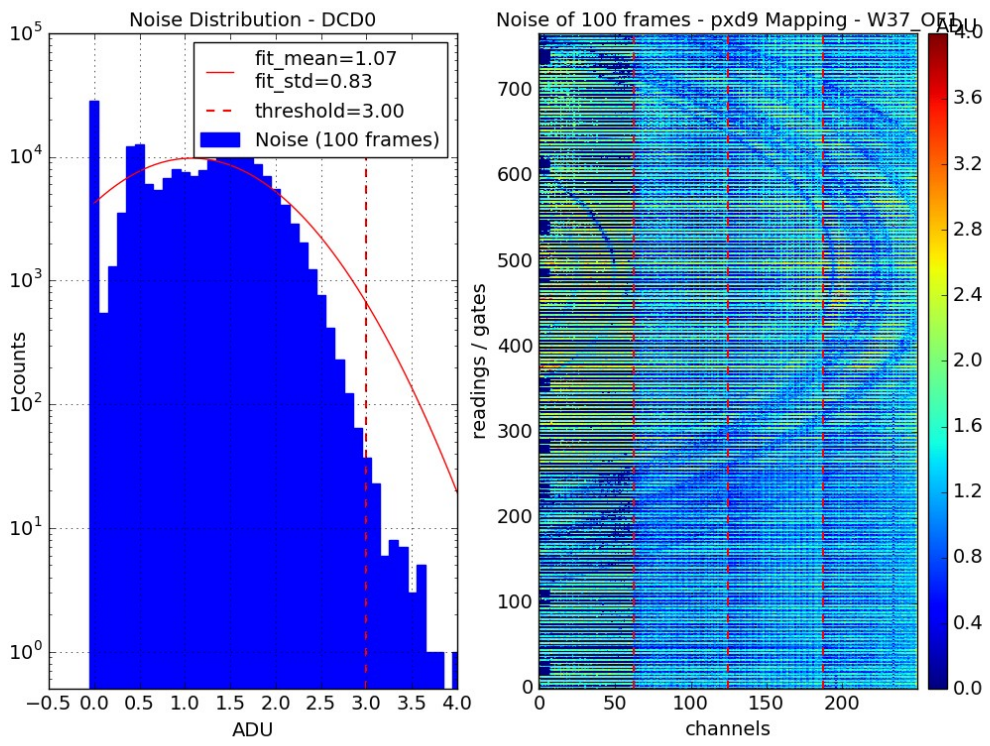
ACMC on

ACMC

- ACMC off: https://elog.belle2.org/elog/PXD-Mass-Testing/229
- ACMC on: https://elog.belle2.org/elog/PXD-Mass-Testing/228

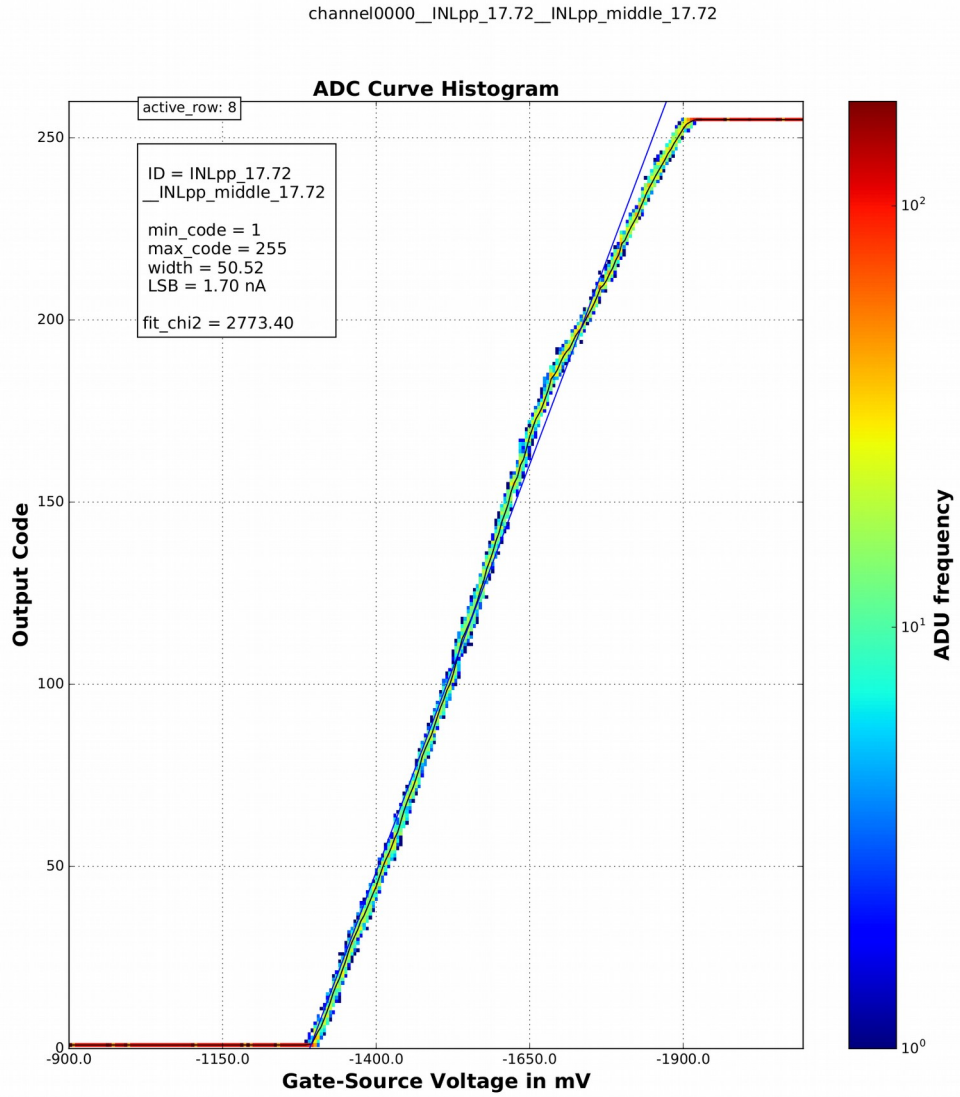


ACMC off



ACMC on

ADC Curves



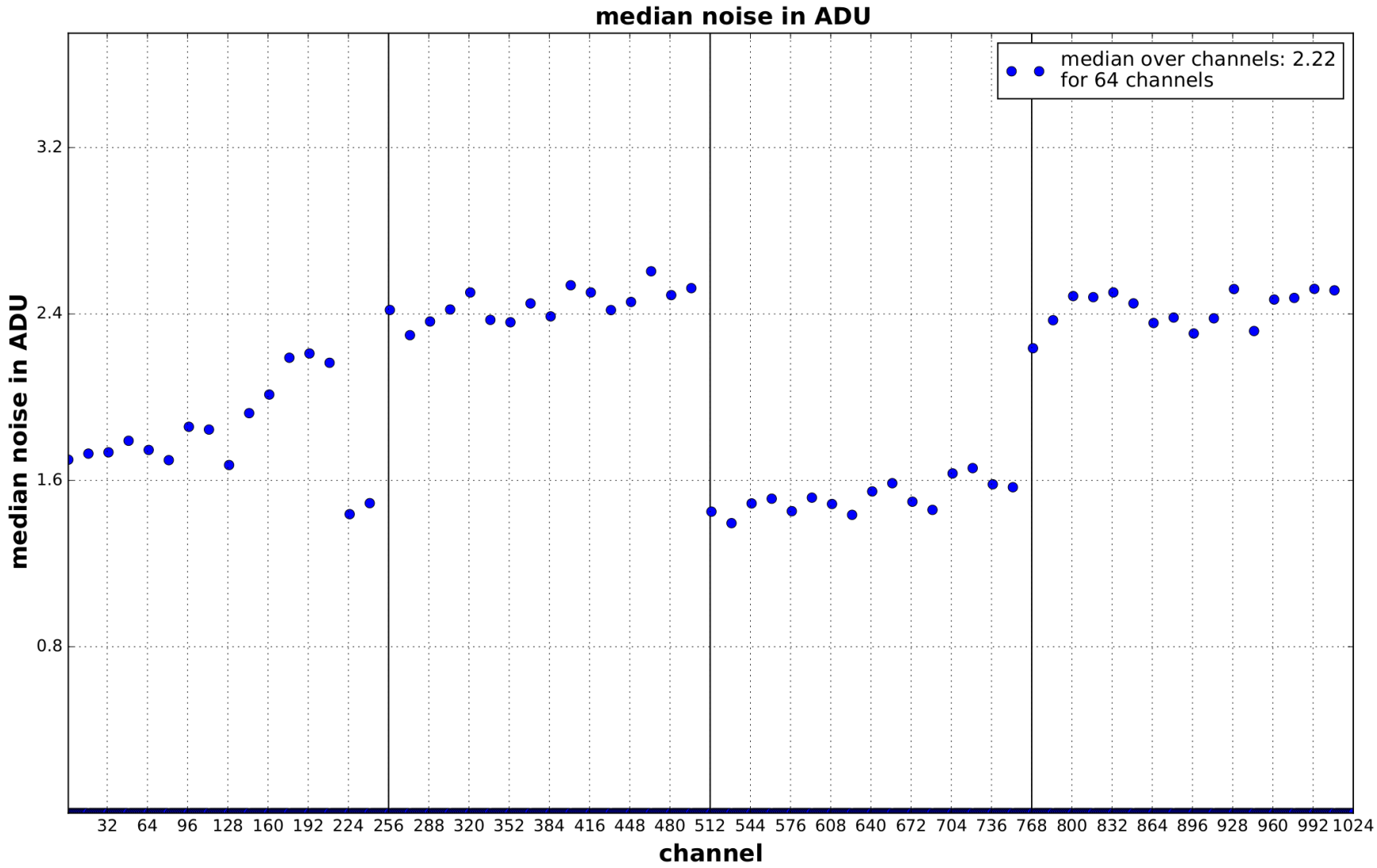
- Only gate source measurements possible

- ADC curves quite noisy

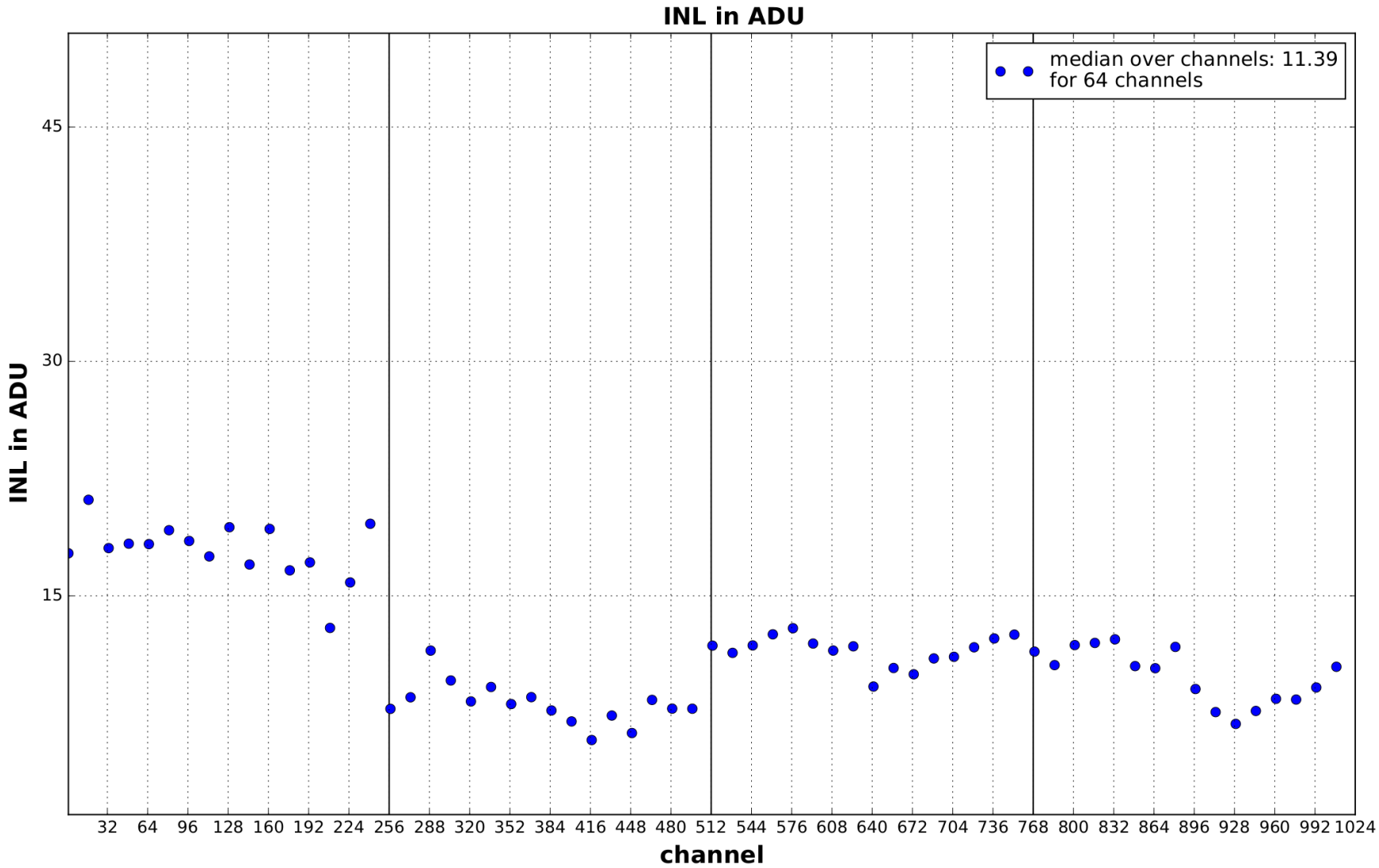
- high INL

- measurement very time consuming (~10 minutes for 64 channels)

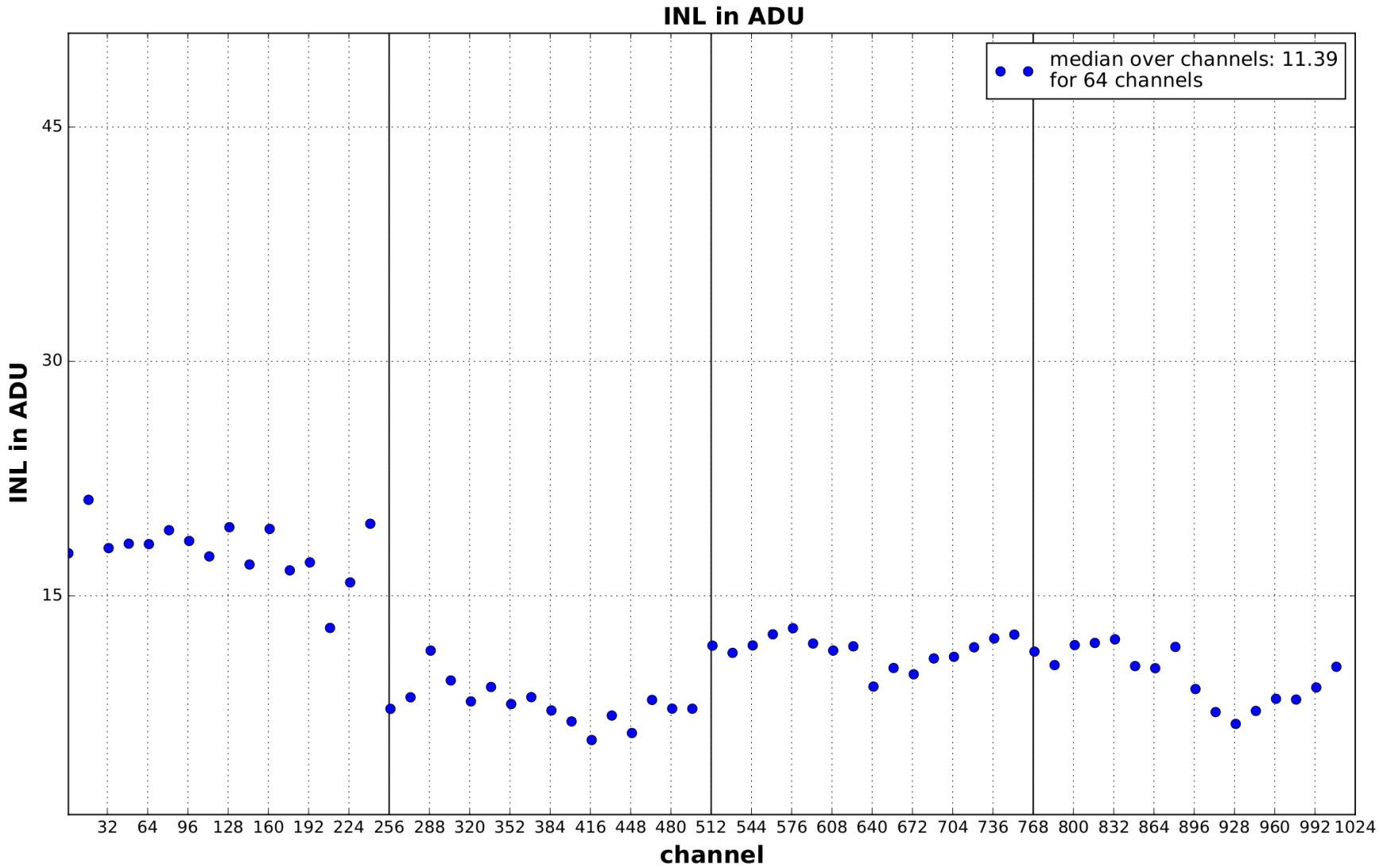
ADC Curves

- 
median noise in ADU
median over channels: 2.22
for 64 channels
median noise in ADU
3.2
2.4
1.6
0.8
32 64 96 128 160 192 224 256 288 320 352 384 416 448 480 512 544 576 608 640 672 704 736 768 800 832 864 896 928 960 992 1024
channel

ADC Curves

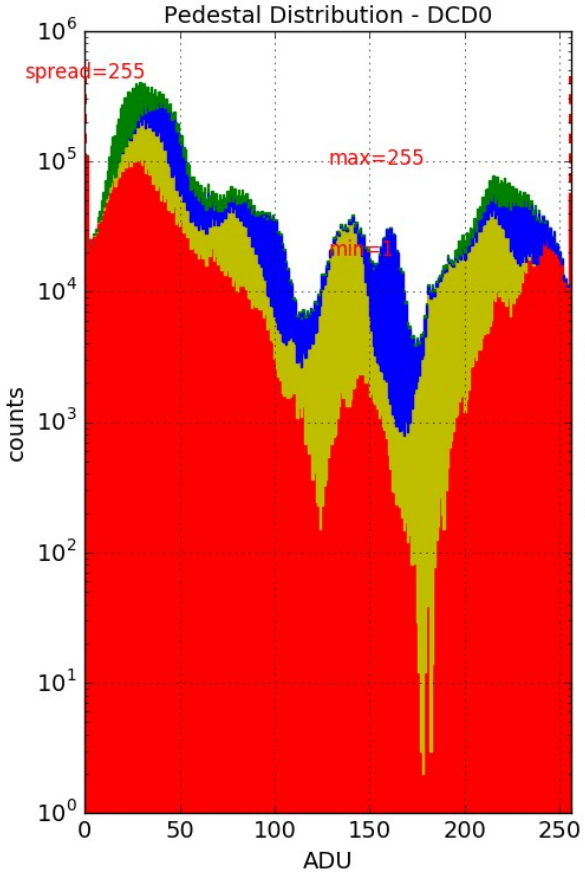
- 
INL in ADU
median over channels: 11.39
for 64 channels
INL in ADU
45
30
15
32 64 96 128 160 192 224 256 288 320 352 384 416 448 480 512 544 576 608 640 672 704 736 768 800 832 864 896 928 960 992 1024
channel

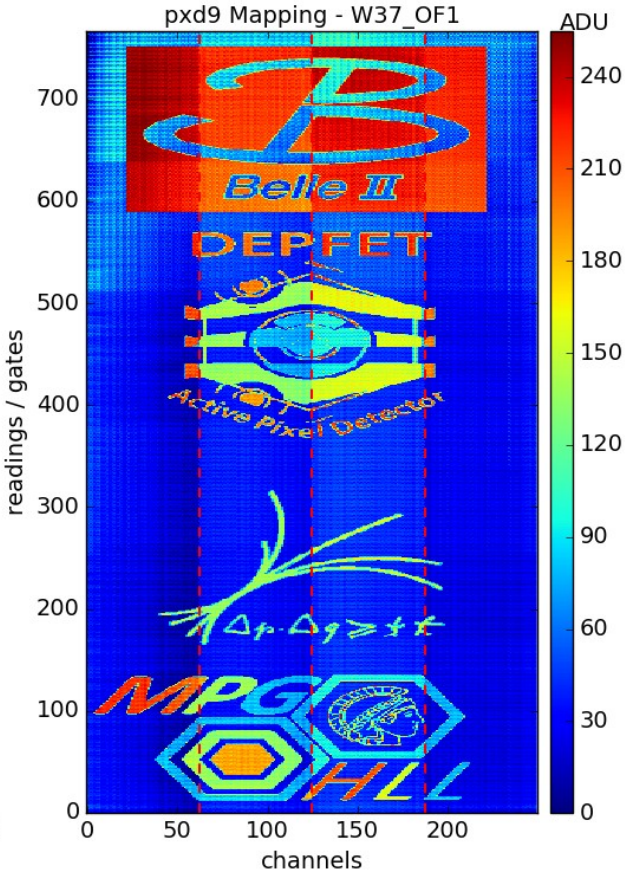
ADC Curves

- 
INL in ADU
median over channels: 11.39
for 64 channels
INL in ADU
45
30
15
32 64 96 128 160 192 224 256 288 320 352 384 416 448 480 512 544 576 608 640 672 704 736 768 800 832 864 896 928 960 992 1024
channel

Offset Delays

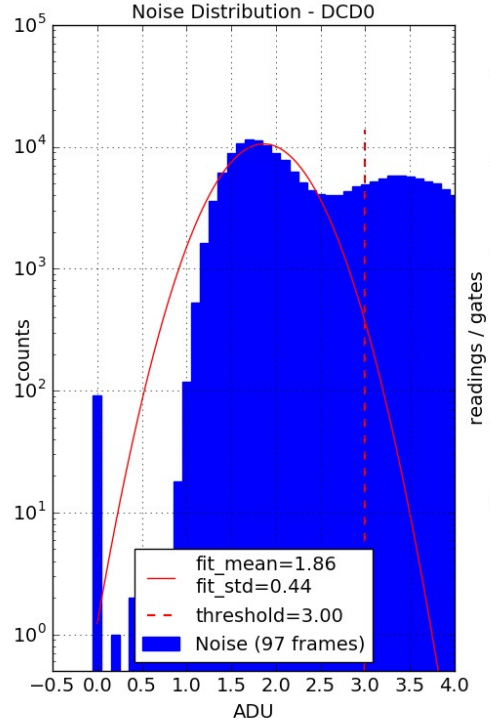
- Matrix blocked (2000 mV) and delay optimization performed
- Local delays set to [3,4]

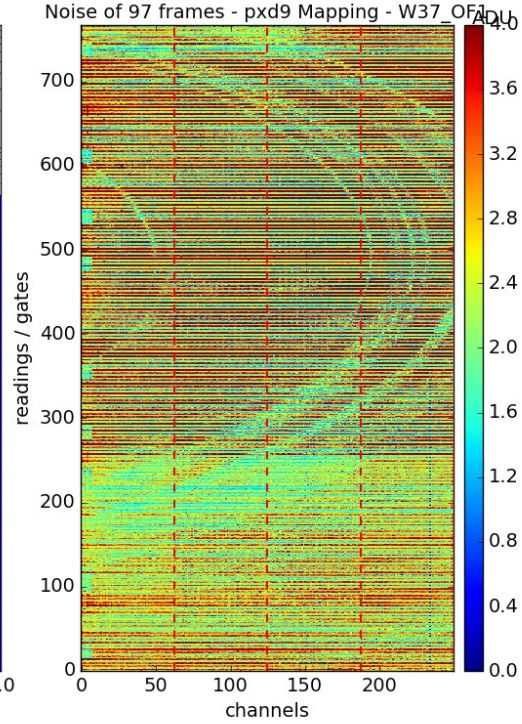


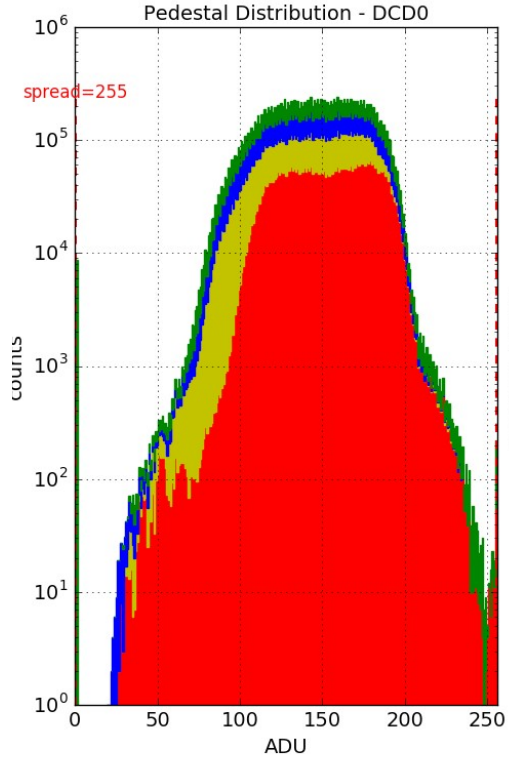


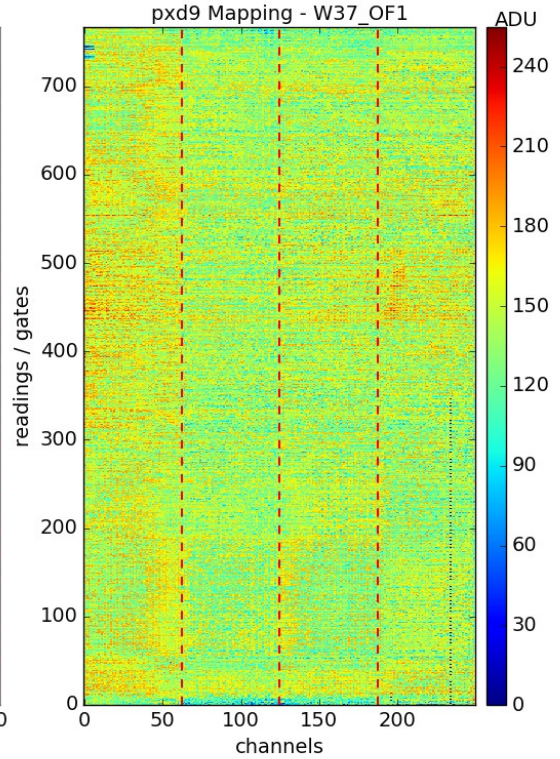
Offset Calibration

- Scan: https://elog.belle2.org/elog/PXD-Mass-Testing/288
- Analysis: https://elog.belle2.org/elog/PXD-Mass-Testing/289









Pedestals with offset correction enabled

Summary

- DHPT HS Links
  - stable links found
- Delays
  - delays optimized
- ADCs optimization using small parameter space
  - only allchannel scan performed
- 2bit offset (delay and current source optimization)
  - optimization succesfully performed
- DCD analog common mode correction
  - functionality confirmed
- Source measurement different regions
  - not yet performed
- Gated mode: simplified test using manual switch for the VETO and standard DHH firmware
  - not yet performed