GCK Jitter

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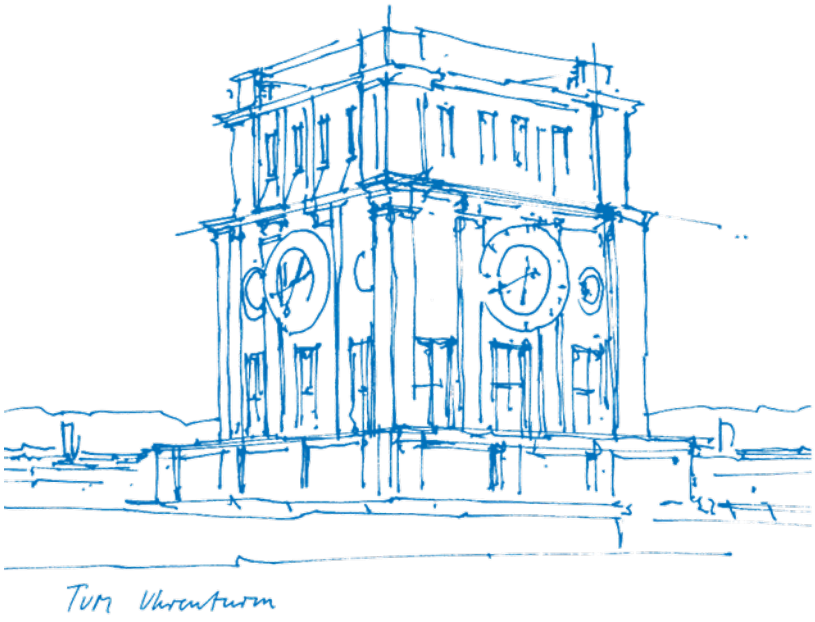
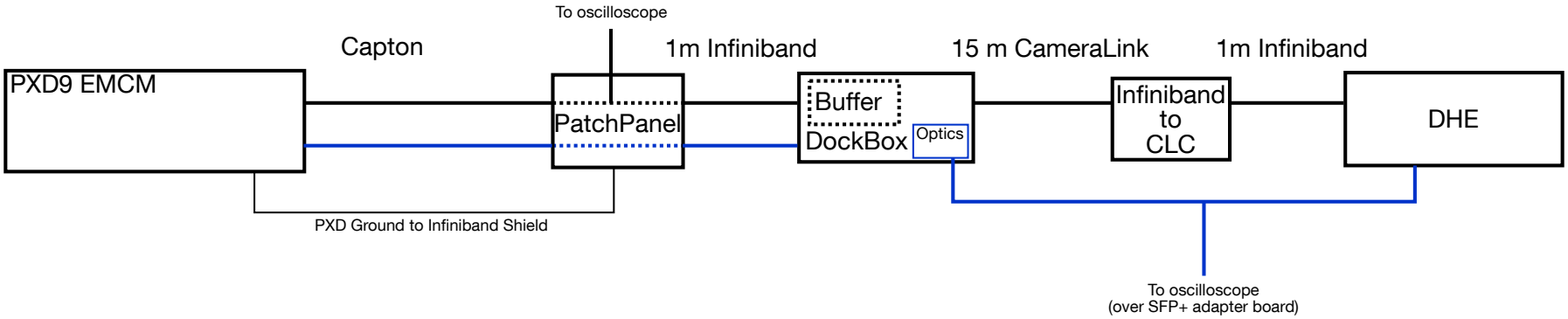


Our Setup


To oscilloscope
Capton
1m Infiniband
15 m CameraLink
1m Infiniband
PXD9 EMCM
PatchPanel
Buffer
DockBox
Optics
Infiniband
to
CLC
DHE
PXD Ground to Infiniband Shield
To oscilloscope
(over SFP+ adapter board)

Time Interval Error

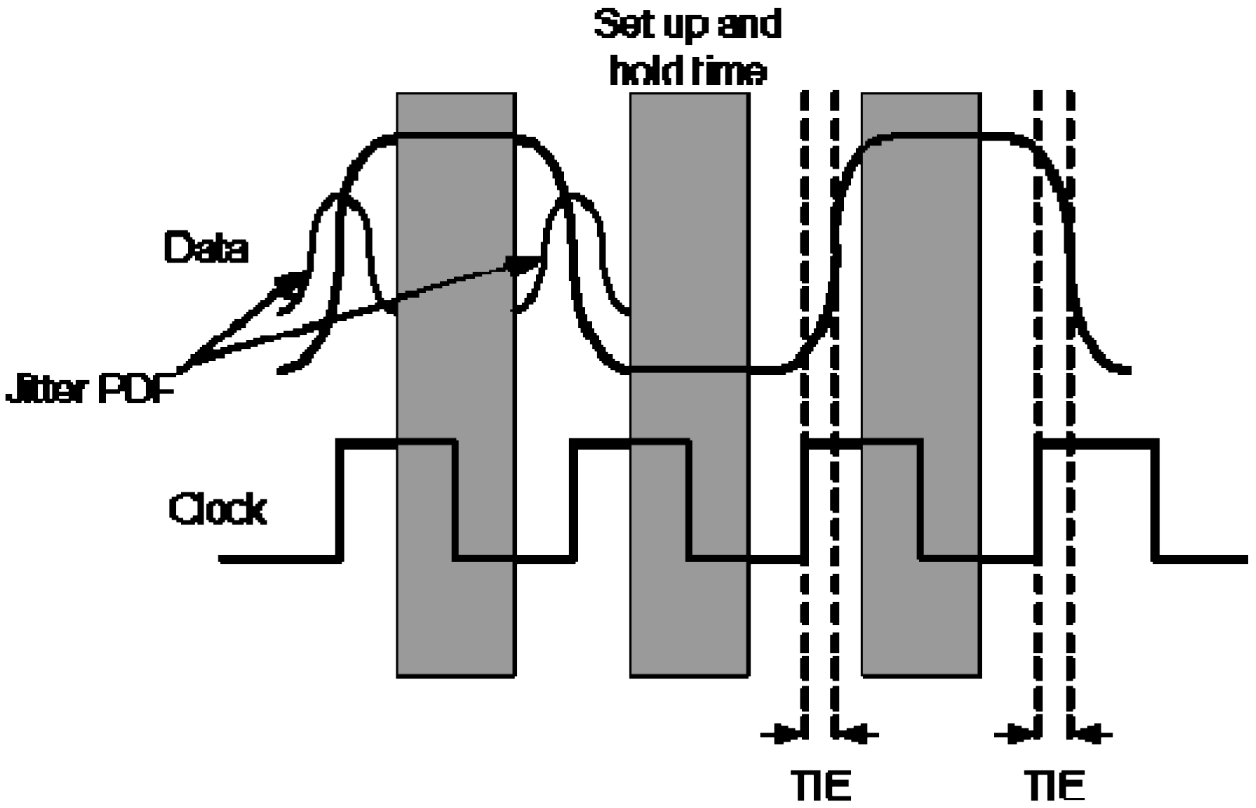


Figure: Calculation of the TIE, from SDA6000A manual, LeCroy

GCK Jitter

Previous GCK Measurements

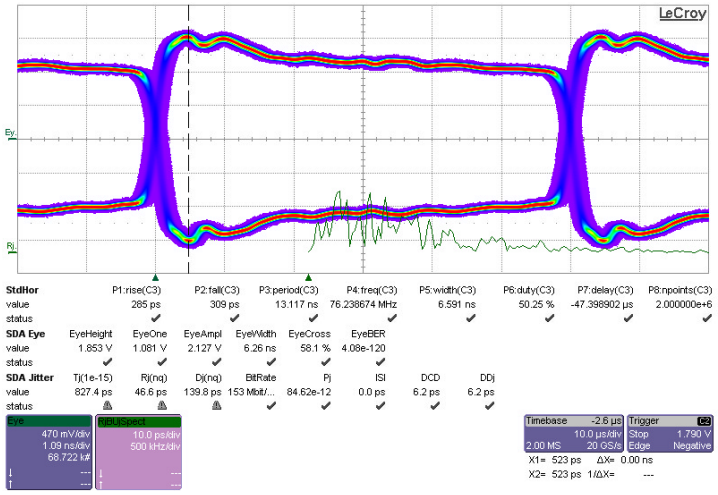


Figure: GCK after 15 m CameraLink cable with clock buffer

Previous GCK Measurements

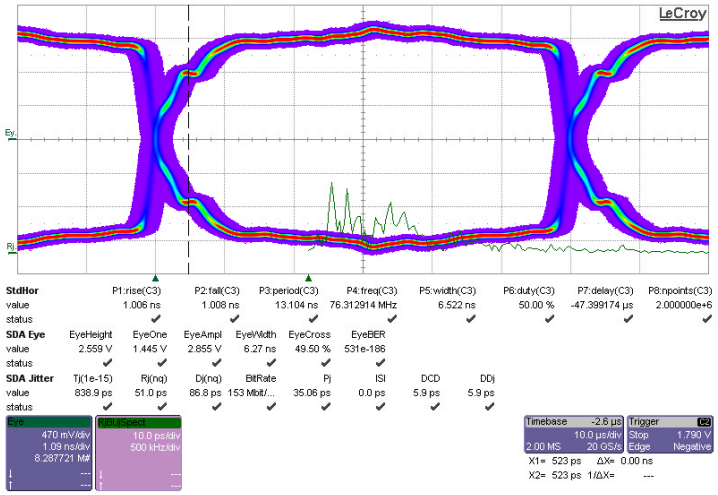
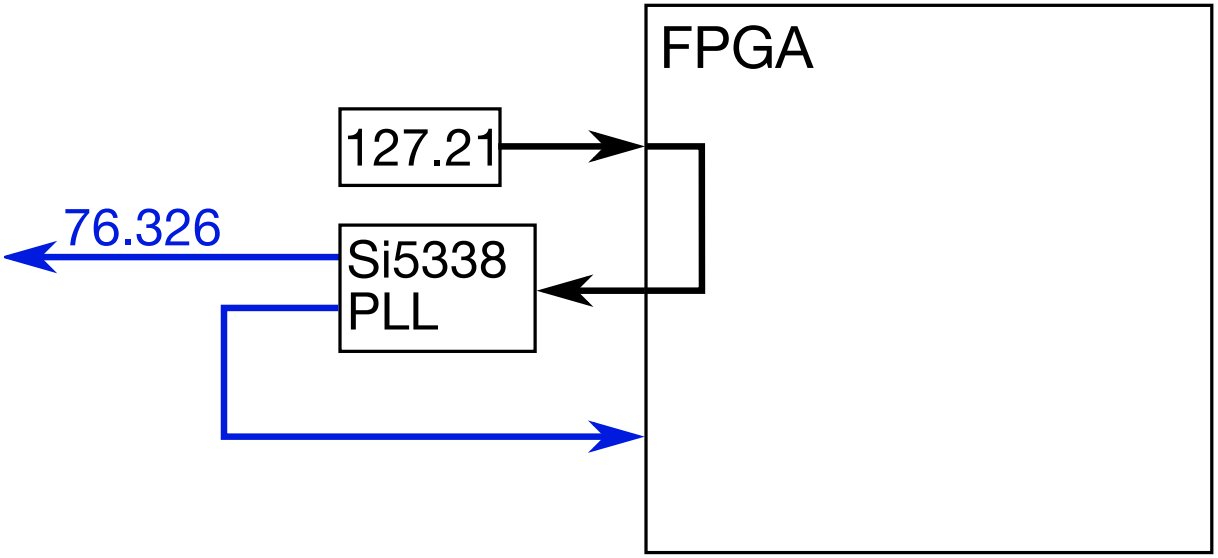
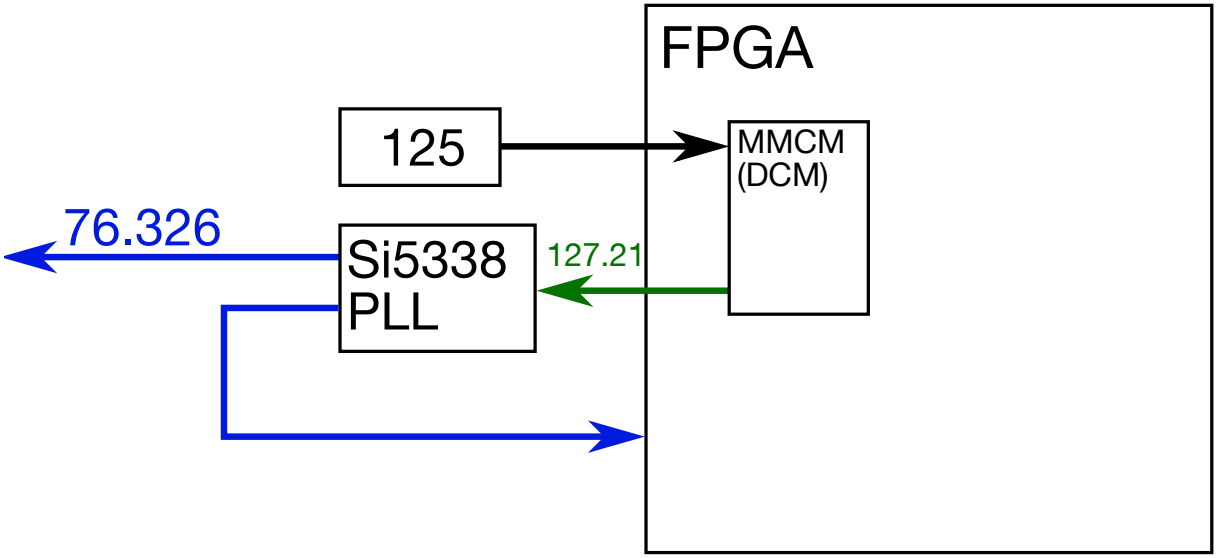


Figure: GCK after 1m infiniband cable

GCK Generation, Initial



GCK Generation, for Lab setups, since Dec 2015



- Why? We didn't have enough 127.21 MHz oscillatiors

First GCK Measurements

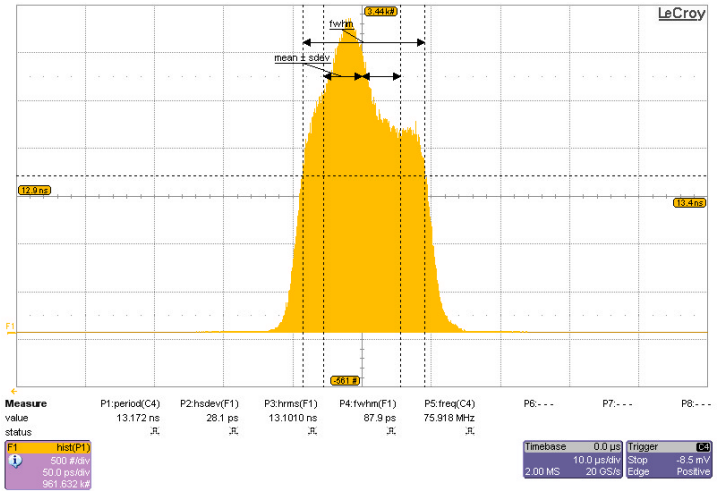


Figure: GCK after synthesis in FPGA (from 2012)

Improved GCK

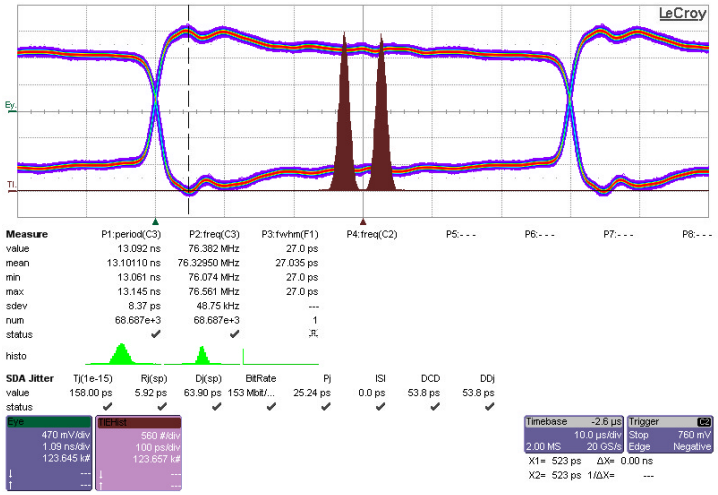


Figure: GCK after 15 m CameraLink cable with the clock buffer

Improved GCK

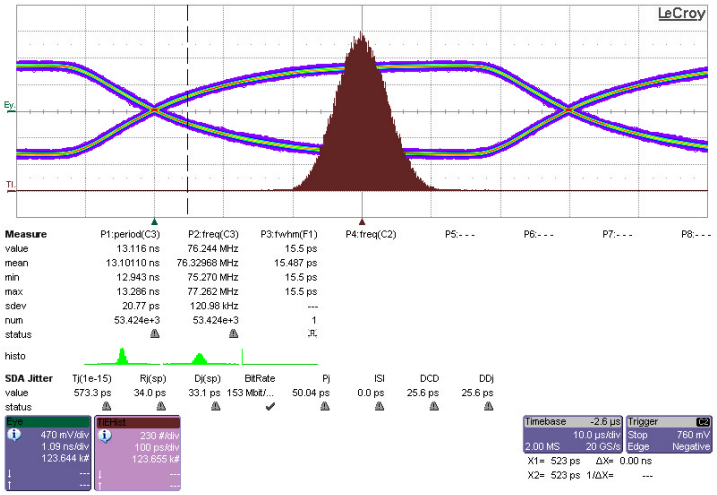


Figure: GCK after 15 m CameraLink cable without the clock buffer

Improved GCK

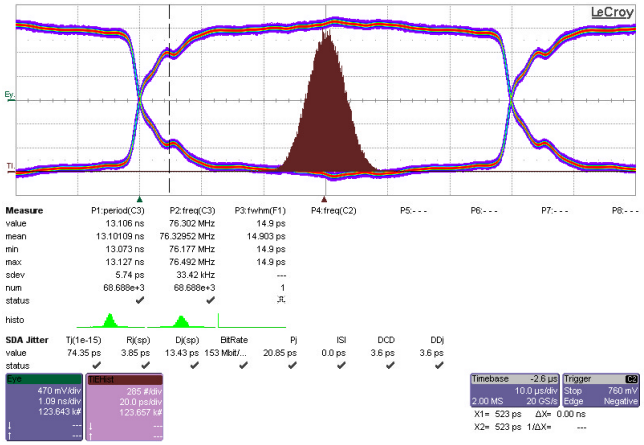


Figure: GCK after 1m infiniband cable

Data Link

Signal Eye Diagrams

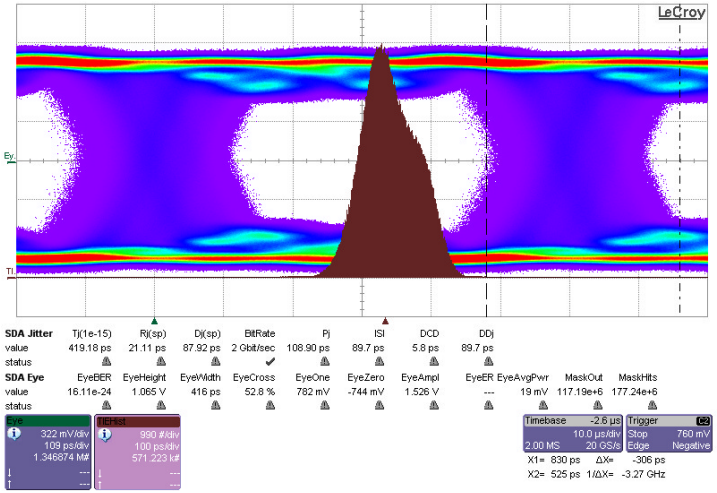


Figure: DHPT0 link with all DHPTs in phase

- GCK phase (to trigger) = 78
- **ref_clk_dly = 0**
- pll_cml_dly = 2
- idac_cml_txbias = 58
- idac_cml_txbiasd = 255

Signal Eye Diagrams

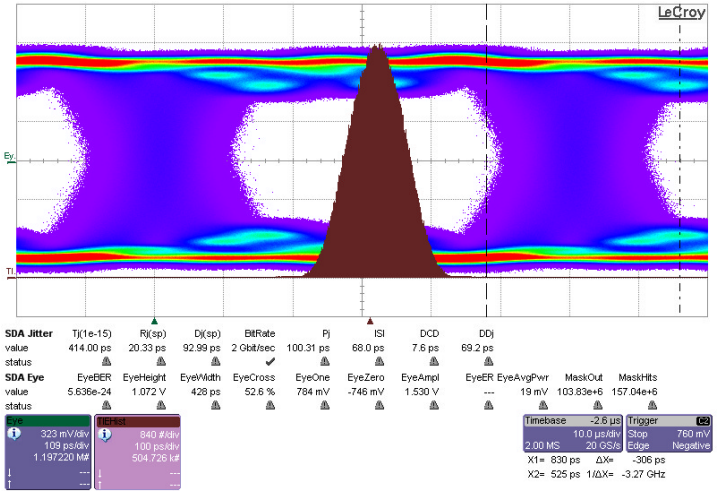


Figure: DHPT0 link with long reset

- GCK phase (to trigger) = 78
- **ref_clk_dly = 11**
- pll_cml_dly = 2
- idac_cml_txbias = 58
- idac_cml_txbiasd = 255

Signal Eye Diagrams

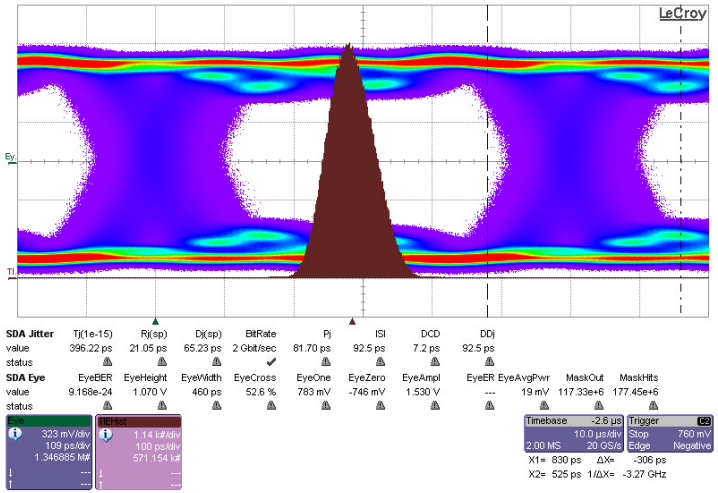


Figure: DHPT0 link without long reset

- GCK phase (to trigger) = 78
- **ref_clk_dly = 11**
- pll_cml_dly = 2
- idac_cml_txbias = 58
- idac_cml_txbiasd = 255

Signal Eye Diagrams

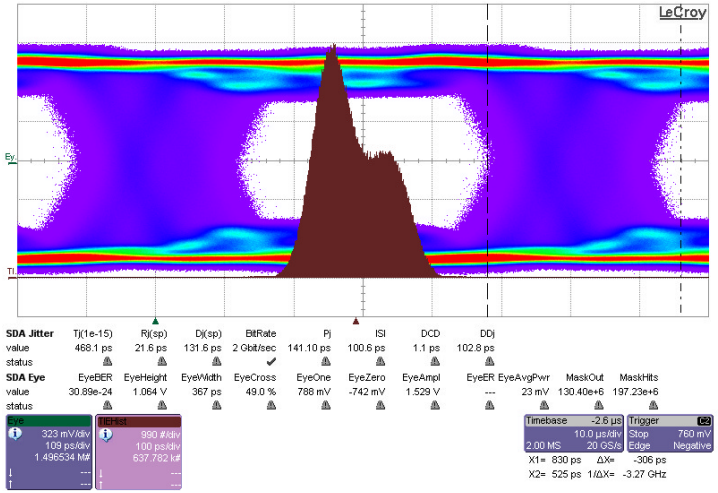


Figure: DHPT0 link without ground connection

- GCK phase (to trigger) = 78
- ref_clk_dly = 11
- pll_cml_dly = 2
- idac_cml_txbias = 58
- idac_cml_txbiasd = 255

Signal Eye Diagrams

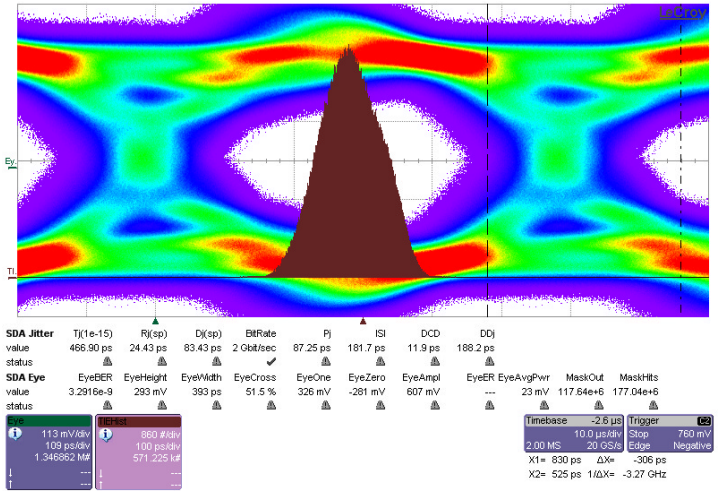


Figure: DHPT0 link after 1m Infiniband

- GCK phase (to trigger) = 78
- ref_clk_dly = 0
- pll_cml_dly = 2
- idac_cml_txbias = 100
- idac_cml_txbiasd = 255

Summary

- We found a bug in the lab firmware, which caused high clock jitter
- Software programming of the Si5338 cleaned up
  - precize frequency generation (e.g. 62.5 MHz in EPICS generates 62.5 MHz)
- Ground connection between PXD9 and DHE improves jitter
- All four links work for hours, then fail simultaneously
  - high deterministic jitter on the data line
  - FFT of the jitter show peak at 9.54 MHz (GCK/8)
  - with or without CameraLink cable
- Observed the influence of the phase of different modules on the jitter shape
  - changed parameter ref_clk_dev_dly
- If you change GCK phase, do not use long_reset with DHPT 1.2b: it will re-calibrate the phase
  - it would be nice to have some information about the mechanism of the phase calibration
- DHPT temperature sensor returns unphysical results
  - Temperatures: DHP1–135.29 DHP2–138.72 DHP3–202.47 DHP4–200.01