W38_IB & W40_IF Update

Pablo Gomis (IFIC), Felix Mueller (MPP)

pxdtest1: W38_IB

pxdtest8: W40_IF

Minimum Tests Required before glueing

- ✔ **DHPT HS Links**
  - short scan (to have a reference for later)
    - bias 200 to 250, step 5
    - bias_d 100 to 150, step 5
    - delay 0
- ✔ **Delays**
- ? **ADCs optimization using small parameter space**
- ✔ **Pedestal/noise (1k frames)**
- ✔ **2bit offset (delay and current source optimization)**
- ✔ **Pedestal/noise (1k frames)**
- ✔ **DCD analog common mode correction**
- ✔ **Pedestal/noise (1k frames)**
- **Source measurement different regions** (tbd. latest by Lab Framework meeting Tuesday June 11th)
  - ✔ Threshold 5
  - ✔ Verify shape of the spectra
  - ✘ ✔ SNR in different regions
  - ~~Adjust VNSubIn~~ ACMC ✔
- ✘ **Gated mode: simplified test using manual switch for the VETO and standard DHH firmware** (metho

Commands (not compliant to the coding guidelines):

Pedestals using the MEMDUMP command:

https://confluence.desy.de/display/BI/Phase+2+PXD9+Module+Testing

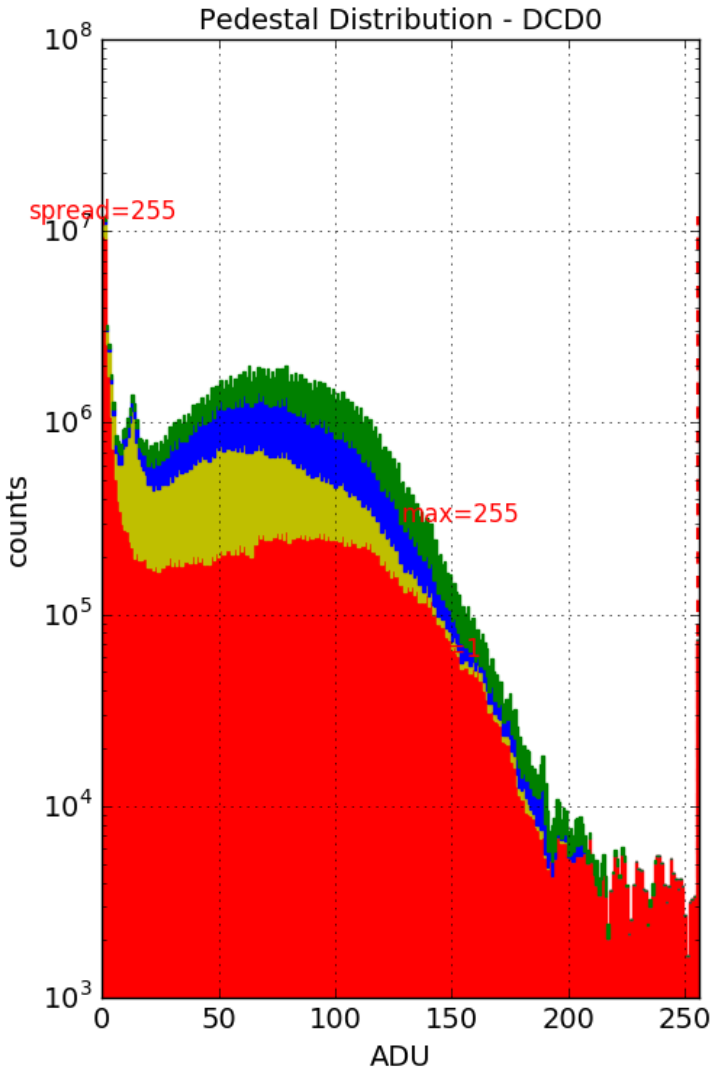
W38_IB

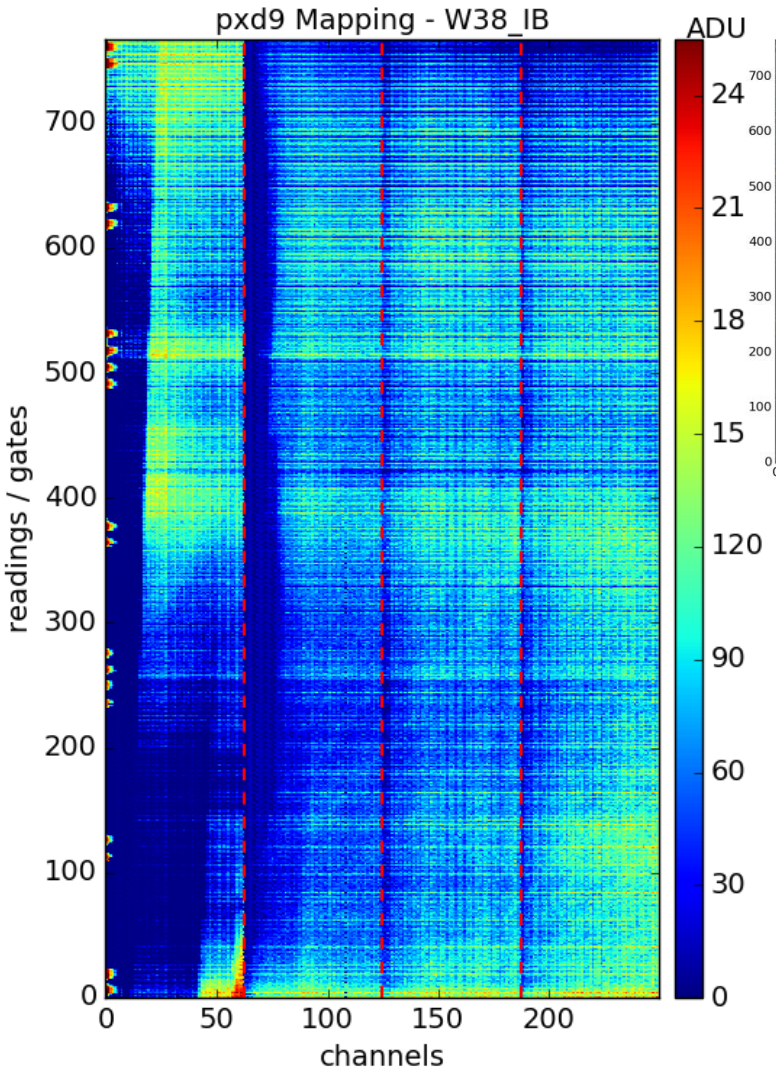
W38_IB – pedestals **without** Offsets and **no** ACMC

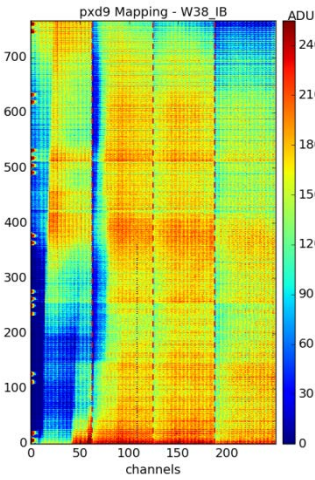
already shown on August 2, 2017

PXD:H1012:R4:dacvnsubin:VALUE:set = 35
PXD:H1012:R2:dacvnsubin:VALUE:set = 32
PXD:H1012:R3:dacvnsubin:VALUE:set = 35
PXD:H1012:R1:dacvnsubin:VALUE:set = 25

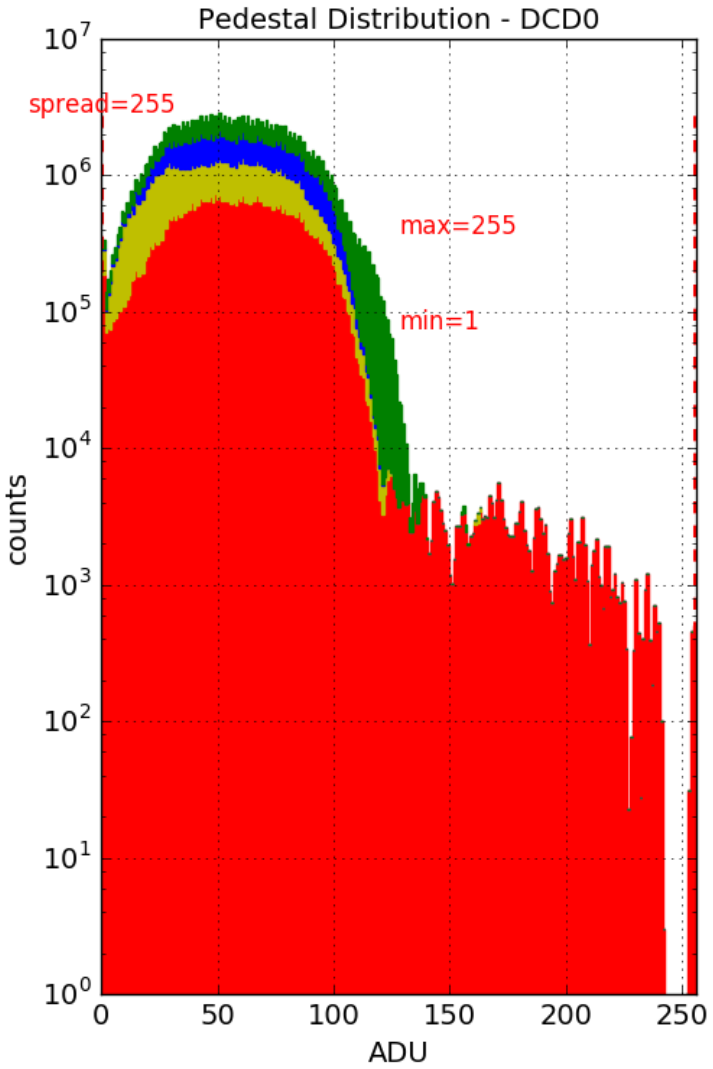
PXD:H1012:R4:dacvnsubin:VALUE:set = 33
PXD:H1012:R2:dacvnsubin:VALUE:set = 28
PXD:H1012:R3:dacvnsubin:VALUE:set = 31
PXD:H1012:R1:dacvnsubin:VALUE:set = 22

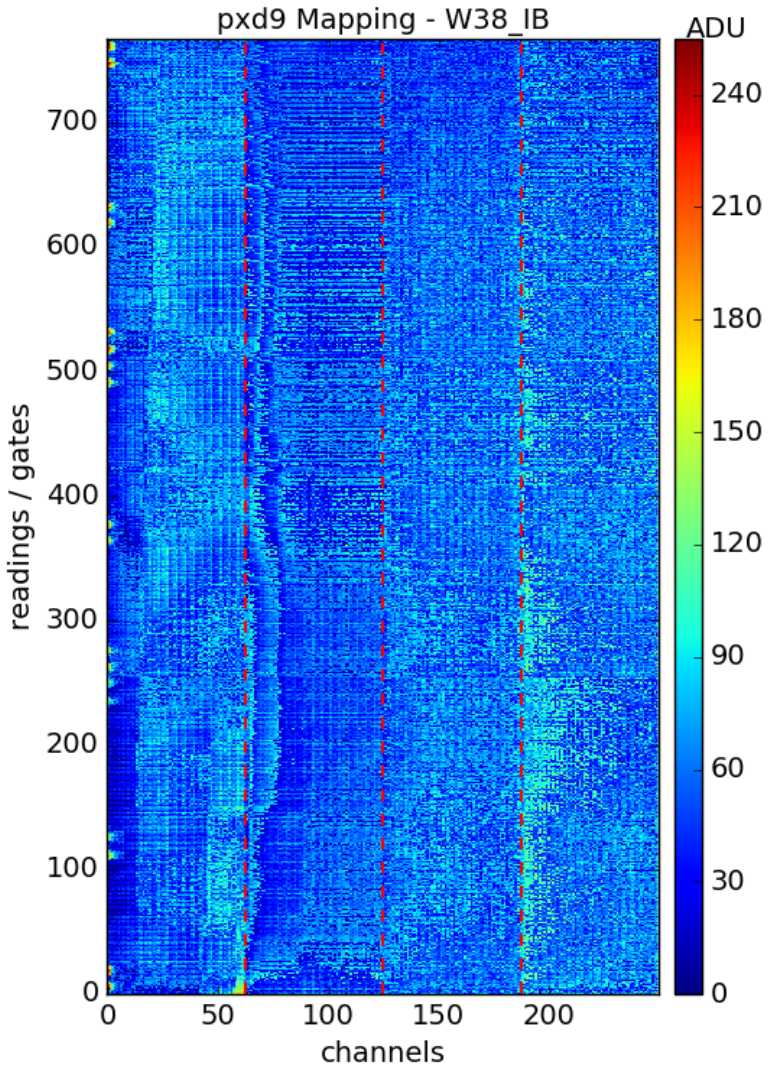




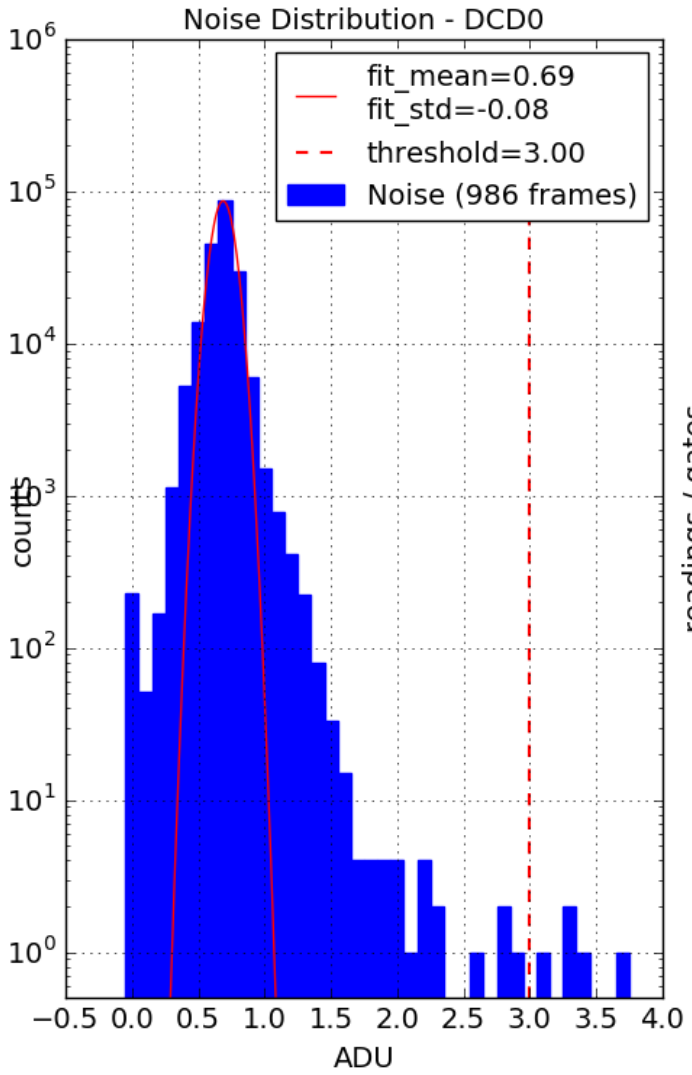


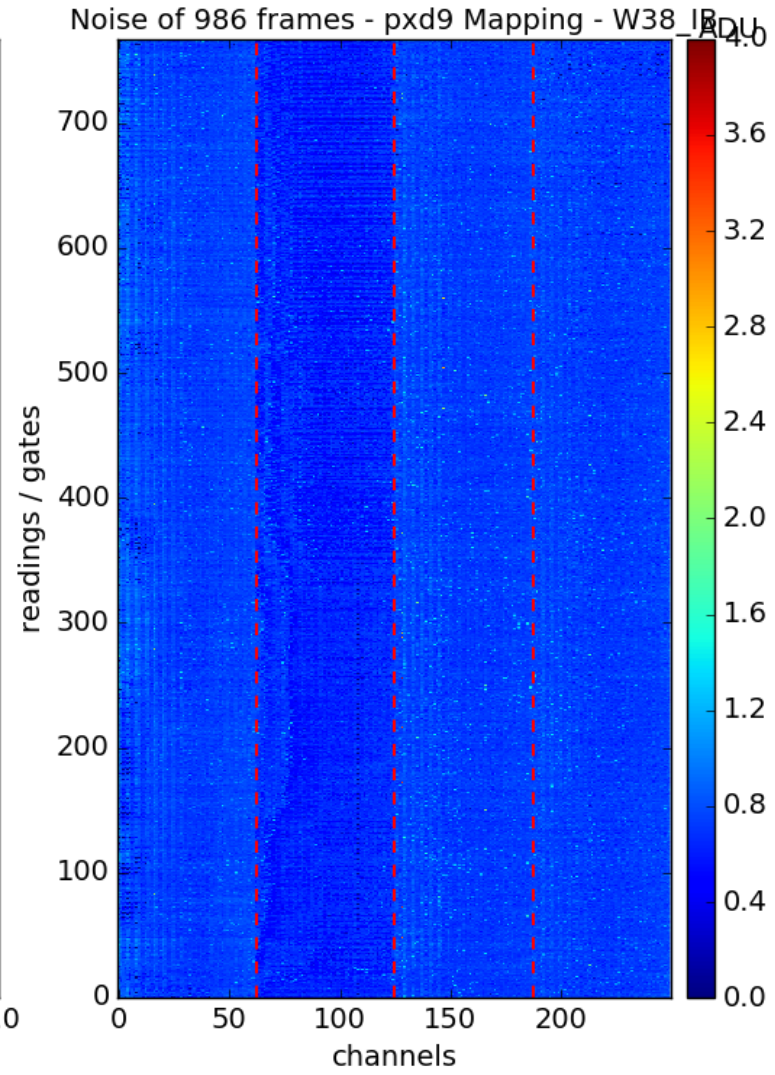
W38_IB – pedestals - with Offsets and ACMC





W38_IB – noise – with Offsets and ACMC





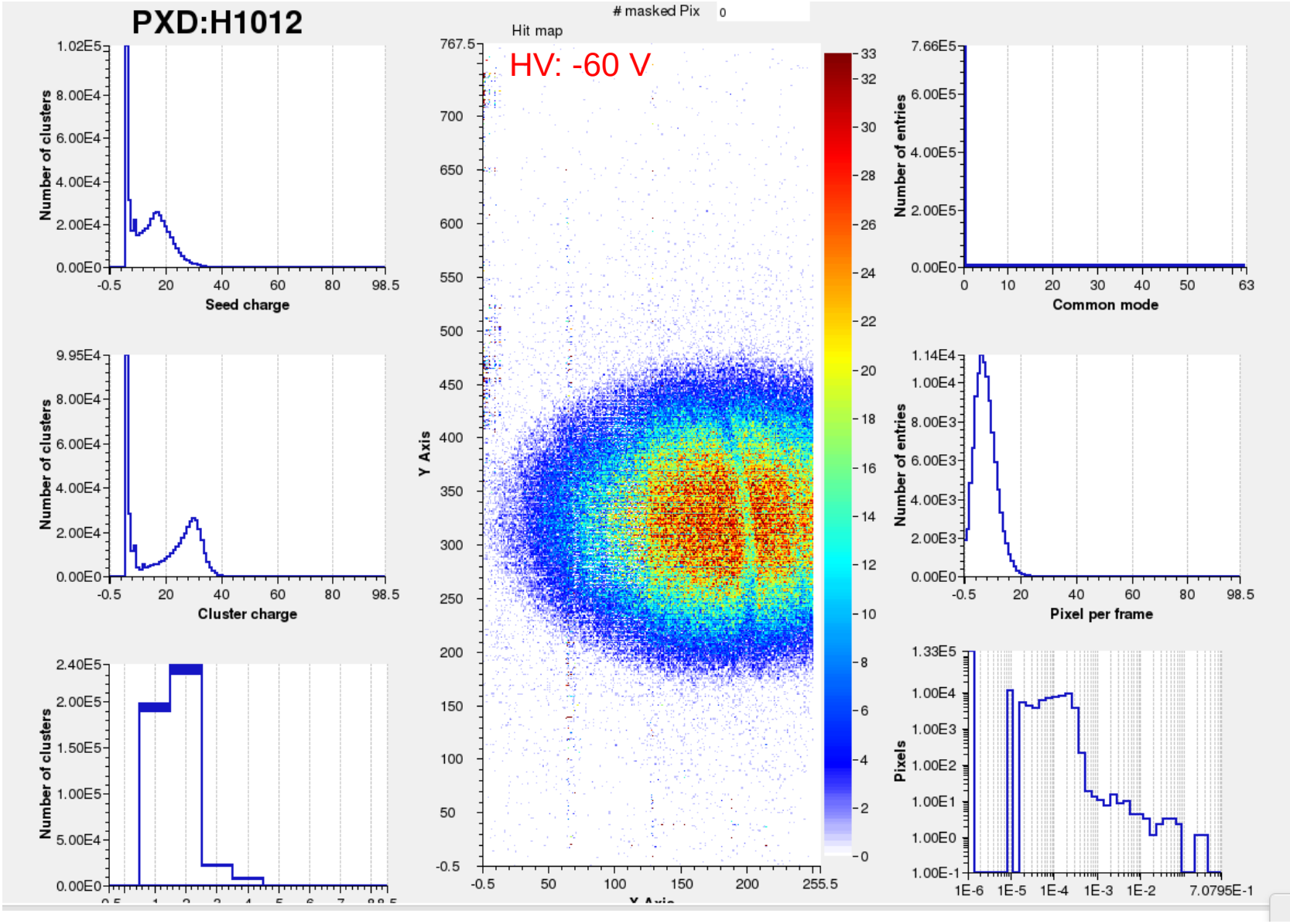
W38_IB – source measurements

sw-dvdd-voltage 1.798 V, 20 mA
sw-refin-voltage -5.202 V, 0 mA
sw-sub-voltage -7.000 V, -10 mA
dhp-core-voltage 1.198 V, 672 mA
dhp-io-voltage 1.801 V, 290 mA
dcd-amplow-voltage 0.275 V, -702 mA
dcd-avdd-voltage 1.727 V, 2716 mA
dcd-dvdd-voltage 1.800 V, 834 mA
dcd-refin-voltage 0.723 V, 262 mA
bulk-voltage 10.000 V, 0 mA
ccg1-voltage 0.000 V, 0 mA
ccg2-voltage -0.001 V, 0 mA
ccg3-voltage 0.005 V, 0 mA
clear-off-voltage 5.008 V, -20 mA
clear-on-voltage 19.002 V, 27 mA
drift-voltage -5.003 V, 0 mA

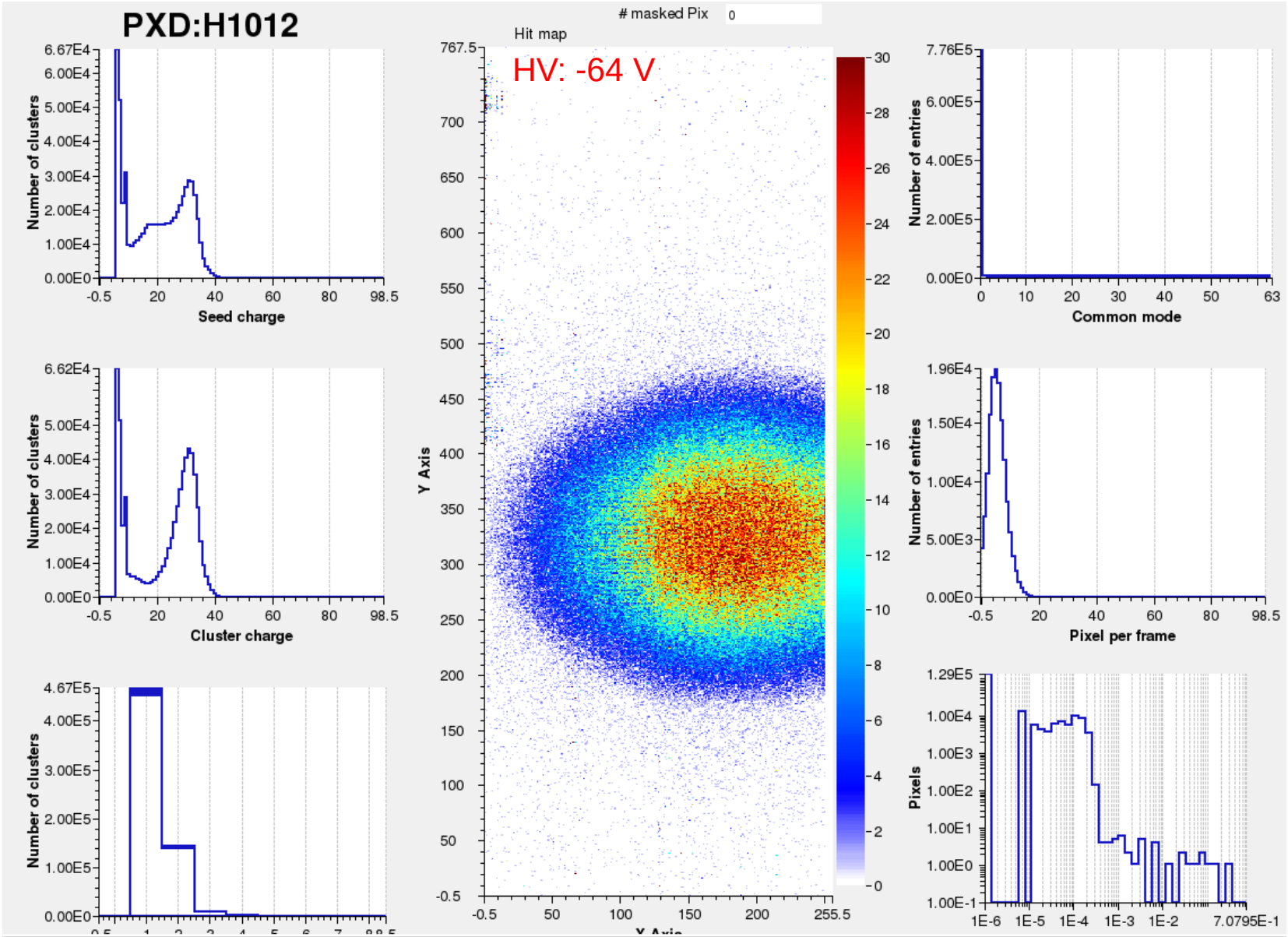
gate-off-voltage 2.998 V, 24 mA
gate-on1-voltage -2.500 V, -5 mA
gate-on2-voltage -2.501 V, -5 mA
gate-on3-voltage -2.502 V, -5 mA
guard-voltage -4.999 V, 0 mA
hv-voltage **-70.099 V**, 12 mA
source-voltage 6.002 V, 73 mA

HV scan from -60 V to -80 V (most likely depending on wafer, e.g. for W30_OB1, -70 V was the best)

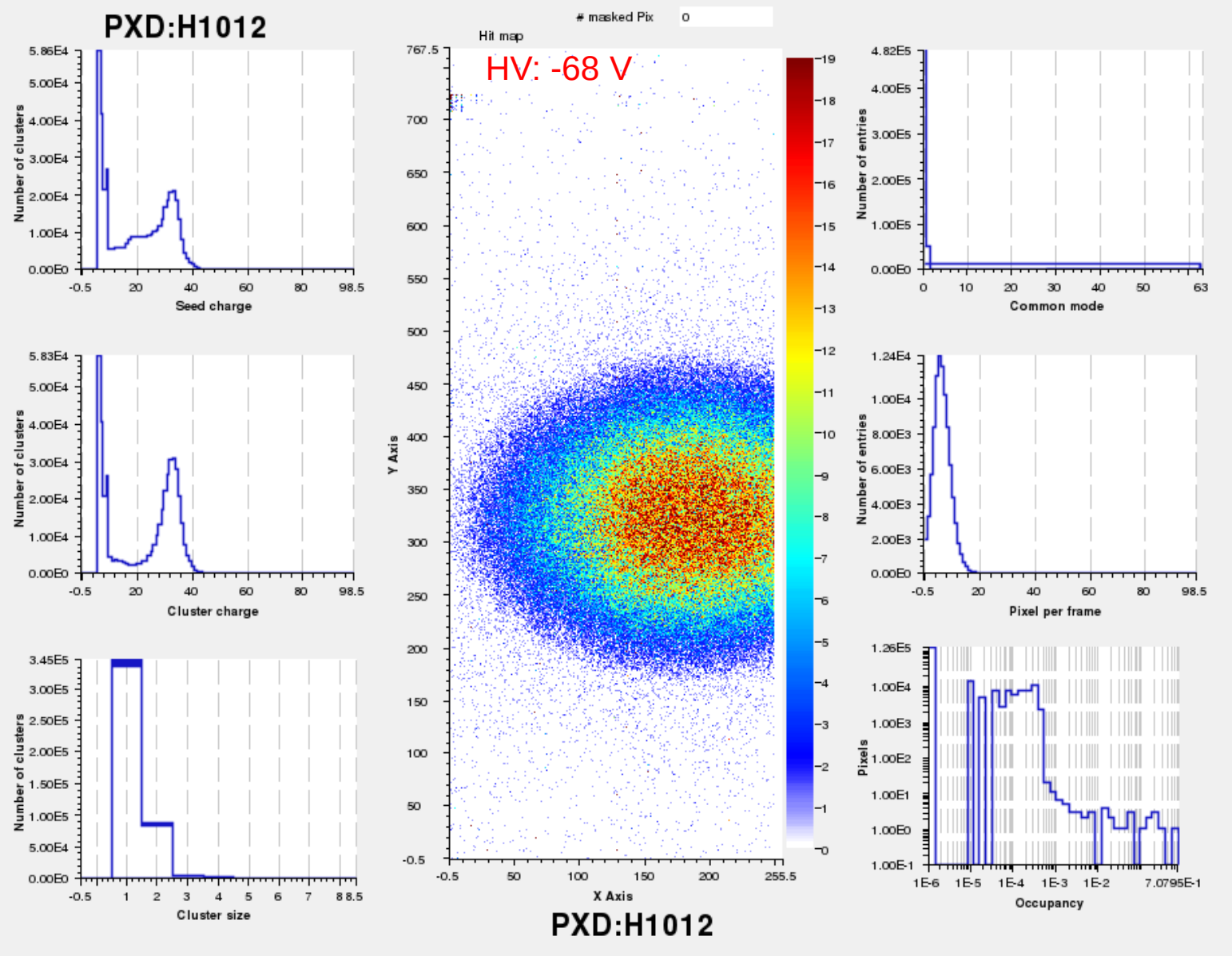
W38_IB – source measurements



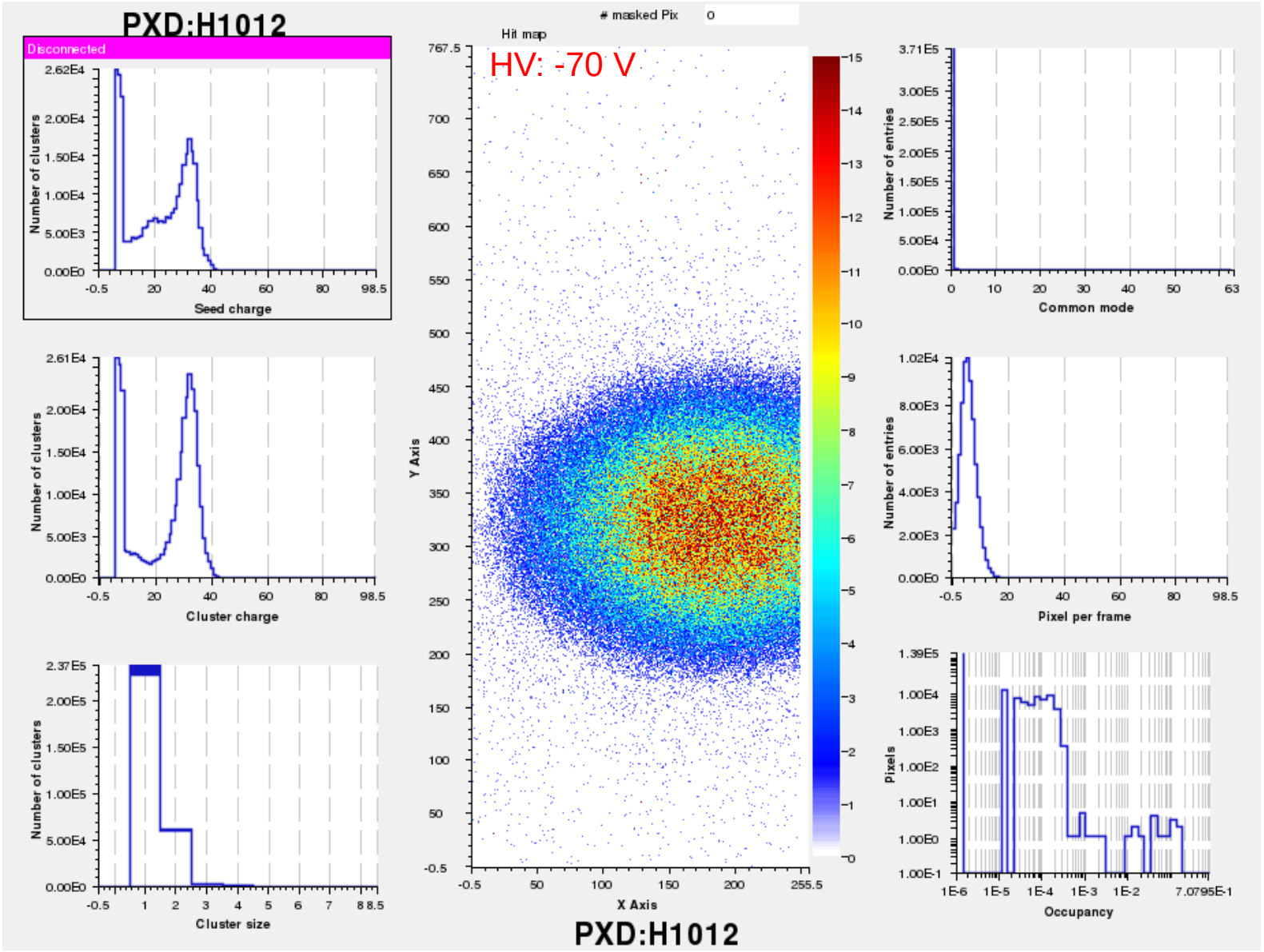
W38_IB – source measurements



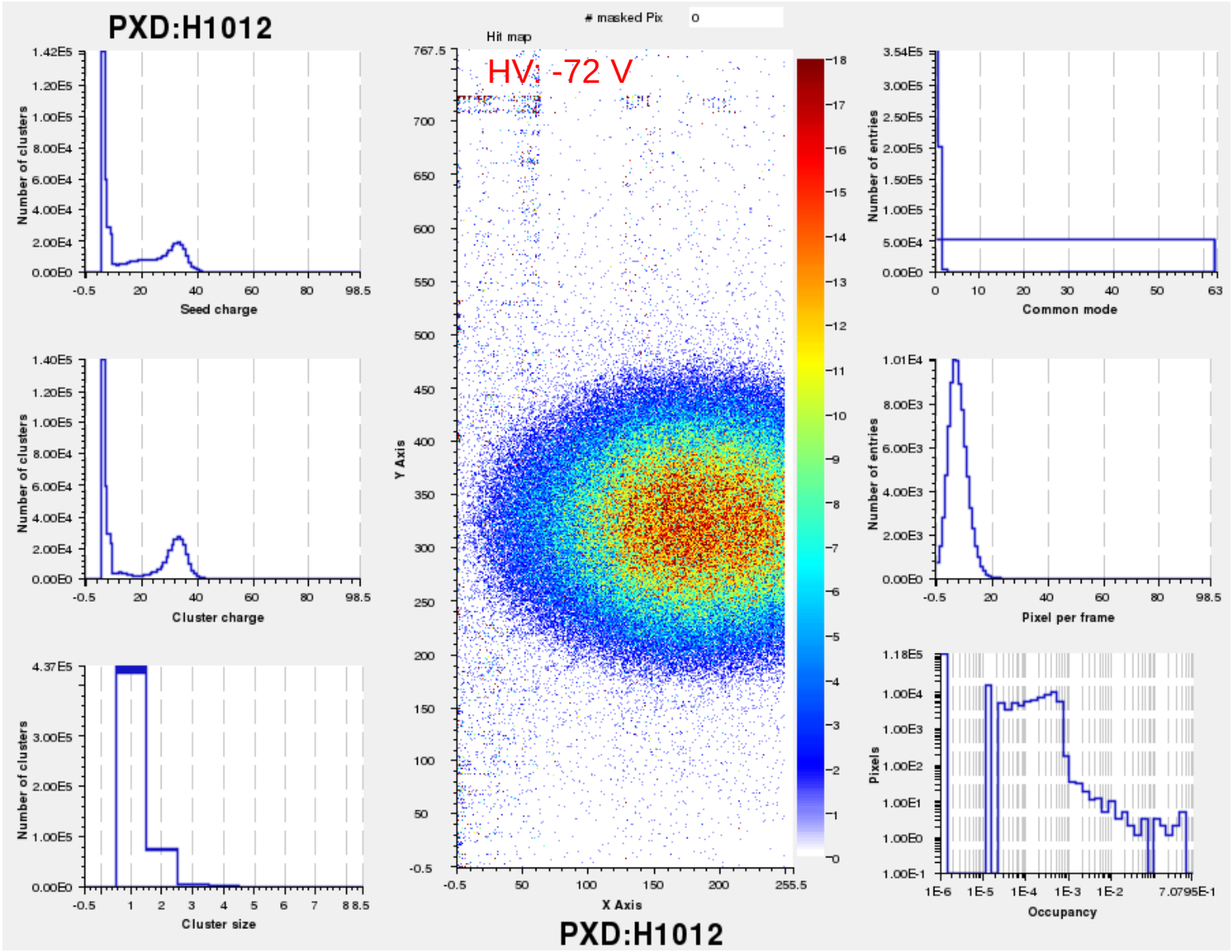
W38_IB – source measurements



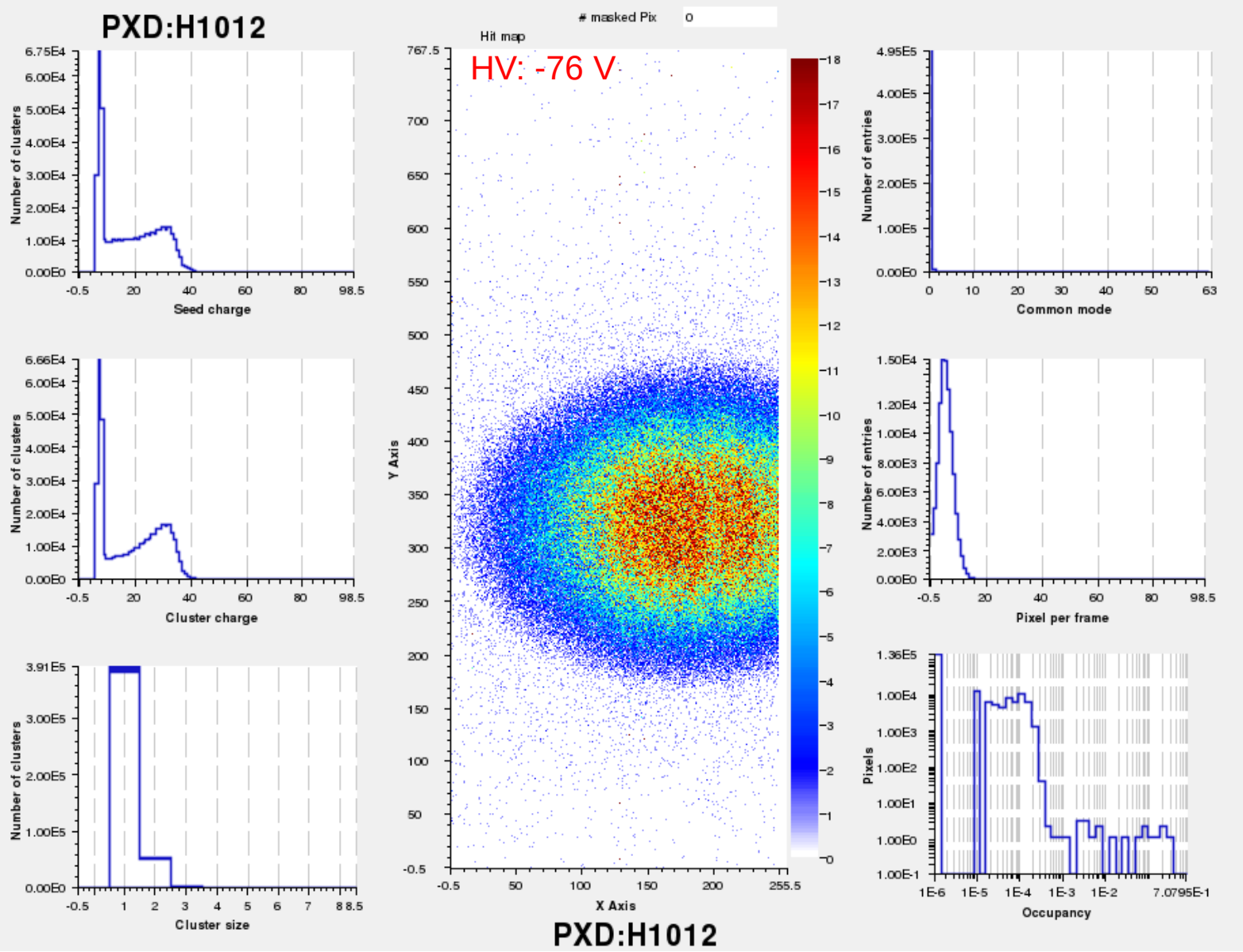
W38_IB – source measurements



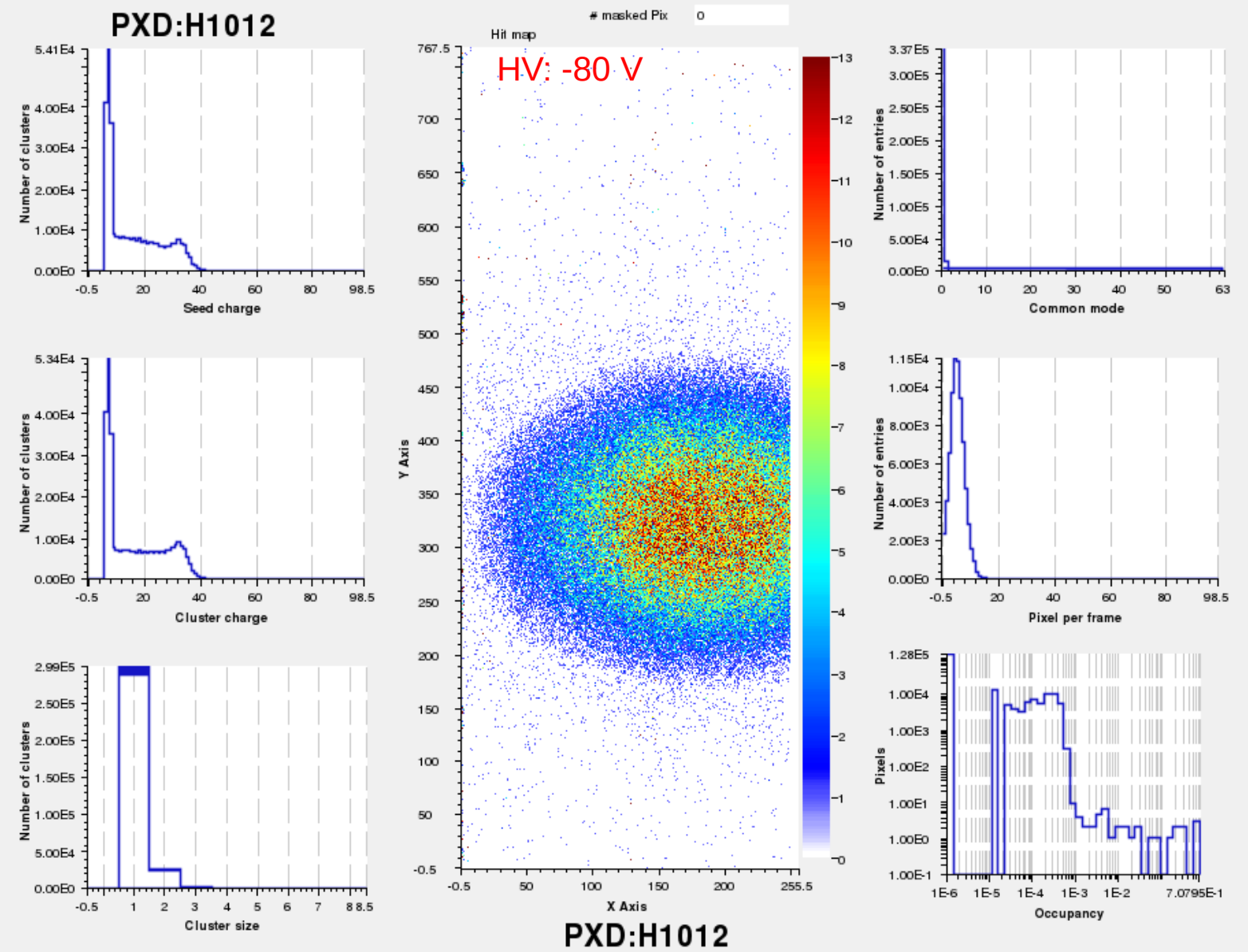
W38_IB – source measurements



W38_IB – source measurements



W38_IB – source measurements

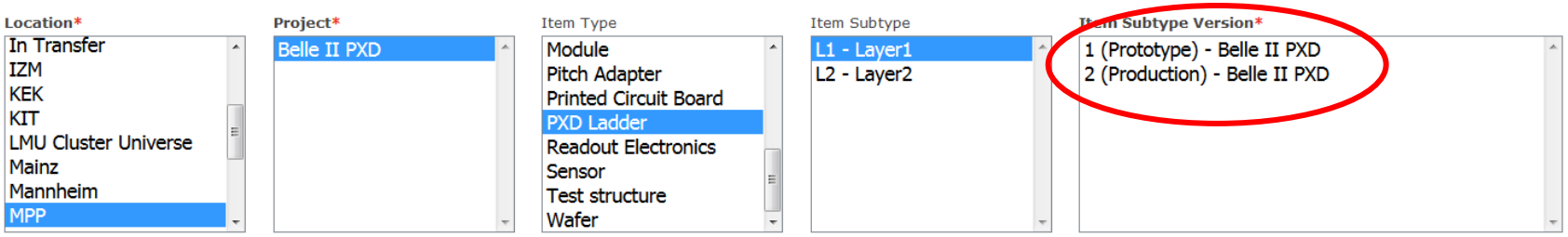


Glueing

W40_IF & W38_IB have been glued together on Tuesday, August 8, still in the jig

expected to have them back tomorrow (Thursday August 10)

which one for phase 2 ?



DEPFET LAB MEETING
9TH AUGUST 2017

W40_IF SOURCE SCAN

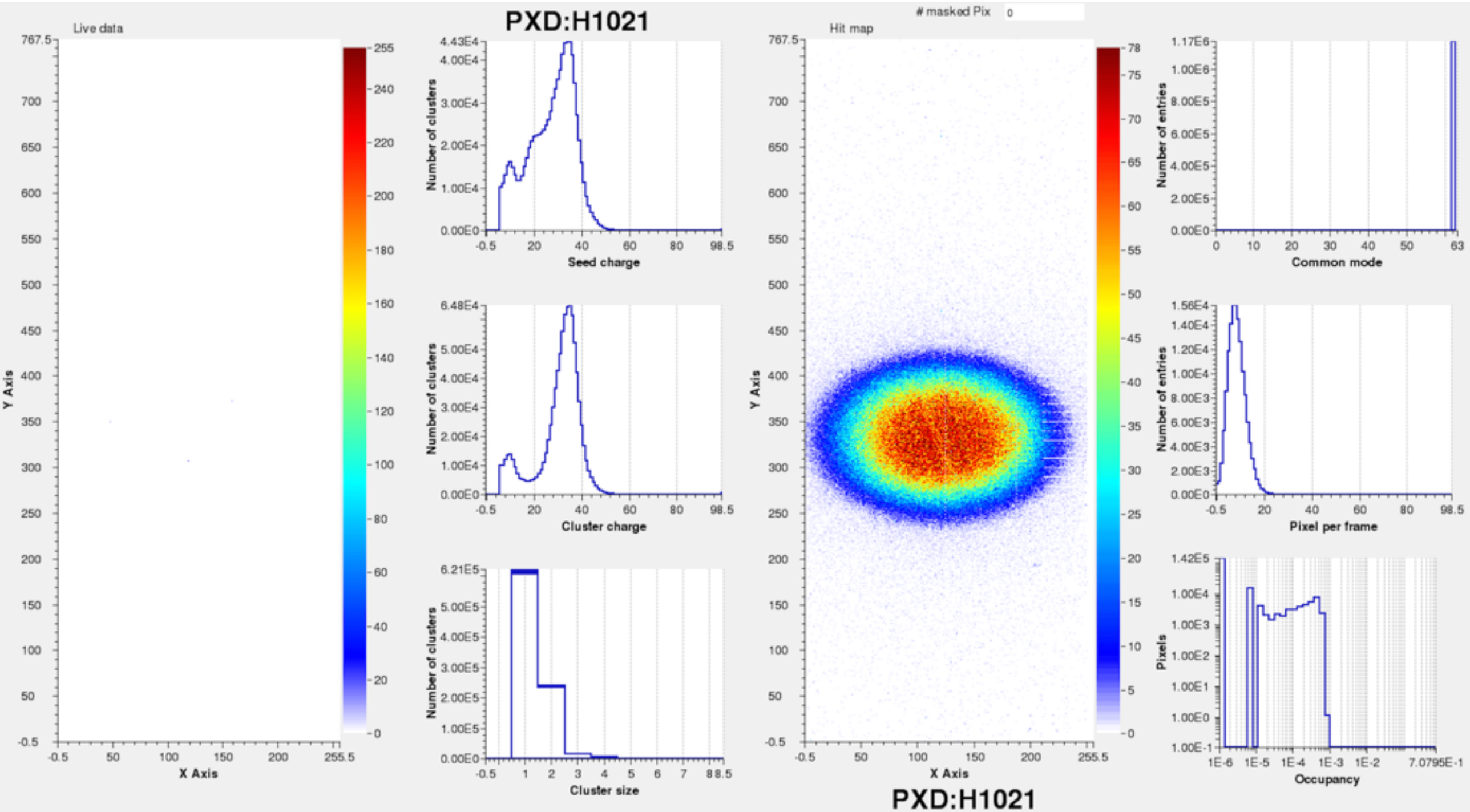
PABLO GOMIS*, FELIX MÜLLER+

* IFIC (UNIVERSITAT DE VALÈNCIA/CSIC)
+ MAX PLANCK INSTUTE FOR PHYSICS (MPG)

SETUP: PXDTEST8

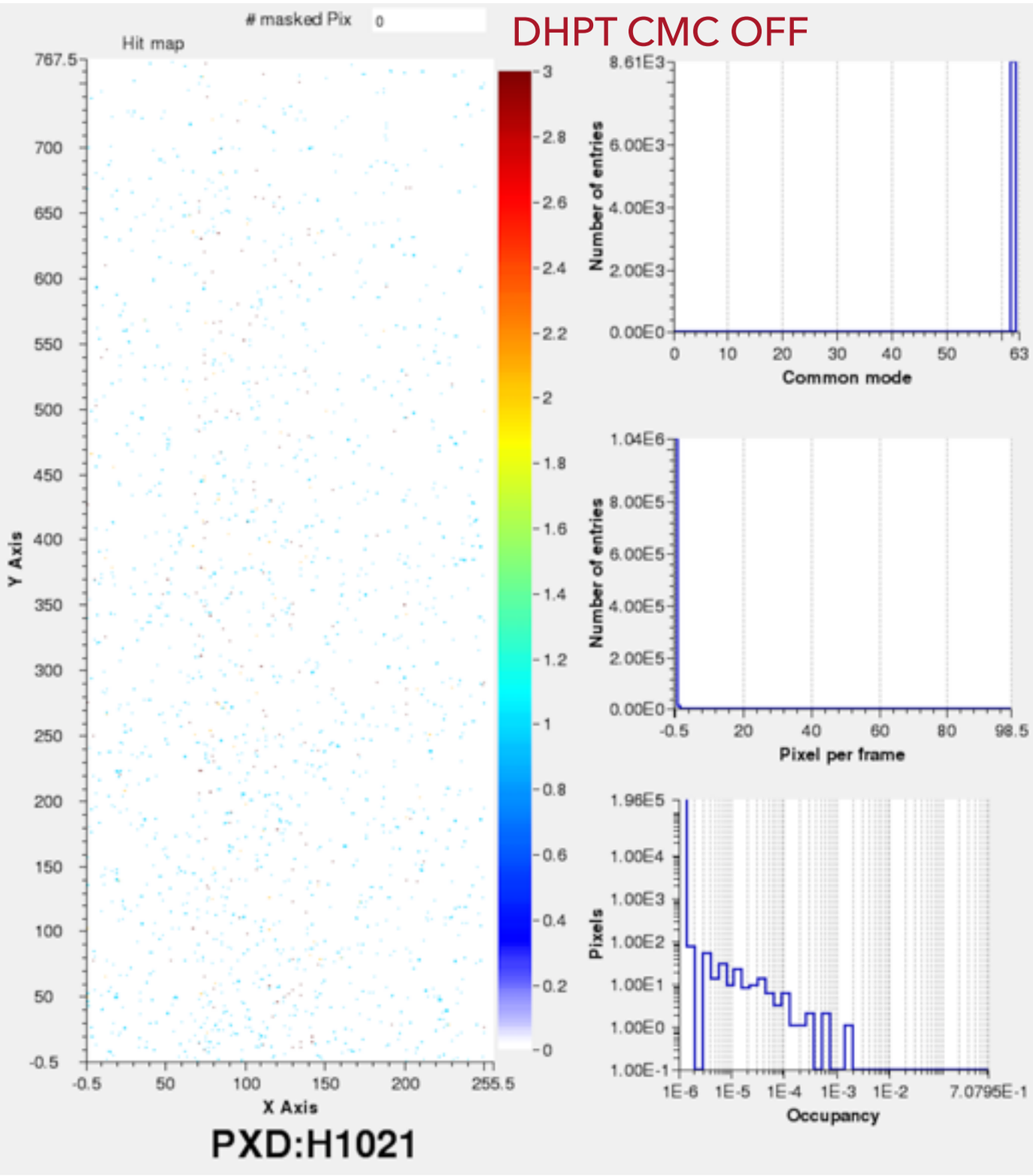
- pxdtest8
  - IF lab patch panel
  - Clamp attached and wide aluminum cooling adaptor
    - DHP temps checked in between measurements: 55-60°C
  - Latest DHE firmware (21/06/17 22:00 release)
  - Source (Cd^{109}, 370MBq @ 15/11/16)
- Commit ID (#520)
  - Nominal frequency (76.23 MHz)
  - Standard values from the template
  - Optimized delays
  - Fully stable HSL
  - DCD ACMC on
  - 2bit DAC on

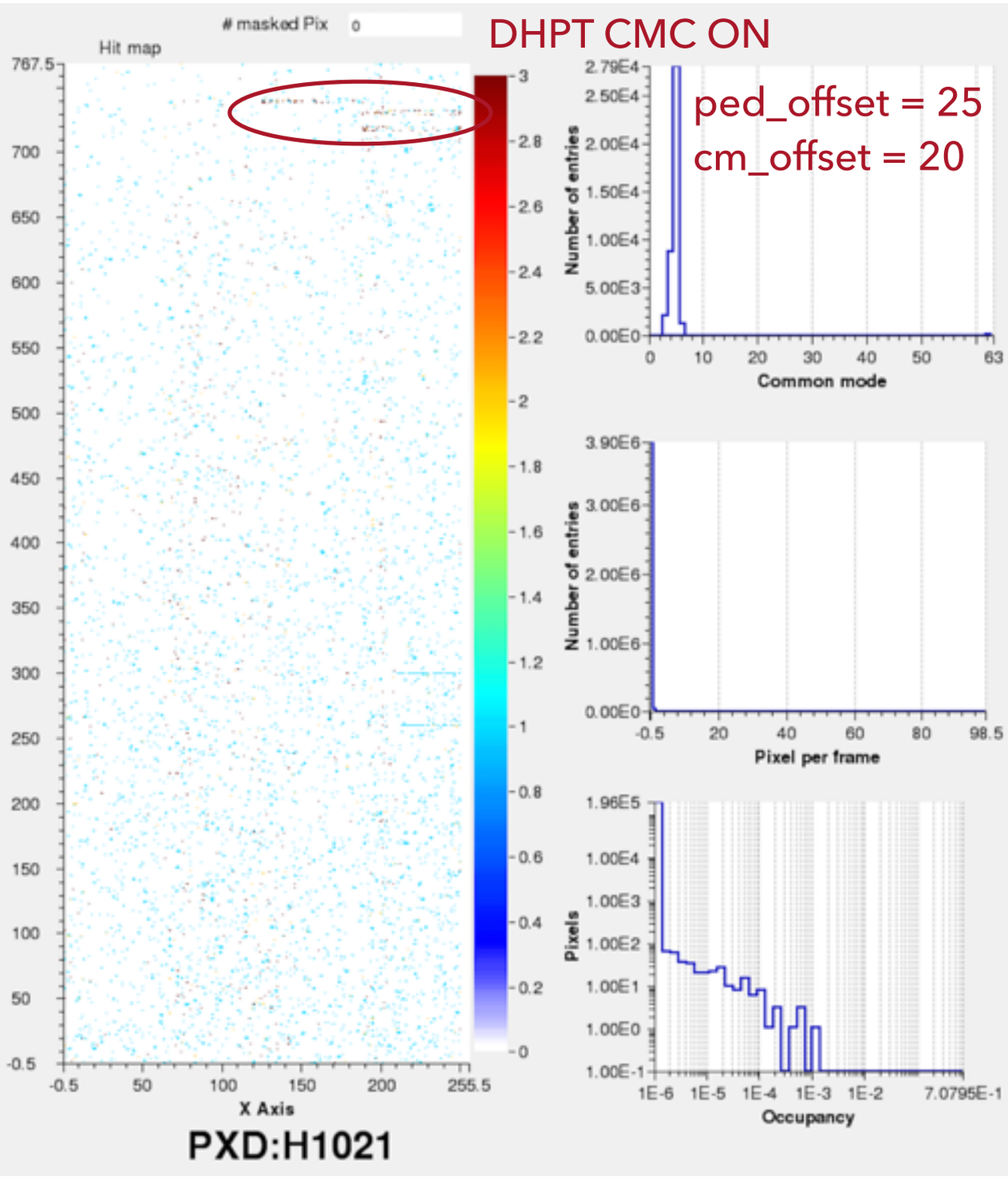
DATA ACQUISITION: ONLINE MONITOR



- Online monitor used to “analyze” the data, as no scripts are yet available

DHPT CMC: ON VS OFF

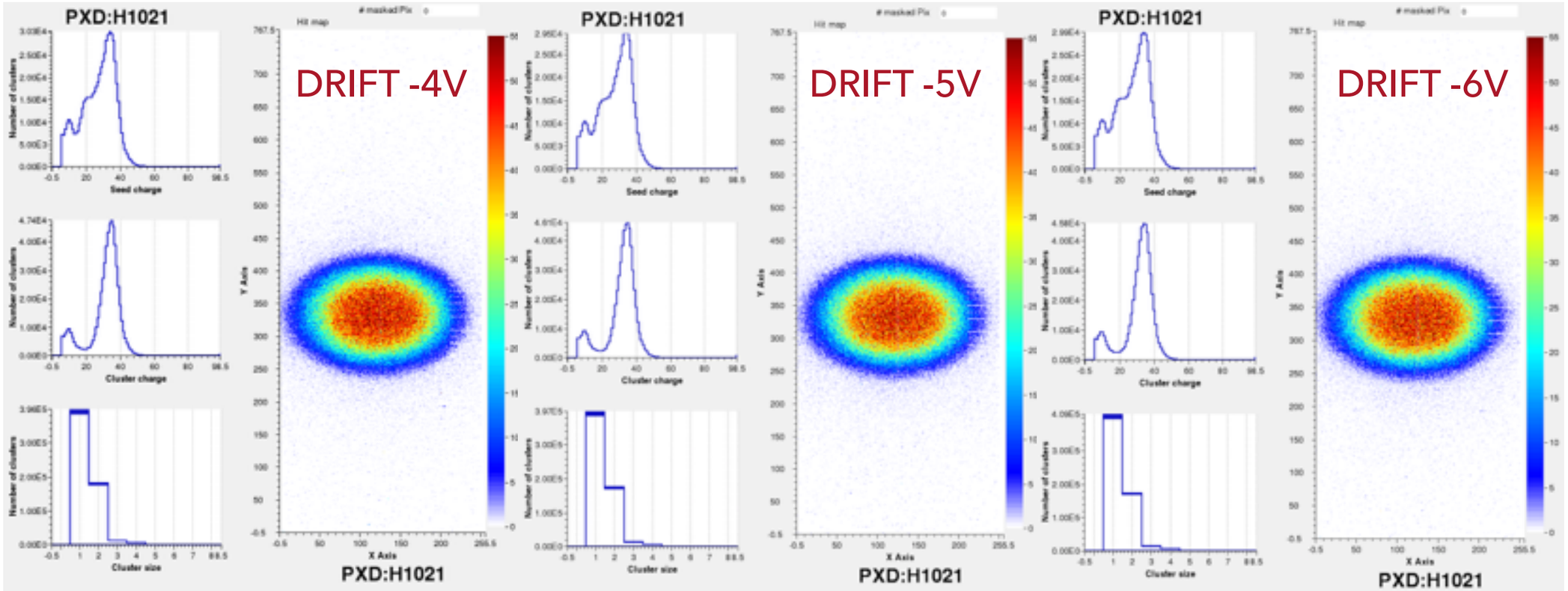




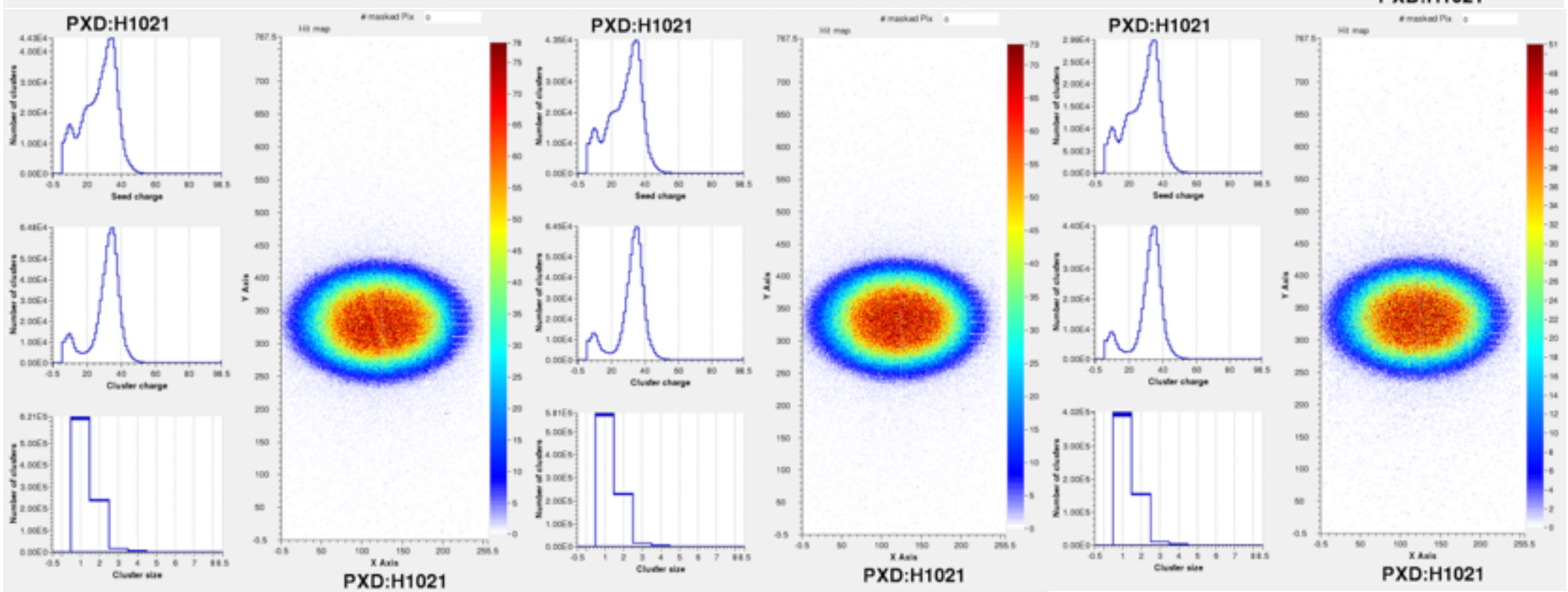
- When using the “digital” CMC some noisy pixels appear in the hitmaps

VOLTAGE SCAN: HV -56V, -60 V

HV -56V



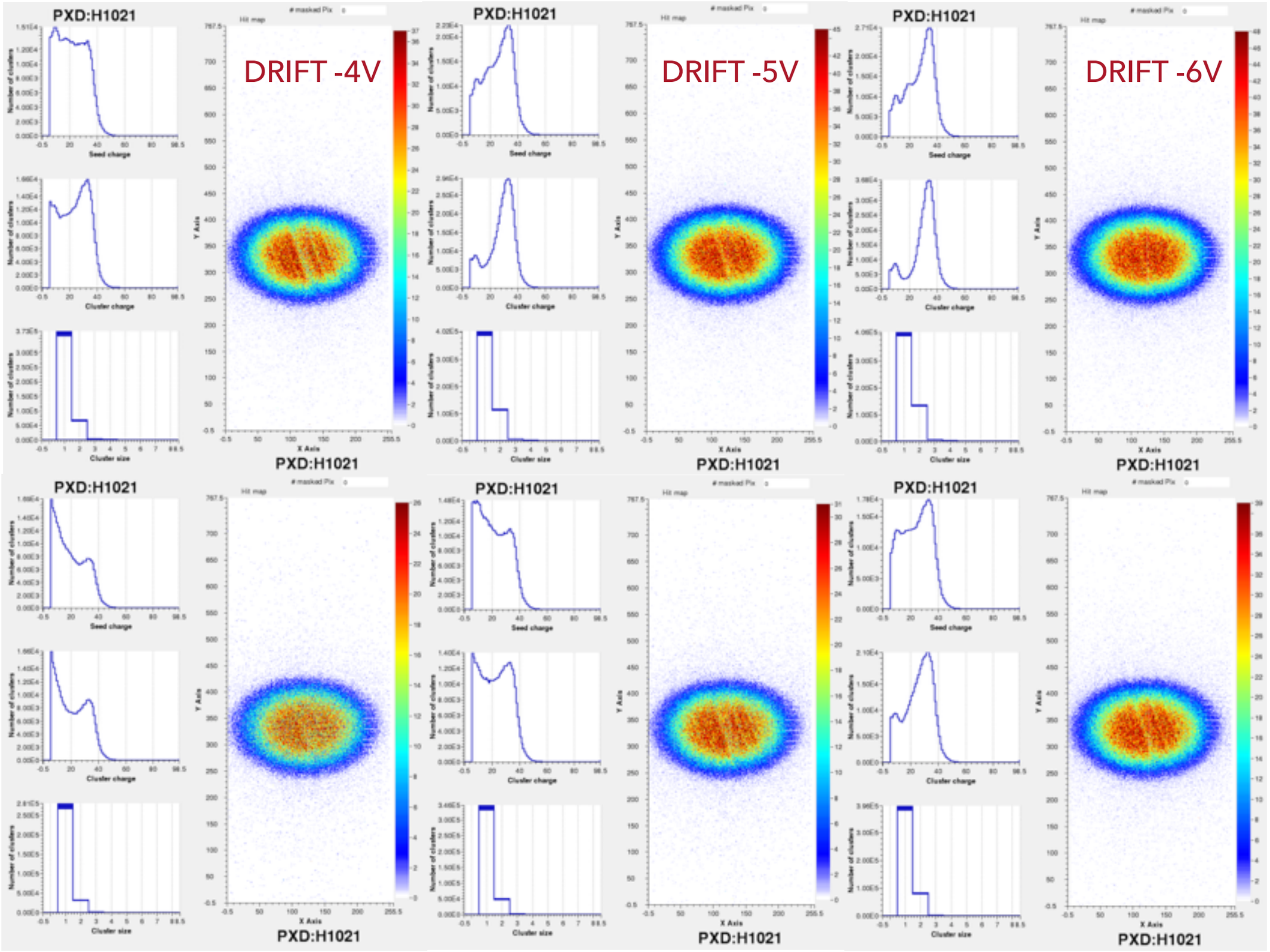
HV -60V



VOLTAGE SCAN: HV -64V, -68V

HV -64V

HV -68V

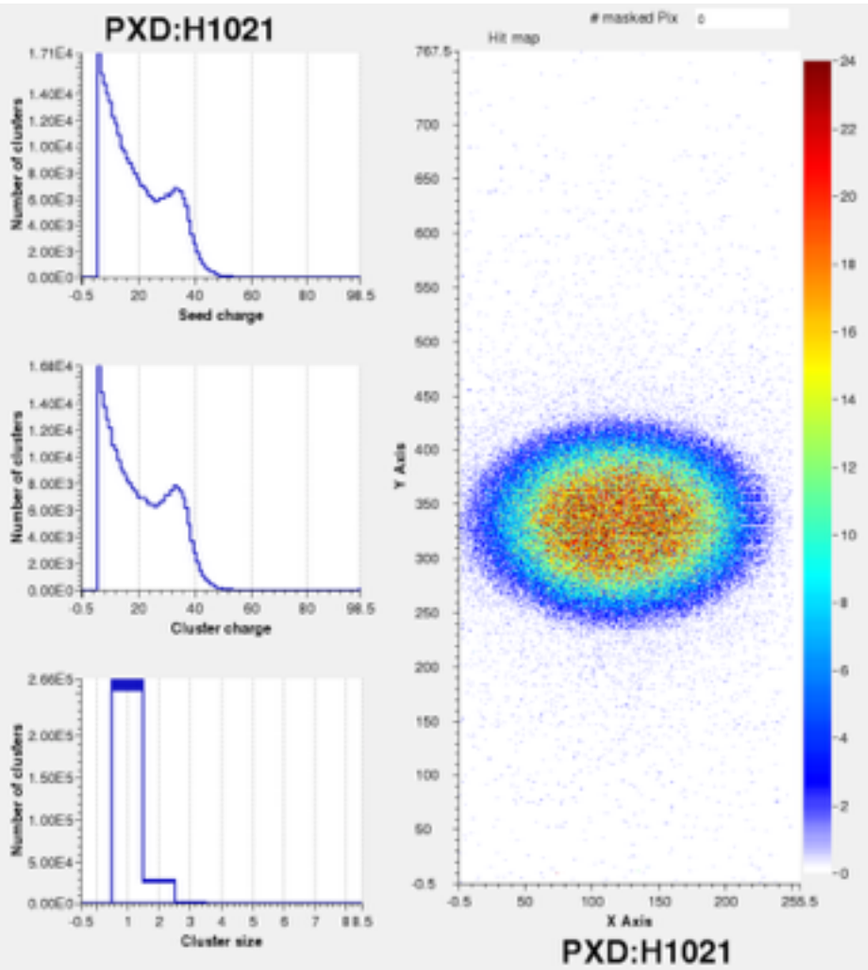


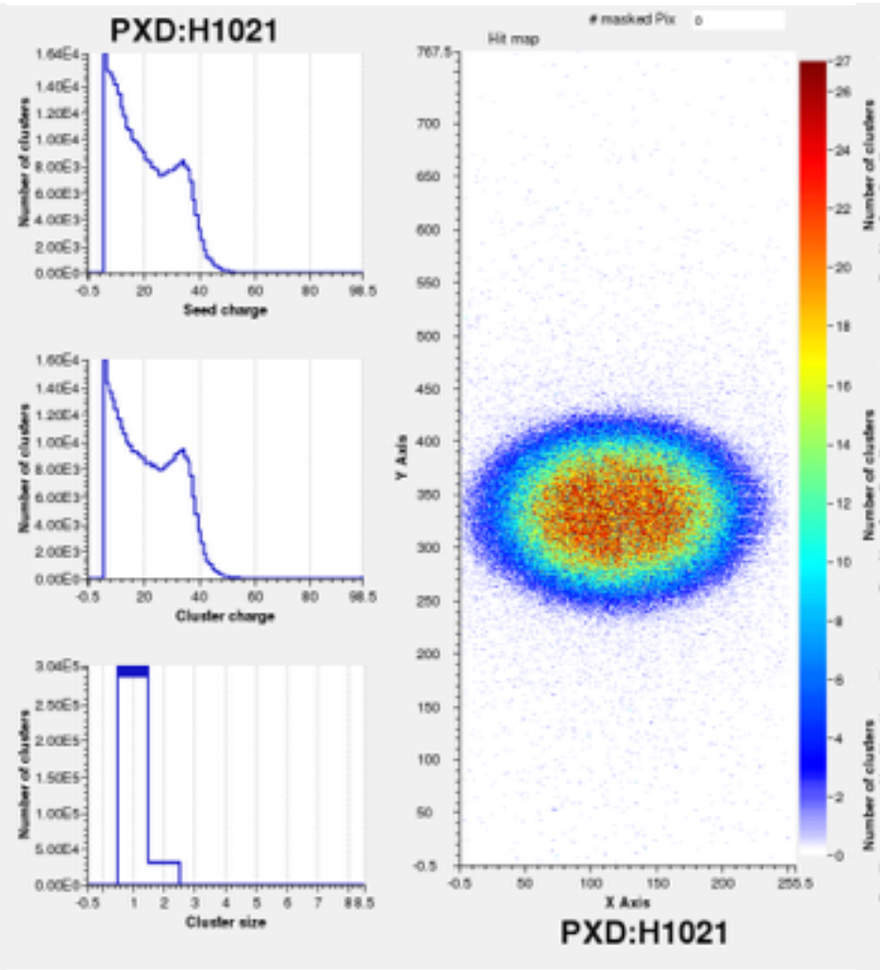
VOLTAGE SCAN: HV -72V

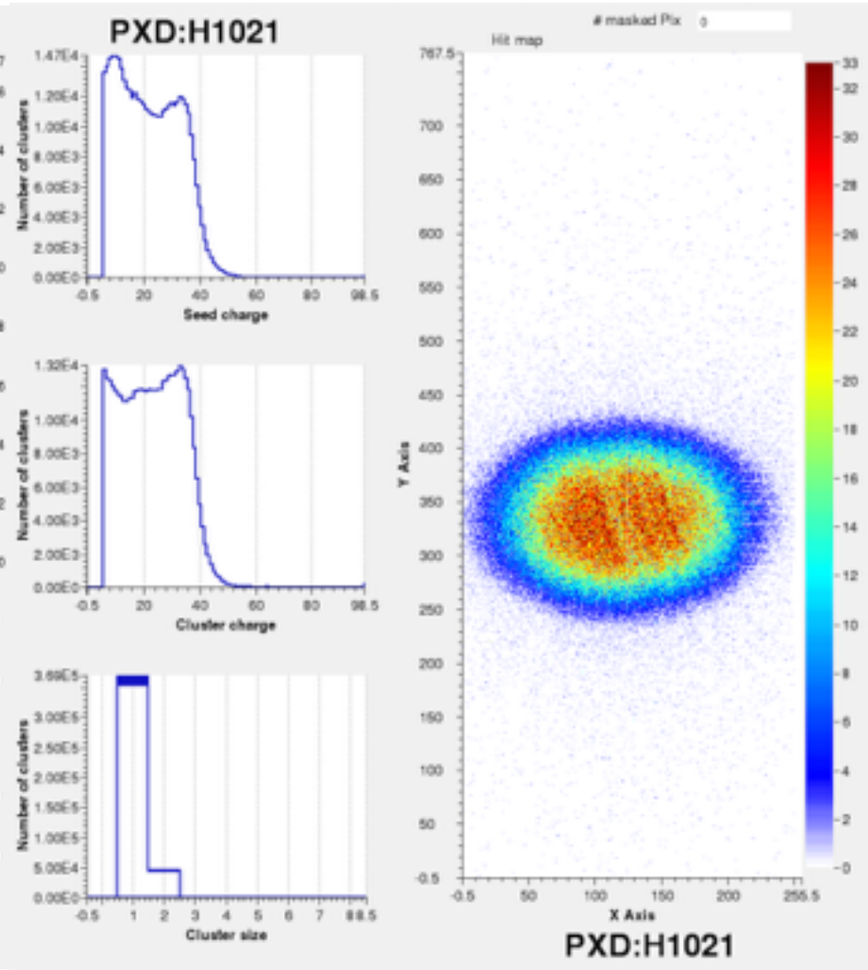
DRIFT -4V

DRIFT -5V

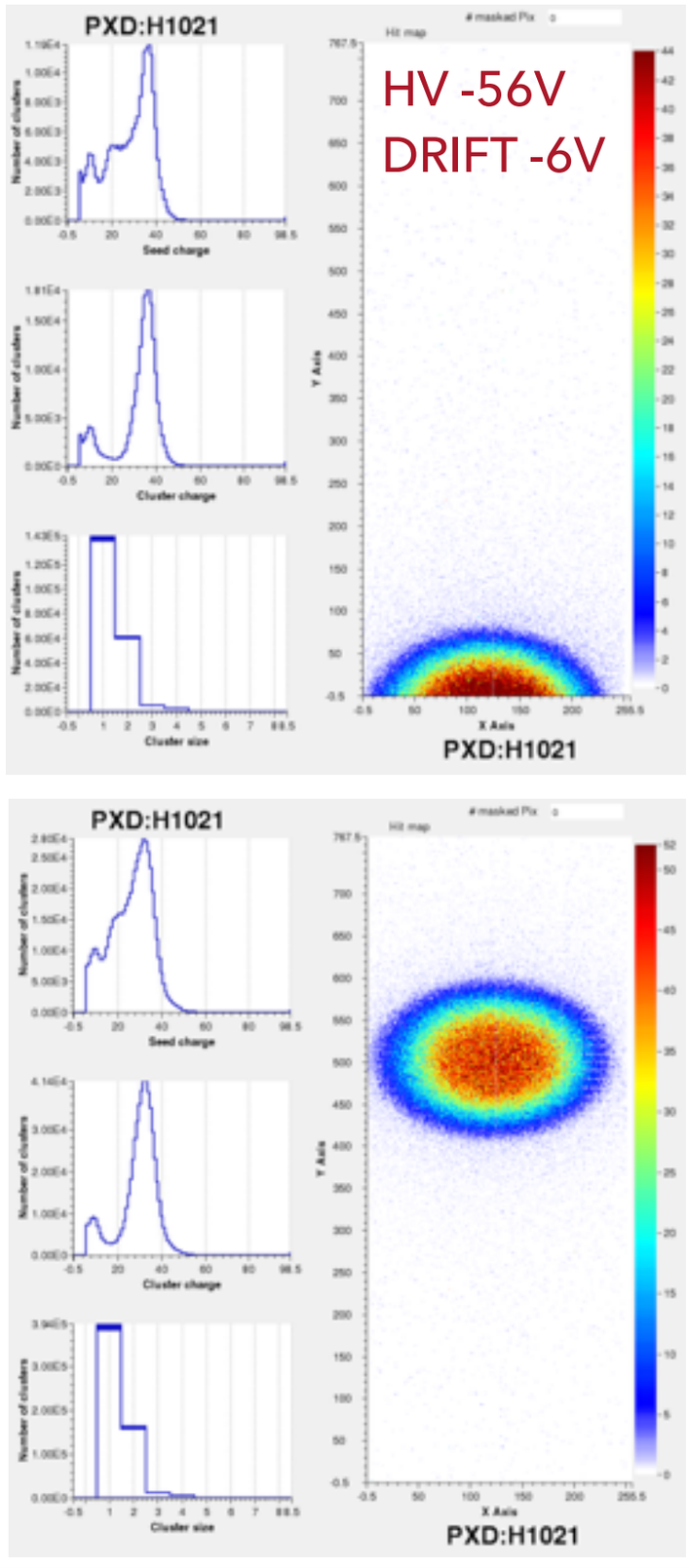
DRIFT -6V

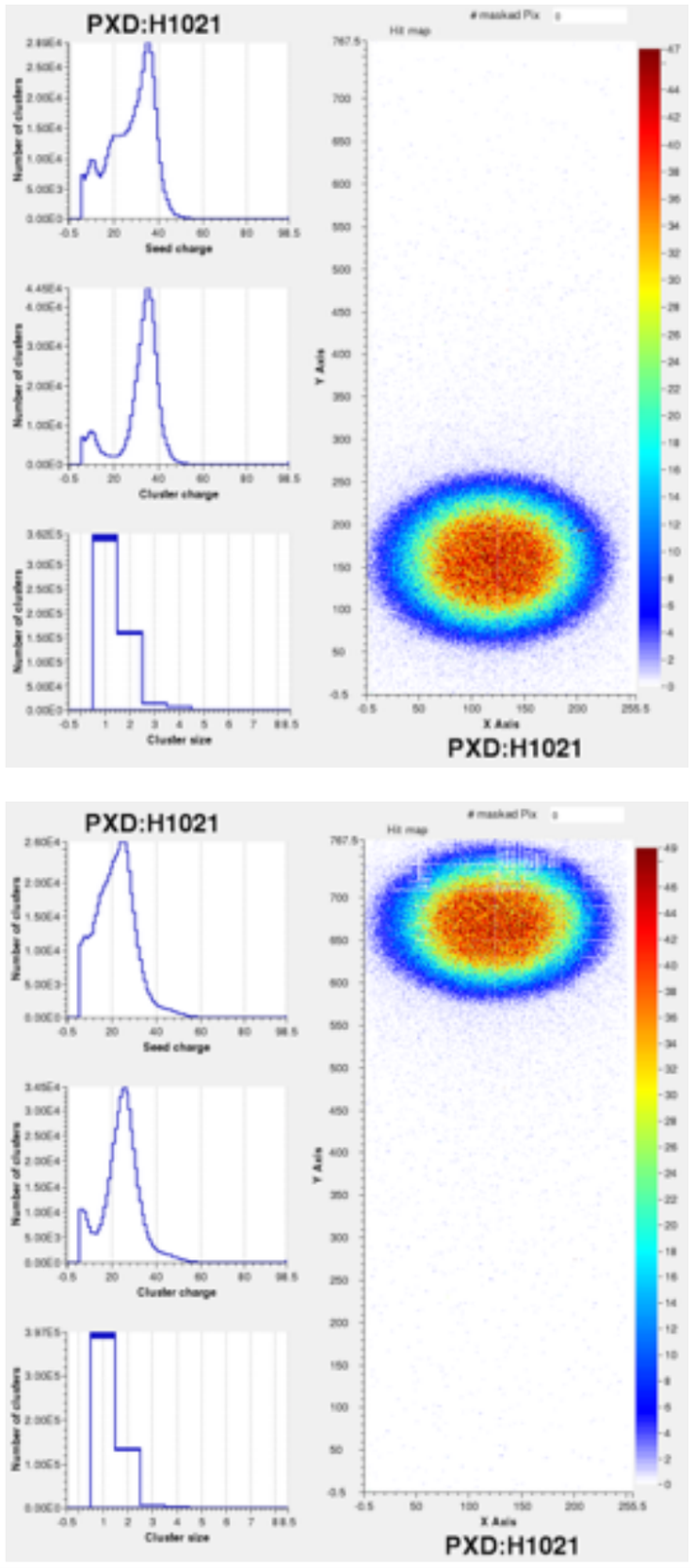


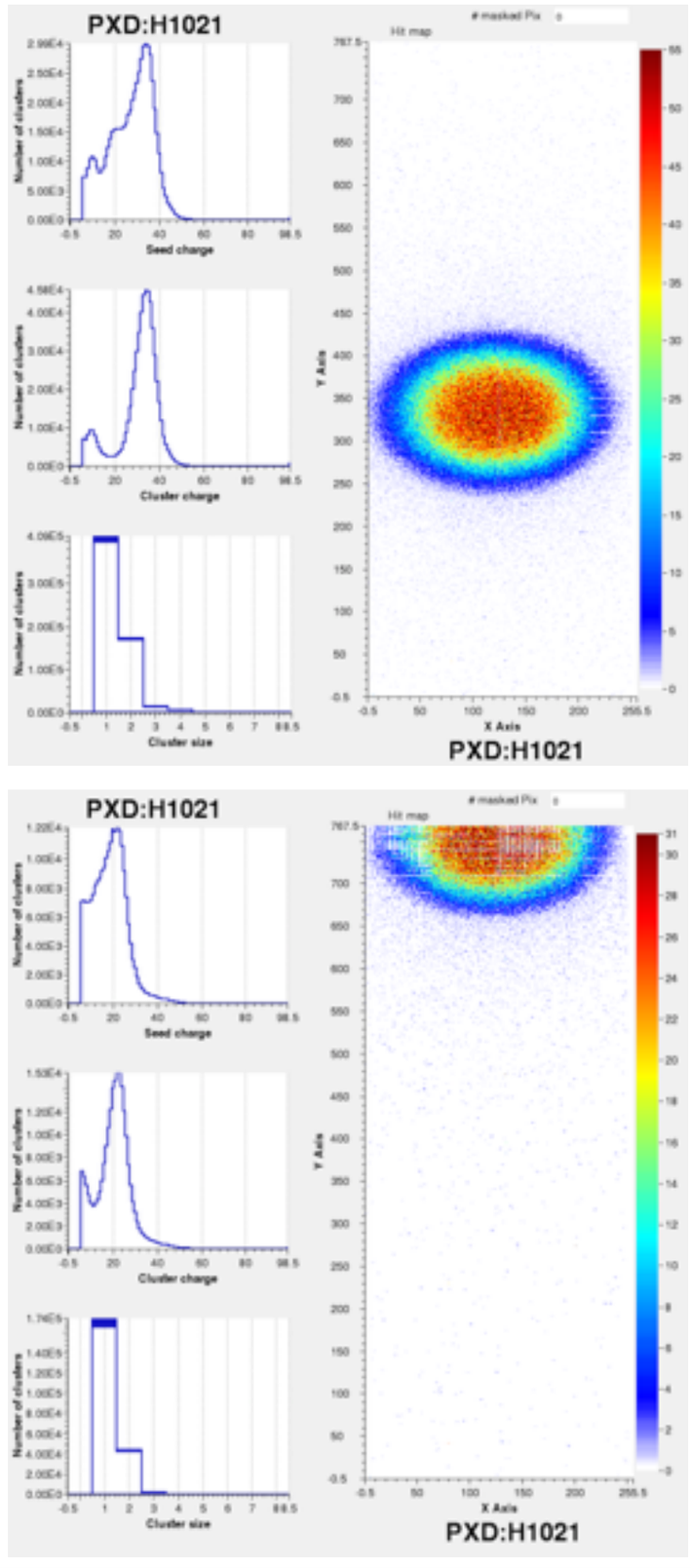




SPATIAL SCAN: MOVING THE SOURCE AROUND

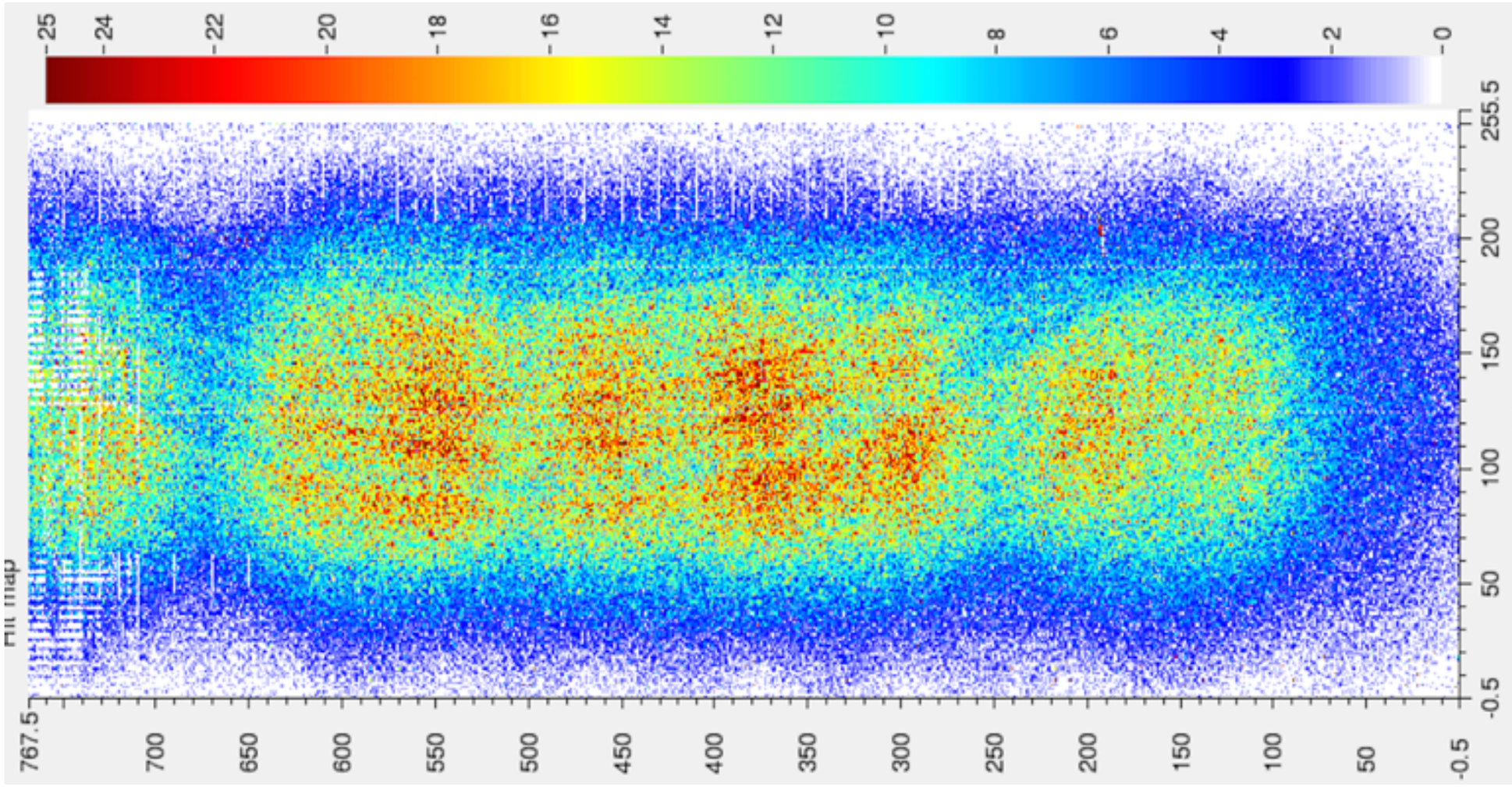






“SOURCE PAINTING”: LOOKING FOR THE RINGS

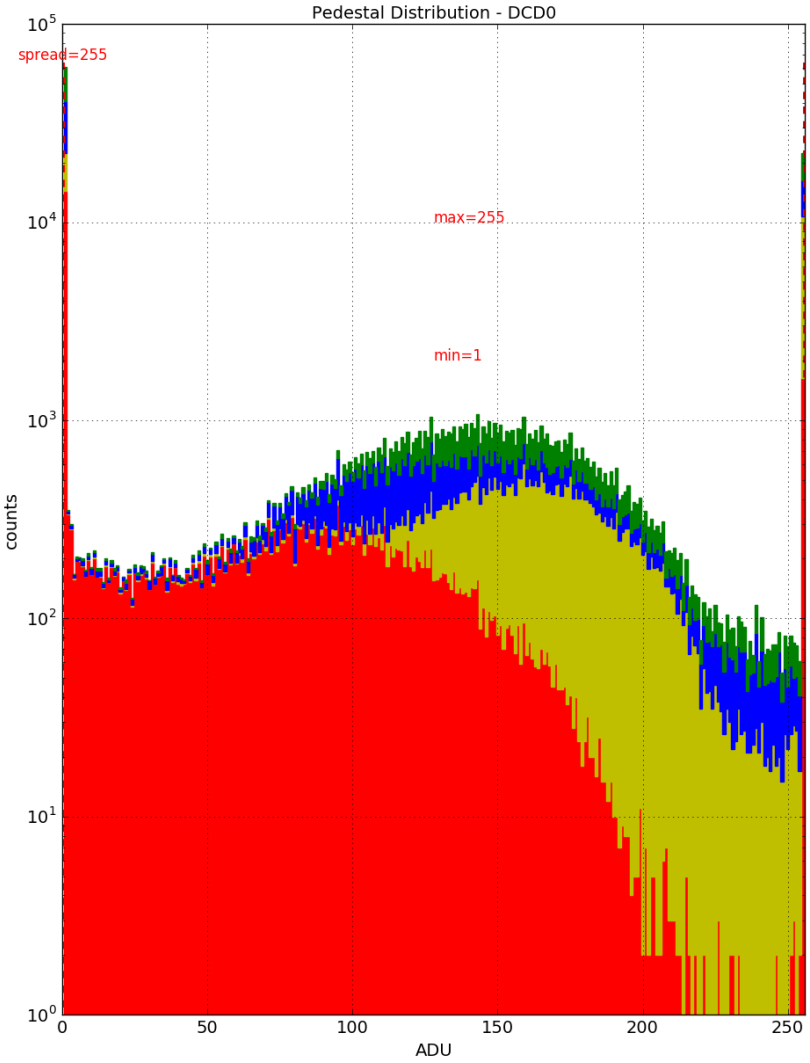
HV -64V
DRIFT -4V

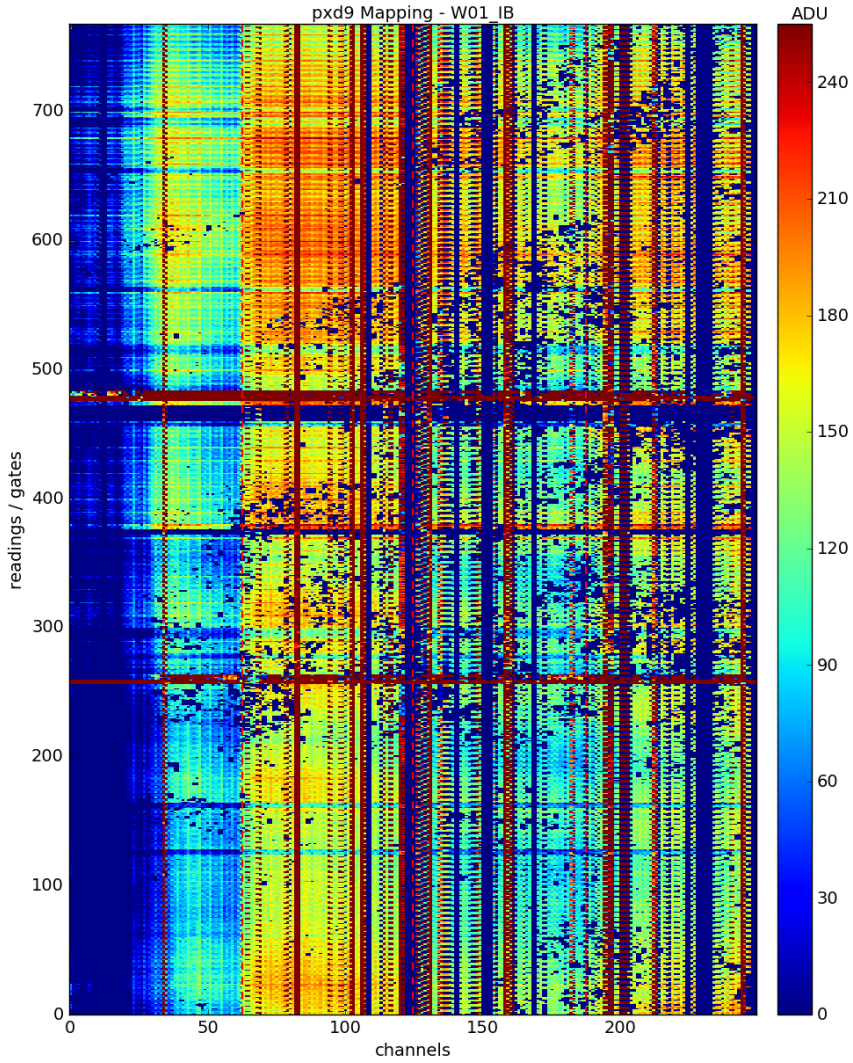


Phase 3 Module – W01_IB

Kapton with bad impedance line; anyway: all four links are stable

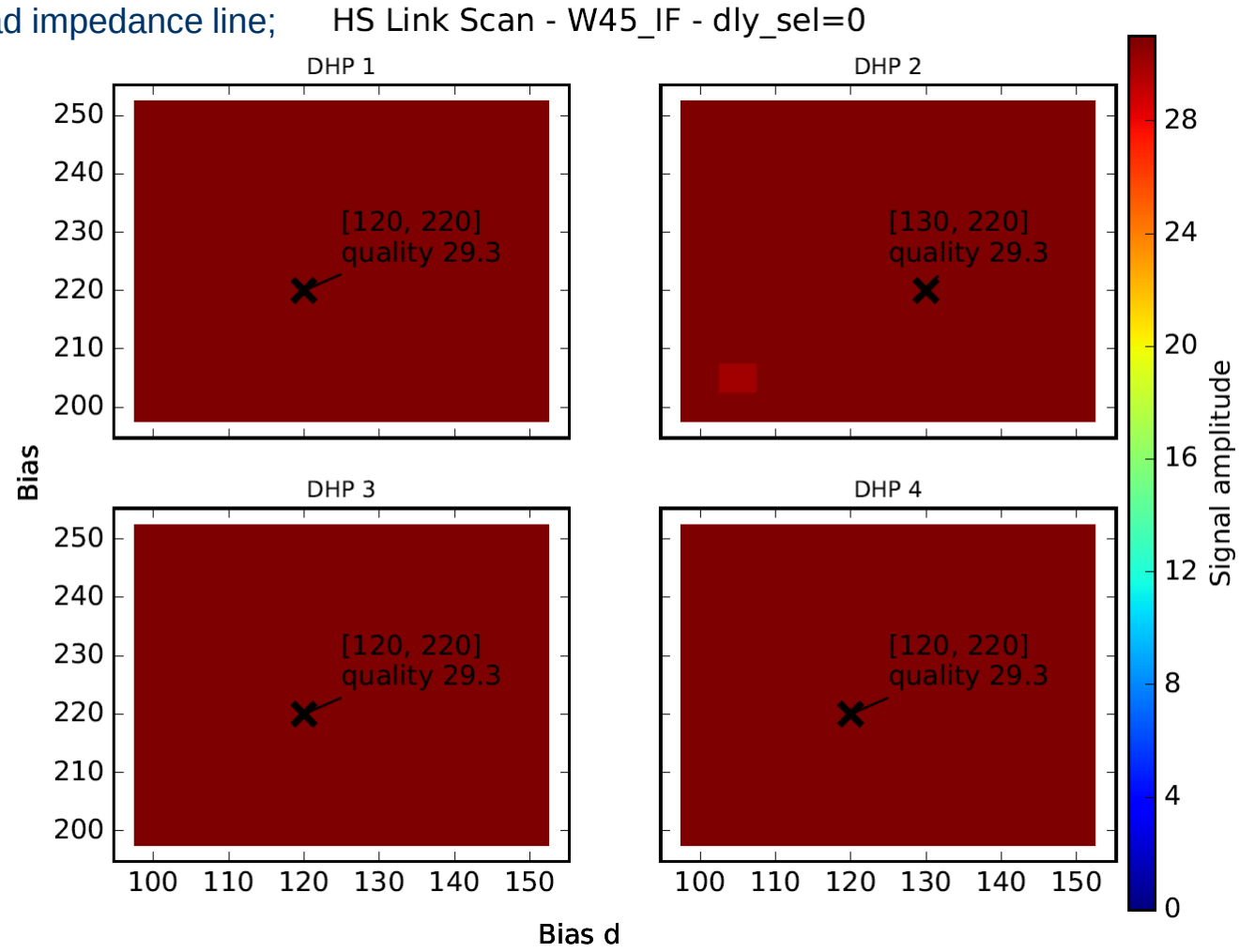
approximately 50 drain openings





Phase 3 Module – W45_IF

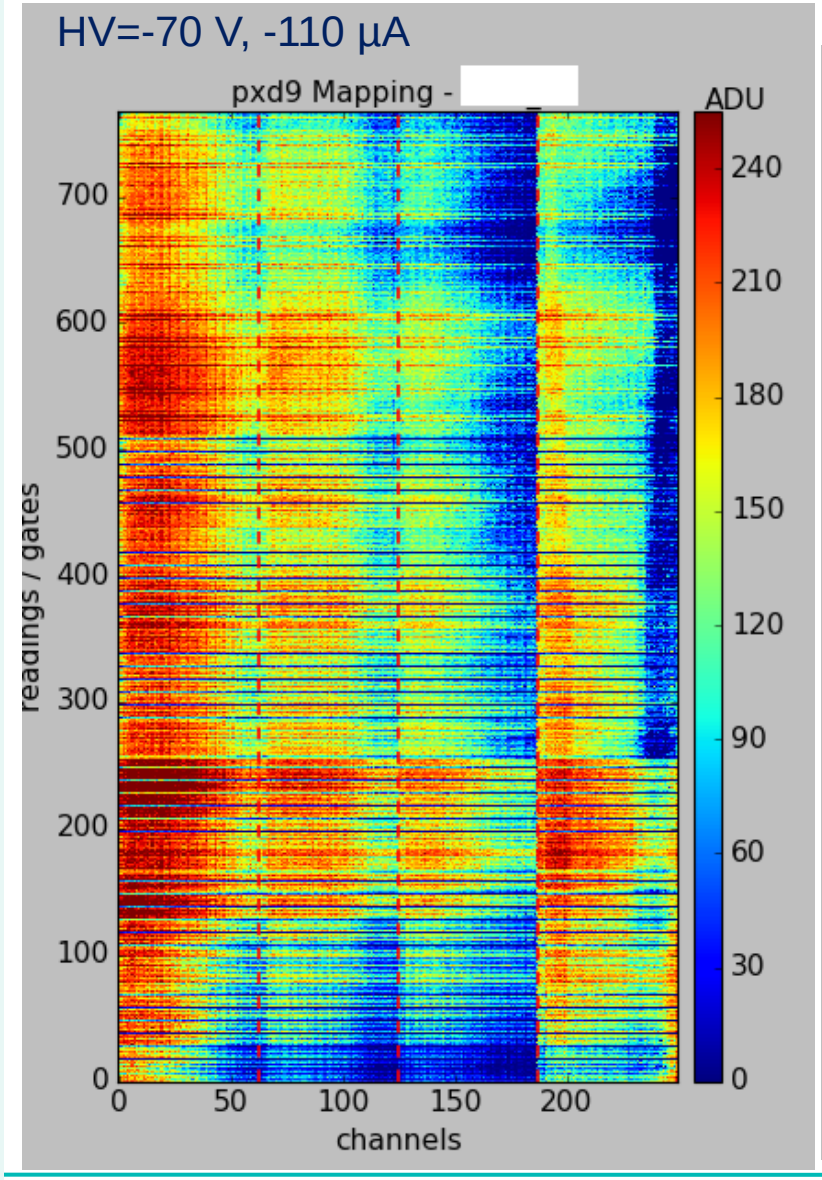
Kapton with bad impedance line;



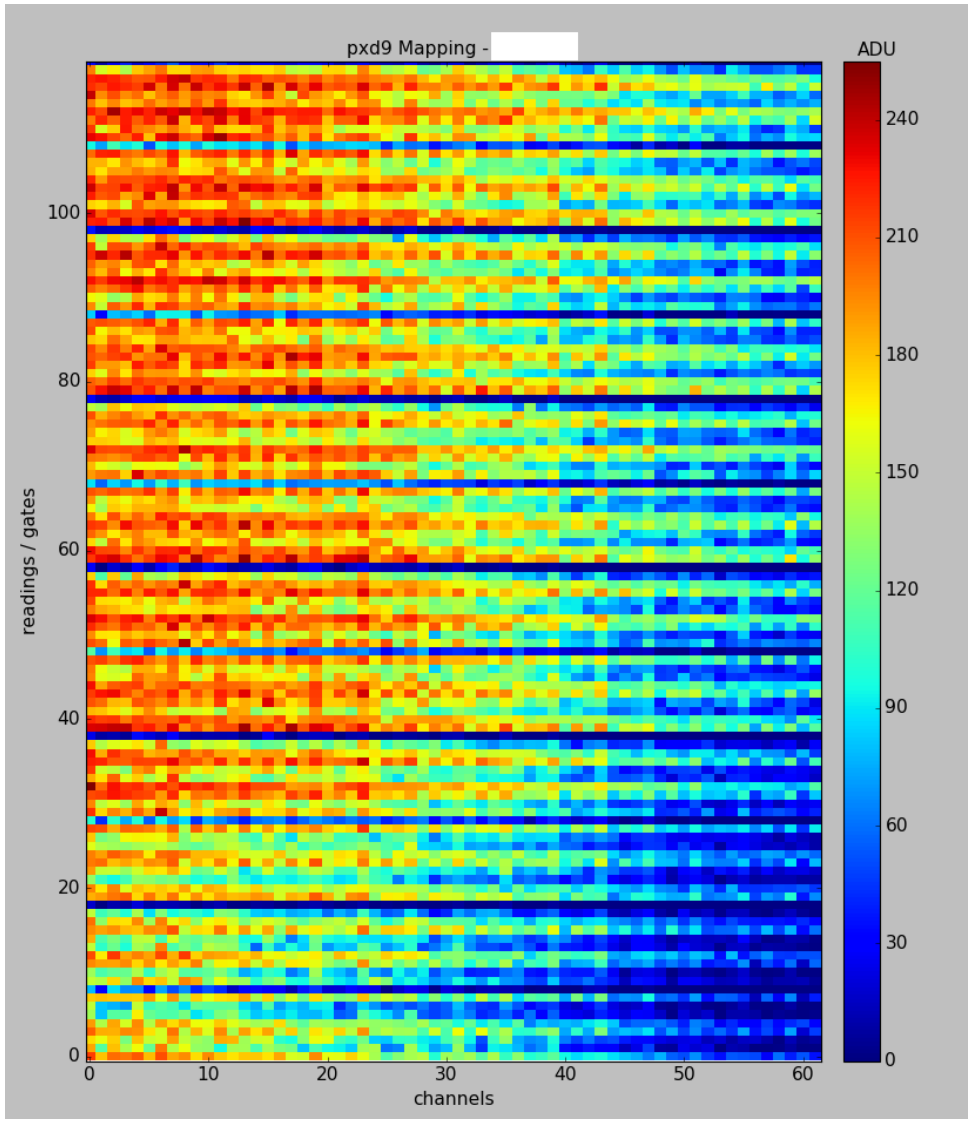
Matrix is under investigation

Phase 3 Module – W45_IF

HV=-70 V, -110 µA



Matrix is under investigation



to do

W37_OF1 source measurements

open topics:

- source measurement scripts – the ones used in online monitor; for reliable offline analysis, like S/N ratio, peak to valley, etc.
- not all scripts are well-developped according to the coding guidelines (offsets, sampling point curve, source measurements, gated mode)
- Problem: measuring and performing development (not quick and dirty) cannot be done simultaneously – ideas?

Services

Delivery:

4 Stück zum 11.08.17 (L1BWD, L1FWD, L2BWD, L2FWD)

4 Stück zum 31.08.17 (L1BWD, L1FWD, L2BWD, L2FWD)

Problems with