Modules from batch P3-1 overview

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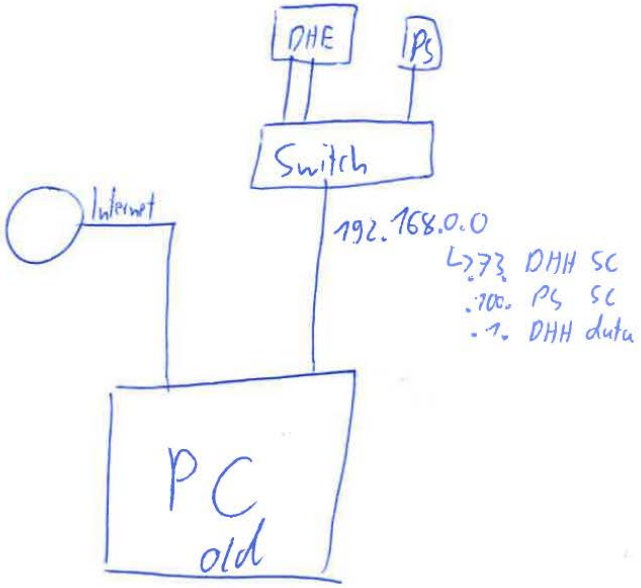
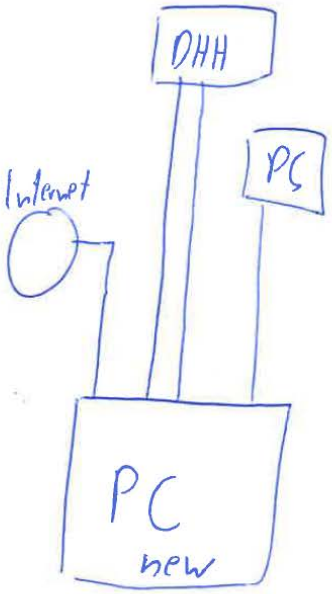
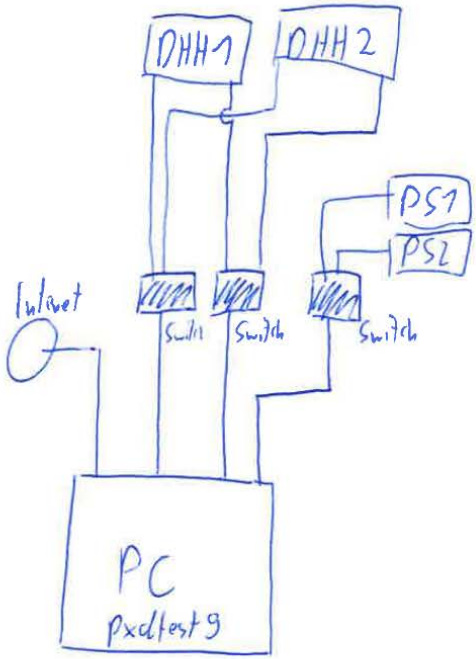
Setup configuration

dedicated network cards for DHH SC, DHH data, PS SC

1 archiver for all setups







Power Up Sequence & PS & DHE

With the new network configuration we can use the automatic power up sequence

(check whether the Switcher sequence is written into the DHP memory correctly)

received 2 new PS from LMU (since 3/5 showed strange behavior)

The setups are equipped partially with PS with OVP (over voltage protection) but disabled, since the PS sequence violates the constraints of the OVP

PS are tested without module (voltage checks) and with W31_OB1 (module on ladder L2X12)

to do: need to change PS sequence such that it does not violate the OVP constraints

changed R76 to 16 kOhm for sensing the DHP voltage

DHH Firmware / Ladder setup

Stable Firmware, which was/is used for module testing

https://wwwold.e18.physik.tu-muenchen.de/belle/firmware/dhe_2017062122_hll0_copper.zip

For ladder we need two DHEs, with 2 different IP addresses: 192.168.73.10 + .11

Only a more developed version is available with 192.168.73.11; what are the differences?

How to operate the modules synchronously (clock and readout)? Will there be any problems regarding X-talk? How to proceed? DHC required? Software?

batch P3-1

since last lab meeting (20.09.2017) the setups were modified and the archiver was prepared; module testing is now ongoing

W47_IB: hs_link, delays, pedestals, adc_curves, sample_point_curve

W02_IB: hs_link, delays, pedestals, adc_curves

W47_IF: hs_link, delays, pedestals, adc_curves (started and interrupted)

Software issues:

- adc_curve measurement seems to run unstable (observed on different setups, root partition runs out of space)
- sampling_point_curve: need to verify switcher sequence; this additional check requires to set GateOn=GateOff and ClearOn=ClearOff, i.e., measurement extends to approximately 10-20 min (instead of 2 min)

Suggestion - Temperature

What frequency is used for the temperature readout?

For the testing, a fraction of the scripts have long communication (a couple of minutes) with ASICs via JTAG (writing pedestal masks, writing offsets)

Can the process of writing JTAG be interrupted for intermediate temperature readout in order to avoid overheating?

In what time interval does the temperature increase (depending on missing/defective clamps / loss of cooling system)