



$$\Delta p \cdot \Delta q \geq \frac{1}{2} \hbar$$



Test reports from MPP

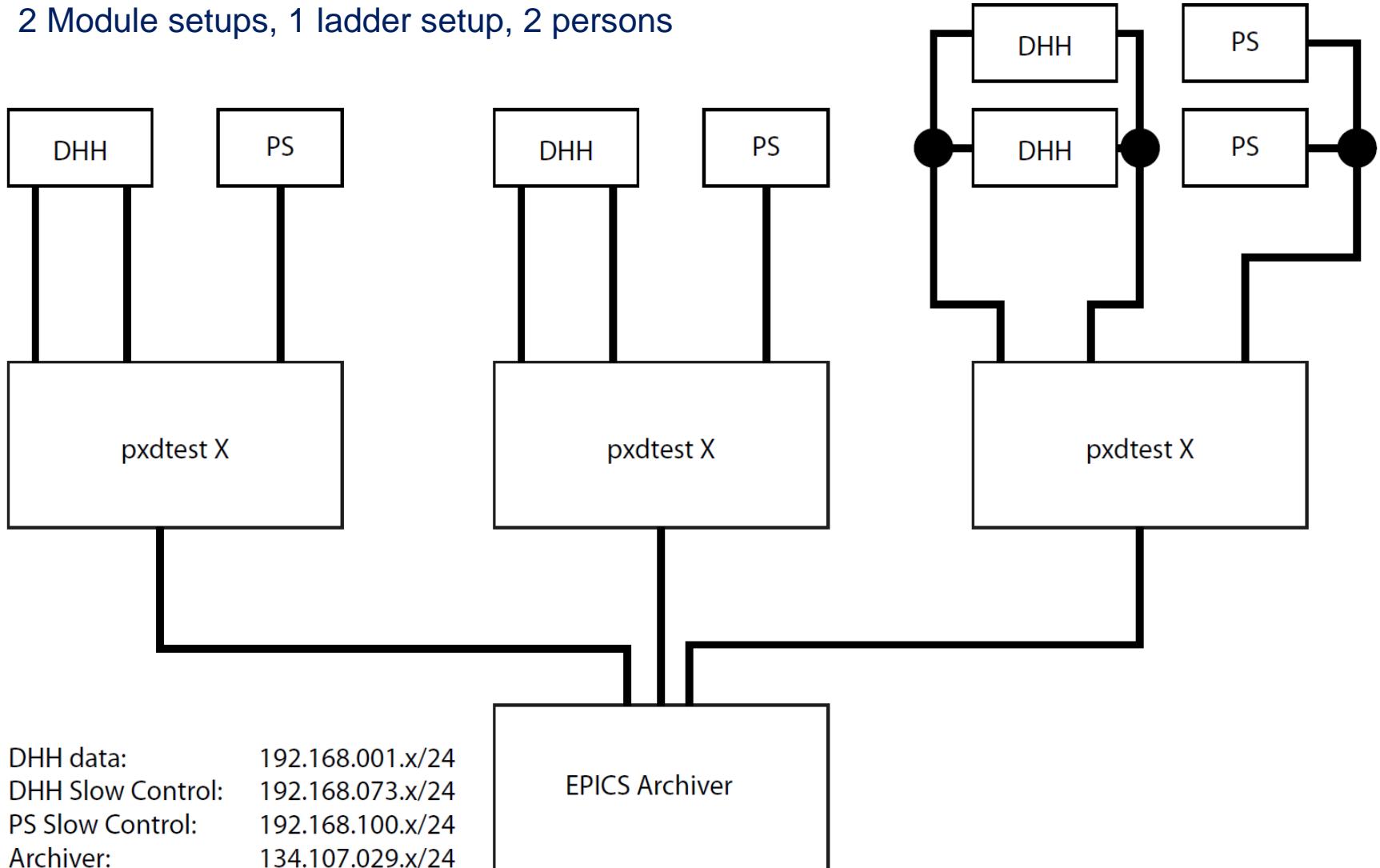
Philipp Leitl, Felix Mueller

PXD BPAC pre-meeting 29.09.2017



Setup configuration

2 Module setups, 1 ladder setup, 2 persons

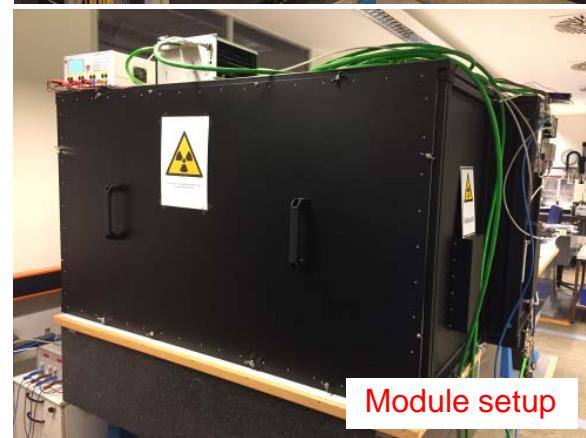
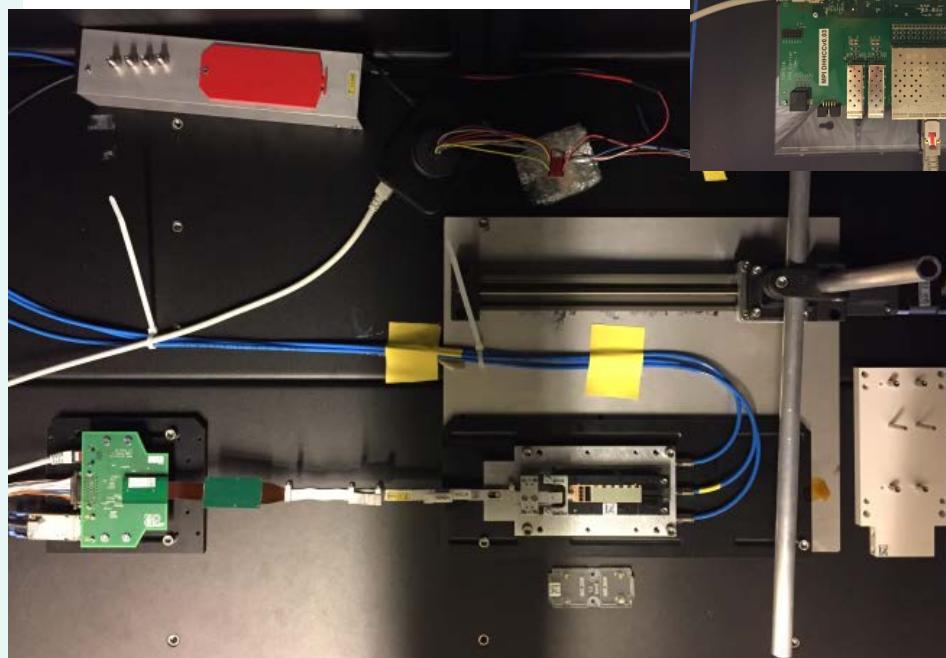




Setups



Module setup



Module setup



Ladder setup



Module checks before glueing

- **DHPT high speed (HS) Links**
short scan (to have a reference for later)
 - bias 200 to 250, step 5
 - bias_d 100 to 150, step 5
 - delay 0

~15 min
- **Delays** ~15 min
- **ADCs optimization using small parameter space** ~14 h (night scan)
- **Pedestal/noise (1k frames)** ~10 min
- **2-bit offset (delay and current source optimization)** ~ 15 min
- **Pedestal/noise (1k frames)** ~10 min
- **DCD analog common mode correction (ACMC)** ~1 min
- **Pedestal/noise (1k frames)** ~10 min
- **Source measurement different regions** ~ ? min/h
 - Threshold 5
 - Verify shape of the spectra
 - SNR in different regions
 - Adjust VNSubIn / Use ACMC



Module checks before glueing - Issues

- **DHPT high speed (HS) Links**
short scan (to have a reference for later)
 - bias 200 to 250, step 5
 - bias_d 100 to 150, step 5
 - delay 0
- **Delays** ✓
- **ADCs optimization using small parameter space**
- **Pedestal/noise (1k frames)** not defined what to analyse – compare etc?
- **Sampling Point Curve** – missing: verification of the Switcher sequence in DHP memory
- **2-bit offset (delay and current source optimization)** coding guidelines missing but working
- **Pedestal/noise (1k frames)** - same as above
- **DCD analog common mode correction (ACMC)**
- **Pedestal/noise (1k frames)** - same as above
- **Source measurement different regions** – not tested at MPP up to now (is the stepper implemented)
 - Threshold 5
 - Verify shape of the spectra
 - SNR in different regions
 - Adjust VNSubIn / Use ACMC



Modules tested at MPP

before glueing to ladders

W31_IF, W37_IB = L1X12 (prototype)

W31_OB1, W30_OF1 = L2X12 (prototype, W30_OF1 3 Switchers without substrate connrction)

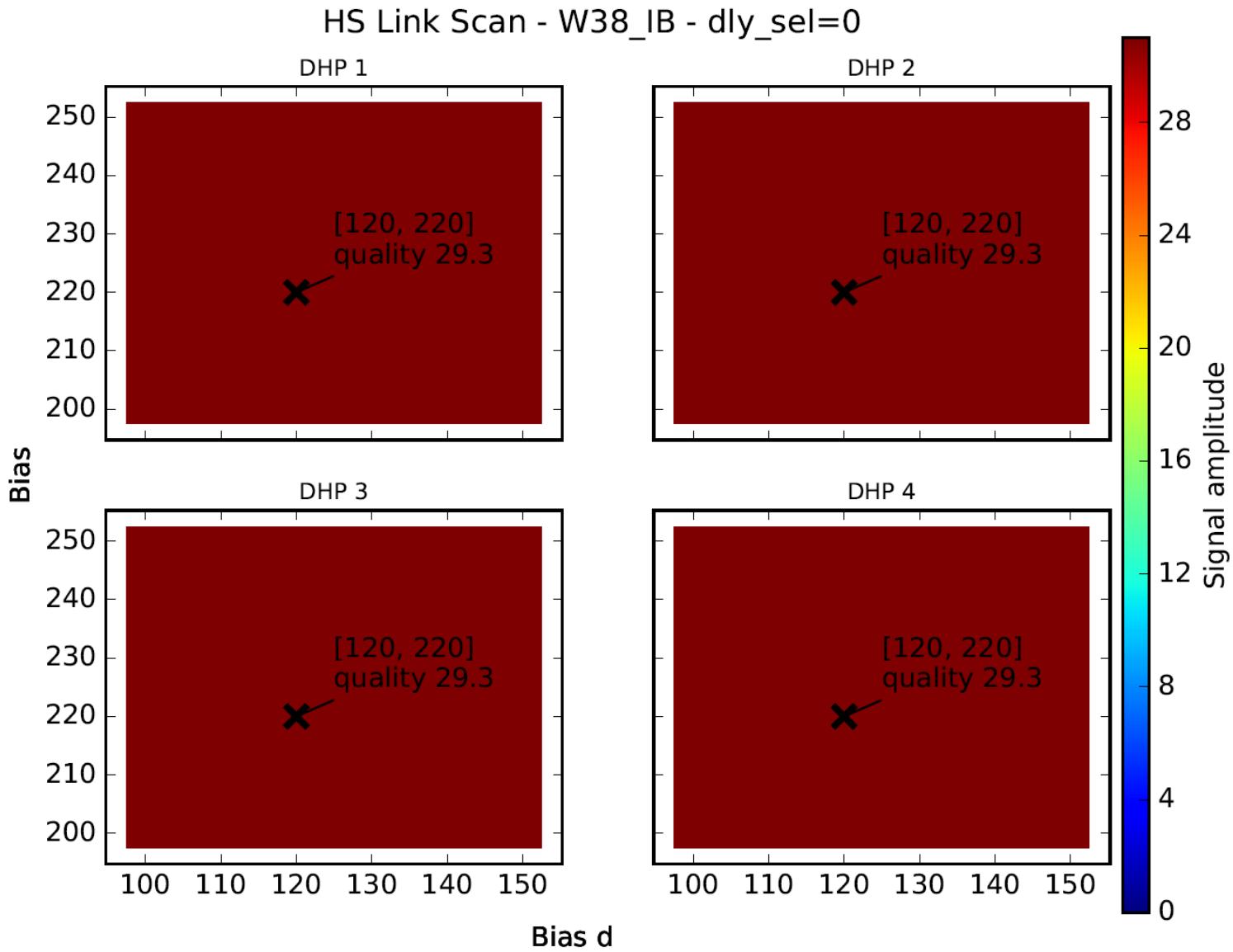
W38_IB, W40_IF = L_001 (production)

W01_IB, W45_IF = L1-03 (production)

W37_OF1

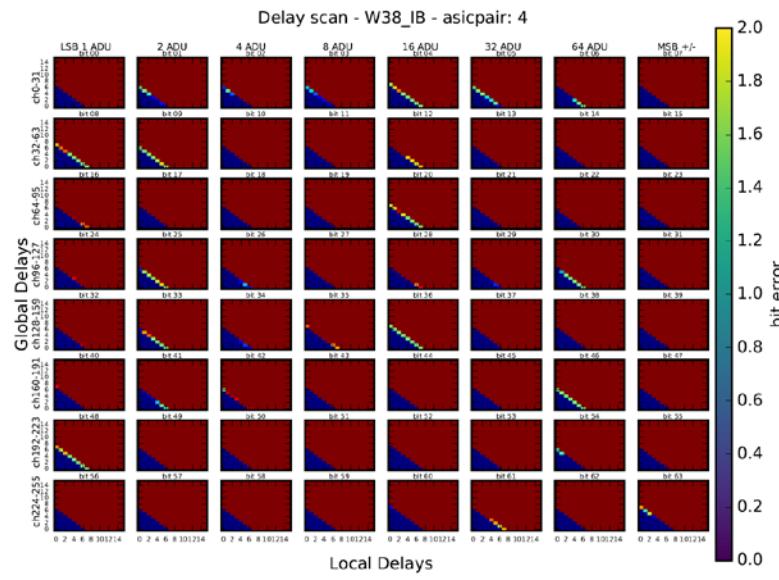
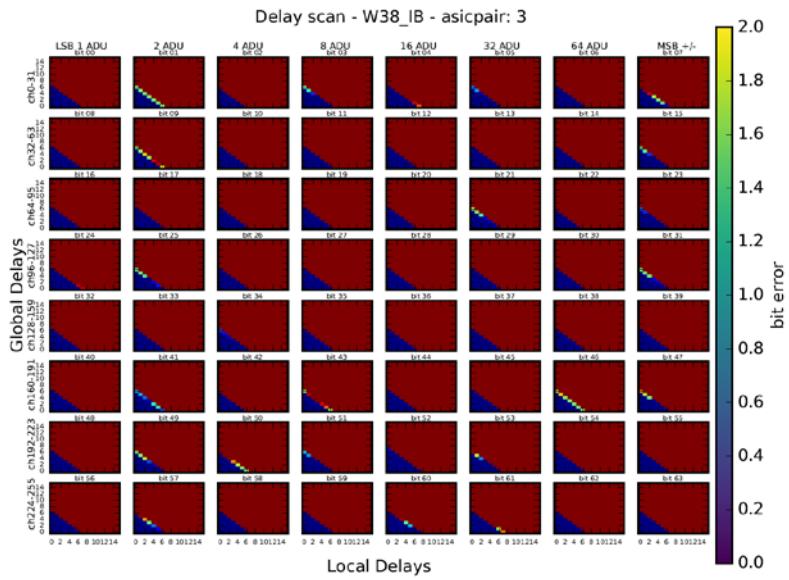
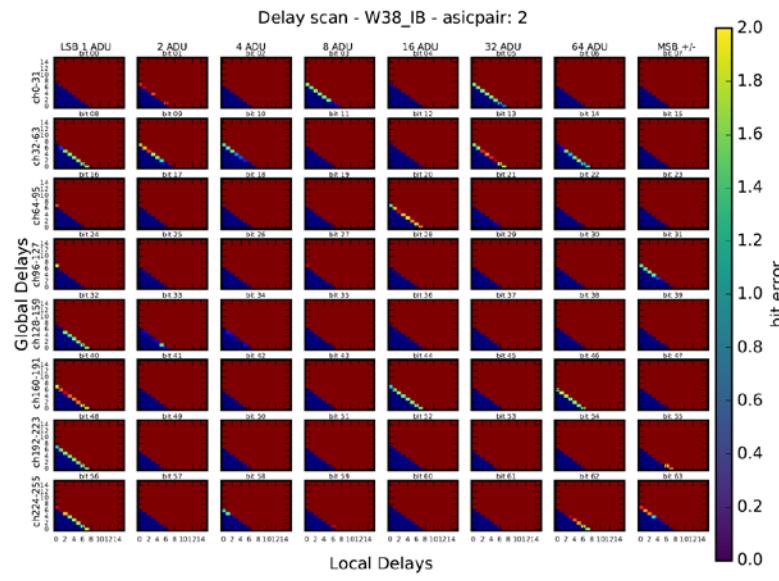
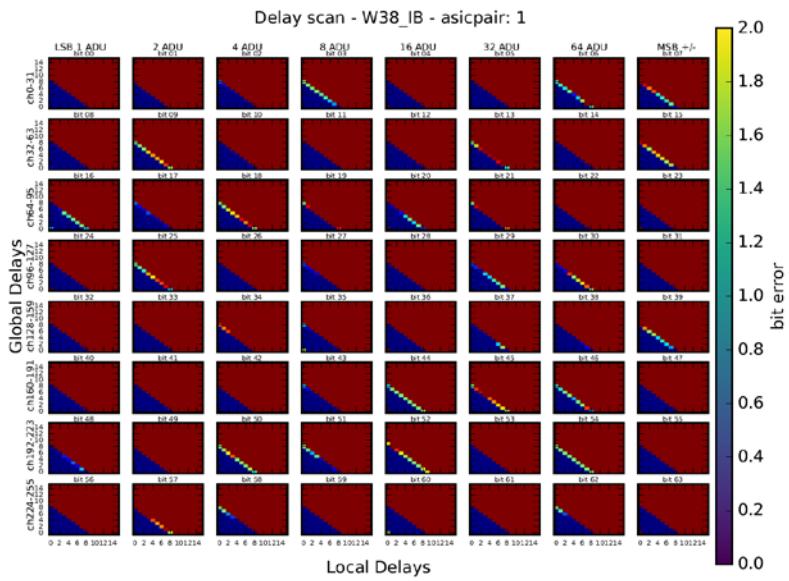


W38_IB – HS links





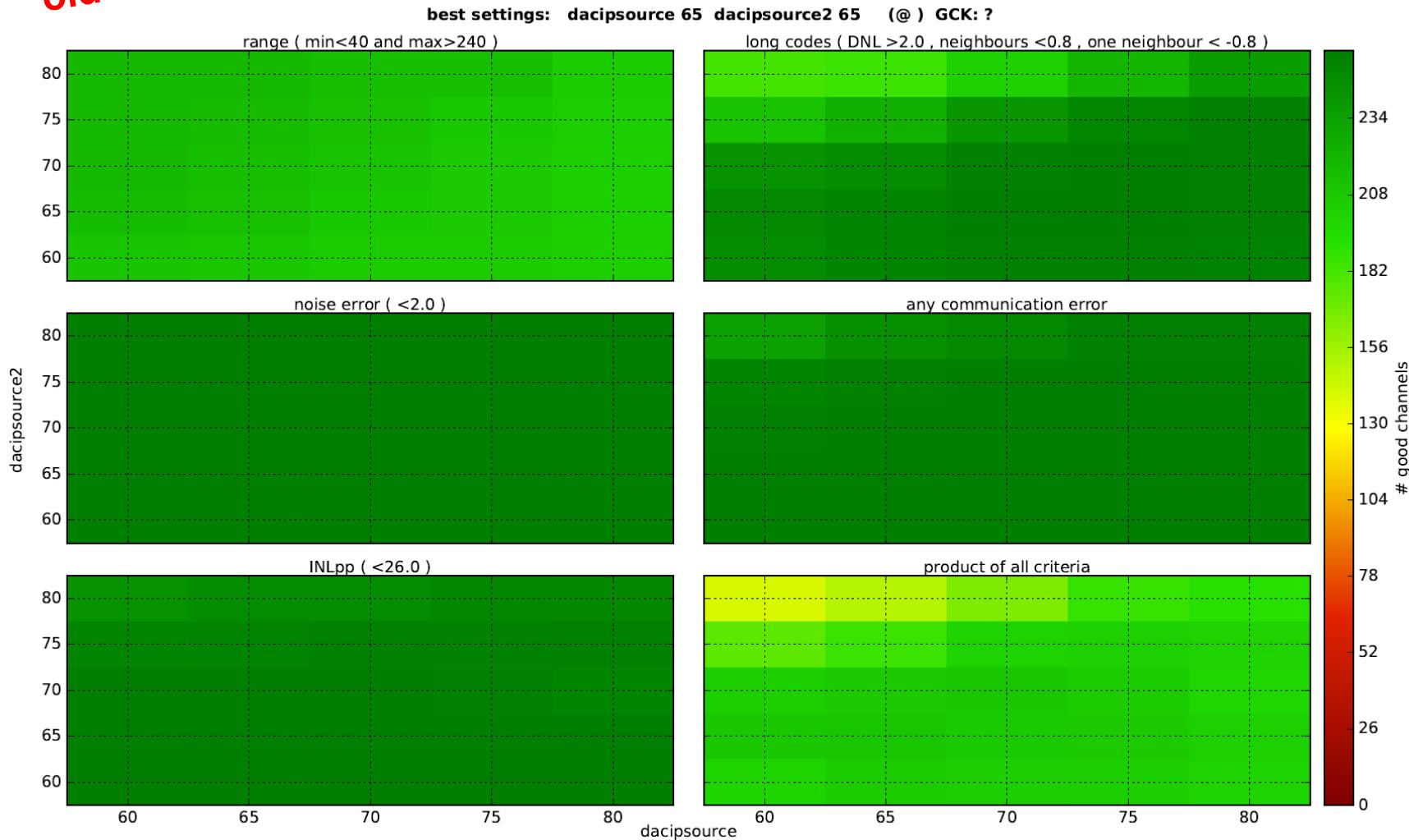
W38_IB – delays





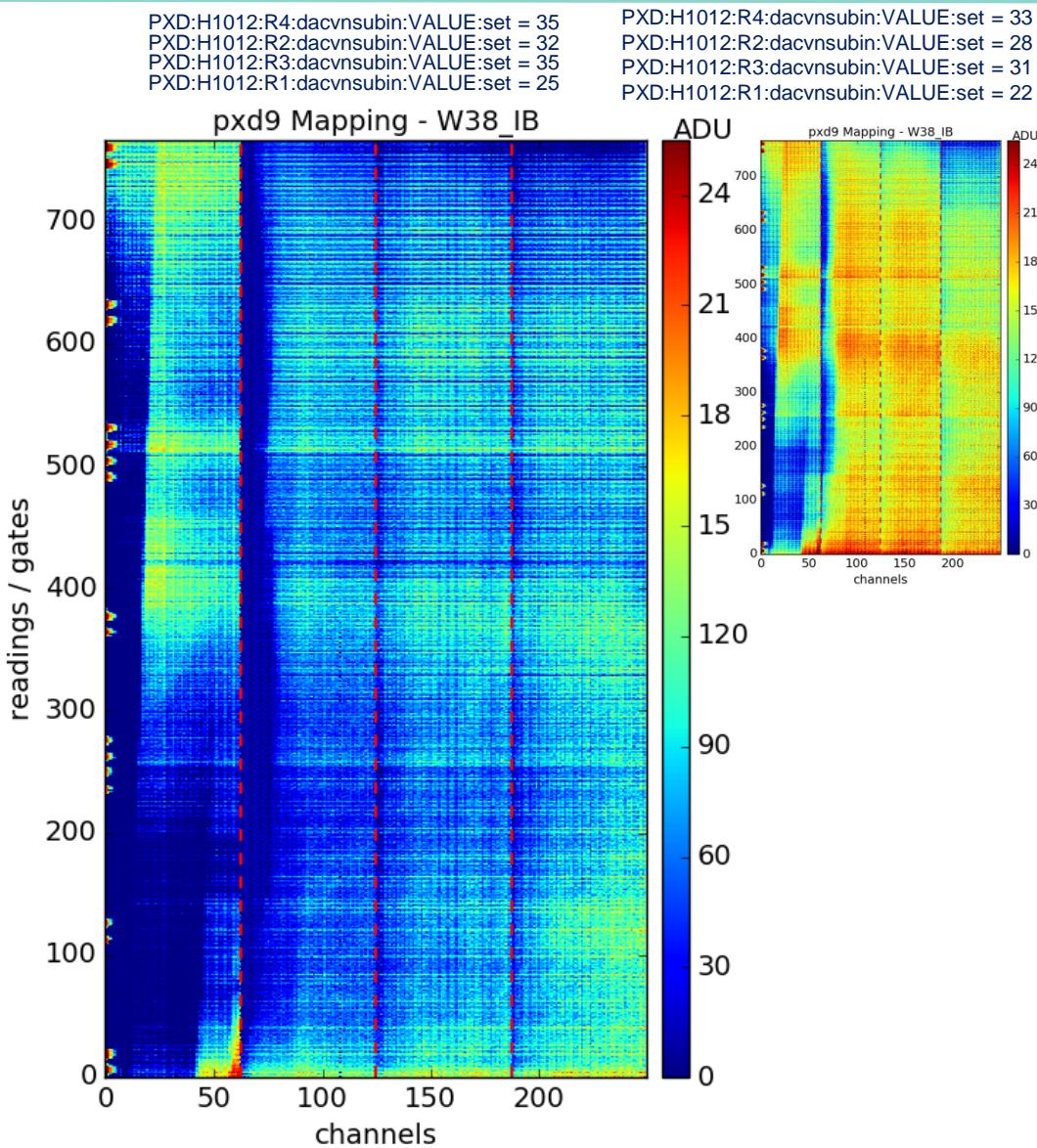
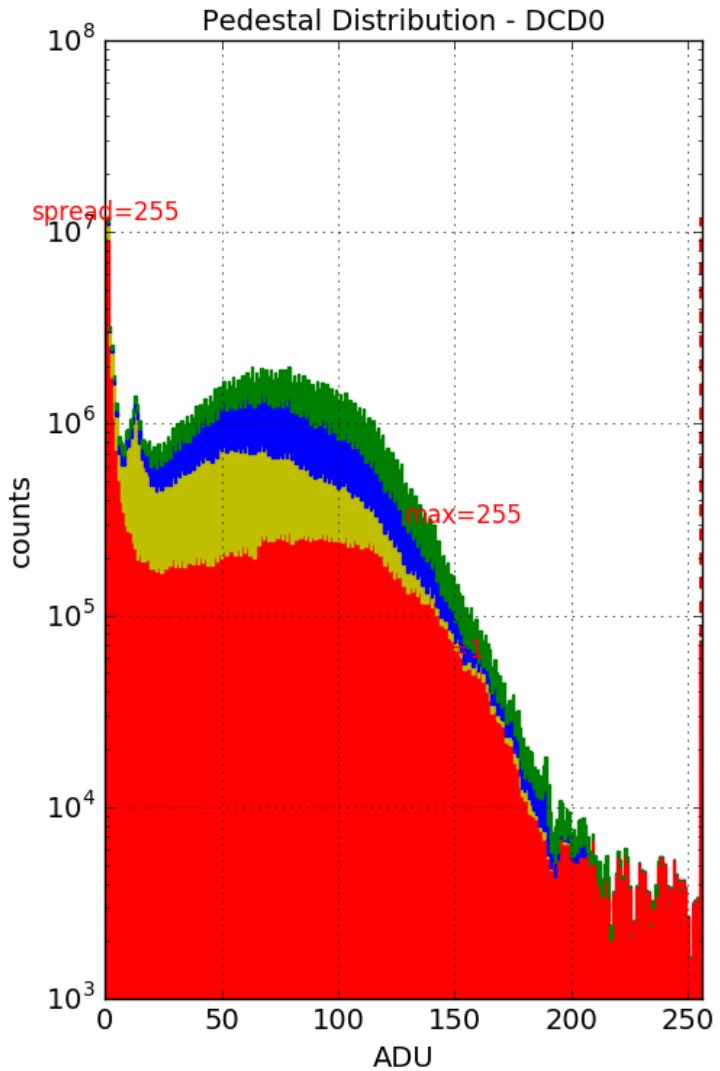
W38_IB – ADC curves

old analysis script



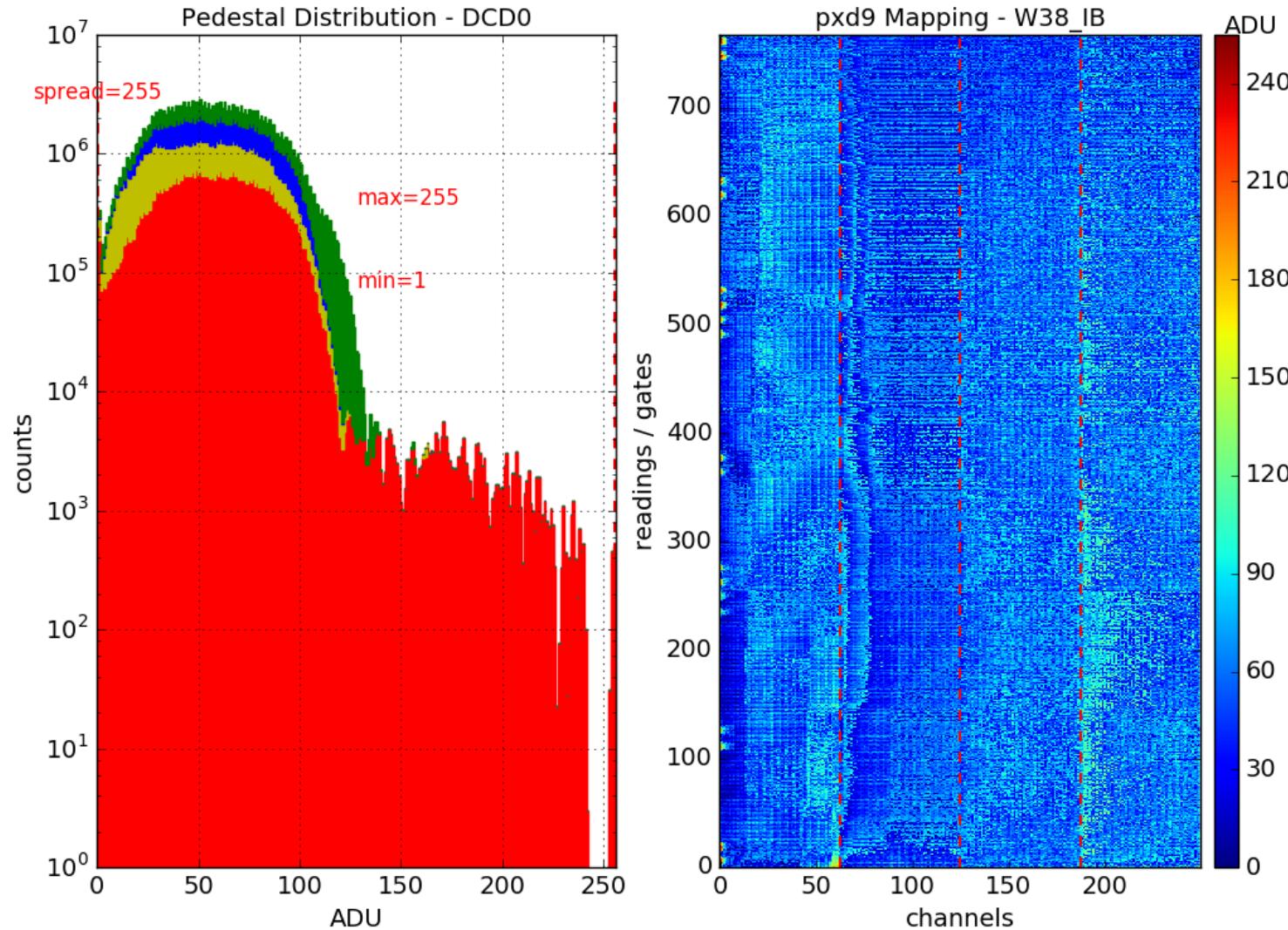


W38_IB – pedestals without Offsets and no ACMC



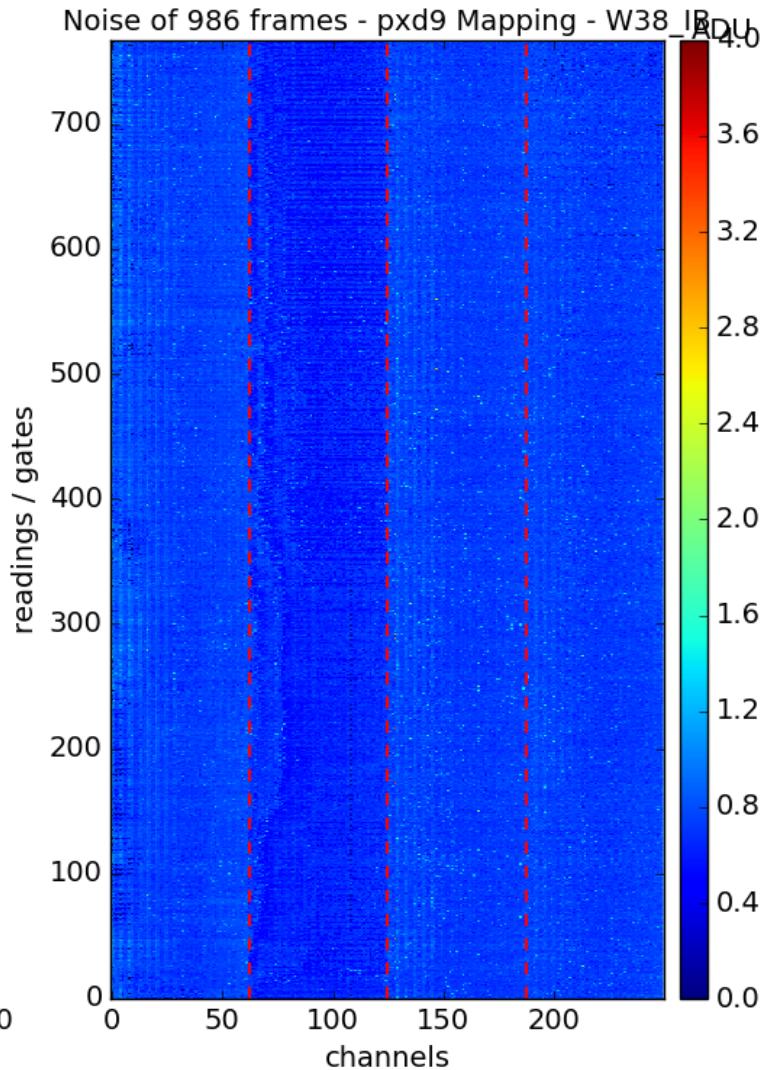
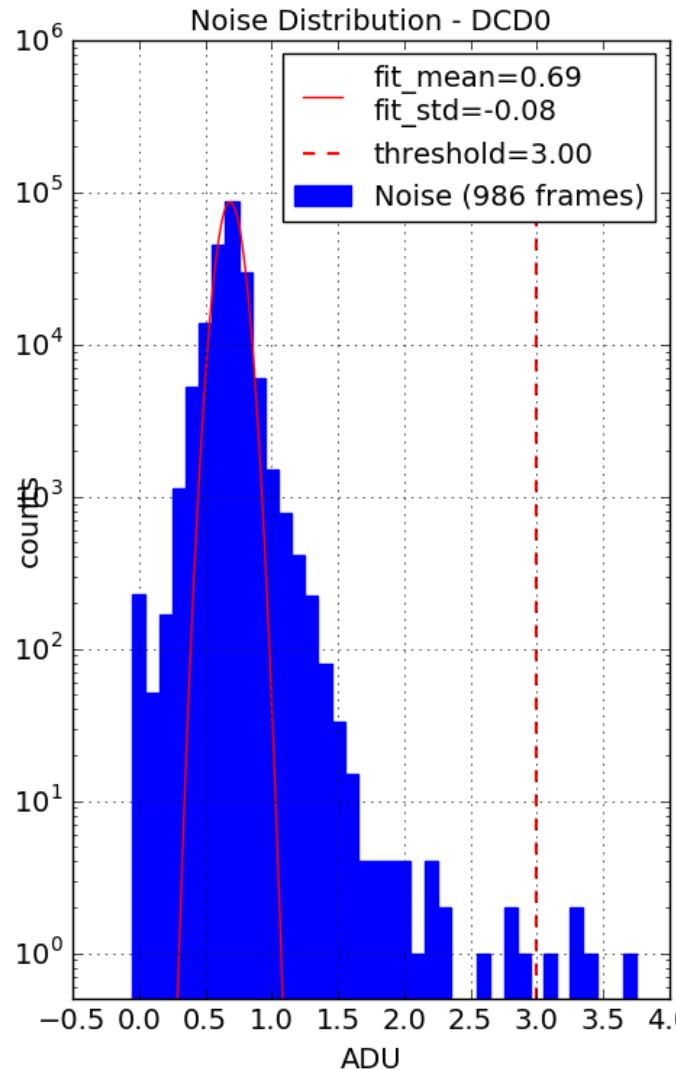


W38_IB – pedestals - with Offsets and ACMC



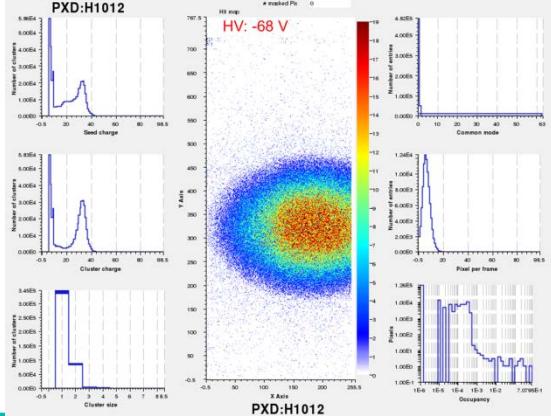
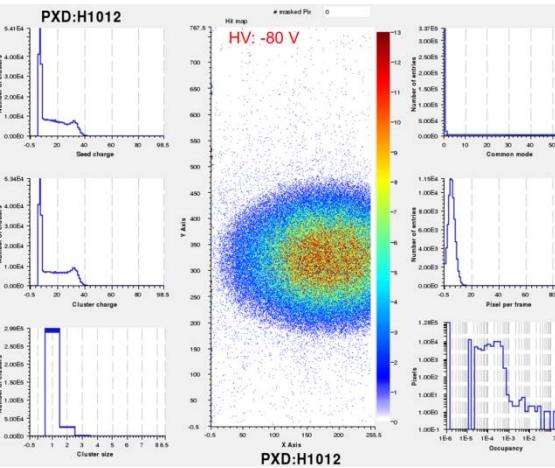
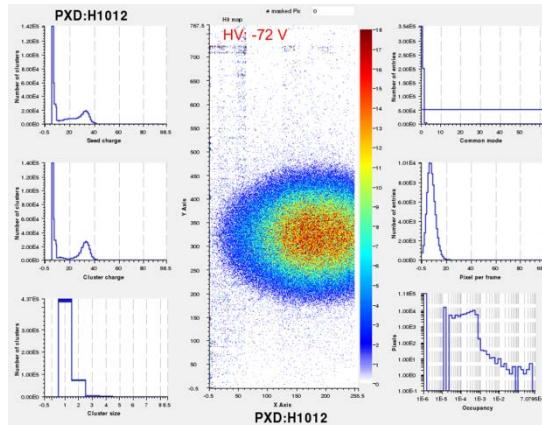
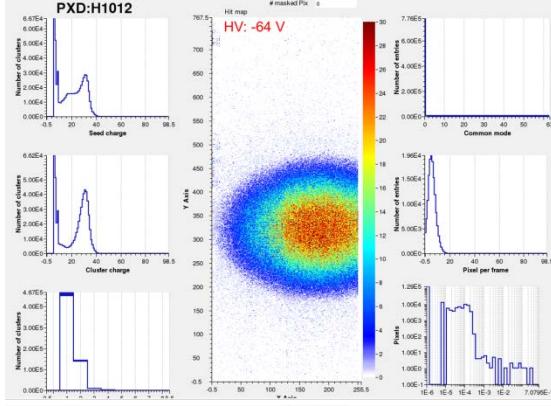
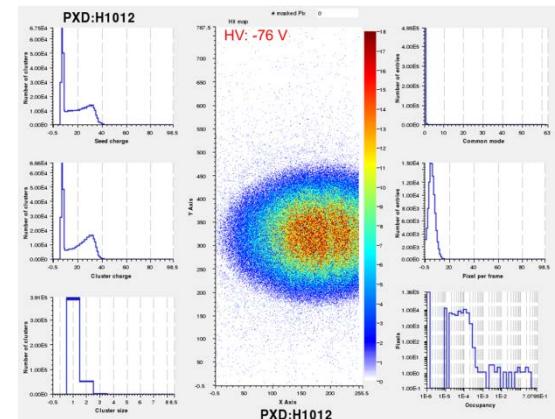
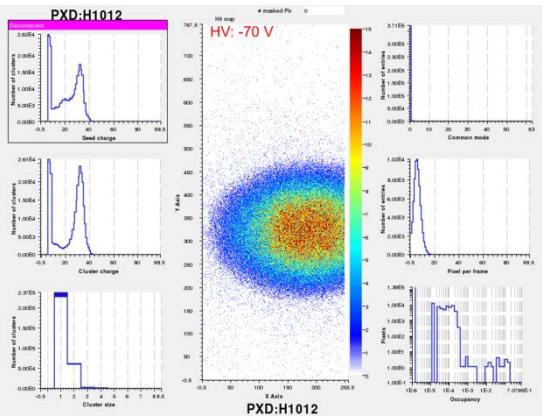
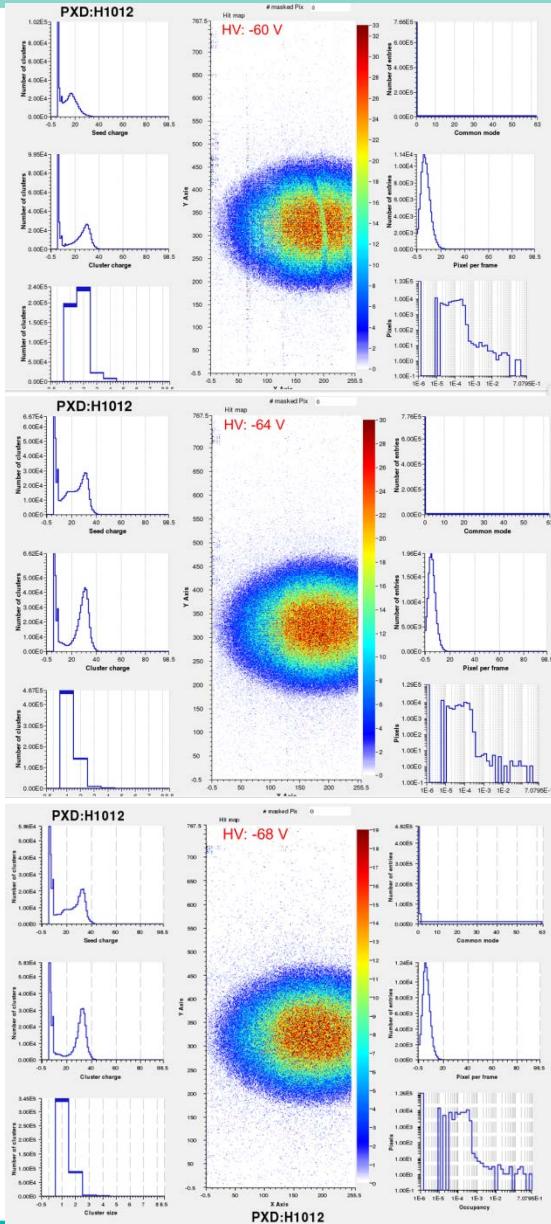


W38_IB – noise – with Offsets and ACMC



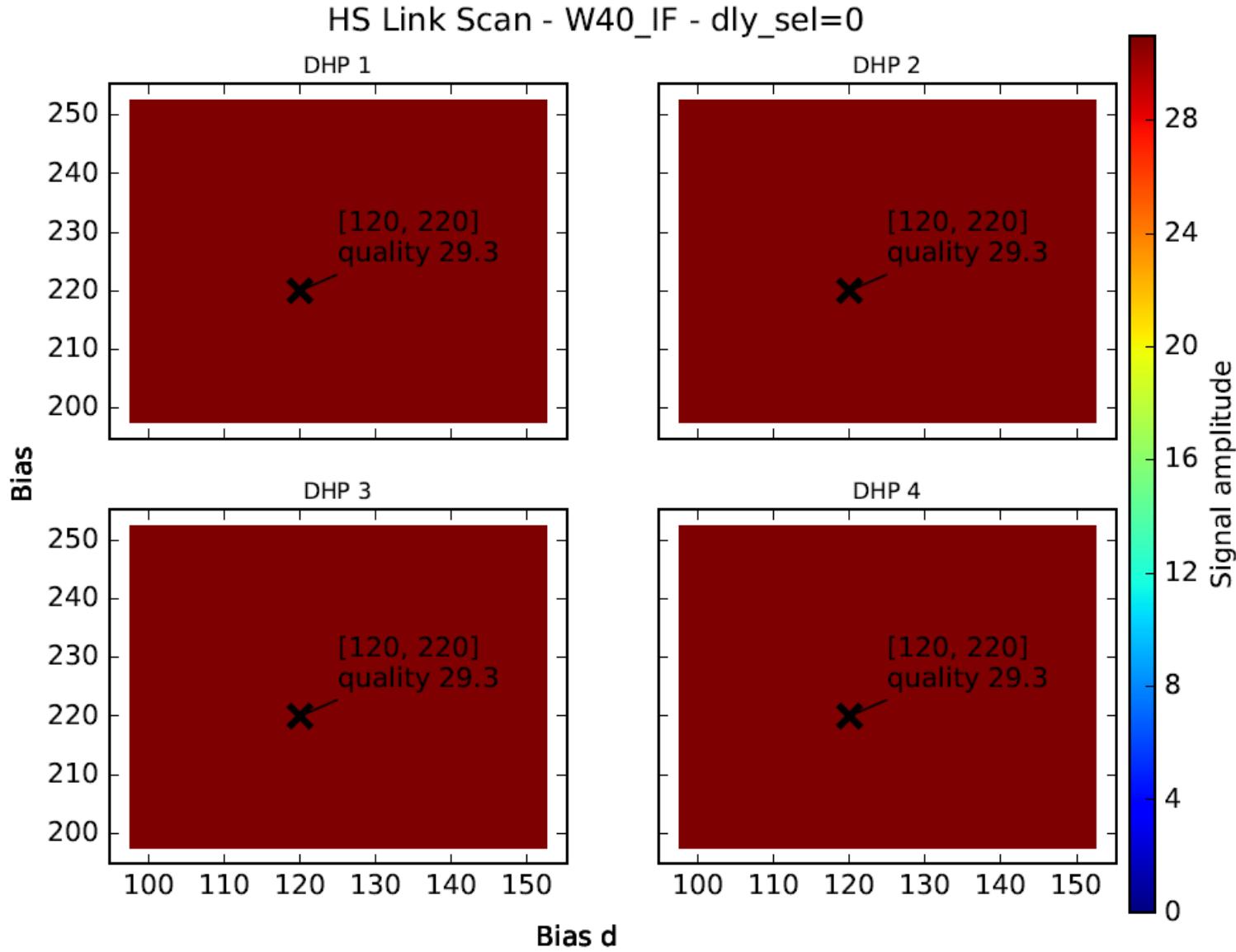


W38_IB – source measurements



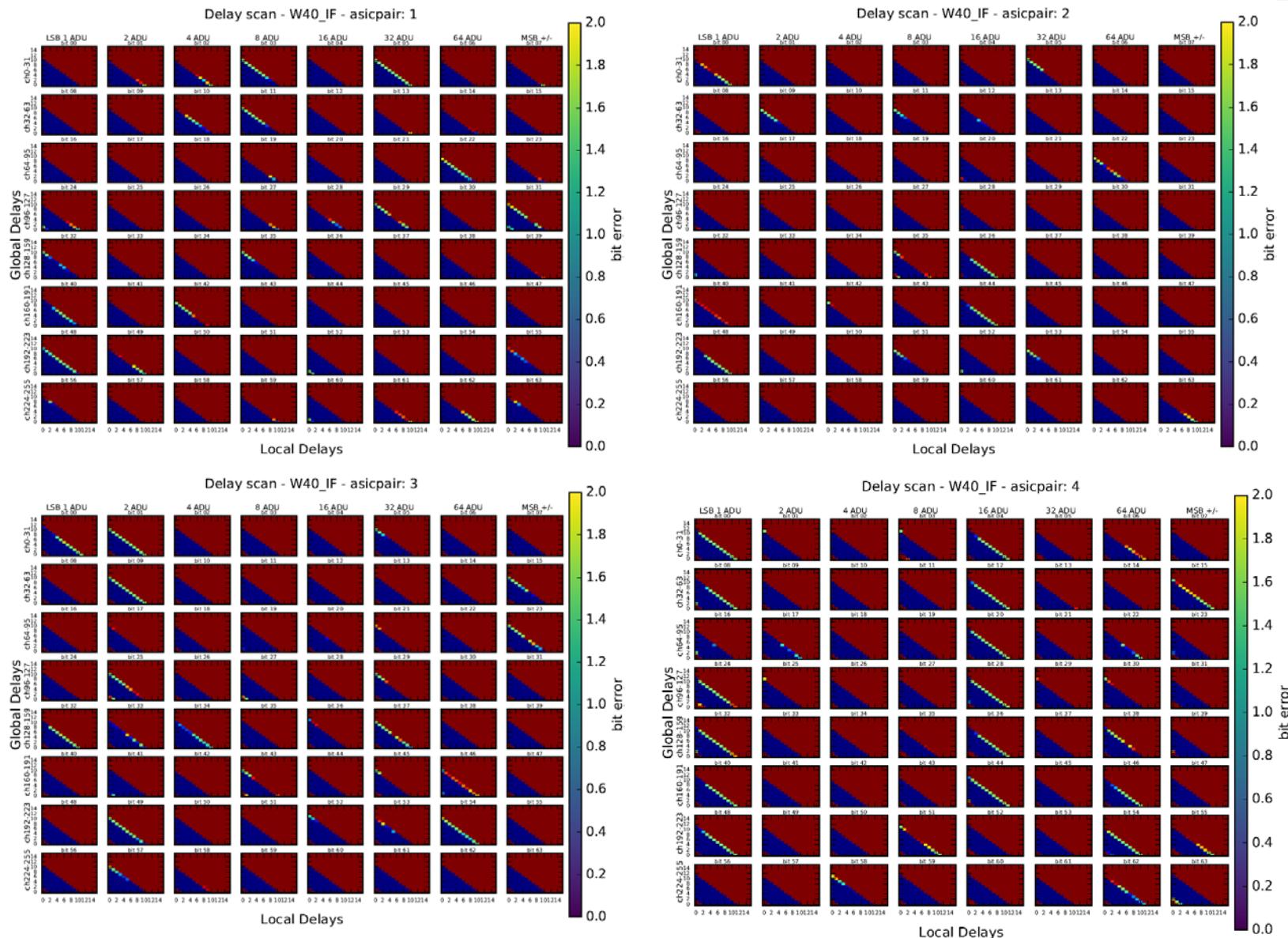


W40_IF – HS links





W40_IF – delays





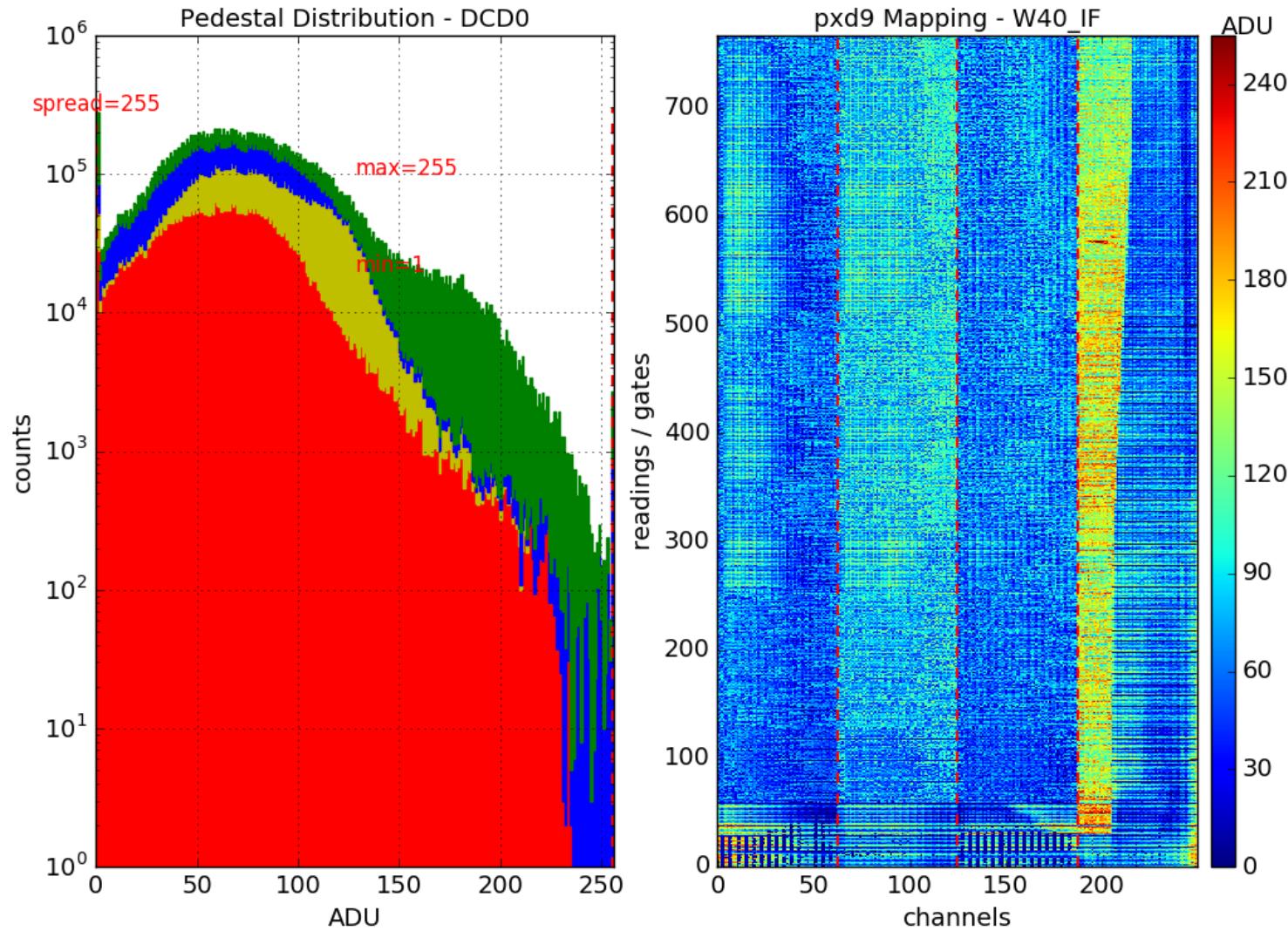
W40_IF – ADC curves

Measurements done, analysis missing

Problem with analysis

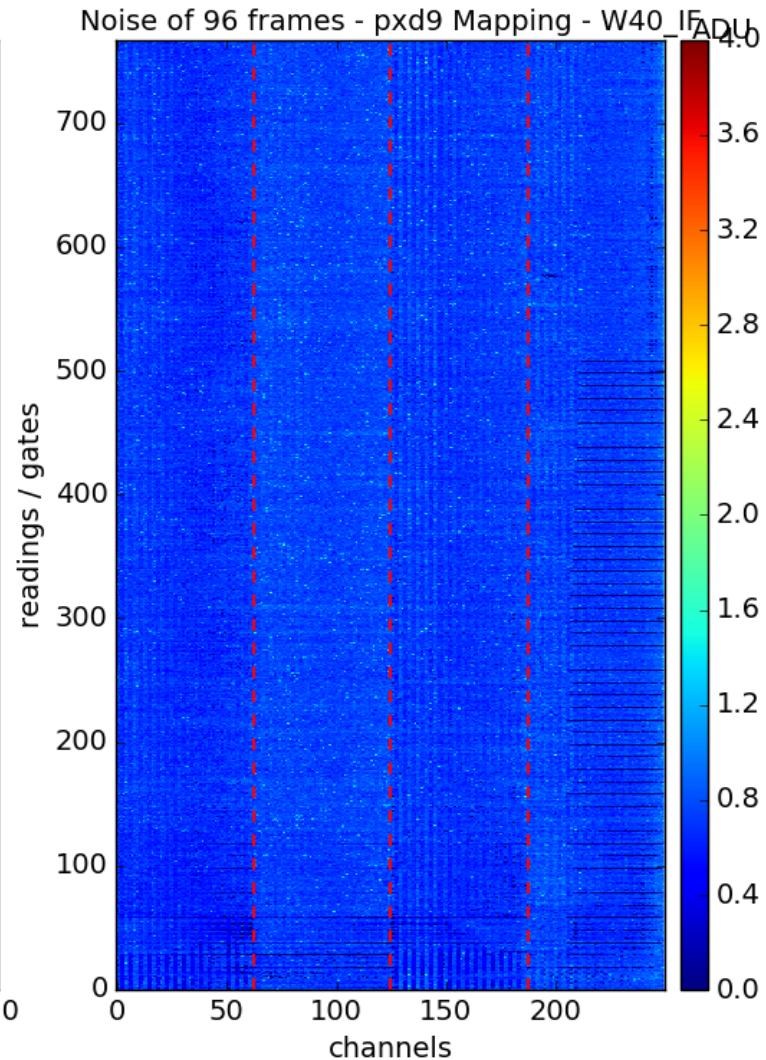
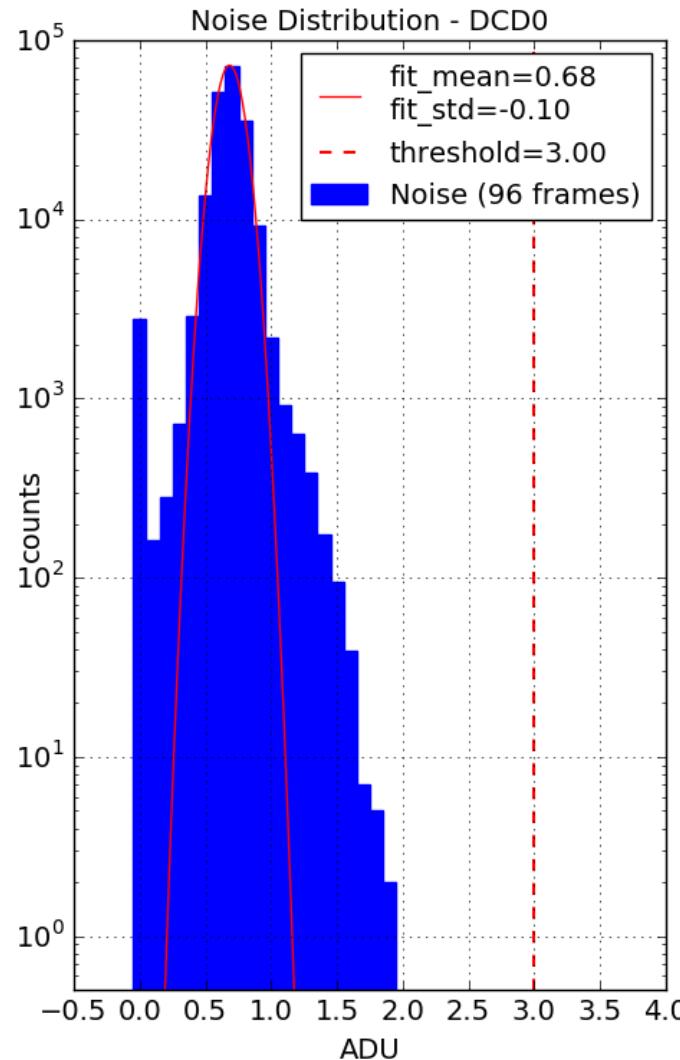


W40_IF – pedestals – with Offsets and ACMC





W40_IF – noise – with Offsets and ACMC



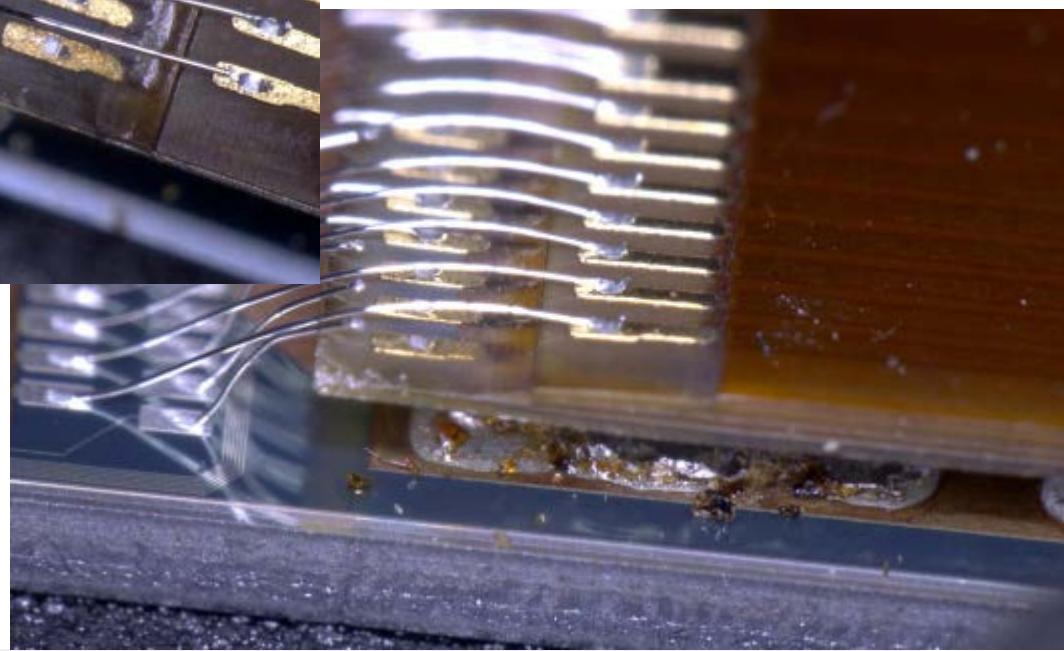
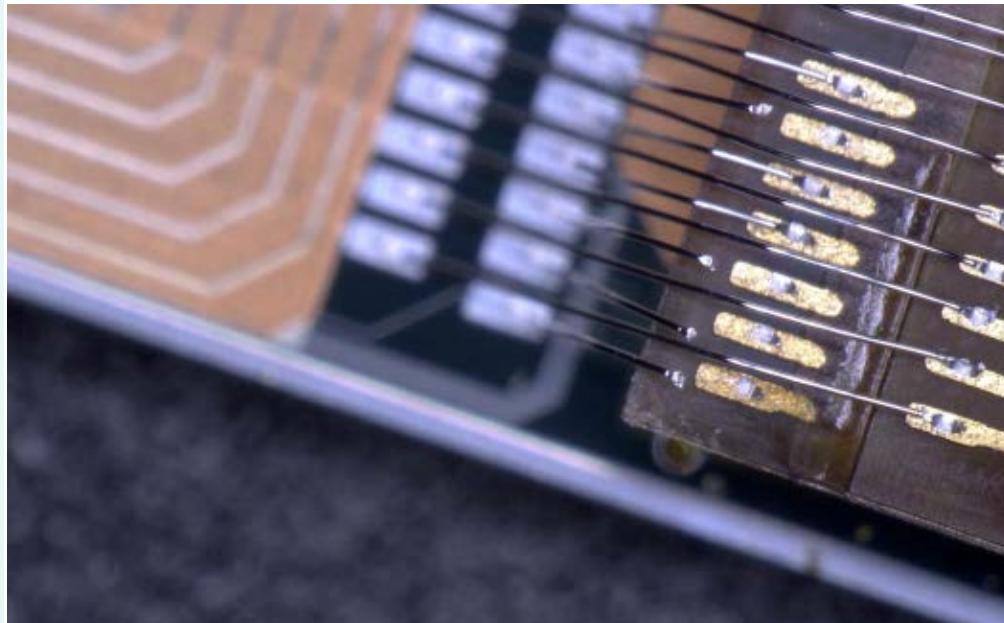


W40_OF – source measurements

/pxdtest8/W40_IF/source/2017_08_07	
	Name
..	
run001_nosource	
run002_nosource	
run003_nosource_dcmc_threshold5_ped25_cm20	
run004_nosource_no-dcmc_threshold5	
run005_source_threshold5_hv60_drift4	
run006_source_threshold5_hv60_drift5	
run007_source_threshold5_hv60_drift6	
run008_source_threshold5_hv64_drift4	
run009_source_threshold5_hv64_drift5	
run010_source_threshold5_hv64_drift6	
run011_source_threshold5_hv68_drift4	
run012_source_threshold5_hv68_drift5	
run013_source_threshold5_hv68_drift6	
run014_source_threshold5_hv72_drift4	
run015_source_threshold5_hv72_drift5	
run016_source_threshold5_hv72_drift6	
run017_source_threshold5_hv56_drift4	
run018_source_threshold5_hv56_drift5	
run019_source_threshold5_hv56_drift6	
run020_source_threshold5_hv56_drift6_pos1	
run021_source_threshold5_hv56_drift6_pos0	
run022_source_threshold5_hv56_drift6_pos3	
run023_source_threshold5_hv56_drift6_pos4	
run024_source_threshold5_hv56_drift6_pos5	
run025_source_threshold5_hv64_drift4_painting	



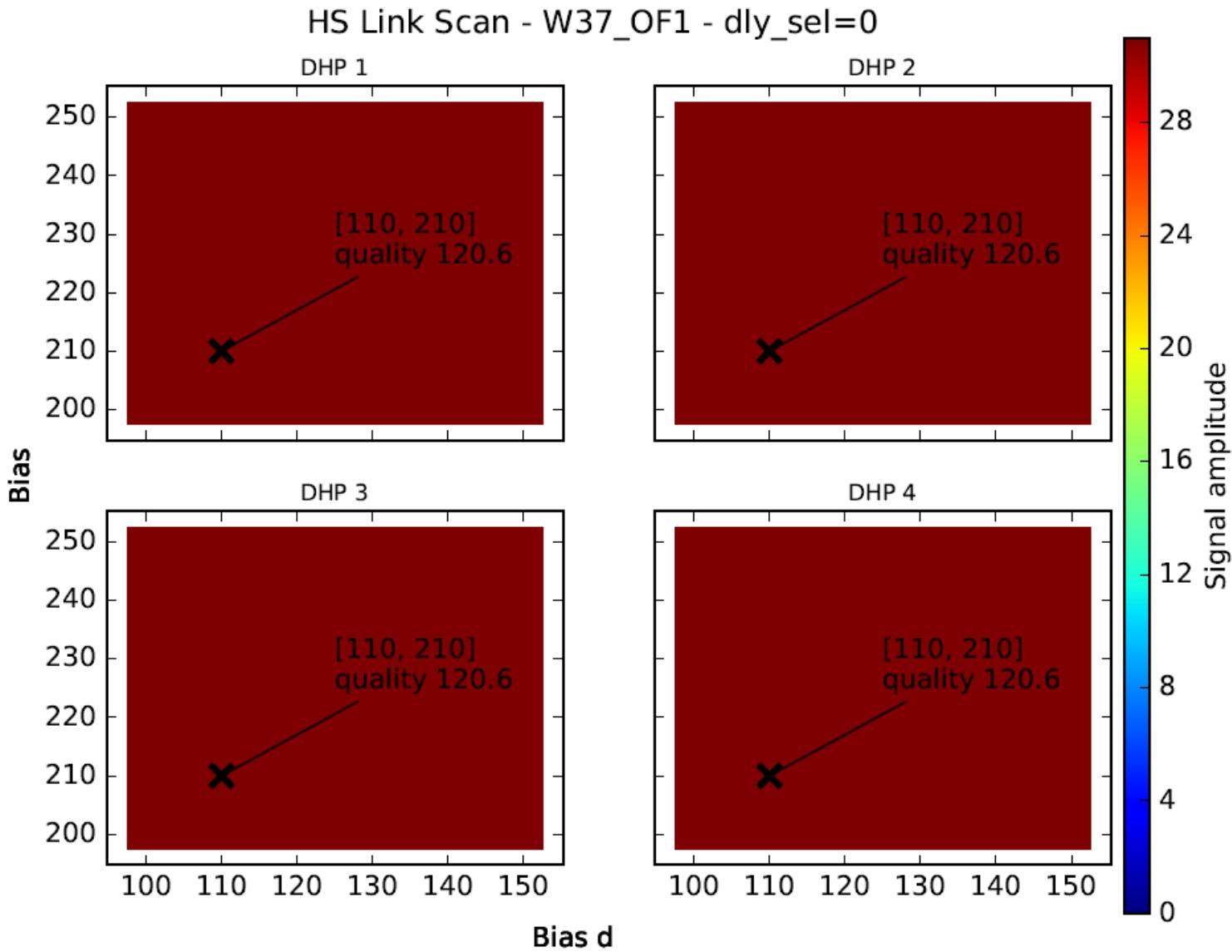
W38_IB & W40_IF - ladder



15 mA	30 mA	-4000 mV	3000 mV	3000 mV	■	3050 mV	3009 mV	5 mA	gate-on2
15 mA	30 mA	-4000 mV	3000 mV	3000 mV	■	810 mV	733 mV	16 mA	gate-on3
30 mA	30 mA	0 mV	3000 mV	6000 mV	■	3056 mV	3023 mV	10 mA	gate-off
120 mA	150 mA	0 mV	6000 mV	7000 mV	■	7238 mV	6002 mV	24 mA	source

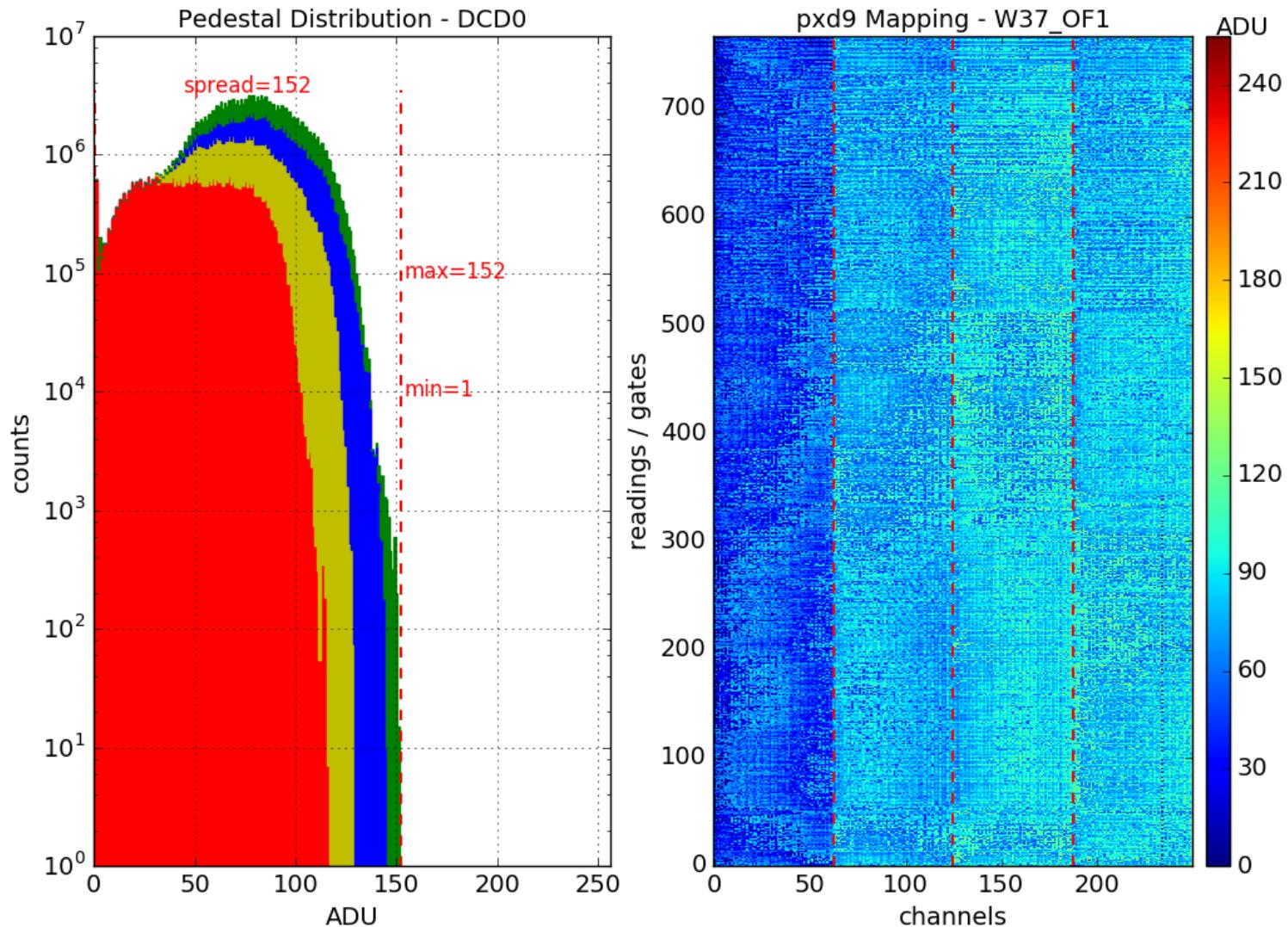


W37_OF1 – HS links



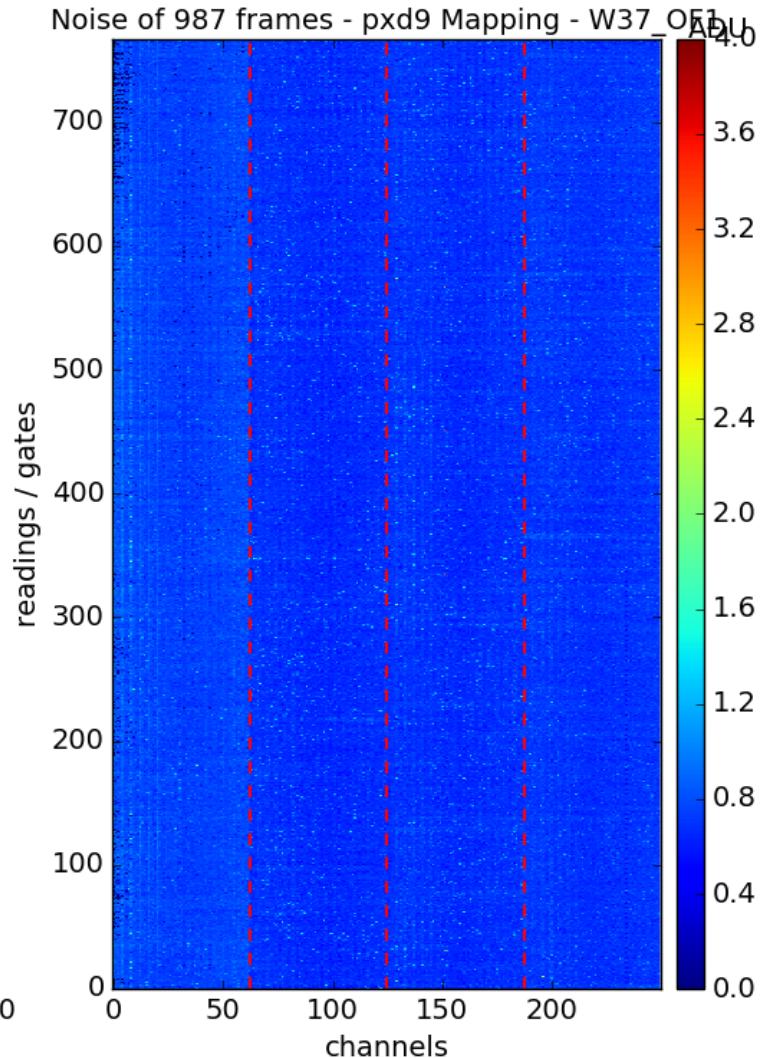
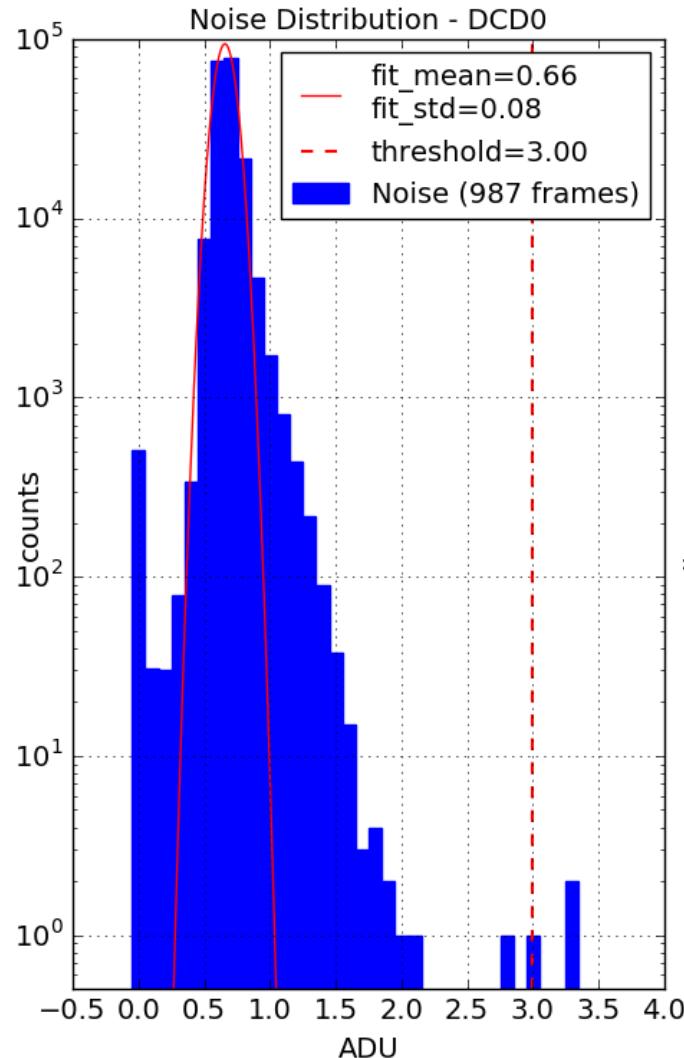


W37_OF1 – pedestals with ACMC and offsets



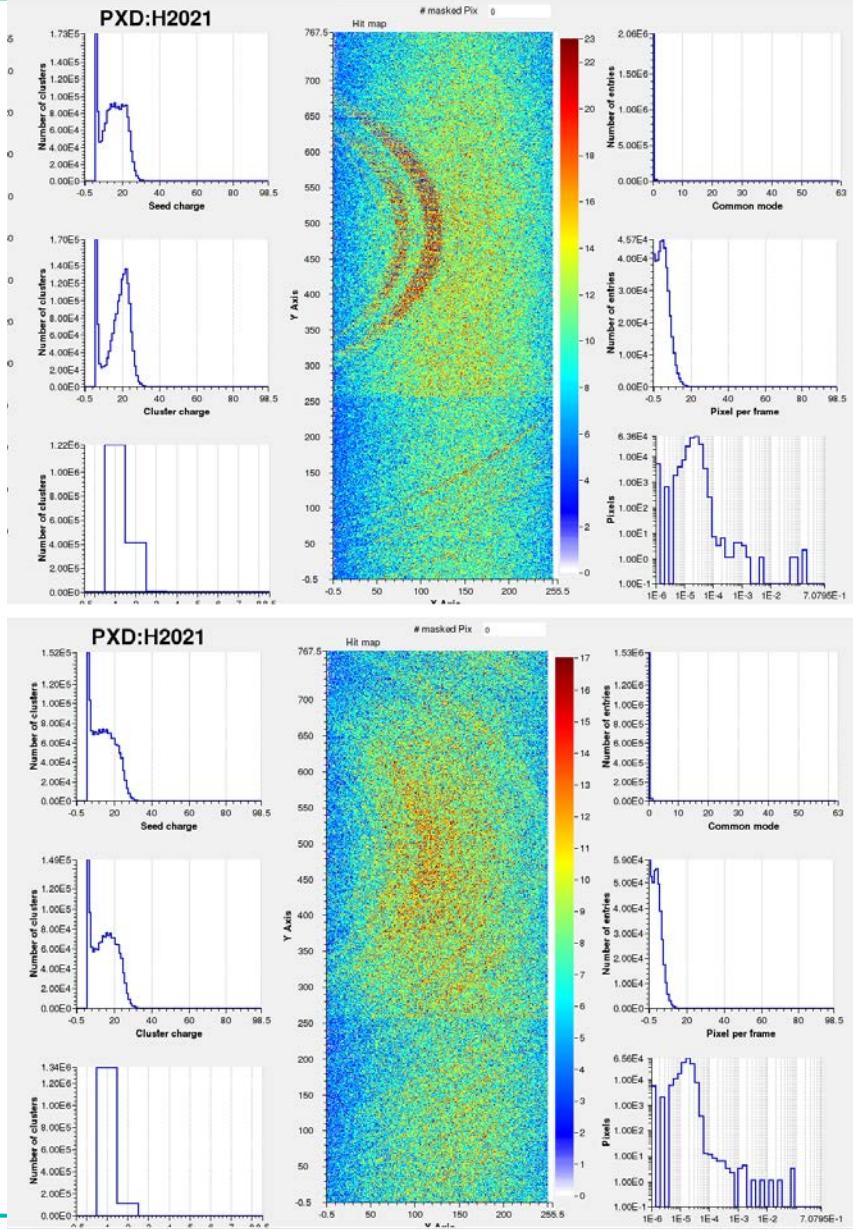


W37_OF1 – noise with ACMC and offsets





W37_OF1 – source measurements



/pxdtest8/W37_OF1/source/2017_08_10_003

Name

- drift_-3000_hv_-60000
- drift_-3000_hv_-62000
- drift_-3000_hv_-64000
- drift_-3000_hv_-66000
- drift_-3000_hv_-68000
- drift_-3000_hv_-70000
- drift_-3000_hv_-72000
- drift_-3000_hv_-74000
- drift_-3000_hv_-76000
- drift_-3000_hv_-78000
- drift_-3000_hv_-80000
- drift_-4000_hv_-60000
- drift_-4000_hv_-62000
- drift_-4000_hv_-64000
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- drift_-5000_hv_-70000
- drift_-5000_hv_-72000
- drift_-5000_hv_-74000
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- drift_-5000_hv_-78000
- drift_-5000_hv_-80000

/pxdtest8/W37_OF1/source/2017_08_10_003

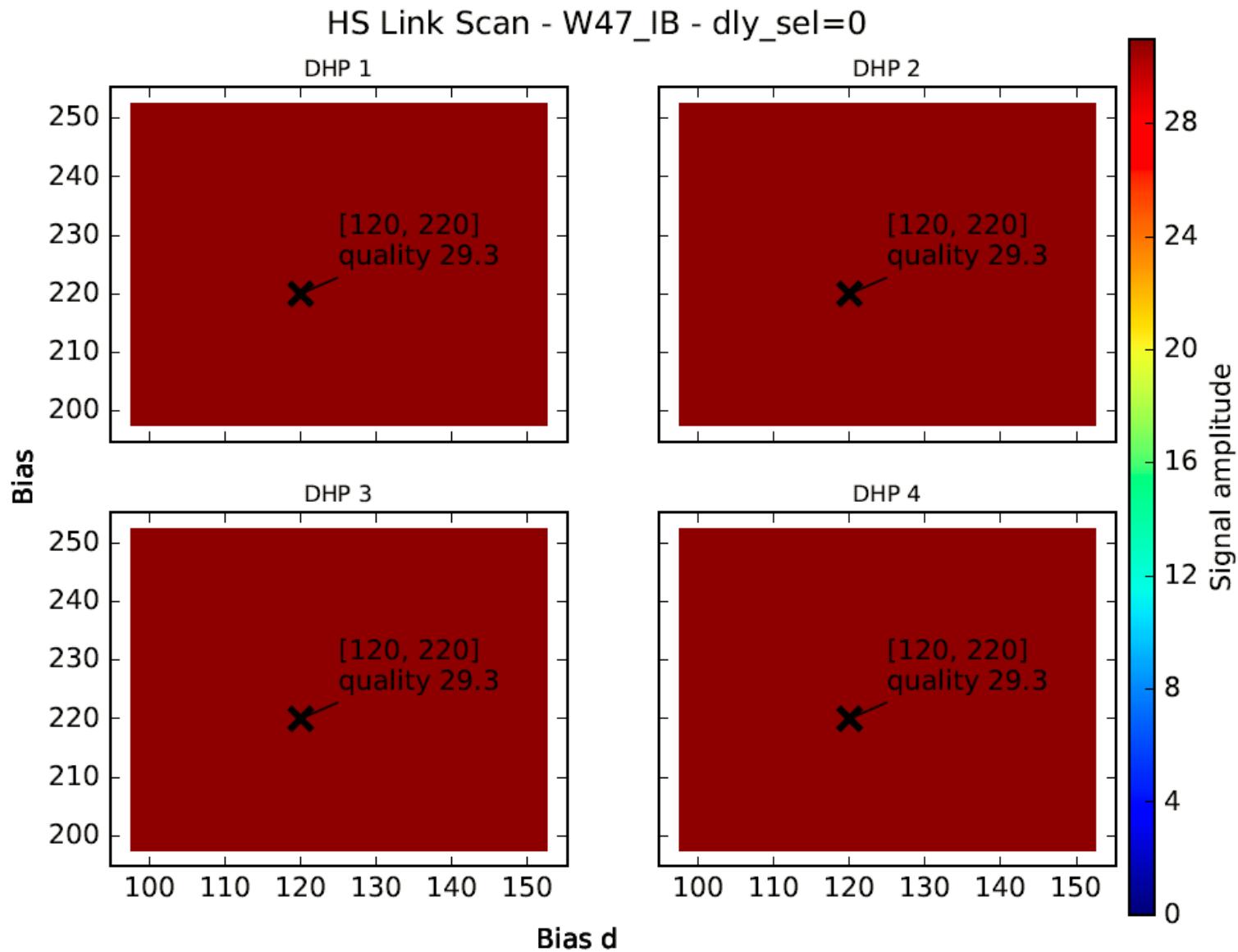
Name

- drift_-5000_hv_-78000
- drift_-5000_hv_-80000
- drift_-6000_hv_-60000
- drift_-6000_hv_-62000
- drift_-6000_hv_-64000
- drift_-6000_hv_-66000
- drift_-6000_hv_-68000
- drift_-6000_hv_-70000
- drift_-6000_hv_-72000
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- drift_-6000_hv_-76000
- drift_-6000_hv_-78000
- drift_-6000_hv_-80000

see talk by Harrison

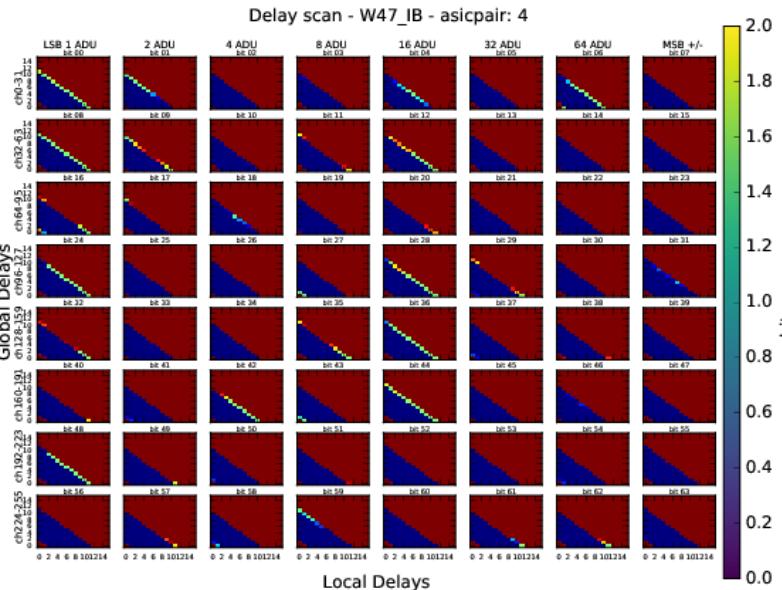
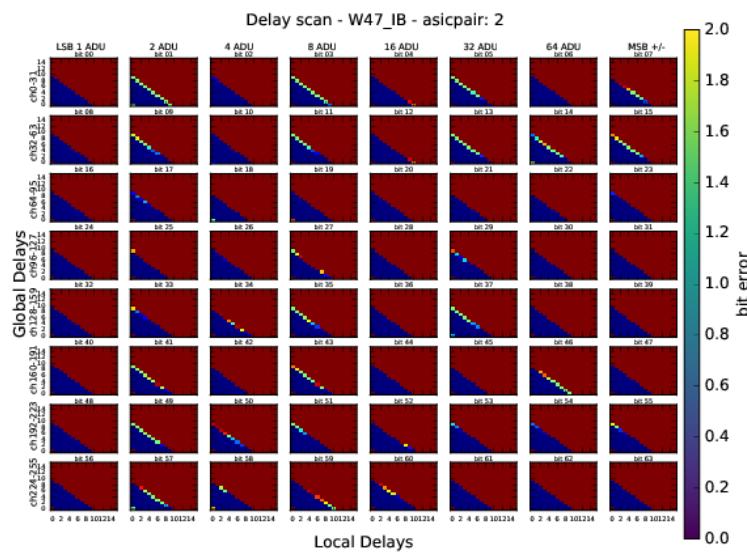
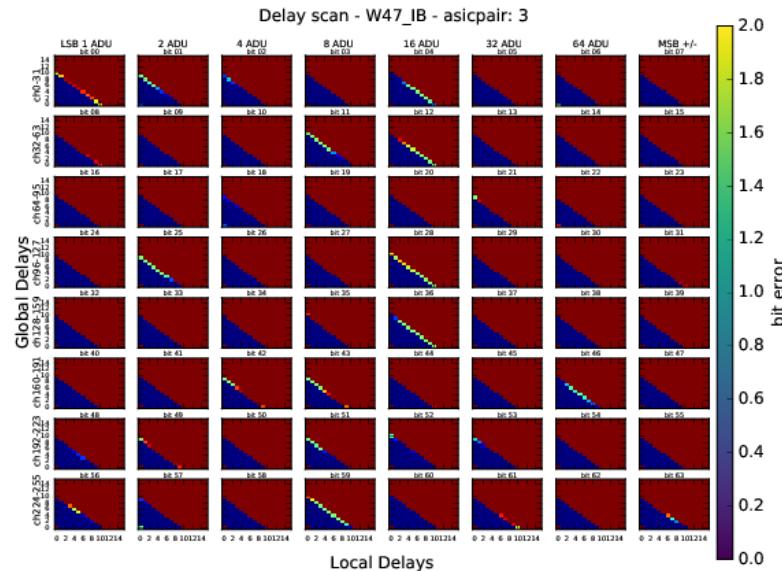
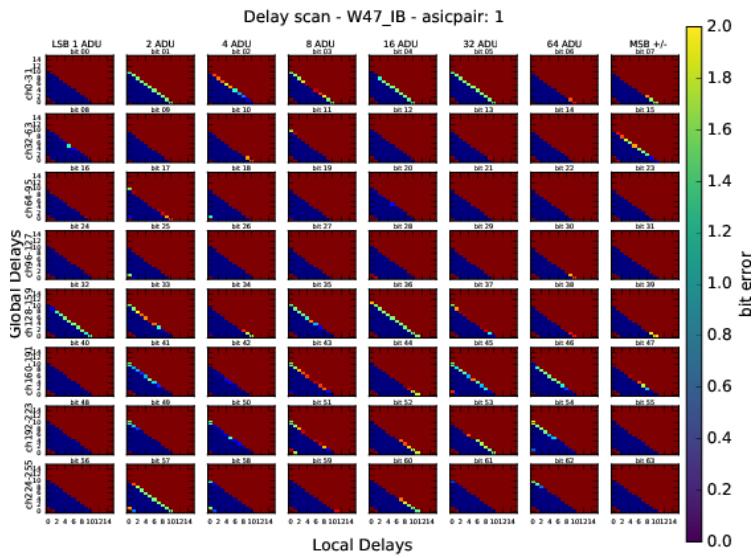


W47_IB – HS link



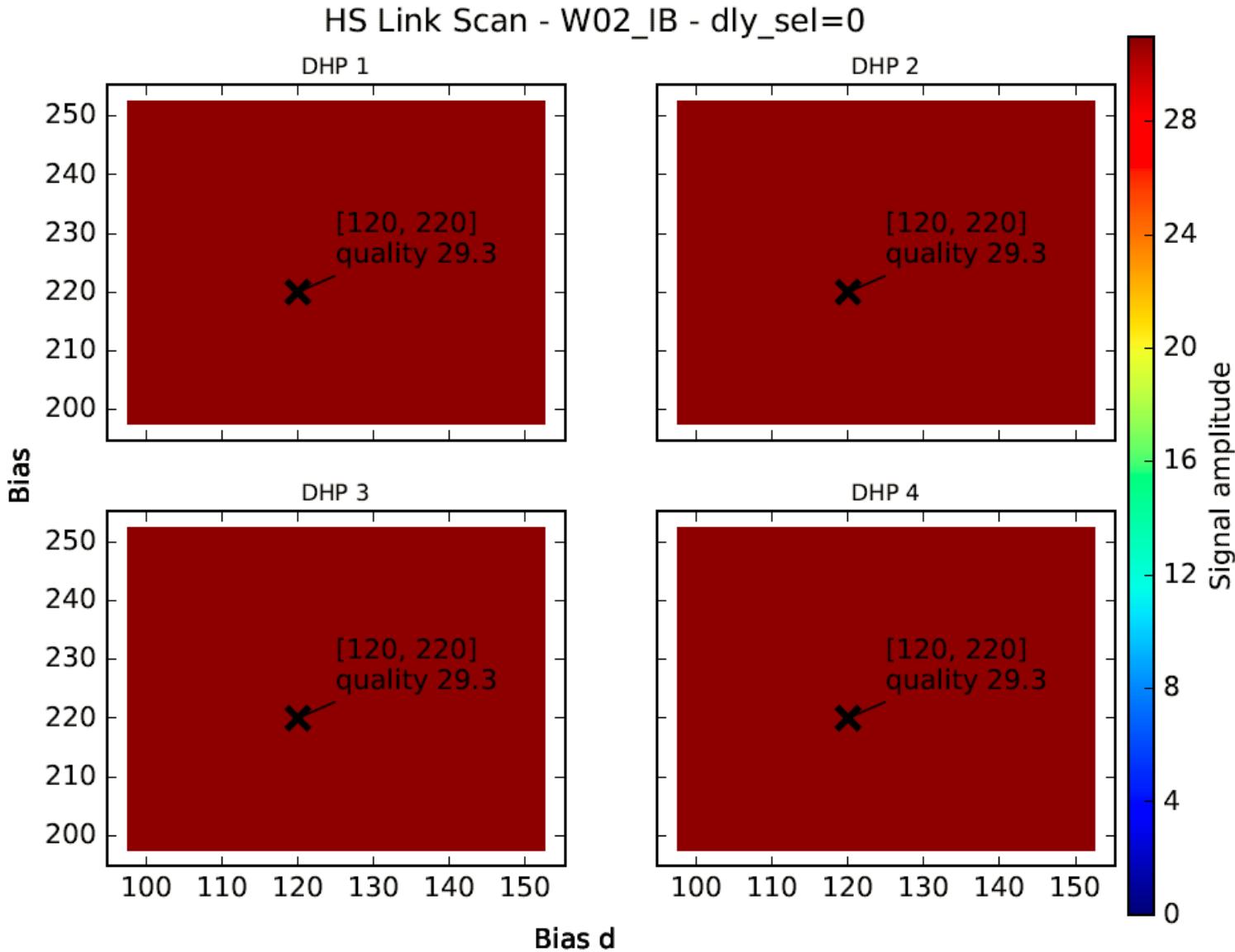


W47_IB – delays



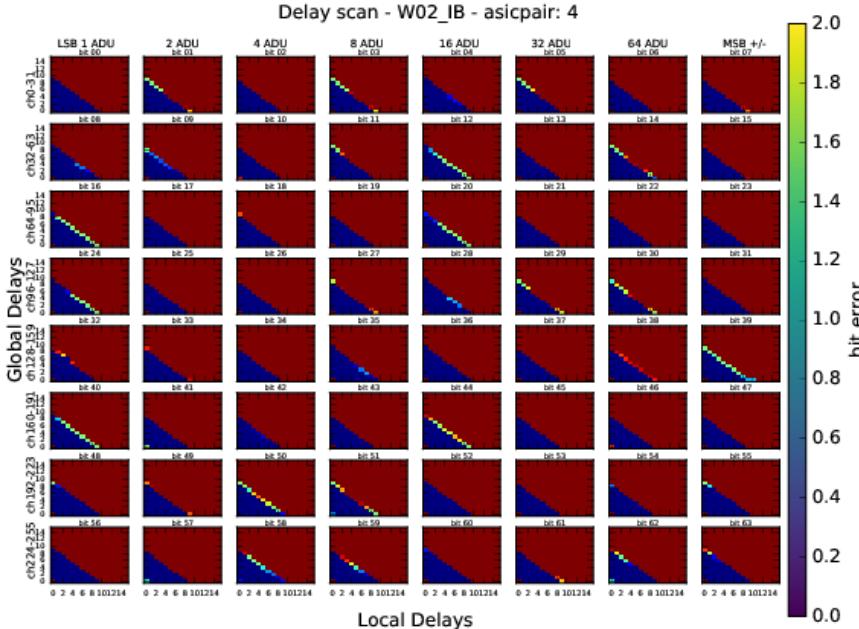
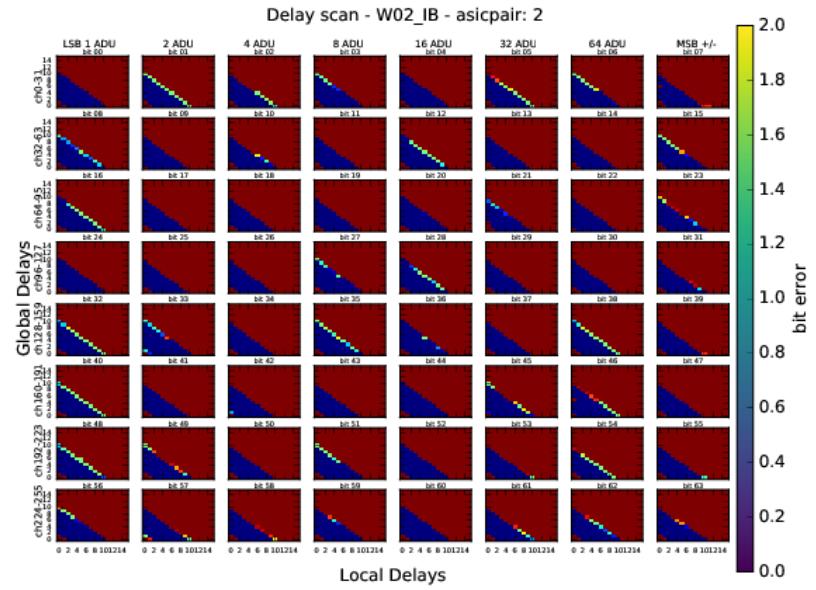
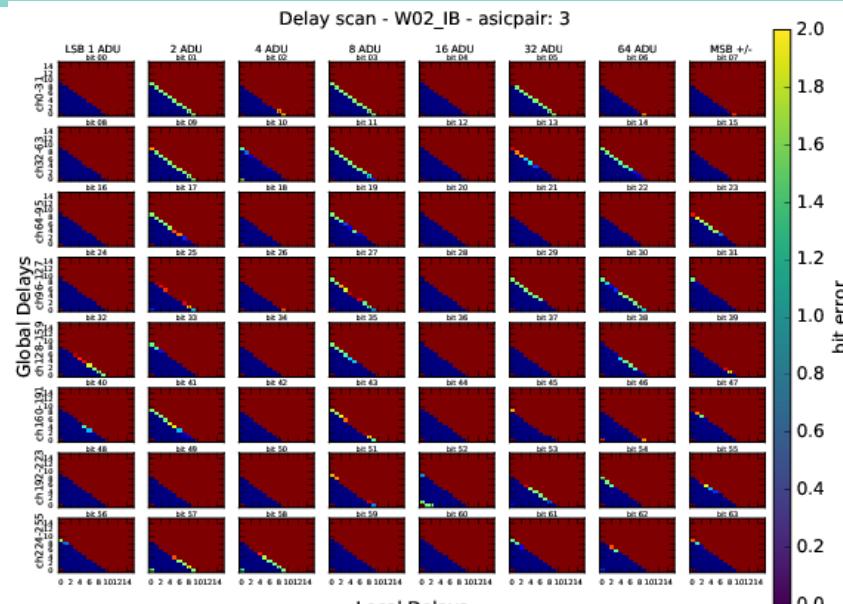
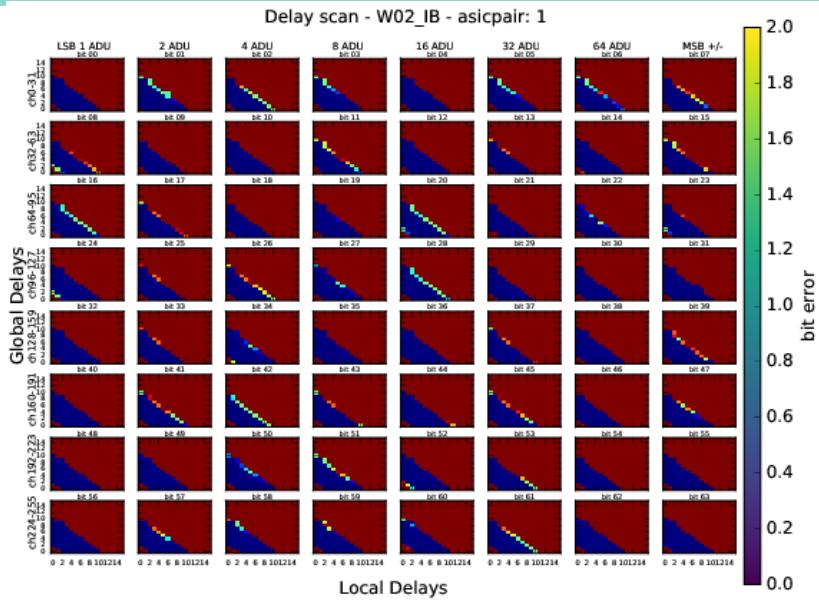


W02_IB – HS link



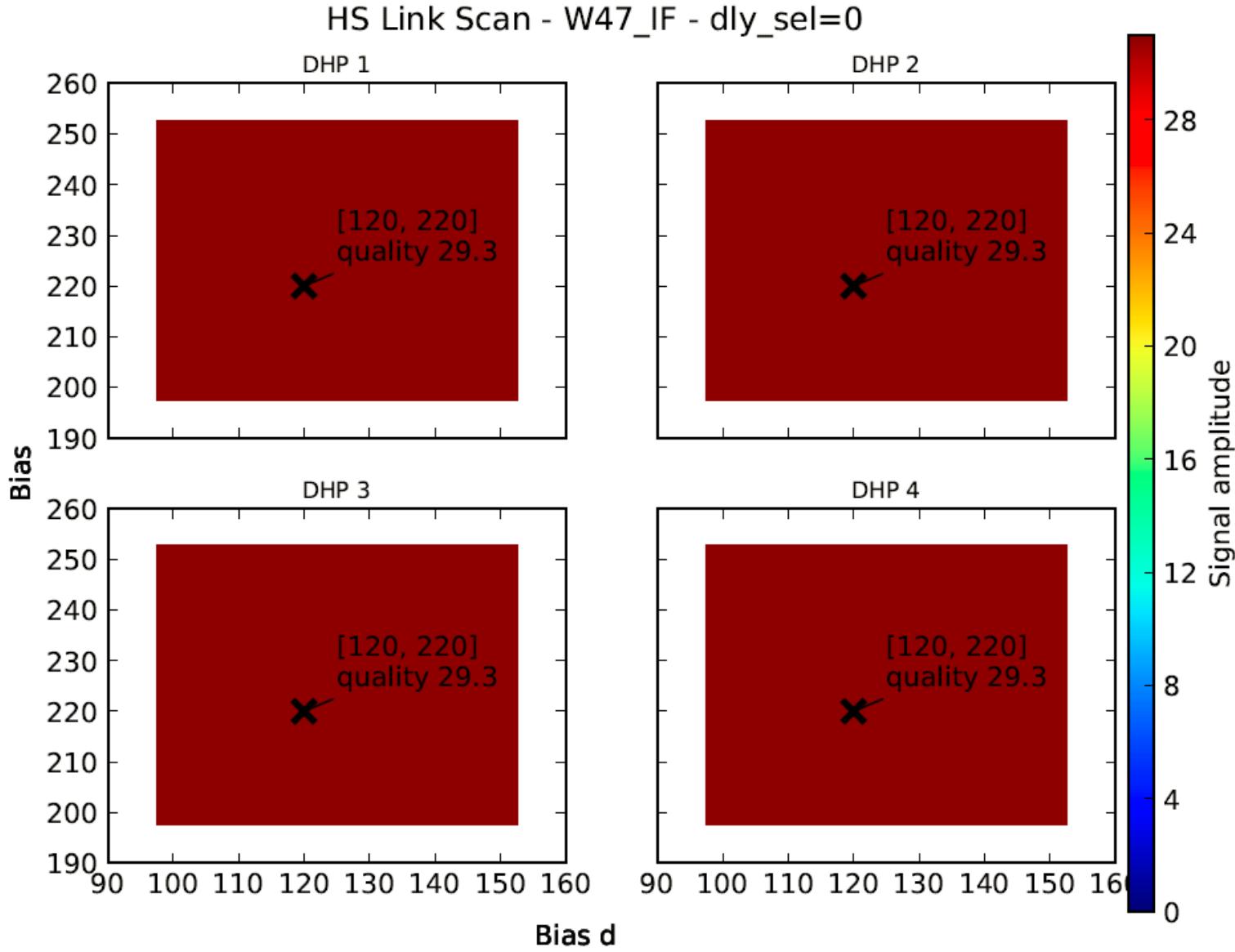


W02_IB – delays



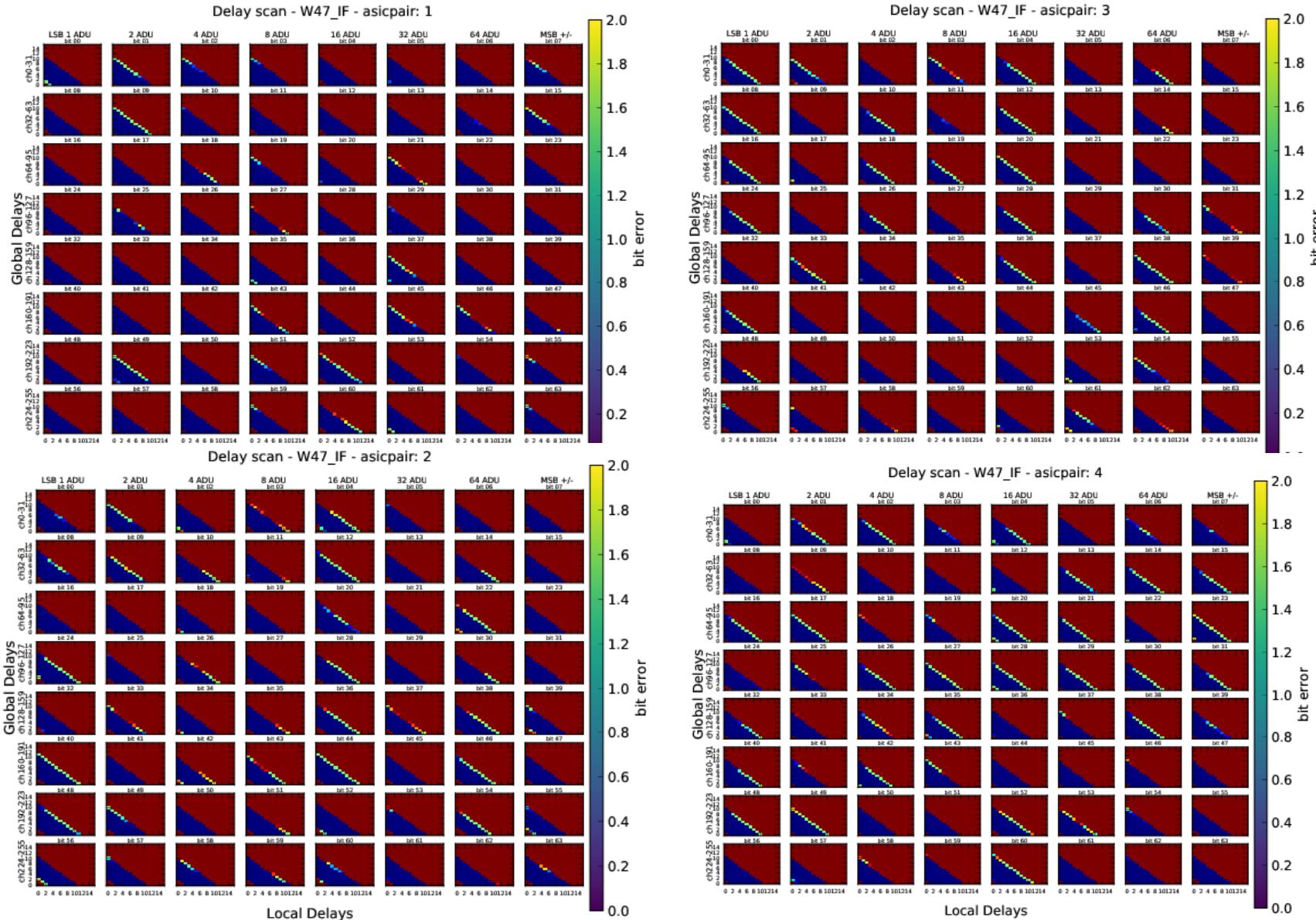


W47_IF – HS link





W47_IF – delays





batch P3-1

W47_IB: hs_link, delays, pedestals, adc_curves, sample_point_curve (analysis must be performed)

W02_IB: hs_link, delays, pedestals, adc_curves

W47_IF: hs_link, delays, pedestals, adc_curves

W44_IF: not yet tested

W46_IF. HLL for rings and GM

Module	Summary Link	Testing Locations	Last Update	Probe Card Scan	HS Link Scan	HS Link Analysis	Delay Scan	Delay Analysis	Pedestal Scan	ADC Scan	ADC Analysis	Sampling Point Curve Scan	Sampling Point Curve Analysis	Source Scan	Source Analysis
W02_IB	359	Munich	2017/09/19 (Delay Analysis)	Done	Done	Passed (A)	Done	Done (-)	Todo	Todo	Todo	Todo	Todo	Todo	Todo
W47_IB	335	Munich	2017/09/27 (Sampling Point Curve Scan)	Done	Done	Passed (A)	Done	Done (-)	Todo	Done	Todo	Done	Done (-)	Todo	Todo
W47_IF	410	Munich	2017/09/26 (Delay Analysis)	Done	Done	Passed (A)	Done	Done (-)	Todo	Todo	Todo	Todo	Todo	Todo	Todo



Open Issues

Sampling Point Curve: Verification of Switcher Sequence in DHP memory

Offsets: elog connection; coding guide lines

pedestals: elog connection; coding guide lines

source: needs to be tested; different positions?; include stepper?

power up sequence: including OVP: Harrison took care

ADC-curves: define parameter ranges, reduce ranges?

Archiver; Which PVs are important – what is the exact meaning?

scripts for archiver:

[https://stash.desy.de/projects/B2G/repos/pxd_sc_lab_framework/browse/configurations/epics_archiver
?at=refs%2Fheads%2Ffeature%2Farchiver-scripts](https://stash.desy.de/projects/B2G/repos/pxd_sc_lab_framework/browse/configurations/epics_archiver?at=refs%2Fheads%2Ffeature%2Farchiver-scripts)